

MOSFET, N-Channel, POWERTRENCH[®]

80 V, 80 A, 4.5 mΩ



ON Semiconductor[®]

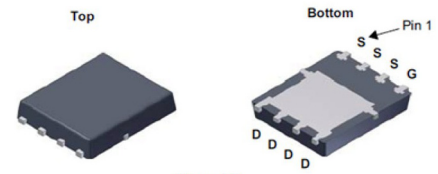
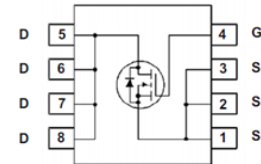
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Features

- Typical $R_{DS(on)} = 3.7\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- Typical $Q_{g(tot)} = 57\text{ nC}$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- UIS Capability
- Wetable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

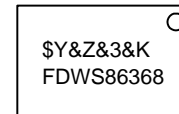
Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems



DFN8 5.1x6.3, 1.27P
CASE 506DW

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDWS86368	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDWS86368–F085

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Drain Current –Continuous ($V_{GS} = 10\text{ V}$) (Note 1) $T_C = 25^\circ\text{C}$	80	A
	–Pulsed $T_C = 25^\circ\text{C}$	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	82	mJ
P_D	Power Dissipation	214	W
	Derate Above 25°C	1.43	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 40\ \mu\text{H}$, $I_{AS} = 64\ \text{A}$, $V_{DD} = 80\ \text{V}$ during inductor charging and $V_{DD} = 0\ \text{V}$ during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a $1\ \text{in}^2$ pad of 2 oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDWS86368	FDWS86368–F085	DFN8 5.1x6.3, 1.27P (Pb-Free)	3000 units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

FDWS86368–F085

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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OFF CHARACTERISTICS

B_{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	80			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 25^\circ\text{C}$			1	μA
		$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 175^\circ\text{C}$ (Note 4)			1	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$			±100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_J = 25^\circ\text{C}$		3.7	4.5	$\text{m}\Omega$
		$I_D = 80 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_J = 175^\circ\text{C}$ (Note 4)		7.4	9.0	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$			4350	pF	
C_{oss}	Output Capacitance				636	pF	
C_{rss}	Reverse Transfer Capacitance				20	pF	
R_g	Gate Resistance	$f = 1 \text{ MHz}$			2.5	Ω	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	$V_{DD} = 64 \text{ V}$, $I_D = 80 \text{ A}$		57	75	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ V to } 2 \text{ V}$			8		nC
Q_{gs}	Gate-to-Source Gate Charge				23		nC
Q_{gd}	Gate-to-Drain "Miller" Charge				11		nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 40 \text{ V}$, $I_D = 80 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$			60	ns
$t_{d(on)}$	Turn-On Delay				23	ns
t_r	Rise Time				22	ns
$t_{d(off)}$	Turn-Off Delay				32	ns
t_f	Fall Time				13	ns
t_{off}	Turn-Off Time				59	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 80 \text{ A}$ $V_{GS} = 0 \text{ V}$, $I_{SD} = 40 \text{ A}$			1.25 1.2	V
t_{rr}	Reverse-Recovery Time	$I_F = 80 \text{ A}$, $\Delta I_{SD}/\Delta t = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 64 \text{ V}$		58	75	ns
Q_{rr}	Reverse-Recovery Charge			49	67	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

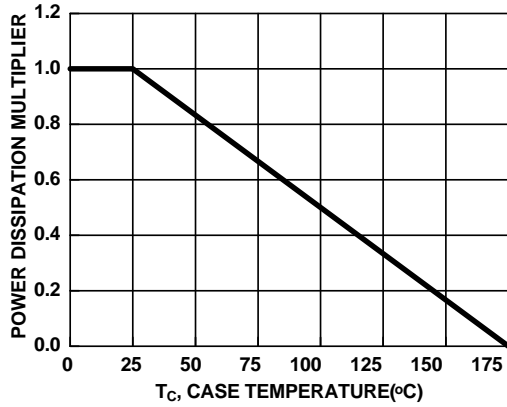


Figure 1. Normalized Power Dissipation vs. Case Temperature

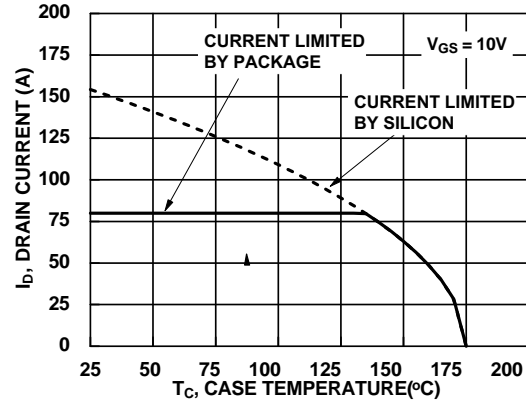


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

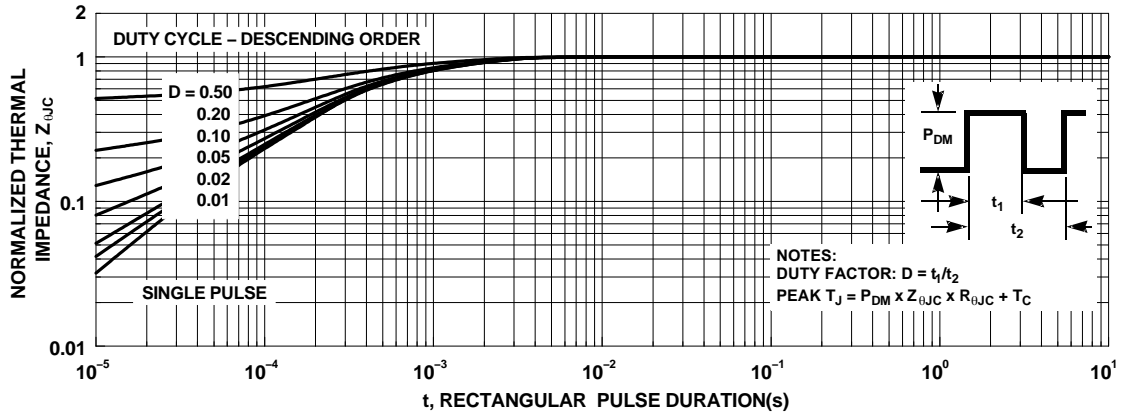


Figure 3. Normalized Maximum Transient Thermal Impedance

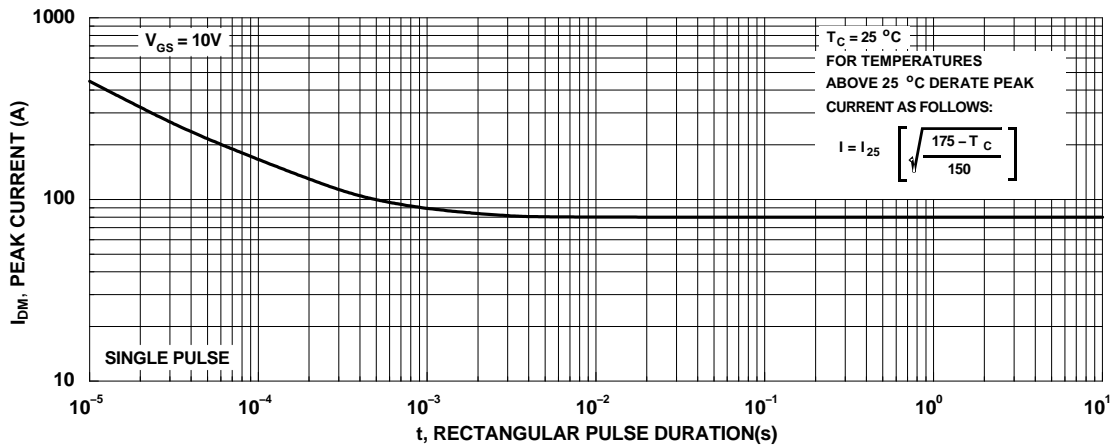


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

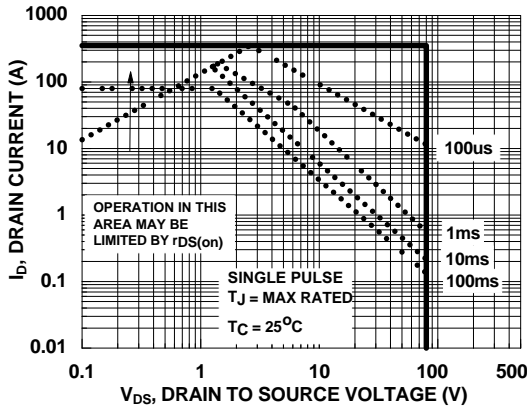
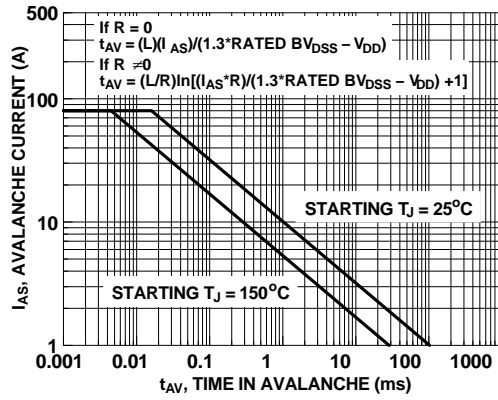


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

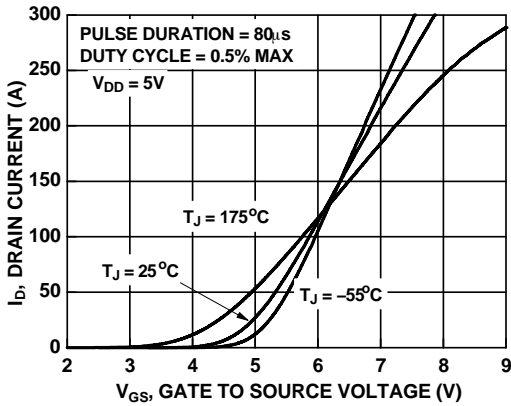


Figure 7. Transfer Characteristics

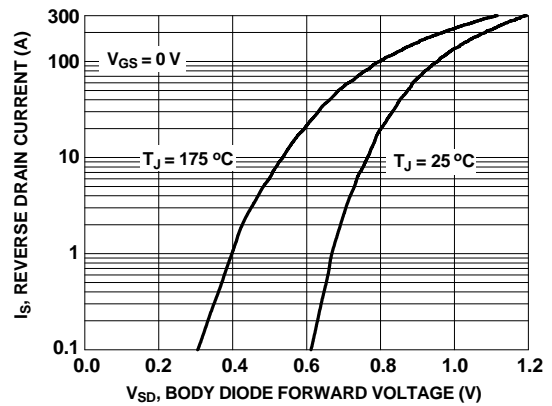


Figure 8. Forward Diode Characteristics

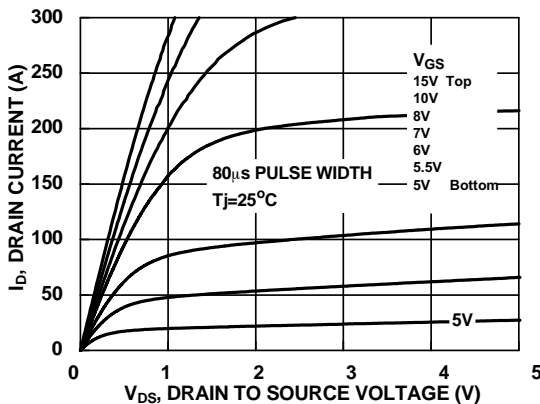


Figure 9. Saturation Characteristics

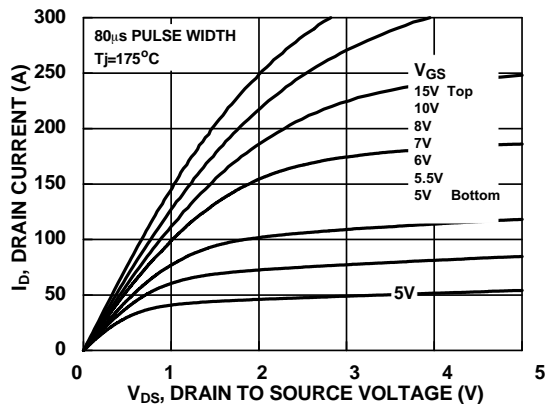


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

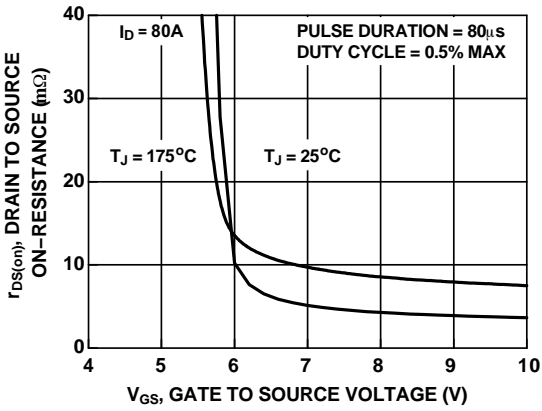


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

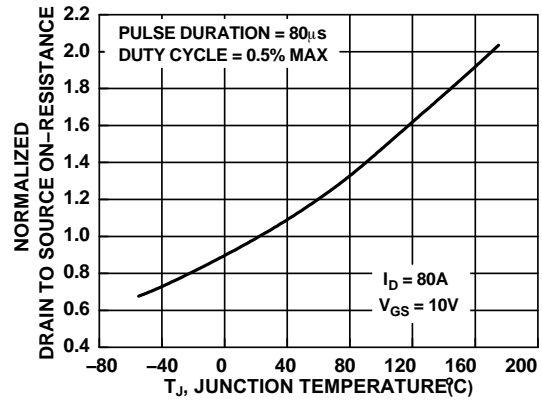


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

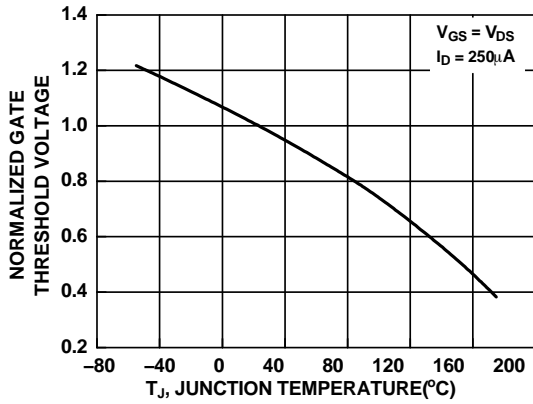


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

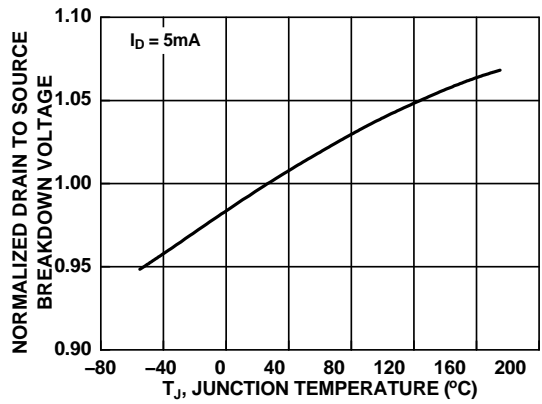


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

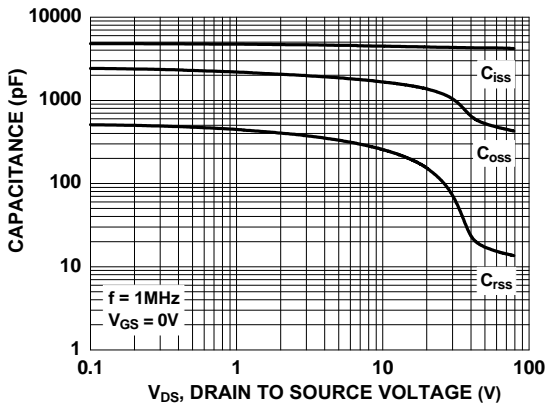


Figure 15. Capacitance vs. Drain to Source Voltage

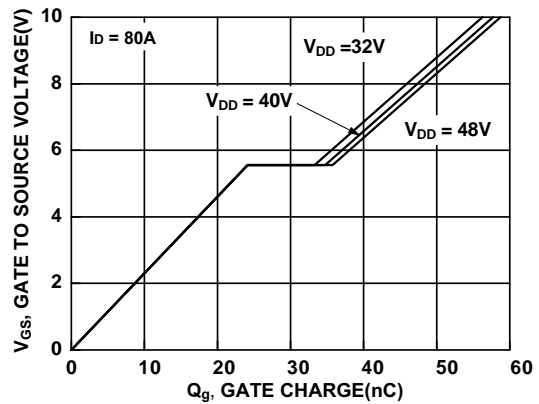


Figure 16. Single Pulse Maximum Power Dissipation

MECHANICAL CASE OUTLINE

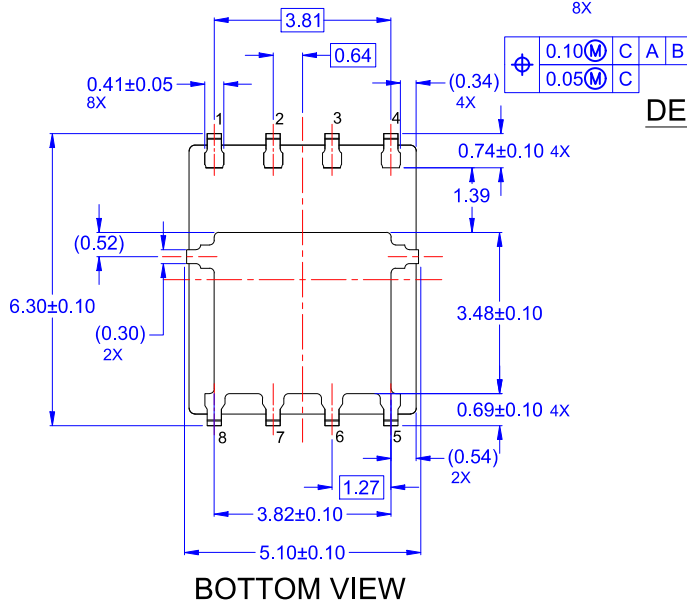
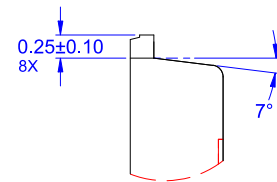
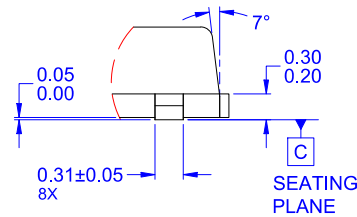
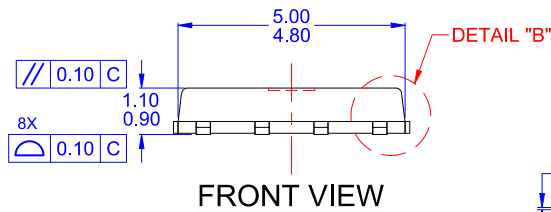
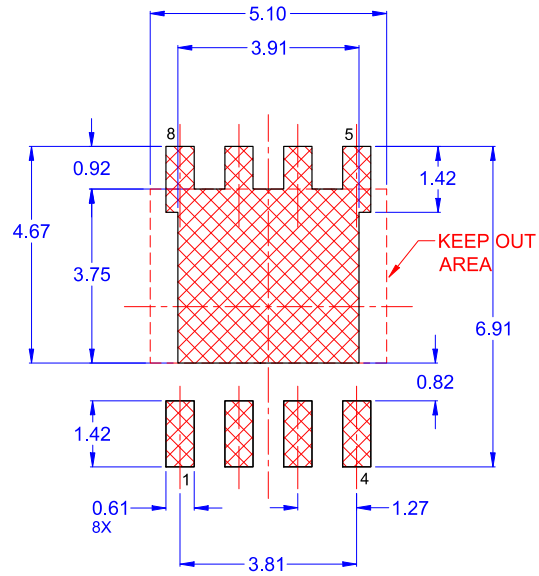
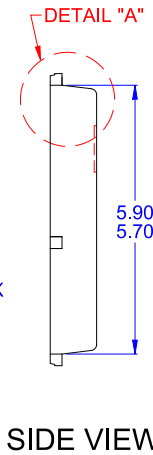
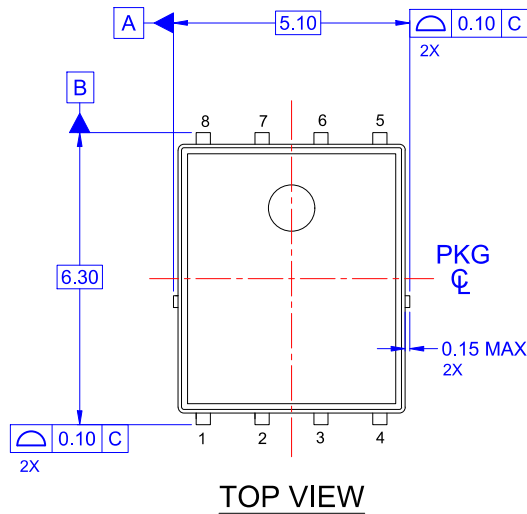
PACKAGE DIMENSIONS

ON Semiconductor®



DFN8 5.1x6.3, 1.27P
CASE 506DW
ISSUE O

DATE 28 FEB 2017



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, ISSUE B, VAR AA, DATED 10/2009.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

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DESCRIPTION:	DFN8 5.1x6.3, 1.27P	PAGE 1 OF 1

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