

NTMD6N04, NVMD6N04

MOSFET – Power, Dual N-Channel, SOIC-8 40 V, 5.8 A

Features

- Designed for use in low voltage, high speed switching applications
- Ultra Low On-Resistance Provides Higher Efficiency and Extends Battery Life
 - $R_{DS(on)} = 0.027 \Omega$, $V_{GS} = 10 \text{ V}$ (Typ)
 - $R_{DS(on)} = 0.034 \Omega$, $V_{GS} = 4.5 \text{ V}$ (Typ)
- Miniature SOIC-8 Surface Mount Package Saves Board Space
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- NVMD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC-DC Converters
- Computers
- Printers
- Cellular and Cordless Phones
- Disk Drives and Tape Drives

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Drain Current (Note 1)	I_D	5.8	Adc
– Continuous @ $T_A = 25^\circ\text{C}$			
– Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	29	Apk
Drain Current (Note 2)	I_D	4.6	Adc
– Continuous @ $T_A = 25^\circ\text{C}$			
Total Power Dissipation	P_D		W
@ $T_A = 25^\circ\text{C}$ (Note 1)		2.0	
@ $T_A = 25^\circ\text{C}$ (Note 2)		1.29	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 40 \text{ Vdc}$, $V_{GS} = 5.0 \text{ Vdc}$, V_{dc} , Peak $I_L = 7.0 \text{ Apk}$, $L = 10 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	245	mJ
Thermal Resistance	$R_{\theta JA}$		$^\circ\text{C/W}$
– Junction-to-Ambient (Note 1)		62.5	
– Junction-to-Ambient (Note 2)		97	
Maximum Lead Temperature for Soldering Purposes for 10 Sec	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1" pad size, $t \leq 10 \text{ s}$

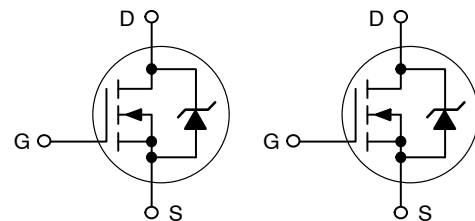


ON Semiconductor®

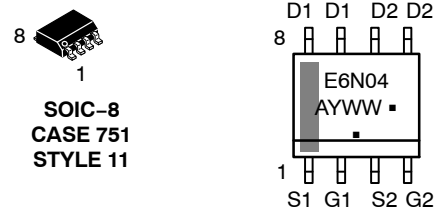
<http://onsemi.com>

V_{DSS}	$R_{DS(on)}$ Typ	I_D Max
40 V	27 m Ω @ $V_{GS} = 10 \text{ V}$	5.8 A

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



E6N04 = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMD6N04R2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NVMD6N04R2G*	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMD6N04, NVMD6N04

2. When surface mounted to an FR4 board using 1" pad size, $t = \text{steady state}$

NTMD6N04, NVMD6N04

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μA) Temperature Coefficient (Positive)	$V_{(BR)DSS}$ $V_{(BR)DSS}/T_J$	40 -	47 45	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 40 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = 40 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	± 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Temperature Coefficient (Negative)	$V_{GS(th)}$ $V_{GS(th)}/T_J$	1.0 -	1.9 4.7	3.0 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V _{GS} = 10 Vdc, I _D = 5.8 Adc) (V _{GS} = 4.5 Vdc, I _D = 3.9 Adc)	R _{DS(on)}	- -	0.027 0.034	0.034 0.043	Ω
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 5.8 Adc)	g _{FS}	-	8.12	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 32 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	-	723	900	pF
Output Capacitance		C _{oss}	-	156	225	
Reverse Transfer Capacitance		C _{rss}	-	53	75	

SWITCHING CHARACTERISTICS (Notes 3 & 4)

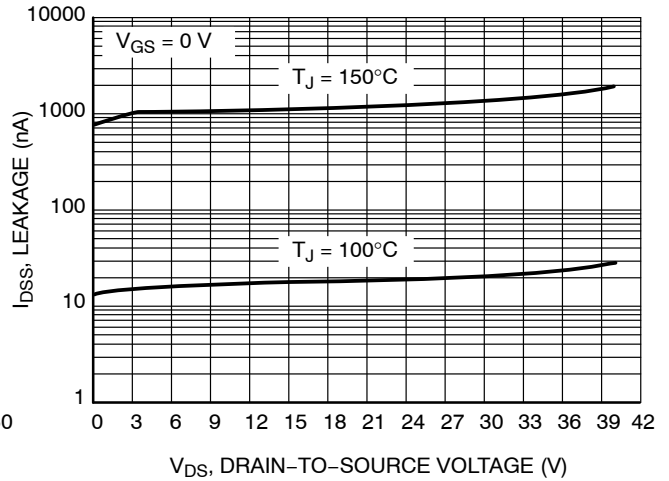
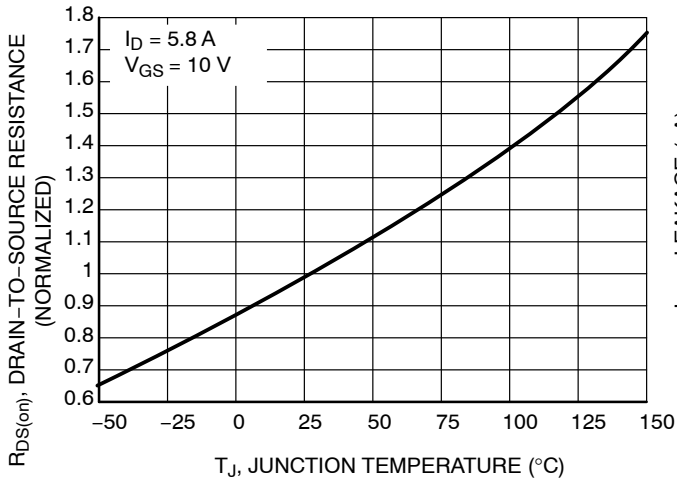
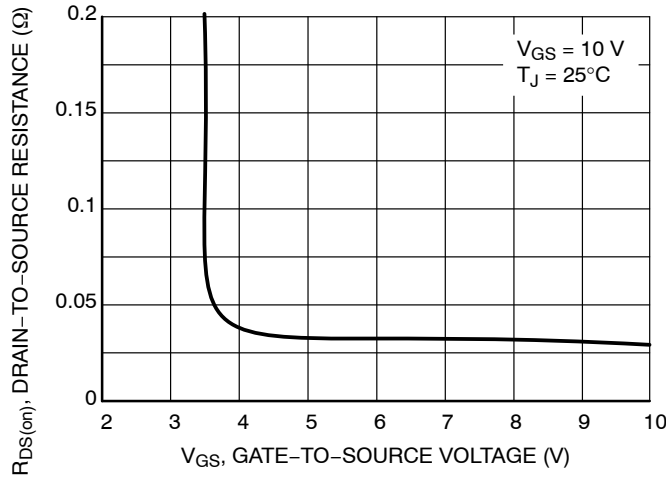
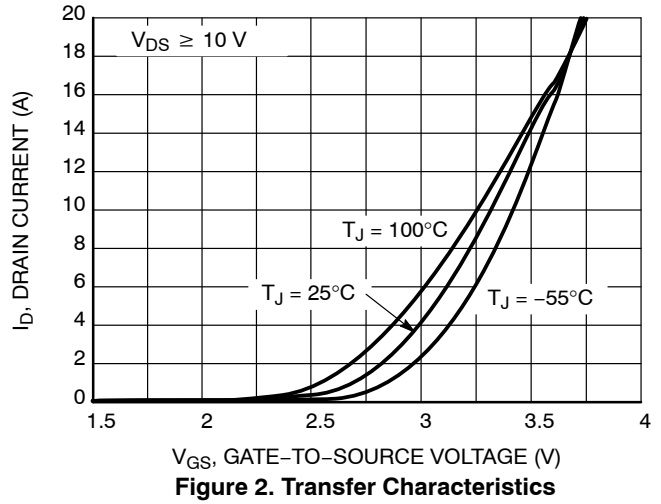
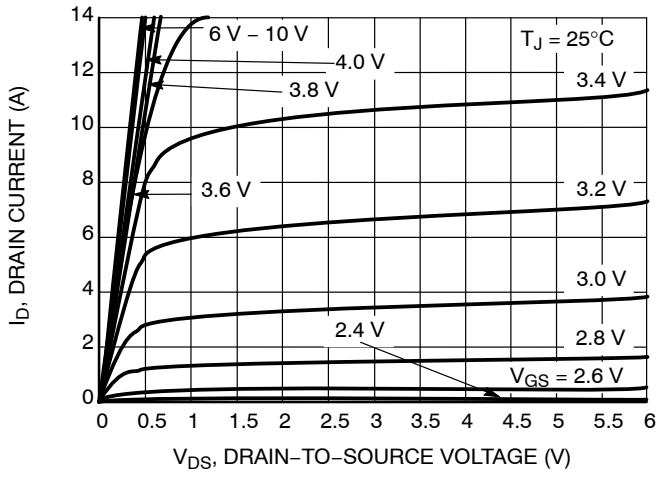
Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 5.8 A, V _{GS} = 10 V, R _G = 6 Ω)	t _{d(on)}	-	10	18	ns
Rise Time		t _r	-	20	35	
Turn-Off Delay Time		t _{d(off)}	-	45	70	
Fall Time		t _f	-	40	65	
Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 5.8 A, V _{GS} = 4.5 V, R _G = 6 Ω)	t _{d(on)}	-	15	-	ns
Rise Time		t _r	-	55	-	
Turn-Off Delay Time		t _{d(off)}	-	30	-	
Fall Time		t _f	-	35	-	
Gate Charge	(V _{DS} = 20 Vdc, V _{GS} = 10 Vdc, I _D = 5.8 A)	Q _T	-	20	30	nC
		Q _{gs}	-	2.5	-	
		Q _{gd}	-	5.5	-	

BODY-DRAIN DIODE RATINGS (Note 3)

Diode Forward On-Voltage	(I _S = 1.7 Adc, V _{GS} = 0 V) (I _S = 1.7 Adc, V _{GS} = 0 V, T _J = 150°C)	V _{SD}	- -	0.76 0.56	1.1 -	Vdc
Reverse Recovery Time	(I _S = 1.7 A, V _{GS} = 0 V, di _S /dt = 100 A/μs)	t _{rr}	-	23	-	ns
		t _a	-	16	-	
		t _b	-	7	-	
Reverse Recovery Stored Charge (I _S = 1.7 A, di _S /dt = 100 A/μs, V _{GS} = 0 V)		Q _{RR}	-	20	-	nC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

NTMD6N04, NVMD6N04



NTMD6N04, NVMD6N04

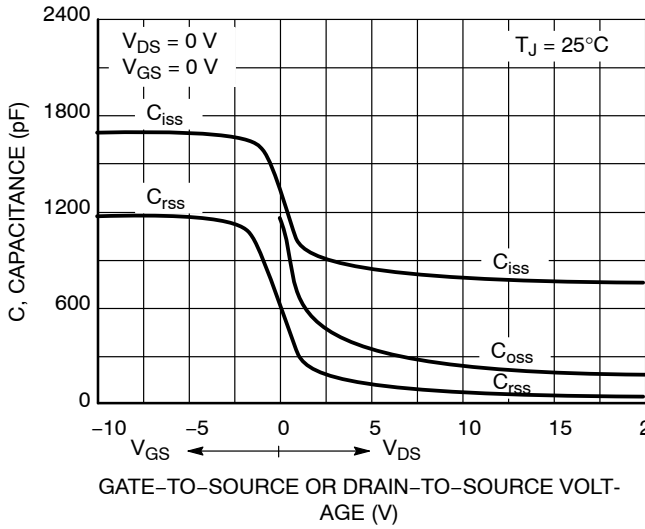


Figure 6. Capacitance Variation

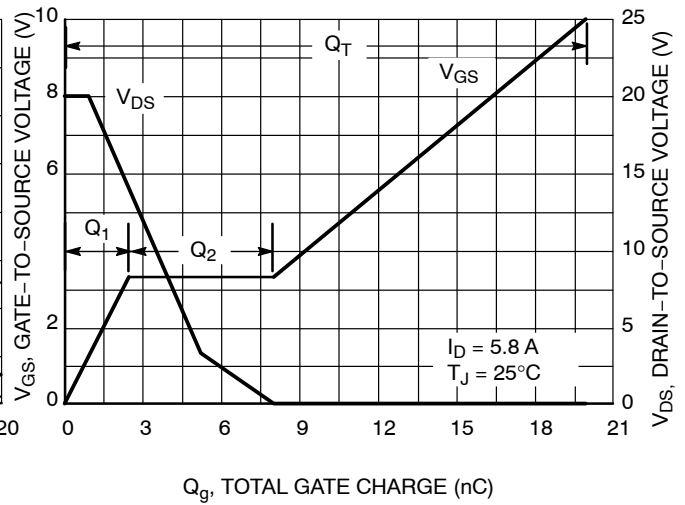


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

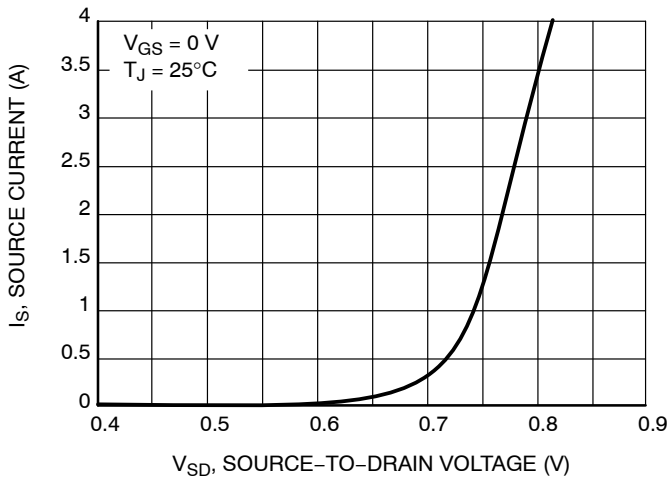


Figure 8. Diode Forward Voltage vs. Current

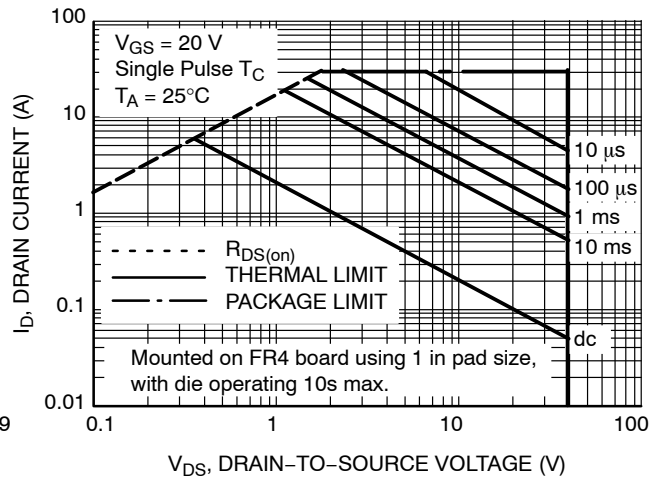
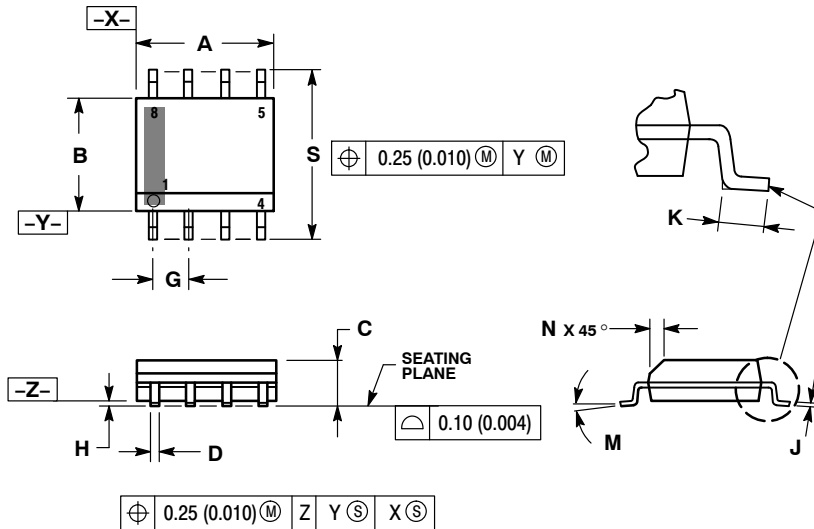


Figure 9. Maximum Rated Forward Biased Safe Operating Area

NTMD6N04, NVMD6N04

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

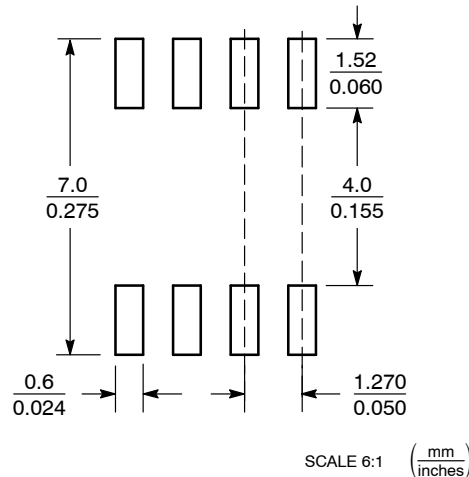


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 11:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative