

# **General Description**

The B32CDM8, B48CDM8 and the B64CDM8 are 8 by 8 (row by column) dot matrix LED displays combined with a multiplexed drive, integrated circuit with a cascadable serial interface. The displays are designed so that they can be mounted in a horizontal chain and can also be expanded in a vertical plane allowing versatile displays to be built. The cascade direction is user selectable. The devices are available in high efficiency red, green and yellow colour variants. LED sizes include (active display area) 32mm by 32mm, 38mm by 38mm and 60mm by 60mm.

The on board driver chip has a serial input format that features serial data, clock and chip enable. A single 5 volt supply is required. The serial bus signals interface is HCMOS levels and the format is compatible with SPI, QSPI and MICROWIRE. It features slew rate limiting for reduced EMI. The undecoded mode allows the driver to be programmed with row and column data thus allowing a wide range of characters to be generated. An external resistor sets the maximum brightness that can then be digitally dimmed in 16 levels. A test mode forces all LED's on. Low power shutdown reduces current to 150uA.

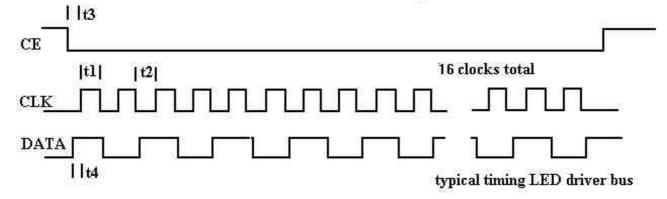
Configuration		Dimer	nsions	
	Dim (mm)	B32	B48	B64
	A	2.54	2.54	2.54
	В	4.0	6.0	7.62
	C	32.0	38.0	60.4
	D	32.0	38.0	60.4
	Е	2.75	5.0	5.0
	Depth	18.0	18.0	18.0

Pinout

2	3	4	5
Data i/o	Chip select	Clock	0V L
Data i/o	Chip select	Clock	0V R
В	С		
Data i/o L	Data input		
Data i/o R	Data input		
	Data i/o B Data i/o L	Data i/oChip selectBCData i/o LData input	Data i/oChip selectClockBCData i/o LData input

Parameter	Min	Тур	Max	Units	Conditions
Supply voltage	4.0	5.0	5.5	V	
Shutdown supply current			150	uA	All leds off
Power supply current		330		mA	All segs on
Display scan rate	500	800	1300	Hz	8 digits scanned
Input voltage logic 0 (VL)	-0.3		0.8	V	Vcc=5.0 volts
Input voltage logic 1 (VH)	3.5			V	Vcc=5.0 volts
Segment drive current(seg off)			1	uA	
Segment drive current(seg on)	-30	-40	-45	mA	
Segment matching		3		%	
Output sink current (digit off)			10	uA	Vdig=10 volts
Output sink current (digit on)	320			mA	Vout=0.65
Clock High time	50			ns	tr = tf = 20ns
Clock Low time	50			ns	
Clock period	100			ns	
CS fall to SCLK rise setup	25			ns	
Clk rise to CS rise hold time	0			ns	
Din setup time	25			ns	
Din hold time	0			ns	
Output data prop delay			25	ns	
Load rising edge to next clk rising edge	50			ns	
Minimum CS or load pulse high time	50			ns	
Data input to seg delay	2.5			ns	
Data input hold time	300			ns	
Brightness setting resistor		9.53		k ohms	Vdd=5V +/- 109
Operating temperature	0		70	deg C	Vdd=5V 4 LED
					on

LED Driver Bus Timing



# **Pin Functions**

## +5v Pin 1

+5 volts power supply to LED's and driver chip tolerance +-10%

# Data i/o Pin 2

This pin acts as either a data input to the display from the host (or in a cascade the data output from the previous chip) or as a data output to the next display device in the chain. This pin is used to daisy chain devices

# Chip enable Pin 3

Chip select - this pin must be low for a data transfer to occur. he last 16 bits of serial data are latched on CS rising edge.

## Clock Pin 4

Clock line - On clocks rising edge data is shifted into the internal shift register. On clocks falling edge data is shifted out of Dout.

## 0 Volts Pin 5

The chip and LED's 0 volts line.

There are also two jumper headers on the device. Designation is ABC. The top jumper corresponds to the left hand side of the display (component view), the bottom the right hand. This jumper field allows selection of the data i/o pin on the i/o headers to be either input or output. THEY WILL ALWAYS BE OPPOSING i.e. one input and one output.

### **Serial Data Format (16 bits)**

10 0 0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Х	Х	Х	Х	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

### **Register Address Map**

Register Auur	css map					
Register	D15-D12	A3	A2	A1	A0	Hex code
No operation	X	0	0	0	0	X0
Column 1	X	0	0	0	1	X1
Column 2	X	0	0	1	0	X2
Column 3	X	0	0	1	1	X3
Column 4	X	0	1	0	0	X4
Column 5	X	0	1	0	1	X5
Column 6	X	0	1	1	0	X6
Column 7	X	0	1	1	1	X7
Column 8	X	1	0	0	0	X8
Decode mode	X	1	0	0	1	X9
Intensity	X	1	0	1	0	XA
Scan limit	X	1	0	1	1	XB
Shutdown	X	1	1	0	0	XC
Display test	X	1	1	1	1	XF

# Display command Register Functions

Mode	Address	D7	D6	D5	D4	D3	D2	D1	D0
Shutdown	XCh	Х	Х	Х	Х	Х	Х	Х	0
Mode									
Normal	XCh	Х	Х	Х	Х	Х	Х	Х	1
Operation									

## Shutdown register Format (address Xch)

Decode Mode Register: Setting this register sets no decode operation for each column. Each bit in the register corresponds to one column. A logic 0 enables non decode mode. In non decode mode data bits 0 to 7 correspond to the row lines as outlines in the table below.

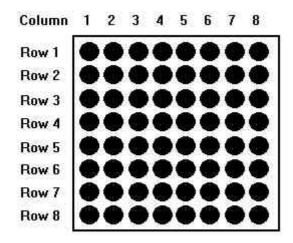
### **Decode Mode register**

Decode Mode	D7	D6	D5	D4	D3	D2	D1	D0	Hex code
No decode for digits 7-0	0	0	0	0	0	0	0	0	00

### Non Decode Mode

	D7	D6	D5	D4	D3	D2	D1	D0
Row	8	1	2	3	4	5	6	7

Row and Column designation



The LED current is set to a maximum value via an on board resistor. This provides the maximum level of brightness. The LED display controller also features a facility to Digitally set the display brightness from the host microcontroller. This control allows the on board pulse width modulator to control the segment current and thus the brightness.

Duty Cycle	D7-D4	D3	D2	D1	D0	Hex code
1/32 (min)	Don't care	0	0	0	0	X0h
3/32	Don't care	0	0	0	1	X1h
5/32	Don't care	0	0	1	0	X2h
7/32	Don't care	0	0	1	1	X3h
9/32	Don't care	0	1	0	0	X4h
11/32	Don't care	0	1	0	1	X5h
13/32	Don't care	0	1	1	0	X6h
15/32	Don't care	0	1	1	1	X7h
17/32	Don't care	1	0	0	0	X8h
19/32	Don't care	1	0	0	1	X9h
21/32	Don't care	1	0	1	0	XAh
23/32	Don't care	1	0	1	1	XBh
25/32	Don't care	1	1	0	0	XCh
27/32	Don't care	1	1	0	1	XDh
29/32	Don't care	1	1	1	0	XEh
31/32	Don't care	1	1	1	1	XFh

#### **Intensity Register Format**

The display also features a scan limit register that sets how many columns are displayed from 1 to 8. These are displayed in a multiplexed manner with a typical display scan rate of 800Hz. Since the number of digits displayed affects the overall display intensity the scan limit registers should be set to 8

**WARNING:** Exercise care to ensure the driver chip does not dissipate excessive power. Using the devices in elevated temperatures without decreasing the driver chip dissipation may result in damage to the device. This can be done by reducing the brightness at elevated temperatures

Scan Limit	D7-D3	D2	D1	D0	Hex		
					code		
Column 0	Dont care	0	0	0	X0h		
Column 0,1	Dont care	0	0	1	X1h		
Column 0,1,2	Dont care	0	1	0	X2h		
Column 0,1,2,3	Dont care	0	1	1	X3h		
Column 0,1,2,3,4	Dont care	1	0	0	X4h		
Column 0,1,2,3,4,5	Dont care	1	0	1	X5h		
Column 0,1,2,3,4,5,6	Dont care	1	1	0	X6h		
Column 0,1,2,3,4,5,6,7	Dont care	1	1	1	X7h		

#### Scan Limit Register format

# LED display characteristics

The Led display provides excellent output brightness verses forward current with intensity matching of better than 10% and a long operating life with minimal display degradation.

**EMC:** The displays are designed with slew limited drivers to ensure minimal EMC emissions. However the cable that is wired to the display is a large source of unwanted emissions. Care should be taken to ensure minimal cable lengths are used where ever possible and a ferrite ring should be added to the cable to provide additional attenuation. The LED's draw quite a high instantaneous current and the power supply and its wiring should be designed to carry the current whilst providing a low impedance path. Additional capacitance may be required at the display. The end product must be compliant with the relevant criteria and the user should check that the display is connected such that it is so.

# LED brightness Min/Typ (mCd)

Color	32mm	48mm	60mm
Green	1.78 / 4.0	1.8 / 4.8	1.8 / 4.8
HE Red	1.78 / 4.0	1.8 / 4.8	1.8 / 4.8
Yellow	1.78 / 3.6	1.8 / 4.5	1.8 / 4.5

**Cascading displays:** The displays are cascadable by connecting the Dout pin from the first display to the Din pin on the next display in line. The other signals (chip enable and clock) are common to all displays. The number of data bits remains the same for each display hence if 4 displays are cascaded then 64 bits are required to alter the displayed value ON ANY DISPLAY. The command set allows for a NO OPERATION which leaves the addressed display with the previous register values.

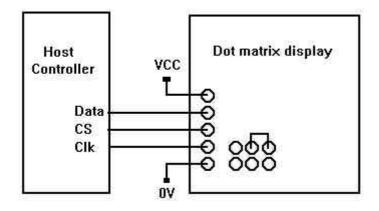
**MAXIMUM RATINGS**: THE USER IS DIRECTED TOWARDS THE MAXIMUM VALUES OUTLINED IN THE ELECTRICAL CHARACTERISTICS. OPERATION OUTSIDE OF THESE LIMITS MAY AFFECT PERMANENT DAMAGE TO THE LED DISPLAY OR THE DRIVER CHIP.

**Additional Information:** The user is directed towards the Maxim Integrated Products data sheet for the MAX7219/MAX7221 for information regarding the serial interface and further display driver commands.

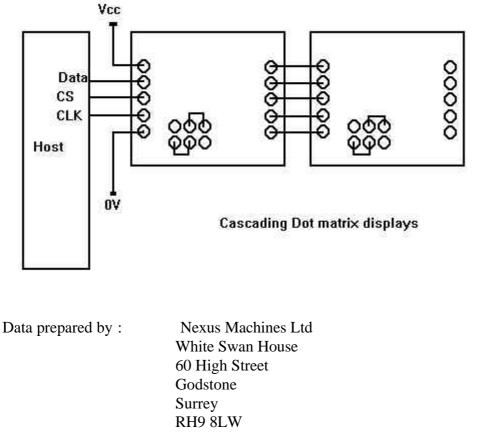
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# **Typical Applications**

Simple single display to microcontroller interface.



Cascading a second dot matrix LED/driver module. If more than 2 devices are connected in the chain then the VCC and 0V wiring should be done using external bussing.



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Please note that the technical support line is charged at £1.00 per minute