Product Change Notification - SYST-23FJMO505

Date:

25 Oct 2019

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - ATtiny1614/1616/1617 Automotive Silicon Errata and Data Sheet Clarification

Notification text:

SYST-23FJMO505

Microchip has released a new Product Documents for the ATtiny1614/1616/1617 Automotive Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny1614/1616/1617 Automotive Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Updated document template. 2) Updated errata 2.4.3 ADC Functionality. 3) Added clarification for ADCn.CALIB.DUTYCYC register description 4) Added clarification for electrical characteristics of ADC and PTC peripheral.
Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 25 Oct 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

ATtiny1614/1616/1617 Automotive Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

ATTINY1614-SSF
ATTINY1614-SSFR
ATTINY1614-SSN
ATTINY1614-SSNR
ATTINY1616-MBT-V01
ATTINY1616-MBT-V03
ATTINY1616-MBT-V07
ATTINY1616-MBT-V09
ATTINY1616-MBT-VAO
ATTINY1616-MFR
ATTINY1616-MNR
ATTINY1616-MNRA0
ATTINY1616-MZT-V02
ATTINY1616-MZT-V04
ATTINY1616-MZT-VAO
ATTINY1616-SF
ATTINY1616-SFR
ATTINY1616-SN
ATTINY1616-SNR
ATTINY1617-MB-VAO
ATTINY1617-MBT-V08
ATTINY1617-MBT-VAO
ATTINY1617-MF
ATTINY1617-MFR
ATTINY1617-MN
ATTINY1617-MNR
ATTINY1617-MZ-V06
ATTINY1617-MZ-VAO
ATTINY1617-MZT-V05
ATTINY1617-MZT-V06
ATTINY1617-MZT-VAO

ATtiny1614/1616/1617 Automotive Silicon Errata and Data Sheet Clarification

The ATtiny1614/1616/1617 Automotive devices you have received conform functionally to the current device data sheet (DS40002021), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the ATtiny1614/1616/1617 Automotive devices.

Note:

- This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.
- Refer to the Device/Revision ID section in the current device data sheet (DS40002021) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance.

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.
- ***** This silicon revision was never released to production.

Peripheral	Issue Summary	Affected Revisions
		Rev. A
Device	2.2.1 On 24-Pin Automotive Devices Pin PC5 is Not Available	X
AC	2.3.1 AC Interrupt Flag Not Set Unless Interrupt is Enabled	X
	2.3.2 False Triggers May Occur Under Certain Conditions	X
	2.3.3 False Triggering When Sweeping Negative Input of the AC When the Low-Power Mode is Disabled	X
ADC	2.4.1 SAMPDLY and ASDV Does Not Work Together With SAMPLEN	X
	2.4.2 Pending Event Stuck When Disabling the ADC	X
	2.4.3 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X
	2.4.4 ADC Interrupt Flags Cleared When Reading RESH	X
	2.4.5 Changing ADC Control Bits During Free-Running Mode not Working	X
	2.4.6 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X
	2.4.7 ADC Wake-Up with WCOMP	X
CCL	2.5.1 Connecting LUTs in Linked Mode Require OUTEN Set to ‘1’	X
	2.5.2 D-latch is Not Functional	X
RTC	2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X
	2.6.2 Disabling the RTC Stops the PIT	X
TCB	2.7.1 Minimum Event Duration Must Exceed the Selected Clock Period	X
	2.7.2 The TCB Interrupt Flag is Cleared When Reading CCMPH	X
	2.7.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock	X
	2.7.4 The TCA Restart Command Does Not Force a Restart of TCB	X
TCD	2.8.1 TCD Event Output Lines May Give False Events	X
	2.8.2 TCD Auto-Update Not Working	X
TWI	2.9.1 TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible	X
	2.9.2 TWI Master Mode Wrongly Detects the Start Bit as a Stop Bit	X
	2.9.3 TWI Smart Mode Gives Extra Clock Pulse	X
	2.9.4 The TWI Master Enable Quick Command is Not Accessible	X

.....continued		
Peripheral	Issue Summary	Affected Revisions
		Rev. A
USART	2.10.1 TXD Pin Override Not Released When Disabling the Transmitter	X
	2.10.2 Frame Error on a Previous Message May Cause False Start Bit Detection	X

2. Silicon Errata Issues

2.1 Errata Details

- **-** Erratum is not applicable.
- **X** Erratum is applicable.
- ***** This silicon revision was never released to production.

2.2 Device

2.2.1 On 24-Pin Automotive Devices Pin PC5 is Not Available

On 24-pin automotive devices pin PC5 is not available.

Work around

Do not connect pin PC5 and disable input on pin (PORTC.PINTCRL5.ISC=0x4).

Affected Silicon Revisions

Rev. A							
X							

2.3 AC - Analog Comparator

2.3.1 AC Interrupt Flag Not Set Unless Interrupt is Enabled

ACn.STATUS.CMP is not set if the ACn.INTCTRL.CMP is not set.

Work around

Enable ACn.INTCTRL.CMP or use ACn.STATUS.STATE for polling.

Affected Silicon Revisions

Rev. A							
X							

2.3.2 False Triggers May Occur Under Certain Conditions

False triggers may occur on falling input pin:

- If the slew rate on the input signal is greater than 2 V/µs for common-mode voltage below 0.5V
- If the slew rate on the input signal is greater than 10 V/µs for common-mode voltage above 0.5V
- If the slew rate on the input signal is greater than 10 V/µs for any common-mode voltage and Low-Power mode is enabled

Work around

None.

Affected Silicon Revisions

Rev. A							
X							

2.3.3 False Triggering When Sweeping Negative Input of the AC When the Low-Power Mode is Disabled

A false trigger may occur if sweeping the negative input of the AC with a negative slope, and the AC has Low-Power mode disabled.

Work around
Enable Low-Power mode in AC.CTRLA.LPMODE.

Affected Silicon Revisions

Rev. A							
X							

2.4 ADC - Analog-to-Digital Converter

2.4.1 SAMPDLY and ASDV Does Not Work Together With SAMPLEN

Using SAMPCTRL.SAMPLEN at the same time as CTRLD.SAMPDLY or CTRLD.ASDV will cause an unpredictable sampling length.

Work around
When setting SAMPCTRL.SAMPLEN greater than 0x0, the CTRLD.SAMPDLY and CTRLD.ASDV must be cleared.

Affected Silicon Revisions

Rev. A							
X							

2.4.2 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work around
Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. A							
X							

2.4.3 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work around
If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. A							
X							

2.4.4 ADC Interrupt Flags Cleared When Reading RESH

ADCn.INTFLAGS.RESRDY and ADCn.INTFLAGS.WCOMP are cleared when reading ADCn.RESH.

Work around
In 8-bit mode, read ADCn.RESH to clear the flag or clear the flag directly.

Affected Silicon Revisions

Rev. A							
X							

2.4.5 Changing ADC Control Bits During Free-Running Mode not Working

If control signals are changed during Free-Running mode, the new configuration is not properly taken into account in the next measurement. This is valid for the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL registers and the ADC.MUXPOS, ADC.WINLT and ADC.WINHT registers.

Work around
Disable ADC Free-Running mode before updating the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL, ADC.MUXPOS, ADC.WINLT or ADC.WINHT registers.

Affected Silicon Revisions

Rev. A							
X							

2.4.6 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work around
Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. A							
X							

2.4.7 ADC Wake-Up with WCOMP

When waking up from STANDBY Sleep mode with ADC WCOMP interrupt, the ADC is disabled for a few cycles before the device enters ACTIVE mode. A new INITDLY is required before the next conversion.

Work around
Use INITDLY before the next conversion.

Affected Silicon Revisions

Rev. A							

X							

2.5 CCL - Configurable Custom Logic

2.5.1 Connecting LUTs in Linked Mode Require OUTEN Set to '1'

Connecting the LUTs in linked mode require LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work around
Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. A							
X							

2.5.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work around
None.

Affected Silicon Revisions

Rev. A							
X							

2.6 RTC - Real-Time Counter

2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Work around
None.

Affected Silicon Revisions

Rev. A							
X							

2.6.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work around
Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. A							
X							

2.7 TCB - Timer/Counter B

2.7.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work around

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

Affected Silicon Revisions

Rev. A							
X							

2.7.2 The TCB Interrupt Flag is Cleared When Reading CCMPH

TCBn.INTFLAGS.CAPT is cleared when reading TCBn.CCMPH instead of CCMPL.

Work around

Read both TCBn.CCMPL and TCBn.CCMPH.

Affected Silicon Revisions

Rev. A							
X							

2.7.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock

The TCB Input Capture Frequency and Pulse-Width Measurement mode may lock to Freeze state if CLKSEL in TCB.CTRLA is set to any other value than 0x0.

Work around

Only use CLKSEL equal to 0x0 when using Input Capture Frequency and Pulse-Width Measurement mode.

Affected Silicon Revisions

Rev. A							
X							

2.7.4 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Work around

None.

Affected Silicon Revisions

Rev. A							
X							

2.8 TCD - Timer/Counter D

2.8.1 TCD Event Output Lines May Give False Events

The TCD event output lines can give out false events.

Work around
Use the delayed event functionality with a minimum of one cycle delay.

Affected Silicon Revisions

Rev. A							
X							

2.8.2 TCD Auto-Update Not Working

The TCD auto-update feature is not working.

Work around
None.

Affected Silicon Revisions

Rev. A							
X							

2.9 TWI - Two-Wire Interface

2.9.1 TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible

The TIMEOUT bits in the TWI.MCTRLB register are not accessible from software.

Work around
When initializing TWI, BUSSTATE in TWI.MSTATUS should be brought into IDLE state by writing 0x1 to it.

Affected Silicon Revisions

Rev. A							
X							

2.9.2 TWI Master Mode Wrongly Detects the Start Bit as a Stop Bit

If TWI is enabled in Master mode followed by an immediate write to the MADDR register the bus monitor recognizes the Start bit as a Stop bit.

Work around
Wait for a minimum of two clock cycles from TWI.MCTRLA.ENABLE until TWI.MADDR is written.

Affected Silicon Revisions

Rev. A							
X							

2.9.3 TWI Smart Mode Gives Extra Clock Pulse

TWI Master with Smart mode enabled gives an extra clock pulse on the SCL line after sending NACK.

Work around
None.

Affected Silicon Revisions

Rev. A							
X							

2.9.4 The TWI Master Enable Quick Command is Not Accessible

TWI.MCTRLA.QCEN is not accessible from software.

Work around
None.

Affected Silicon Revisions

Rev. A							
X							

2.10 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.10.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work around
There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. A							
X							

2.10.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work around

Wait for the RxD pin to go high before reading RXDATA, for instance by polling the bit in PORTn.IN where the RxD pin is located.

Affected Silicon Revisions

Rev. A							
X							

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002021):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 ADC - Analog-to-Digital Converter

3.1.1 Calibration

Clarifications have been made to the ADCn.CALIB.DUTYCYC register description:

- **Redundant text referring to a minimum operating voltage of 2.7V has been removed.**
- **CLK_{ADC} information moved to ADC electrical characteristics.**

Bit 0 - DUTYCYC Duty Cycle

This bit determines the duty cycle of the ADC clock.

Value	Description
0	50% Duty Cycle
1	25% Duty Cycle

3.2 Electrical Characteristics

3.2.1 ADC

A clarification has been made to the electrical characteristics for the ADC peripheral:

- Added a note for 50% duty cycle

Table 3-1. Clock and Timing Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{ADC}	Sample rate	1.1V ≤ V_{REF}	15	-	115	ksps
		1.1V ≤ V_{REF} (8-bit resolution)	15	-	150	
		V_{REF}=0.55V (10-bit)	7.5	-	20	
CLK_{ADC}	Clock frequency	V_{REF}=0.55V (10-bit)	100	-	260	kHz
		1.1V ≤ V_{REF} (10-bit)	200	-	1500	
		1.1V ≤ V_{REF} (8-bit resolution)	200	-	2000(1)	
Ts	Sampling time		2	2	33	CLK_{ADC} cycles
T_{CONV}	Conversion time (latency)	Sampling time = $2CLK_{ADC}$	8.7	-	50	µs
T_{START}	Start-up time	Internal V_{REF}	-	22	-	µs

Note:

1. **50% duty cycle is required for clock frequencies above 1500 kHz.**

3.2.2 PTC Characteristics - Operating Ratings

Clarifications have been made to the electrical characteristics for the PTC peripheral:

- Redundant V_{DD} and CLK_{PER} characteristics have been removed

- CLK_{ADC} characteristics have been added

Table 3-2. Peripheral Touch Controller Characteristics - Operating Ratings

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
C_{LOAD}	Maximum load		-	48	-	pF
C_{INT}			-	30	-	pF
	Driven Shield Capacitive Drive		-	300	-	pF
CLK_{ADC}	**Supported ADC clock frequency**	**25% duty cycle**	**200**	**-**	**1500**	**kHz**
		50% duty cycle	**200**	**-**	**2000**	

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc Rev.	Date	Comments
B	10/2019	• Updated document template. • Updated errata 2.4.3 ADC Functionality. • Added clarification for ADCn.CALIB.DUTYCYC register description. • Added clarification for electrical characteristics of ADC and PTC peripheral.
A	06/2019	• Initial document release.

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