Product Change Notification - SYST-23PDCT521

Date:

25 Oct 2019

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - ATtiny202/402 Silicon Errata and Data Sheet Clarification

Notification text:

SYST-23PDCT521

Microchip has released a new Product Documents for the ATtiny202/402 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny202/402 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Updated document template. 2) The ADC errata, ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions, has been split into two separate erratas and rewritten. 3) Added clarification for ADC electrical characteristics.
Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 25 Oct 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

ATtiny202/402 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATTINY202-SSF
ATTINY202-SSFR
ATTINY202-SSN
ATTINY202-SSNR
ATTINY402-SSF
ATTINY402-SSFR
ATTINY402-SSN
ATTINY402-SSNR

ATtiny202/402

ATtiny202/402 Silicon Errata and Data Sheet Clarification

The ATtiny202/402 devices you have received conform functionally to the current device data sheet (DS40001969), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the ATtiny202/402 devices.

Note:

- This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.
- Refer to the Device/Revision ID section in the current device data sheet (DS40001969) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance.

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.
- ***** This silicon revision was never released to production.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A	Rev. B
Device	2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)	*	X
ADC	2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	*	X
	2.3.2 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	*	X
	2.3.3 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	*	X
CCL	2.4.1 Connecting LUTs in Linked Mode Require OUTEN Set to '1'	*	X
	2.4.2 D-latch is Not Functional	*	X
RTC	2.5.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	*	X
	2.5.2 Disabling the RTC Stops the PIT	*	X
TCB	2.6.1 Minimum Event Duration Must Exceed the Selected Clock Period	*	X
	2.6.2 The TCA Restart Command Does Not Force a Restart of TCB	*	X
USART	2.7.1 TXD Pin Override Not Released When Disabling the Transmitter	*	X
	2.7.2 Frame Error on a Previous Message May Cause False Start Bit Detection	*	X

2. Silicon Errata Issues

2.1 Errata Details

- **-** Erratum is not applicable.
- **X** Erratum is applicable.
- ***** This silicon revision was never released to production.

2.2 Device

2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)

The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

Work around

If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.3 ADC - Analog-to-Digital Converter

2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work around

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.3.2 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.3.3 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and VDD < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for VDD < 2.7V.

Work around
None.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Require OUTEN Set to '1'

Connecting the LUTs in linked mode require LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work around
Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work around
None.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.5 RTC - Real-Time Counter

2.5.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Work around
None.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.5.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work around

Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.6 TCB - Timer/Counter B

2.6.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work around

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.6.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Work around

None.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.7 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.7.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

2.7.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work around

Wait for the RxD pin to go high before reading RXDATA, for instance by polling the bit in PORTn.IN where the RxD pin is located.

Affected Silicon Revisions

Rev. A	Rev. B						
*	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001969):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Electrical Characteristics

3.1.1 ADC

A clarification has been made to the electrical characteristics for the ADC peripheral:

- Added a note for 50% duty cycle

Table 3-1. Clock and Timing Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{ADC}	Sample rate	1.1V ≤ V_{REF}	15	-	115	ksps
		1.1V ≤ V_{REF} (8-bit resolution)	15	-	150	
		V_{REF}=0.55V (10-bit)	7.5	-	20	
CLK_{ADC}	Clock frequency	V_{REF}=0.55V (10-bit)	100	-	260	kHz
		1.1V ≤ V_{REF} (10-bit)	200	-	1500	
		1.1V ≤ V_{REF} (8-bit resolution)	200	-	2000(1)	
Ts	Sampling time		2	2	33	CLK_{ADC} cycles
T_{CONV}	Conversion time (latency)	Sampling time = $2CLK_{ADC}$	8.7	-	50	µs
T_{START}	Start-up time	Internal V_{REF}	-	22	-	µs

Note:

1. **50% duty cycle is required for clock frequencies above 1500 kHz.**

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc Rev.	Date	Comments
B	10/2019	• Updated document template. • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten. • Added clarification for ADC electrical characteristics.
A	06/2019	• Initial document release.

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