UM11216

PCA9420 evaluation board user manual

Rev. 1.1 — 16 October 2019 User manual

Document information

Information	Content
Keywords	PCA9420UK; PCA9420BS evaluation board
Abstract	This user manual provides guidelines on how to use the PCA9420 evaluation board

Revision history

Revision history

Rev	Date	Description
v.1.1	20191016	Updated Figure 9, Figure 10; updated Section 10
v.1	20190718	Initial version

1 PCA9420UK (WLCSP) and PCA9420BS (QFN) Evaluation Board

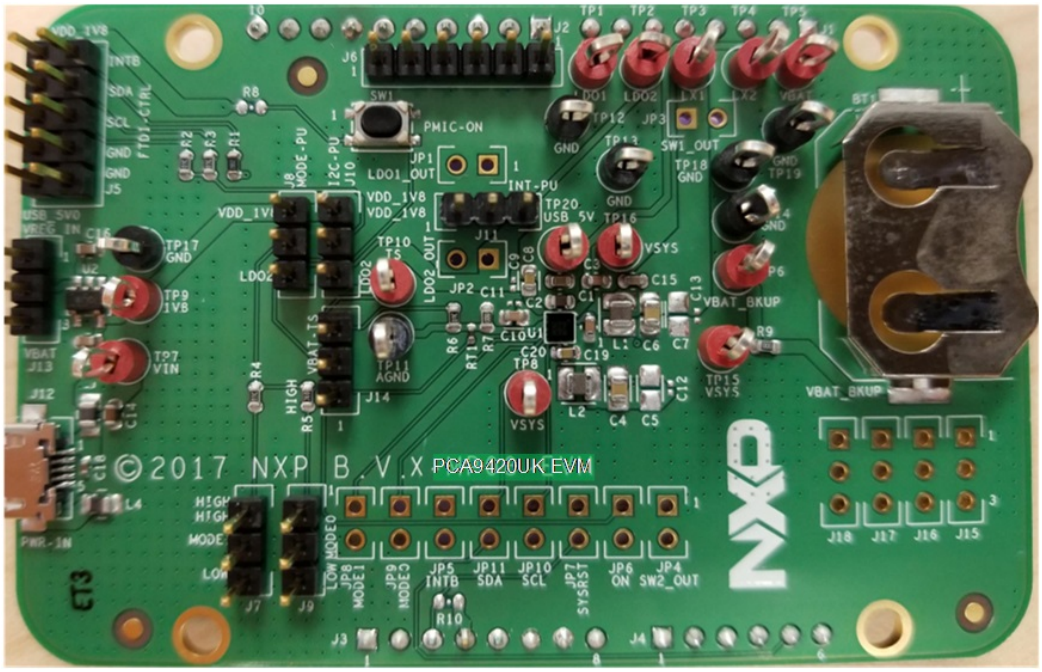

Figure 1. PCA9420UK Evaluation Board

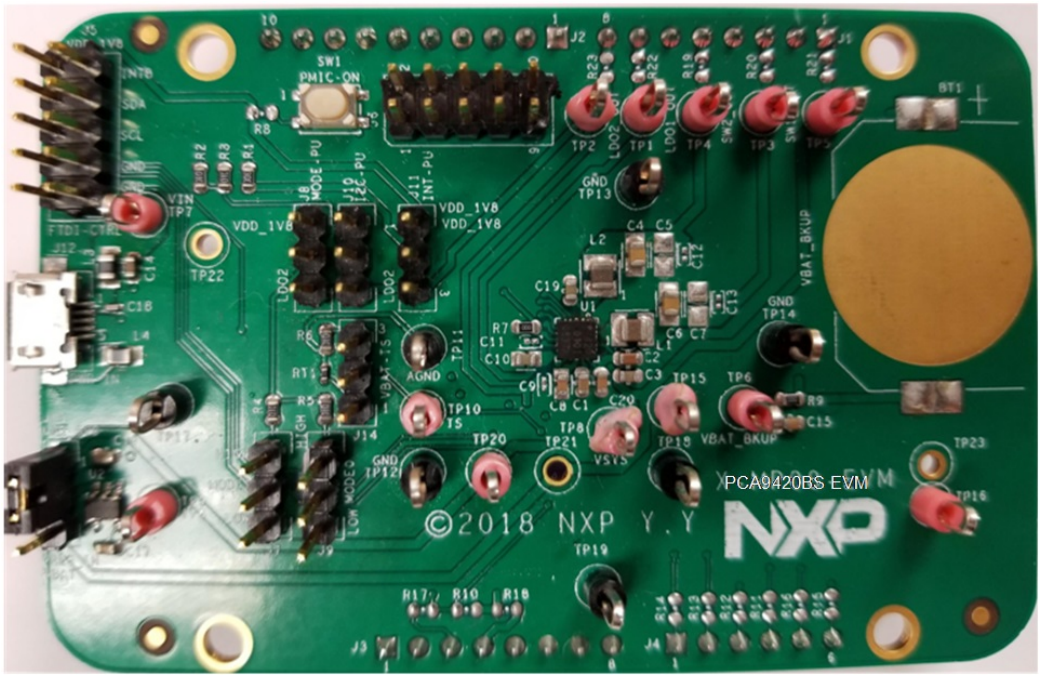

Figure 2. PCA9420BS Evaluation Board

2 Kit contents/packing list

The kit contents include:

- Assembled and tested PCA9420UK and PCA9420BS evaluation board in an anti-static bag
- USB to MPSSE Serial cable for I^2C communication
- USB 2.0 Cable
- Spare jumpers

3 Required equipment

To use this kit, the equipment needed is:

- 1-cell Li-ion Battery
- 5.0V power supply or USB with enough current capability (1.5A or above for maximum performance)
- PCA9420 GUI installed on a Windows PC
- Multimeters to measure regulator outputs
- Oscilloscope (optional)
- USB enabled computer running Windows XP, Vista, 7, 8, or 10

4 Device description

The PCA9420UK/PCA9420BS is a highly-integrated Power Management IC (PMIC), targeted to provide a full power management solution for low power microcontroller applications or other similar applications. The device consists of a linear battery charger capable of charging up to 315mA current. It has I^2C programmable Constant Current (CC) and Constant Voltage (CV) values for flexible configuration. Various built-in protection features such as input overvoltage protection, overcurrent protection, thermal protection, etc. are also provided for safe battery charging. It also features JEITA compliant charging. The device also integrates two step-down (buck) DC/DC converters which have I^2C programmable output voltage. Both buck regulators have integrated high-side and low- side switches and related control circuitry, to minimize the external component counts; a Pulse-Frequency Modulation (PFM) approach is utilized to achieve better efficiency under light load condition. Other protection features such as overcurrent protection, under-voltage lockout (UVLO), etc. are also provided. By default, the input for these regulators is powered by either VIN or VBAT, whichever is greater.

In addition, two on-chip LDO regulators are provided to power up various voltage rails in the system.

Other features such as FM+ I^2C interface, chip enable, interrupt signal, etc. are also provided.

The chip is offered in 2.09mm x 2.09mm, 5 x 5 bump, 0.4mm pitch WLCSP package; and 3mm x 3mm, 24-pin QFN package.

5 Key features

- Linear battery charger for charging single cell li-ion battery
- 20V tolerance on VIN pin
- Programmable input OVP (5.5V or 6V)
- Programmable constant current (up to 315 mA) and pre-charge low voltage current threshold
- Programmable constant voltage regulation
- Programmable automatic recharge voltage and termination current threshold
- Built-in protection features such as input OVP, battery SCP, thermal protection
- JEITA compliant
- Battery attached detection
- Over-temperature protection
- Two step-down DC/DC converters with very low quiescent current
- Programmable output voltage
- SW1: core buck converter, 0.5V~1.5V output, 25mV/step, and a fixed 1.8V, up to 250mA
- SW2: system buck converter, 1.5V~2.1V/2.7V~3.3V output, 25mV/step, up to 500mA
- Low power mode for extra power saving
- Two LDOs
- Programmable output voltage regulation
- LDO1: always-on LDO, 1.70V~1.90V output, 25mV/step, up to 1mA
- LDO2: system LDO, 1.5V~2.1V/2.7V~3.3V output, 25mV/step, up to 250mA
- 1 MHz I^2C-bus slave interface
- -40°C ~ +85°C ambient temperature range

6 Board description

Figure 3 and Figure 4 describe the main elements on the board.

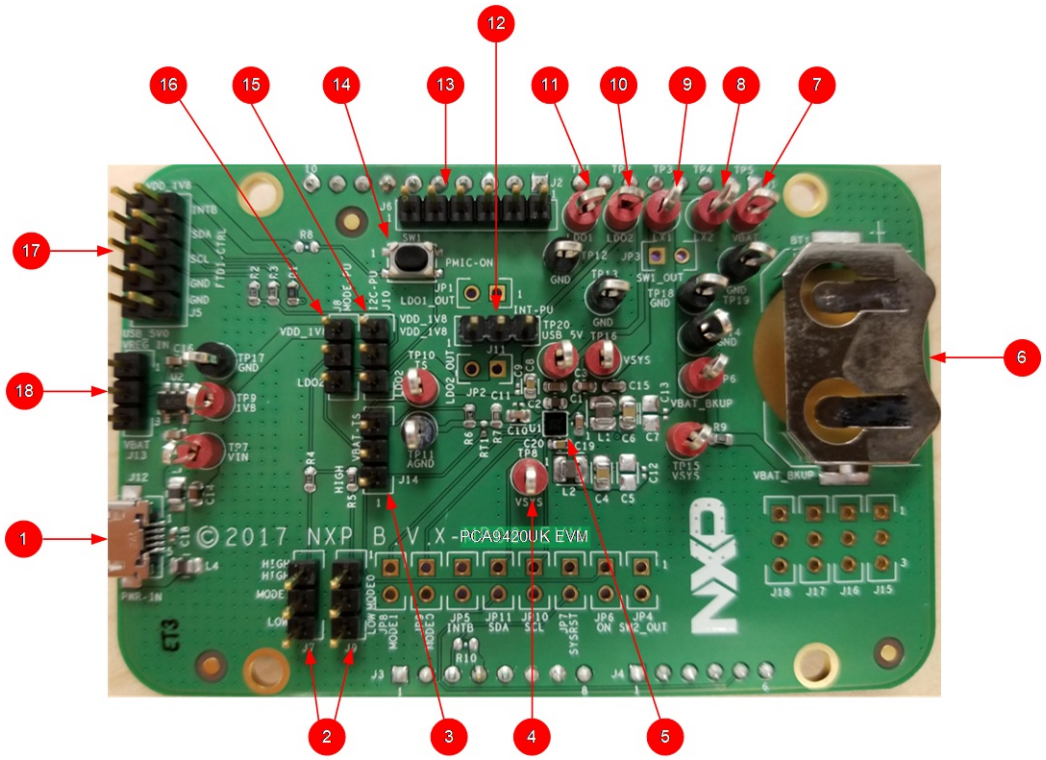

Figure 3. PCA9420UK Board description

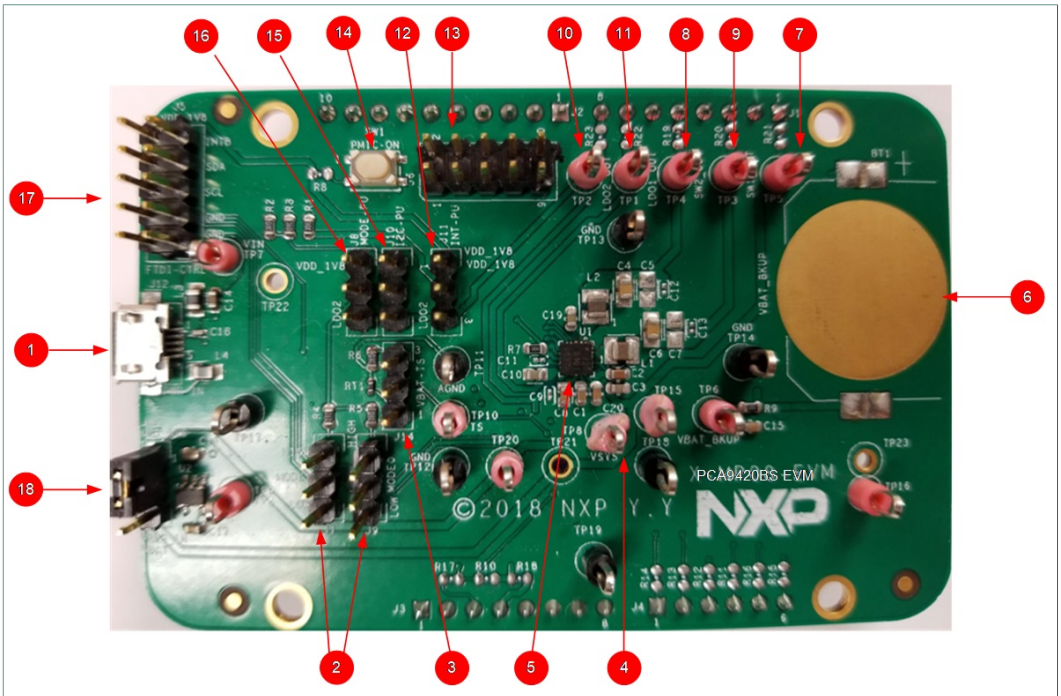

Figure 4. PCA9420BS Board description

Table 1. Board description

Number	Name	Description
1	USB Input	USB power supply for the PCA9420UK
2	Logic pin for MODESEL1&2	Logic high or low for MODESEL1&2 pins
3	VBAT-TS	TS selection pin for either 10k or 100k
4	System Node	Electronic load for system
5	U1	PCA9420UK PMIC
6	VBAT_BKUP	Coil cell battery for back-up purpose
7	VBAT	Connect a Li-ion battery cell
8	SW2_OUT	BUCK2 output
9	SW1_OUT	BUCK1 output
10	LDO2_OUT	LDO2 output
11	LDO1_OUT	LDO1 output
12	INT-PU	Interrupt pull-up to either LDO2 output or an external LDO output
13	PMIC-OUT	All regulators' output
14	SW1	Button connected to ON pin
15	I2C-PU	Logic voltage selection for I^2C
16	MODE-PU	Logic voltage selection for MODESEL0&1 function
17	FTDI-CTRL	I^2C interface
18	VREG_IN	Input selection for an external LDO between VBAT and USB input

7 Jumper and switch definitions

Figure 5 and Figure 6 show the location of jumpers and switch on the evaluation board.

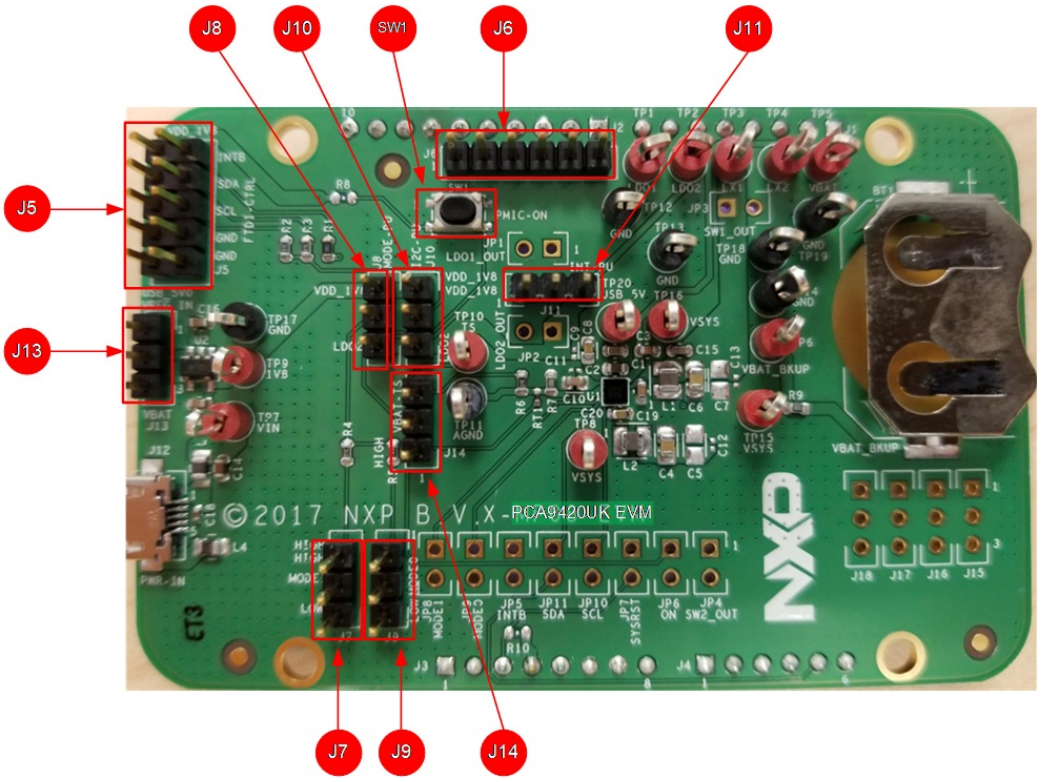

Figure 5. Jumper and switch locations for PCA9420UK

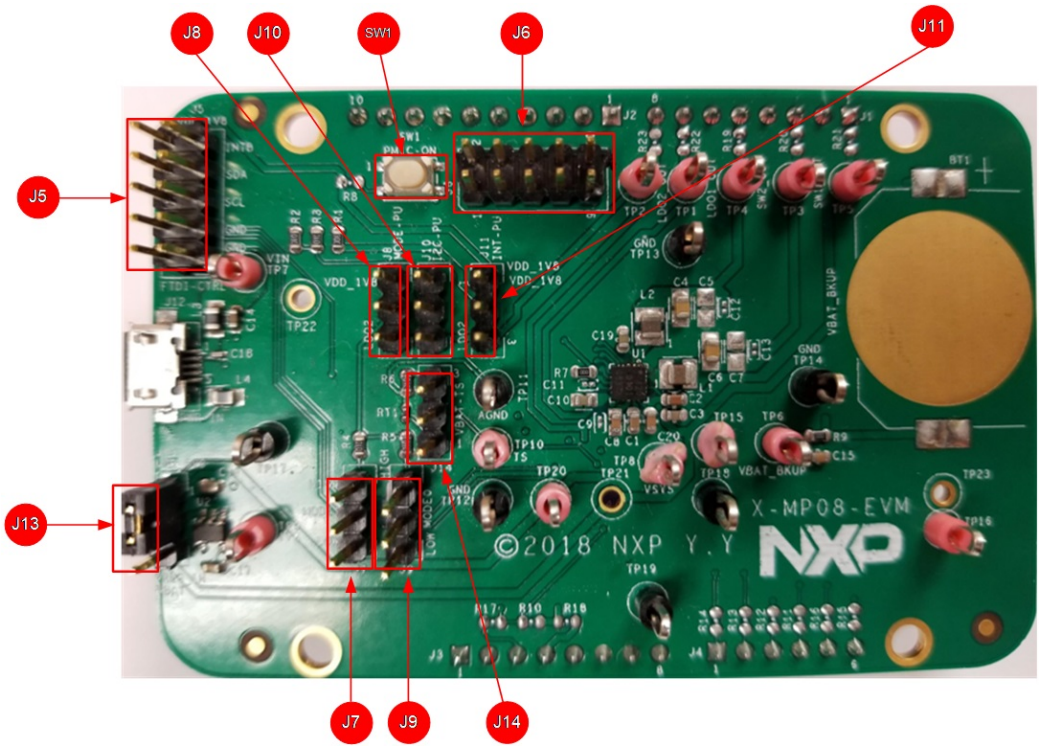

Figure 6. Jumper and switch locations for PCA9420BS

Table 2 describes the function and settings for each jumper and switch.

Table 2. Jumper and switch definitions

Jumper/ Switch	Description	Setting	Connection/Result
SW1	ON	Open	Connect ON pin to ground when pressed. Causes wake-up event of PMIC
J5	FTDI-CTRL		I^2C interface connection with FTDI cable. Orange color for SCL, Yellow and Green color for SDA
J6	Voltage monitor		Measure voltages for PCA9420UK 1: VBAT 2: BUCK2 output 3: BUCK1 output 4: LDO2 output 5: LDO1 output
			Measure voltages for PCA9420BS 1: BUCK1 output 3: VBAT 5: LDO2 output 7: LDO1 output 9: BUCK2 output

Jumper/ Switch	Description	Setting	Connection/Result
J7	Logic configuration for MODESEL0	[1-2]	Logic high
		[2-3]	Logic low
J8	Pullup configuration for MODE function	[1-2]	Pullup to external LDO output
		[2-3]	Pullup to LDO2 output
J9	Logic configuration for MODESEL1	[1-2]	Logic high
		[2-3]	Logic low
J10	Pullup configuration for I/O voltage	[1-2]	Pullup to external LDO output
		[2-3]	Pullup to LDO2 output
J11	Logic voltage configuration for INTB	[1-2]	Pullup to external LDO output
		[2-3]	Pullup to LDO2 output
J13	VDD configuration for external LDO	[1-2]	Pullup to USB input
		[2-3]	Pullup to VBAT
J14	NTC configuration	[1-2]	Pulldown to 100k
		[2-3]	Pulldown to 10k

8 Evaluation Board Connections

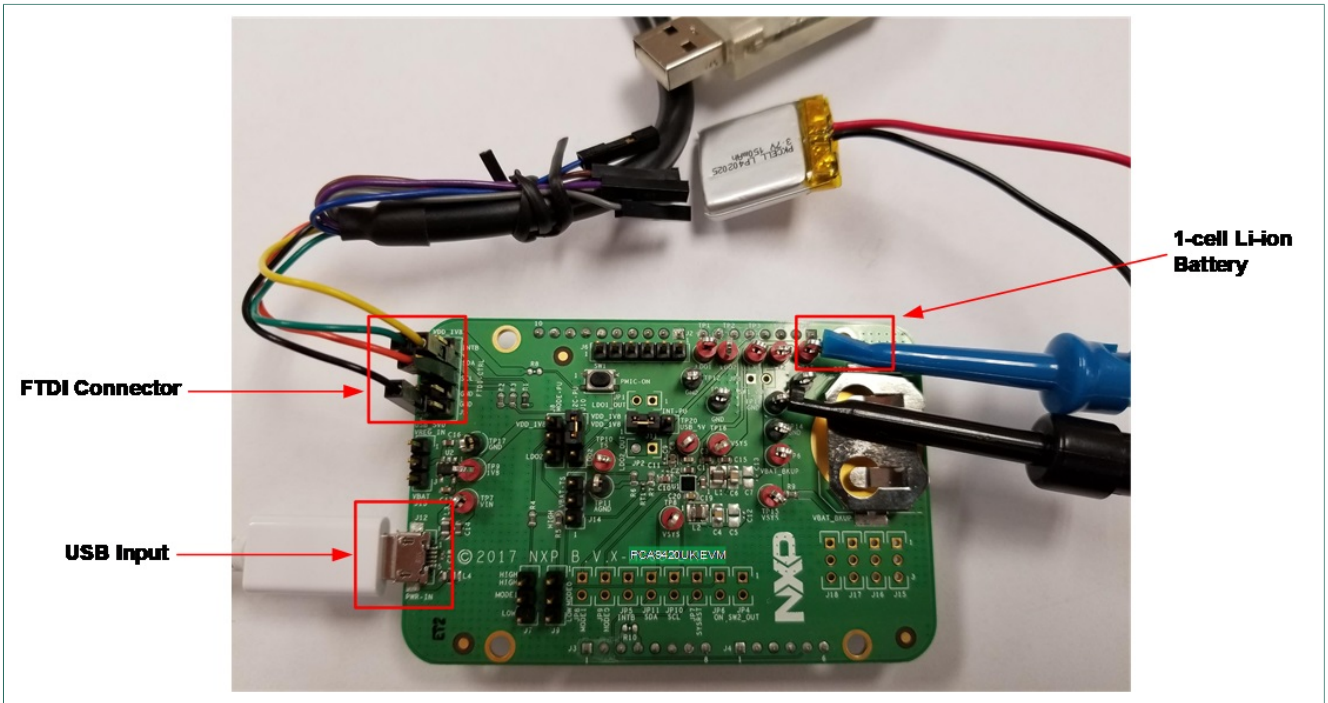

Figure 7. PCA9420UK connection

8.1 Connections

Connect wires on the following pins as shown in Figure 7, and make sure the power supply is turned off during the wiring stage:

- A Li-ion battery – Connect to VBAT test point
- VIN Input – Powered by USB Micro B connector.
- FTDI Connector – Connect to FTDI USB to I2C cable (Yellow/Green to SDA, Orange to SCL, and Black to GND)

9 PCA9420 GUI Software Installation

- Unzip the provided PCA9420 Evaluation Kit GUI installation execution file, follow the step by step instruction on the screen.
- During the installation process, the FTDI interface cable driver will also be installed, please refer to the screen capture for the reference. When correctly installed, the figure shown below on the right pop up on the screen. Click “Finish” button to continue.

Figure 8. GUI Installation

- Once the installation finished, the GUI will be automatically launched. Please note that since the standalone evaluation board has not been powered up, no communication channel is established between the computer (GUI) via the interface cable to the evaluation board, and it shows “Disconnected” at the bottom left of the GUI.

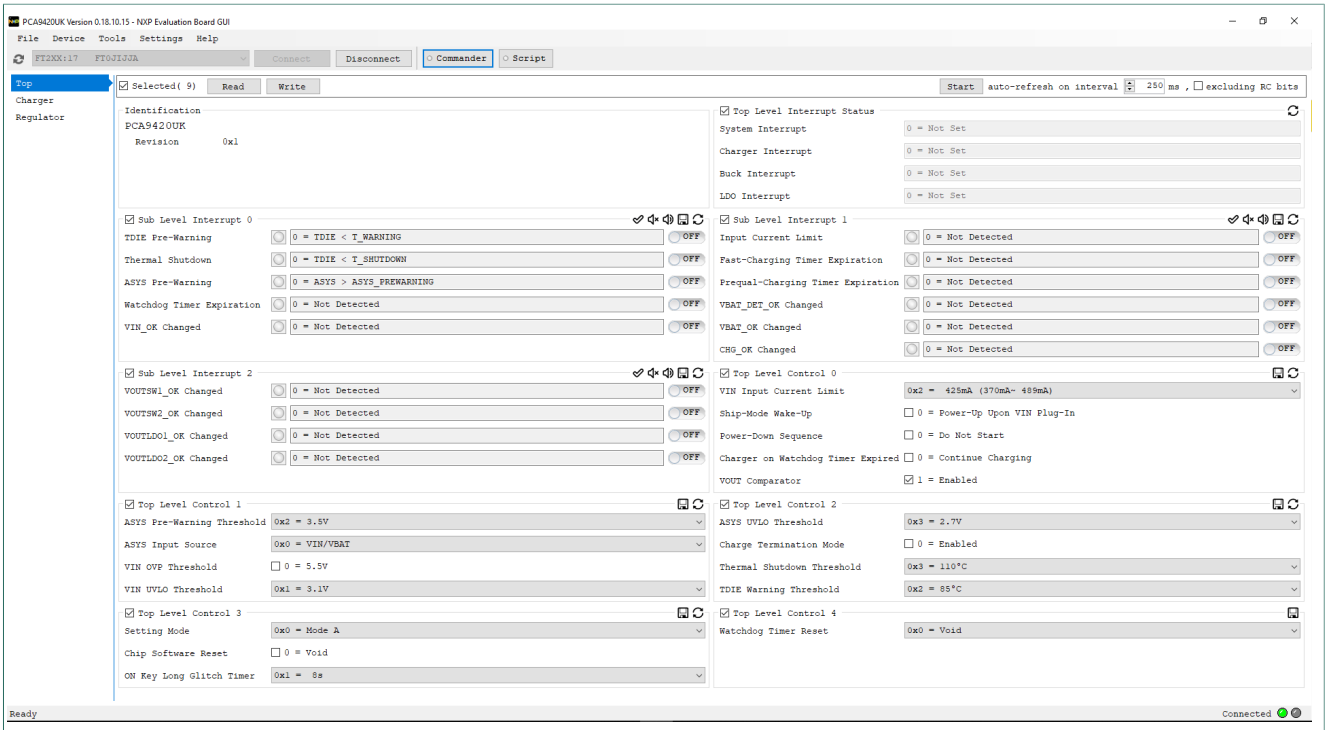

Figure 9. GUI overview

9.1 GUI panels

When the GUI is launched, it looks for a PCA9420UK/PCA9420BS target board connected via the USB cable. If connected, the GUI panels display “Connected” on the bottom left.

10 The GUI Quick Guide

As shown in Figure 10, the GUI is a user-friendly tool which allows access to the on-chip registers to perform write/read commands manually or automatically (depending on GUI setting). Below is a quick guide of the key blocks that the GUI provides.

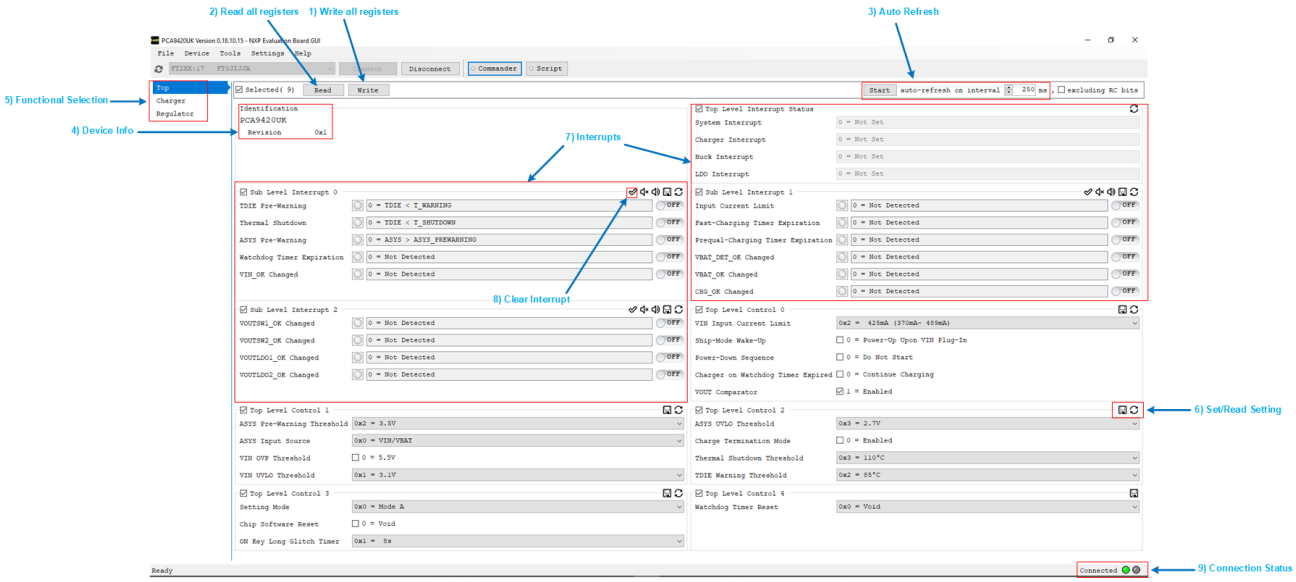

Figure 10. GUI summary

1. **Write All Registers:** Click the write button on the GUI to perform a “write” command to all the designated registers on PCA9420UK/PCA9420BS based on the current GUI setting. It is recommended to disable auto refresh before clicking the write all command, since some of settings might be updated by the auto refresh if turned on.
2. **Read All Registers:** Click the read button on the GUI to perform a “read” command and update all the register values reflected on the GUI
3. **Auto Refresh:** Sets the auto refresh timer for the Interrupts and Status registers. By choosing different options from the drop-down menu, the GUI performs the backend automatic read and refresh functions accordingly.
   - 1/second – Read all registers 1 time per second (1Hz)
   - 2/second – Read all registers 2 times per second (2Hz)
   - 4/second – Read all registers 4 times per second (4Hz)
   - Disabled – Disable the auto read
4. **Device information**: It shows the device ID, device revision and its slave address information. Note that the GUI selects the slave address configured on the evaluation automatically.
5. **Function Selection Tab:** All function related registers are grouped into eight different tabs including “**Top level control**”, “**Interrupts**”, “**Charging Control**”, “**Charging Status**” and “**Group A-D setting**”. Click the tab to access the related registers.
6. **Set/Read Setting:** Set/Read the registers on the selected function tab.
7. **Interrupts:** Related to register 0x01 (TOP_INT), 0x02 (SUB_INT0), 0x04 (SUB_INT1) and 0x06 (SUB_INT2). When related events happen, the unmasked interrupt bits are set and the GUI highlights the checkboxes and changes the background color to RED.
8. **Clear Interrupt:** Related to register 0x02 (SUB_INT0), 0x04 (SUB_INT1) and 0x06 (SUB_INT2). The clear interrupt button is used to CLEAR the interrupt bits. In

the case multiple interrupts bits are set at the same time, the button clears all set interrupts bits.

9. **Connections Status:** When valid communication between GUI and the hardware is established, it shows “**connected**”, otherwise it shows “**disconnected**”. The cable used is also shown at the right side of the connection status bar.

11 Evaluation Board Schematic

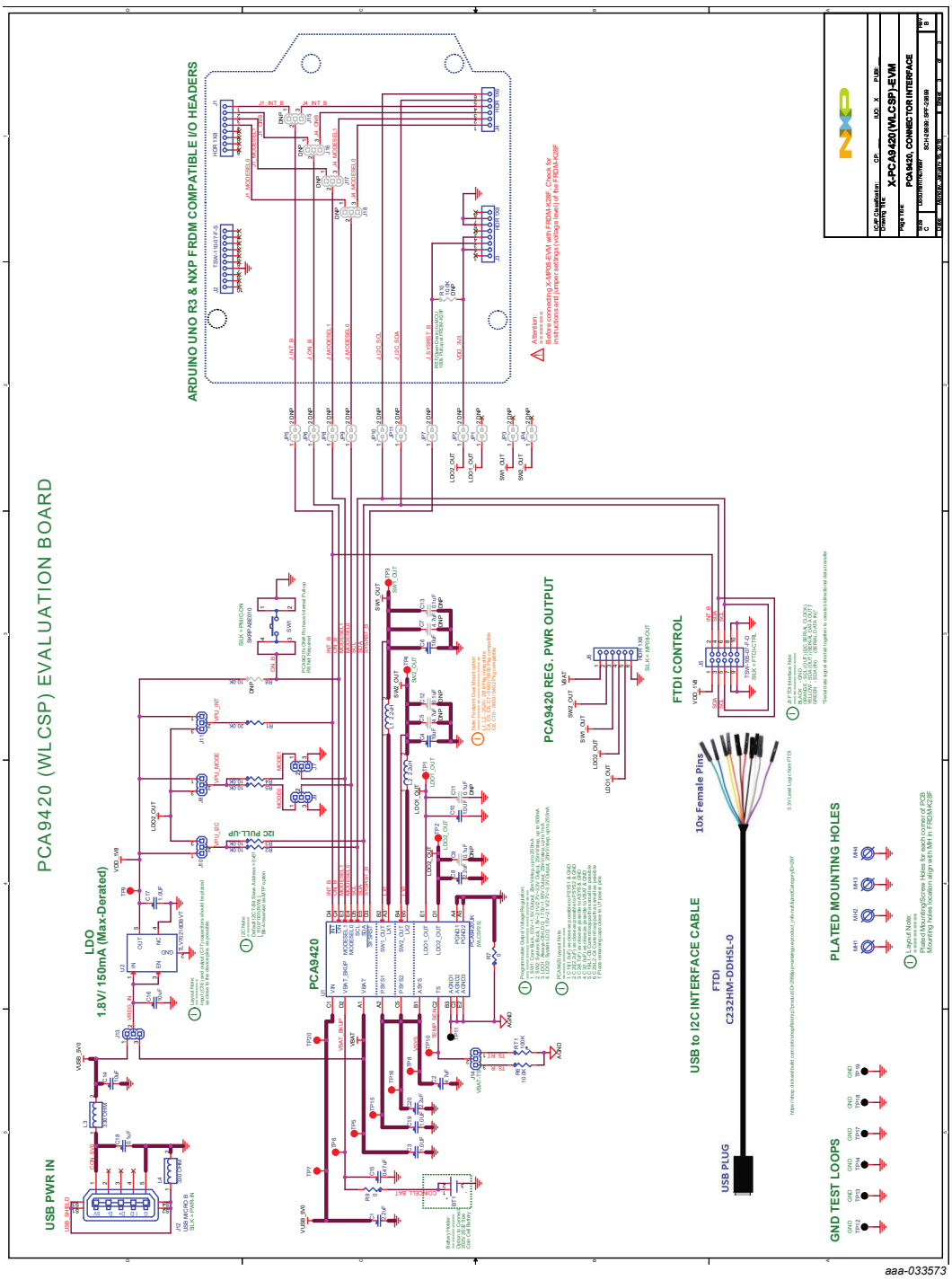

Figure 11. PCA9420 (WLCSP) evaluation board

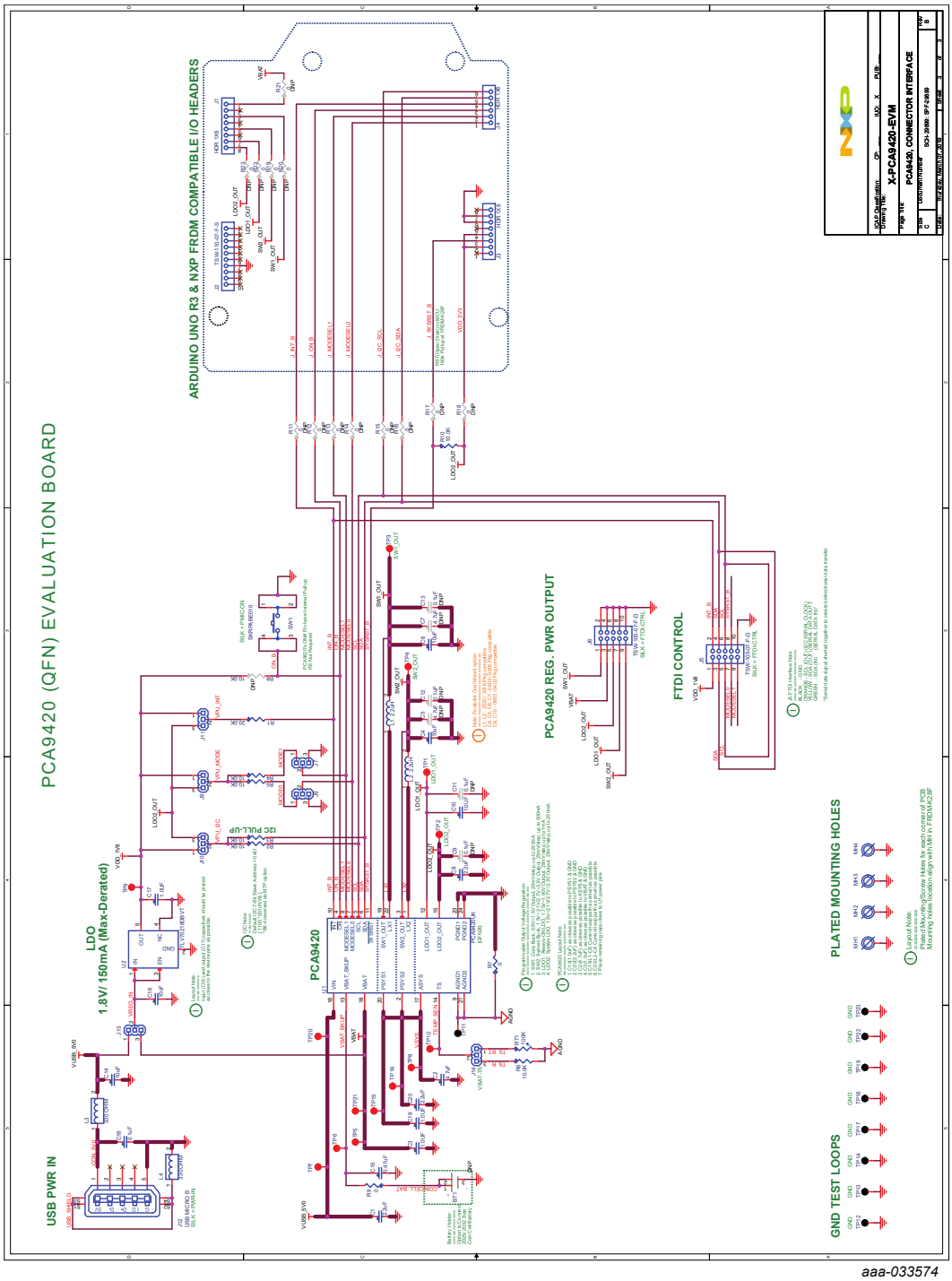

Figure 12. PCA9420 (QFN) evaluation board

12 Evaluation Board BOM List

Table 3. Bill of Materials (BOM)

Ref	Description	Size (inch)	Manufacture	Part Number	Notes
C18	CAP CER 0.1µF 50V 10% X7R	0402	MURATA	GRM155R71H104KE14D	
C3, C10, C17, C19	CAP CER 1.0µF 16V 10% X7R	0603	MURATA	GRM188R71C105KE15	
C15	CAP CER 0.47µF 16V 10% X7R AEC-Q200	0603	MURATA	GCM188R71C474KA55D	
C14, C16	CAP CER 10µF 10V 20% X7R	0603	MURATA	GRM188Z71A106MA73	
C4, C6	CAP CER 10.0µF 16V 10% X7R	0805	MURATA	GRM21BZ71C106KE15	
C1, C8, C20	CAP CER 2.2µF 16V 10% X7R	0603	MURATA	GRM188Z71C225KE43	
C2	CAP CER 4.7µF 16V 10% X7R	0603	MURATA	GRM188Z71C475KE21	
L1, L2	IND PWR 2.2µH@1MHz 2.5A 20%	2016	Samsung Electro Mechanics	CIGT201610EH2R2MNE	
L3, L4	IND FER BEAD 330OHM@100MHZ 2.5A 25% SMT		TDK	MPZ2012S331AT000	
U1	PMIC		NXP	PCA9420UK_WLCSP25	
U2	IC VREG LDO 1.8V 300mA 2-5.5V	SOT23-5	TEXAS INSTRUMENTS	TLV70218DBVT	
R1	RES MF 20.0K 1/10W 1%	0603	BOURNS	CR0603-FX-2002ELF	
R2-R6	RES MF 10.0K 1/10W 1%	0603	YAGEO AMERICA	RC0603FR-0710KL	
R7, R9	RES MF ZERO OHM 1/10W -- AEC-Q200	0603	PANASONIC	ERJ-3GEY0R00V	
RT1	RES THERMISTOR NTC 100K@25 DEGC 100mW 1%	0402	MURATA	NCP15WF104F03RC	
SW1	SW SPST PB SMT 16V 20MA		ALPS ELECTRIC (USA) INC.	SKRPABE010	
BT1	BATTERY HOLDER SMD	CR2025/2032	Linx Technologies	BAT-HLD-001	
TP11-TP14, TP17-TP19	TEST POINT PC MULTI PURPOSE BLK TH		KEYSTONE ELECTRONICS	5011	
TP1-TP10, TP15, TP16, TP20	TEST POINT PC MULTI PURPOSE RED TH		KEYSTONE ELECTRONICS	5010	
J7-J11, J13, J14	HDR 1x3 TH 100MIL SP 343H AU 100L		SAMTEC	TSW-103-07-F-S	
J4, J6	HDR 1X6 TH 100MIL SP 338H AU 100L		SAMTEC	TSW-106-07-F-S	
J5	HDR 2X5 TH 100MIL CTR 338H AU 100L		SAMTEC	TSW-105-07-F-D	

Ref	Description	Size (inch)	Manufacture	Part Number	Notes
J2	HDR 1X10 TH 100MIL CTR 338H AU 100L		SAMTEC	TSW-110-07-F-S	
J1, J3	HDR 1X8 TH 100MIL SP 338H AU 100L		SAMTEC	TSW-108-07-F-S	
J12	CON 5 USB MICRO_ B RA SKT SMT 0.65MM SP 102H AU		WURTH ELEKTRONIK EISOS GMBH & CO. KG	629105136821	
C5, C7	CAP CER 4.7uF 16V 10% X7R	0603	MURATA	GRM188Z71C475KE21	Not Installed
C9, C11-C13	CAP CER 0.1uF 16V 10% X7R	0201	MURATA	GRM033Z71C104KE14	Not Installed
JP1-JP11	HDR 1X2 TH 100MIL SP 338H AU 100L		SAMTEC	TSW-102-07-F-S	Not Installed
J15-J18	HDR 1x3 TH 100MIL SP 343H AU 100L		SAMTEC	TSW-103-07-F-S	Not Installed
R8, R10	RES MF 10.0K 1/10W 1%	0603	YAGEO AMERICA	RC0603FR-0710KL	Not Installed

13 Placement

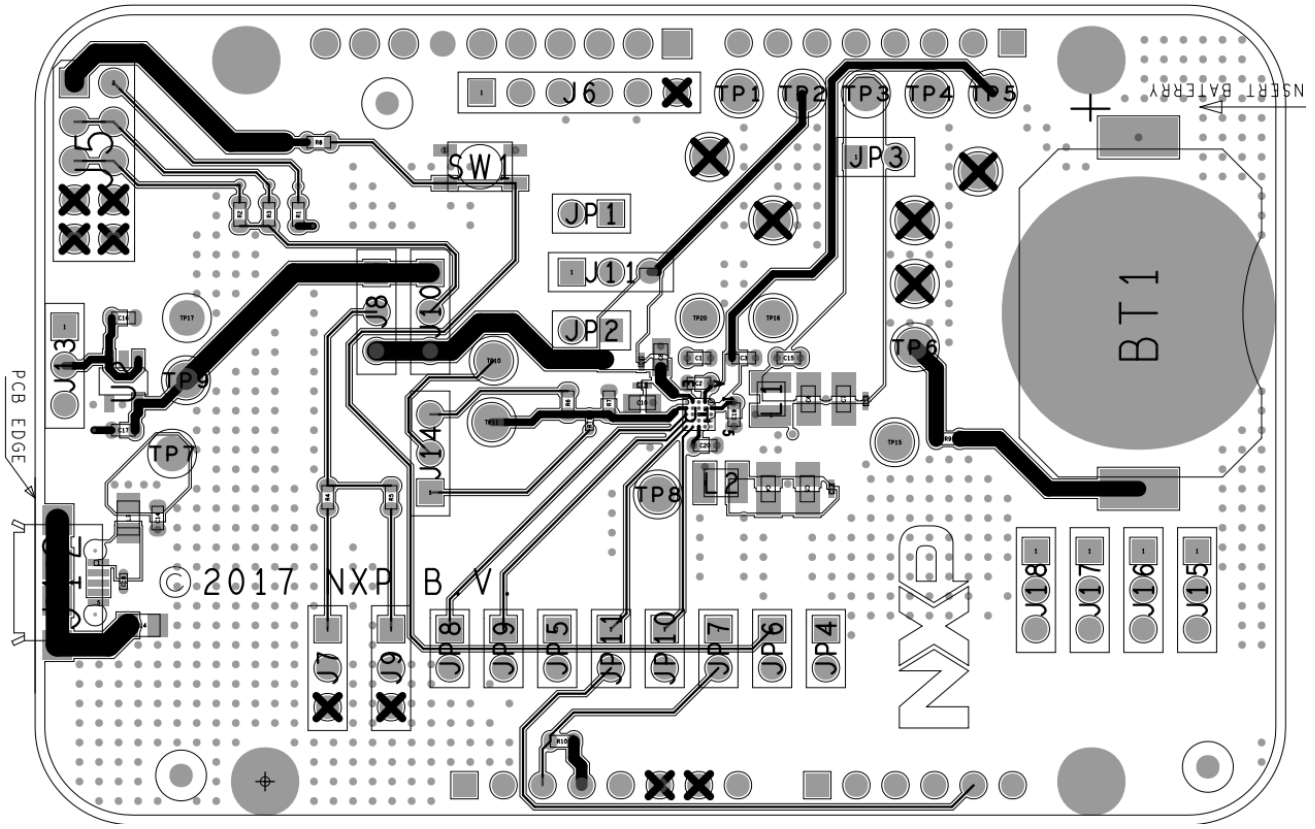

Figure 13. PCA9420UK Evaluation Board Placement

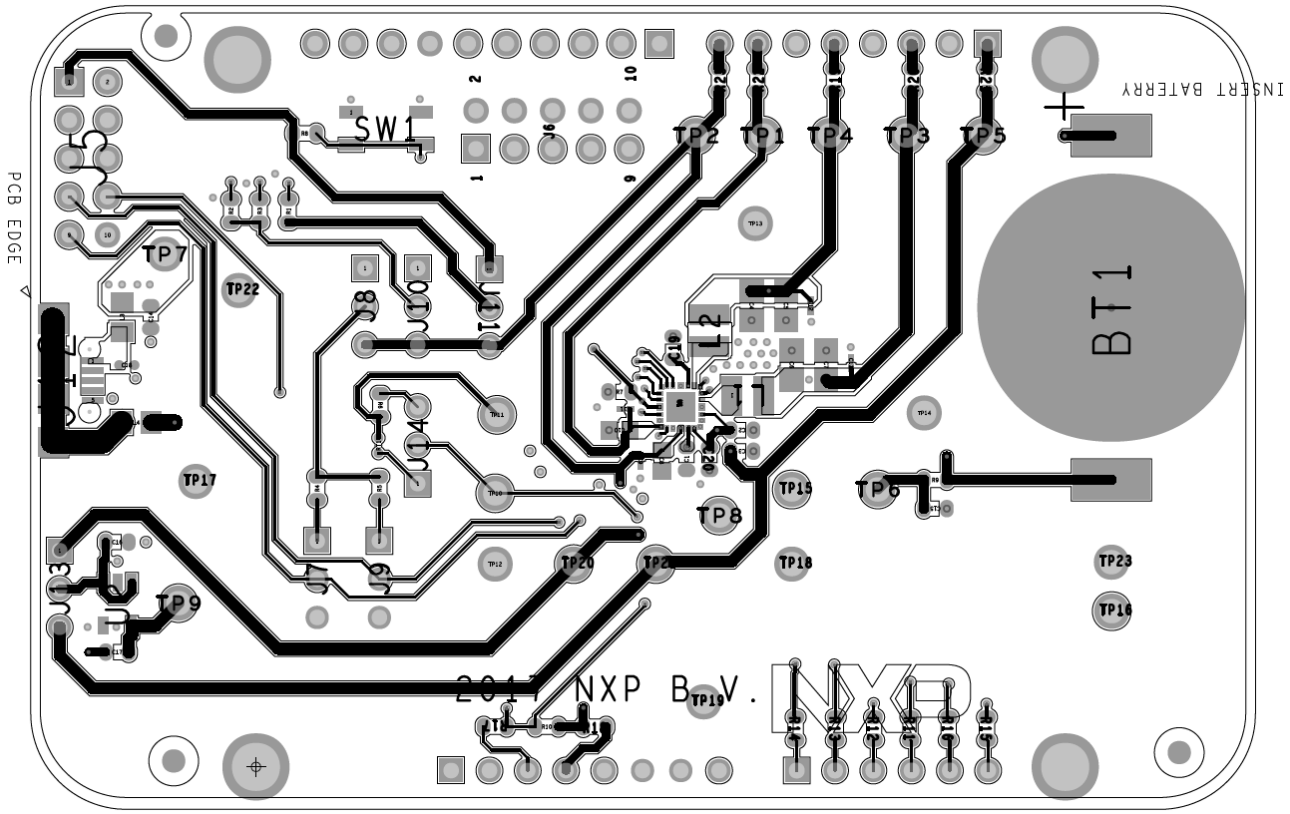

Figure 14. PCA9420BS Evaluation Board Placement

14 Layout Guideline

The following guidelines for PCA9420UK are arranged from most critical to least critical priority:

- Place ASYS input capacitor (C2) as close to ASYS and PGND as possible.
- Place VBAT input capacitor (C3) as close to VBAT and PGND as possible. The input capacitor delivers a high di/dt current pulse when the high-side MOSFET turns on. It is essential that parasitic inductance in the power input traces be minimized for high efficiency and reliability
- Minimize the trace length from LX1, LX2's output capacitor PGND1, PGND2 terminal to the input capacitor's GND terminal. This minimizes the area of the current loop when the high-side MOSFET is conducting. Keep all sensitive signals, such as feedback nodes, outside of these current loops with as much isolation as the design allows.
- Minimize the trace impedance from LX1, LX2 to their respective inductor and from each inductor to the output capacitor for LX1 and LX2. This minimizes the area of each current loop and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency. Keep all sensitive signals, such as feedback nodes outside of these current loops and away from the LX switching voltage with as much isolation as the design allows.
- Create a PGND plane on the 2nd layer of the PCB immediately below the power components and bumps carrying high switching currents. This reduces parasitic inductance in the traces carrying high currents and shields signals on inner PCB layers from the switching waveforms on the top layer of the PCB.

- Connect the feedback terminal (SW1_OUT, SW2_OUT) to the local output capacitors for LX1 and LX2. The SW1_OUT and SW2_OUT connection to the local output capacitors should be placed as close to the PCA9420UK as possible to minimize the effects of voltage drop in the output trace connected to the load.
- Create a small AGND island for the VIN bypass capacitors. Connect this AGND island to the PCA9420UK PGND plane for LX1 and LX2 between the PGND terminals of the SW1_OUT, SW2_OUT output capacitors. This results in the most accurate sensing of the output voltage by the local feedback loop (OUT to AGND).
- Each of the PCA9420UK bumps has approximately the same ability to remove heat from the die. Connect as much metal as possible to each bump to minimize the θ_{JA} associated with the PCA9420UK.

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