Gate Driver Providing Galvanic Isolation Series

Isolation Voltage 2500 Vrms
1ch Gate Driver Providing Galvanic Isolation

BM60060FV-C

General Description

The BM60060FV-C is a gate driver with an isolation voltage of 2500 Vrms. It has an I/O delay time of 210 ns, minimum input pulse width of 90 ns, and incorporates the fault signal output function, under voltage lockout (UVLO) function, short circuit protection (SCP, built-in temperature compensation of detection voltage) function, fast turn off function for short circuit protection, active miller clamping (MC) function, temperature monitoring function, switching controller function, gate resistance switching function and output state feedback function.

Key Specifications

- Isolation Voltage: 2500 Vrms
- Maximum Gate Drive Voltage: 24 V
- I/O Delay Time: 210 ns (Max)
- Minimum Input Pulse Width: 90 ns

Package

Package	W (Typ) x D (Typ) x H (Max)
SSOP-B28W	9.2 mm x 10.4 mm x 2.4 mm

Features

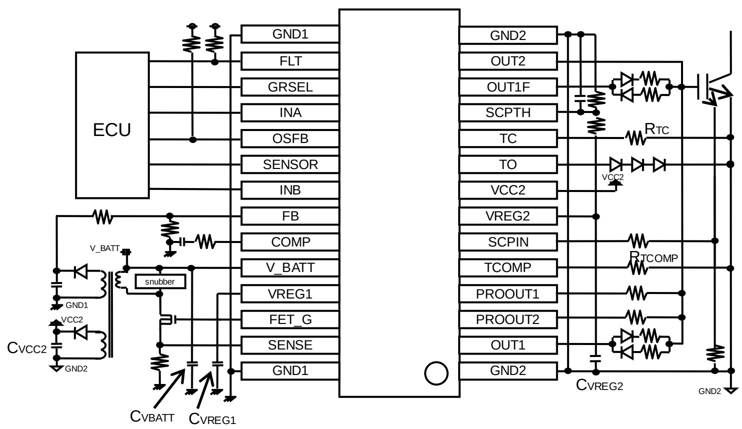
- AEC-Q100 Qualified *(Note 1)*
- Fault Signal Output Function
- Under Voltage Lockout Function
- Short Circuit Protection Function
- Temperature Compensation of Short Circuit Detection Voltage
- Fast Turn Off Function for Short Circuit Protection
- Soft Turn Off Function for Short Circuit Protection (Adjustable Turn Off Time)
- Active Miller Clamping
- Temperature Monitor
- Switching Controller
- Gate Resistance Switching Function
- Output State Feedback Function

(Note 1) Grade1

Applications

- Automotive Inverter
- Automotive DC-DC Converter
- Industrial Inverter System
- UPS System

Typical Application Circuit



〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays.

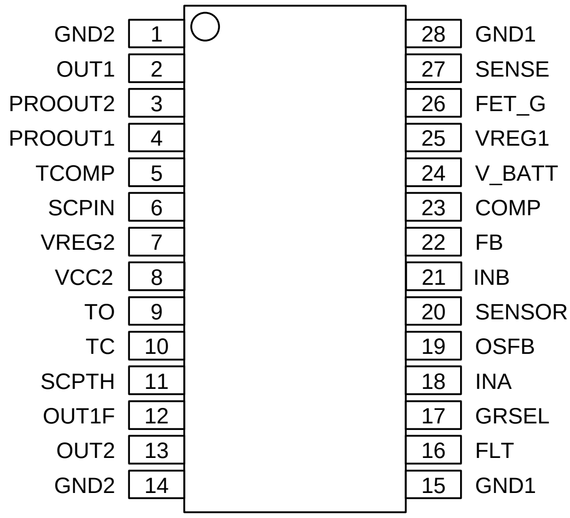
Contents

Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
TC (As Temperature monitor)	R_{TC}	1.25	-	100	kΩ
TC (No Temperature monitor)	R_{TC}	0.1	1	10	MΩ
TCOMP	R_{TCOMP}	9	-	100	kΩ
V_BATT	C_{VBATT}	3	-	-	µF
VCC2	C_{VCC2}	0.4	-	-	µF
VREG1	C_{VREG1}	0.3	1	10	µF
VREG2	C_{VREG2}	0.3	1	10	µF

Pin Configuration

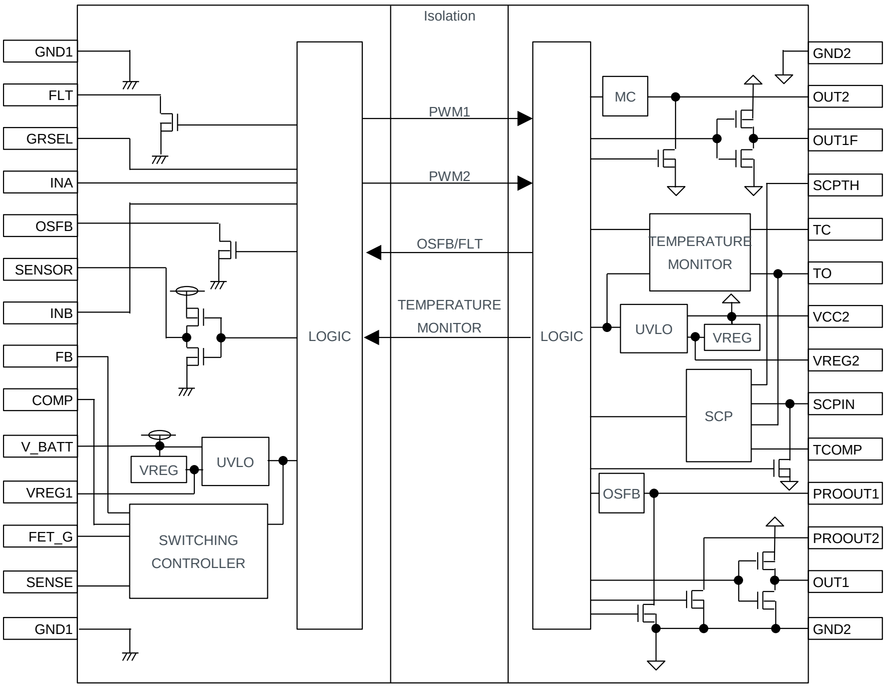
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	GND2	Output-side ground pin
2	OUT1	Output pin
3	PROOUT2	Fast turn off pin for short circuit protection
4	PROOUT1	Soft turn off pin for short circuit protection / Gate voltage input pin
5	TCOMP	Temperature compensation pin of short circuit detection voltage
6	SCPIN	Short circuit detection pin
7	VREG2	Output-side internal power supply pin
8	VCC2	Output-side power supply pin
9	TO	Constant current output pin / Sensor voltage input pin
10	TC	Resistor connection pin for setting constant current
11	SCPTH	Short circuit detection threshold setting pin
12	OUT1F	Output pin
13	OUT2	Miller clamp pin
14	GND2	Output-side ground pin
15	GND1	Input-side ground pin
16	FLT	Fault output pin
17	GRSEL	Gate resistance switching pin
18	INA	Control input pin
19	OSFB	Output state feedback output pin
20	SENSOR	Temperature information output pin
21	INB	Control input pin
22	FB	Error amplifier inverting input pin for switching controller
23	COMP	Error amplifier output pin for switching controller
24	V_BATT	Main power supply pin
25	VREG1	Input-side internal power supply pin
26	FET_G	MOS FET for transformer drive control pin for switching controller
27	SENSE	Current feedback resistor connection pin for switching controller
28	GND1	Input-side ground pin

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Main Power Supply Voltage	$V_{BATTMAX}$	-0.3 to +40.0 *(Note 2)*	V
Output-Side Supply Voltage	V_{CC2MAX}	-0.3 to +30.0 *(Note 3)*	V
INA, INB, GRSEL Pin Input Voltage	V_{INMAX}	-0.3 to +7.0 *(Note 2)*	V
FLT, OSFB Pin Input Voltage	V_{FLTMAX}	-0.3 to +7.0 *(Note 2)*	V
FLT, OSFB Pin Output Current	I_{FLT}	10	mA
SENSOR Pin Output Current	I_{SENSOR}	10	mA
FB Pin Input Voltage	V_{FBMAX}	-0.3 to +7.0 *(Note 2)*	V
FET_G Pin Output Current (Peak 5 µs)	I_{FET_GPEAK}	1	A
SCPIN Pin Input Voltage	$V_{SCPINMAX}$	-0.3 to V_{CC2} + 0.3 or +30.0 *(Note 3)*	V
SCPTH Pin Input Voltage	$V_{SCPTHMAX}$	-0.3 to +7.0 *(Note 3)*	V
TO Pin Input Voltage	V_{TOMAX}	-0.3 to V_{CC2} + 0.3 or +30.0 *(Note 3)*	V
TO Pin Output Current	I_{TOMAX}	8	mA
OUT1, OUT1F Pin Output Current (Peak 5 µs)	$I_{OUT1PEAK}$	10 *(Note 4)*	A
OUT2 Pin Output Current (Peak 5 µs)	$I_{OUT2PEAK}$	10 *(Note 4)*	A
PROOUT1 Pin Output Current (Peak 10 µs)	$I_{PROOUT1PEAK}$	2.5 *(Note 4)*	A
PROOUT2 Pin Output Current (Peak 5 µs)	$I_{PROOUT2PEAK}$	5.0 *(Note 4)*	A
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 2) Relative to GND1
(Note 3) Relative to GND2
(Note 4) Should not exceed Tj = 150 °C

Thermal Resistance (Note 5)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 7)	2s2p (Note 8)	
SSOP-B28W				
Junction to Ambient	θ_{JA}	112.9	64.4	°C/W
Junction to Top Characterization Parameter (Note 6)	Ψ_{JT}	34	23	°C/W

(Note 5) Based on JESD51-2A (Still-Air).
(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 7) Using a PCB board based on JESD51-3.
(Note 8) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Main Power Supply Voltage	V_{BATT} (Note 9)	8	24	V
Output-side Supply Voltage	V_{CC2} (Note10)	13.5	24.0	V
VREG1 pin Output Current	I_{VREG1}	-	0.5	mA
VREG2 Pin Output Current	I_{VREG2}	-	0.5	mA
TO pin Input Voltage	V_{TO} (Note 10)	1.35	3.84	V
SCPTH Pin Input Voltage	V_{SCPTH} (Note10)	0.5	2.0	V
Operating Temperature	Topr	-40	+125	°C

(Note 9) Relative to GND1
(Note 10) Relative to GND2

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO} = 500 V)	R_S	> 10^9	Ω
Insulation Withstand Voltage / 1 min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1 s	V_{ISO}	3000	Vrms

Electrical Characteristics

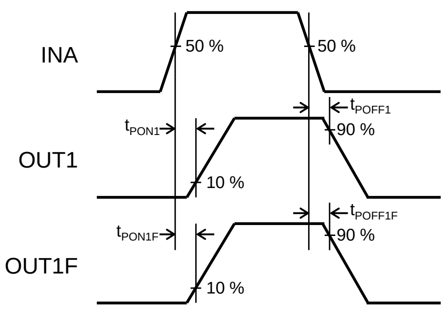
(Unless otherwise specified Ta = -40 °C to +125 °C, V_{BATT} = 8 V to 24 V, V_{CC2} = 13.5 V to 24 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Main Power Supply Circuit Current 1	I_{BATT1}	0.4	1.2	2.0	mA	FET_G switching operation INA, INB not switching
Main Power Supply Circuit Current 2	I_{BATT2}	0.3	1.1	1.9	mA	FET_G Not switching INA, INB not switching
Main Power Supply Circuit Current 3	I_{BATT3}	0.5	1.3	2.1	mA	FET_G switching operation INA = 10 kHz, Duty = 50 % INB = L
Main Power Supply Circuit Current 4	I_{BATT4}	0.5	1.4	2.3	mA	FET_G switching operation INA = 20 kHz, Duty = 50 % INB = L
Output Side Circuit Current	I_{CC2}	1.4	3.0	4.6	mA	R_{TC} = 10 kΩ
VREG1 Output Voltage	V_{REG1}	4.5	5.0	5.5	V	
VREG2 Output Voltage	V_{REG2}	4.8	5.0	5.2	V	
Switching Controller						
FET_G Output Voltage H	V_{FETGH}	4.5	5.0	5.5	V	I_{FET_G} = 0 A (open)
FET_G Output Voltage L	V_{FETGL}	0	-	0.3	V	I_{FET_G} = 0 A (open)
FET_G On Resistance (Source-side)	R_{ONGH}	3	6	12	Ω	I_{FET_G} = 10 mA
FET_G On Resistance (Sink-side)	R_{ONGL}	0.3	0.6	1.3	Ω	I_{FET_G} = 10 mA
Oscillation Frequency	f_{OSC_SW}	80	100	120	kHz	
Soft-start Time	t_{SS}	-	-	50	ms	
FB Threshold Voltage	V_{FB}	1.47	1.50	1.53	V	
FB Input Current	I_{FB}	-0.8	0	+0.8	µA	
COMP Pin Sink Current	$I_{COMPSINK}$	-160	-80	-40	µA	
COMP Pin Source Current	$I_{COMPSOURCE}$	40	80	160	µA	
Error Amplifier Transconductance	gm_{err}	0.5	1.1	2.2	mA/V	Guaranteed by design
V_BATT UVLO Off Voltage	$V_{UVLOBATTH}$	6.5	7.0	7.5	V	
V_BATT UVLO On Voltage	$V_{UVLOBATTL}$	5.5	6.0	6.5	V	
Maximum On Duty	D_{ONMAX}	50	55	60	%	
Over Voltage Detection Threshold	V_{OVTH}	1.88	1.95	2.02	V	
Under Voltage Detection Threshold	V_{UVTH}	1.03	1.10	1.17	V	
Over-current Detection Threshold	V_{OCTH}	0.17	0.20	0.23	V	
Switching Controller Protection Holding Time	$t_{DCDCRLS}$	20	40	60	ms	
Logic Input						
Logic High Level Input Voltage	V_{INH}	0.7 x V_{REG1}	-	5.5	V	INA, INB, GRSEL
Logic Low Level Input Voltage	V_{INL}	0	-	0.3 x V_{REG1}	V	INA, INB, GRSEL
Logic Pull-down Resistance	R_{IND}	25	50	100	kΩ	INA, INB, GRSEL
Logic Input Filtering Time	t_{INFIL}	5	45	90	ns	INA, INB

Electrical Characteristics - continued

(Unless otherwise specified Ta = -40 °C to +125 °C, V_{BATT} = 8 V to 24 V, V_{CC2} = 13.5 V to 24 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output						
OUT1 On Resistance (Source-side)	R_{ONH1}	0.09	0.22	0.42	Ω	I_{OUT1} = 40 mA, Guaranteed by design
OUT1 On Resistance (Sink-side)	R_{ONL1}	0.07	0.20	0.40	Ω	I_{OUT1} = 40 mA, Guaranteed by design
OUT1 Maximum Current (Source-side)	$I_{OUTMAX1H}$	6	-	-	A	V_{CC2} = 15 V, Guaranteed by design
OUT1 Maximum Current (Sink-side)	$I_{OUTMAX1L}$	4	-	-	A	V_{CC2} = 15 V, Guaranteed by design
OUT1 Turn ON Time	t_{PON1}	90	150	210	ns	
OUT1 Turn OFF Time	t_{POFF1}	80	140	200	ns	
OUT1 Propagation Distortion	t_{PDIST1}	-60	-10	+40	ns	t_{POFF1} - t_{PON1}
OUT1 Rise Time	t_{RISE1}	25	50	120	ns	Load = 4.7 Ω + 1 nF
OUT1 Fall Time	t_{FALL1}	25	50	100	ns	Load = 4.7 Ω + 1 nF
OUT1F On Resistance (Source-side)	R_{ONH1F}	0.11	0.25	0.50	Ω	I_{OUT1F} = 40 mA, Guaranteed by design
OUT1F On Resistance (Sink-side)	R_{ONL1F}	0.07	0.18	0.36	Ω	I_{OUT1F} = 40 mA, Guaranteed by design
OUT1F Maximum Current (Source-side)	$I_{OUTMAX1FH}$	3	-	-	A	V_{CC2} = 15 V, Guaranteed by design
OUT1F Maximum Current (Sink-side)	$I_{OUTMAX1FL}$	5	-	-	A	V_{CC2} = 15 V, Guaranteed by design
OUT1F Turn ON Time	t_{PON1F}	90	150	210	ns	
OUT1F Turn OFF Time	t_{POFF1F}	80	140	200	ns	
OUT1F Propagation Distortion	$t_{PDIST1F}$	-60	-10	+40	ns	t_{POFF1F} - t_{PON1F}
OUT1F Rise Time	t_{RISE1F}	25	50	130	ns	Load = 4.7 Ω + 1 nF
OUT1F Fall Time	t_{FALL1F}	25	50	100	ns	Load = 4.7 Ω + 1 nF
PROOUT1 On Resistance	R_{ONPRO1}	0.4	1.2	2.7	Ω	$I_{PROOUT1}$ = 40 mA, Guaranteed by design
PROOUT2 On Resistance	R_{ONPRO2}	0.1	0.3	0.8	Ω	$I_{PROOUT2}$ = 40 mA, Guaranteed by design
PROOUT1 Maximum Current	$I_{OUTMAXPRO1}$	1	-	-	A	V_{CC2} = 15V, Guaranteed by design
PROOUT2 Maximum Current	$I_{OUTMAXPRO2}$	5	-	-	A	V_{CC2} = 15V, Guaranteed by design
OUT2 On Resistance	R_{ON2}	0.10	0.25	0.60	Ω	I_{OUT2} = 40 mA Guaranteed by design
OUT2 On Threshold Voltage	V_{OUT2ON}	1.8	2.0	2.2	V	
OUT2 Output Delay Time	t_{OUT2ON}	-	60	90	ns	Guaranteed by design
Common Mode Transient Immunity	CM	100	-	-	kV/μs	Guaranteed by design
Temperature Monitor						
TC Voltage	V_{TC}	0.975	1.000	1.025	V	
TO Output Current	I_{TO}	0.97	1.00	1.03	mA	R_{TC} = 10 kΩ
SENSOR Output Frequency	f_{OSC_TO}	8	10	14	kHz	
SENSOR Output Duty1	$D_{SENSOR1}$	88.0	90.0	92.0	%	V_{TO} = 1.35 V
SENSOR Output Duty2	$D_{SENSOR2}$	47.6	50.0	52.4	%	V_{TO} = 2.59 V
SENSOR Output Duty3	$D_{SENSOR3}$	6.4	10.0	13.6	%	V_{TO} = 3.84 V
SENSOR On Resistance (Source-side)	$R_{SENSORH}$	-	60	160	Ω	I_{SENSOR} = 5 mA
SENSOR On Resistance (Sink-side)	$R_{SENSORL}$	-	60	160	Ω	I_{SENSOR} = 5 mA



Electrical Characteristics - continued
(Unless otherwise specified Ta = -40 °C to +125 °C, V_{BATT} = 8 V to 24 V, V_{CC2} = 13.5 V to 24 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Protection Function						
VREG1 UVLO Off Voltage	$V_{UVLOREG1H}$	4.05	4.25	4.45	V	
VREG1 UVLO On Voltage	$V_{UVLOREG1L}$	3.95	4.15	4.35	V	
VREG1 UVLO Delay Time (OUT1)	$t_{DUVLOREG1OUT}$	2	10	30	µs	
VREG1 UVLO Delay Time (FLT)	$t_{DUVLOREG1FLT}$	2	10	30	µs	
Output-side UVLO Off Voltage	V_{UVLO2H}	11.5	12.5	13.5	V	
Output-side UVLO On Voltage	V_{UVLO2L}	10.5	11.5	12.5	V	
Output-side UVLO Delay Time (OUT1)	$t_{DUVLO2OUT}$	2	10	30	µs	
Output-side UVLO Delay Time (FLT)	$t_{DUVLO2FLT}$	3	-	65	µs	
VREG2 UVLO Off Voltage	$V_{UVLOREG2H}$	4.05	4.25	4.45	V	
VREG2 UVLO On Voltage	$V_{UVLOREG2L}$	3.95	4.15	4.35	V	
VREG2 UVLO Delay Time (OUT1)	$t_{DUVLOREG2OUT}$	2	10	30	µs	
VREG2 UVLO Delay Time (FLT)	$t_{DUVLOREG2FLT}$	3	-	65	µs	
SCPIN Leading Edge Blanking Time	t_{SCPLEB}	400	450	500	ns	Guaranteed by design
Short Circuit Detection Offset	V_{SCDET}	-25	0	+25	mV	V_{SCPTH} = 0.5 V
TCOMP Pin Output Voltage1	V_{TCOMP1}	3.72	3.84	3.96	V	V_{TO} = 3.84 V
TCOMP Pin Output Voltage 2	V_{TCOMP2}	1.30	1.35	1.40	V	V_{TO} = 1.35 V
SCPIN Pin Output Current 1	I_{SCPIN1}	409	427	445	µA	V_{TO} = 3.84 V, R_{TCOMP} = 9 kΩ
SCPIN Pin Output Current 2	I_{SCPIN2}	11.4	13.5	15.6	µA	V_{TO} = 1.35 V, R_{TCOMP} = 100 kΩ
Short Circuit Protection Delay Time (PROOUT1, PROOUT2)	$t_{DSCPPRO}$	140	230	320	ns	
Short Circuit Protection Delay Time (FLT)	$t_{DSCPFLT}$	1	-	35	µs	
PROOUT2 On Time	t_{PRO2ON}	100	160	220	ns	Guaranteed by design
SCPIN Pin Low Voltage	V_{SCPINL}	-	0.02	0.10	V	I_{SCPIN} = 1 mA
FLT Output On Resistance	R_{FLTL}	-	30	80	Ω	I_{FLT} = 5 mA
Fault Output Holding Time	t_{FLTRLS}	20	40	60	ms	
Gate State H Detection Threshold Voltage	V_{OSFBH}	12.9	13.8	14.7	V	
Gate State L Detection Threshold Voltage	V_{OSFBL}	12.5	13.4	14.3	V	
OSFB Output On Resistance	R_{OSFBL}	-	30	80	Ω	I_{OSFB} = 5 mA

Typical Performance Curves
(Reference data)

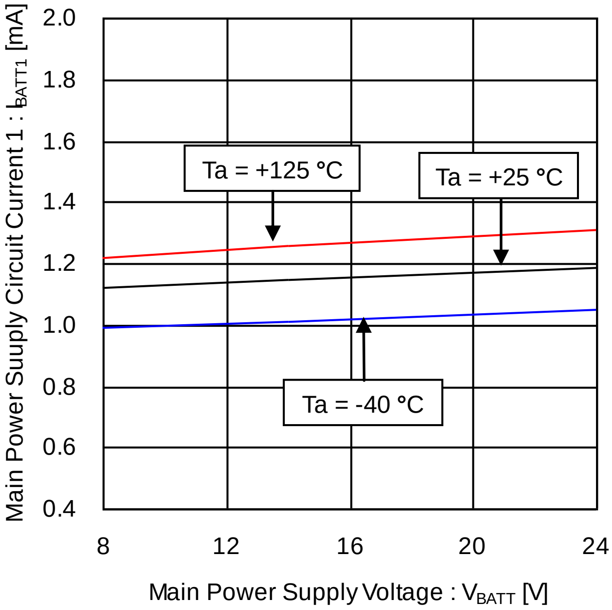


Figure 1. Main Power Supply Circuit Current 1 vs Main Power Supply Voltage (FET_G switching operation, INA not switching)

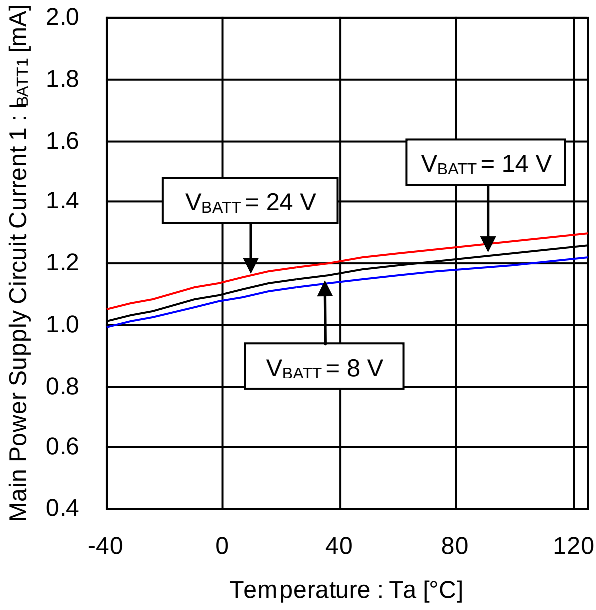


Figure 2. Main Power Supply Circuit Current 1 vs Temperature (FET_G switching operation, INA not switching)

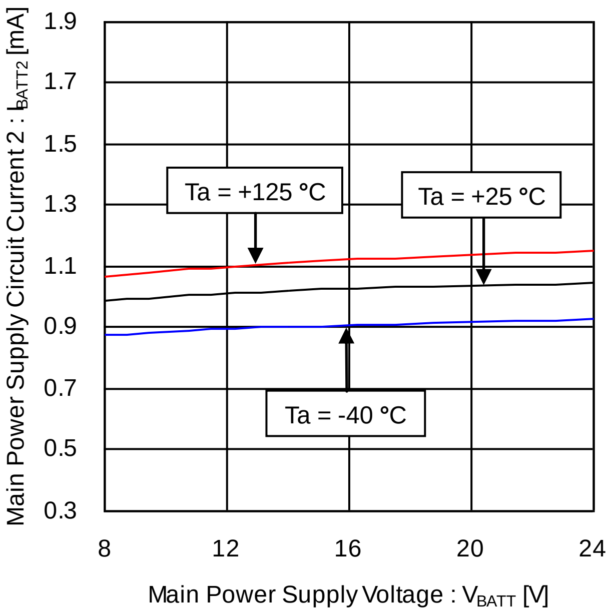


Figure 3. Main Power Supply Circuit Current 2 vs Main Power Supply Voltage (FET_G not switching, INA not switching)

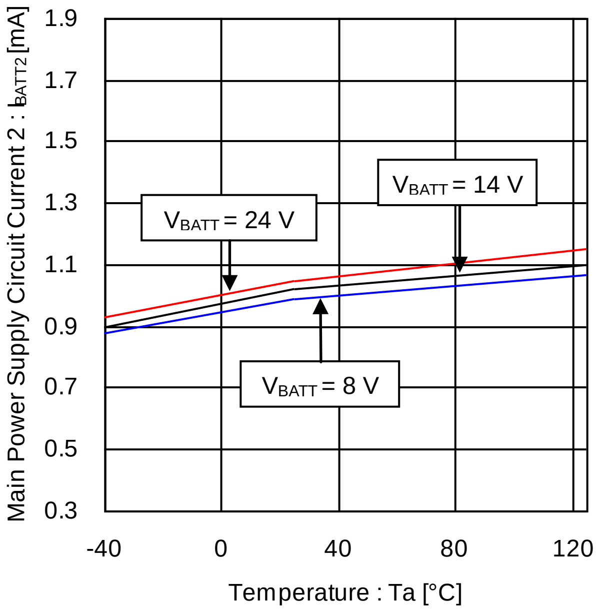


Figure 4. Main Power Supply Circuit Current 2 vs Temperature (FET_G not switching, INA not switching)

Typical Performance Curves - continued
(Reference data)

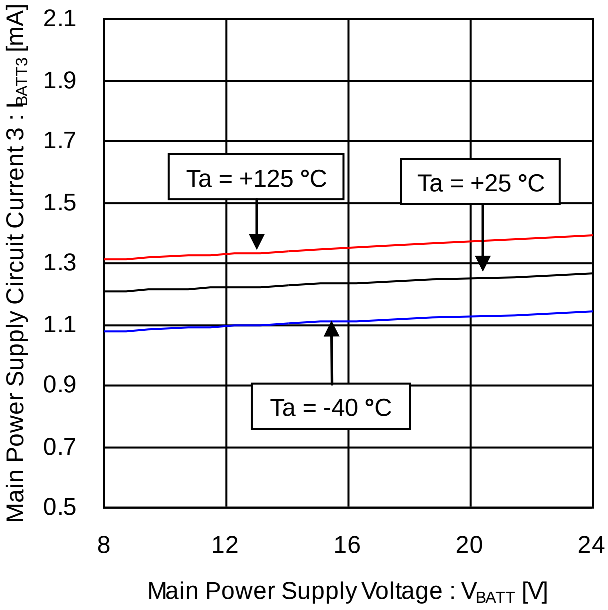


Figure 5. Main Power Supply Circuit Current 3 vs Main Power Supply Voltage
(FET_G switching operation, INA = 10 kHz, Duty = 50 %)

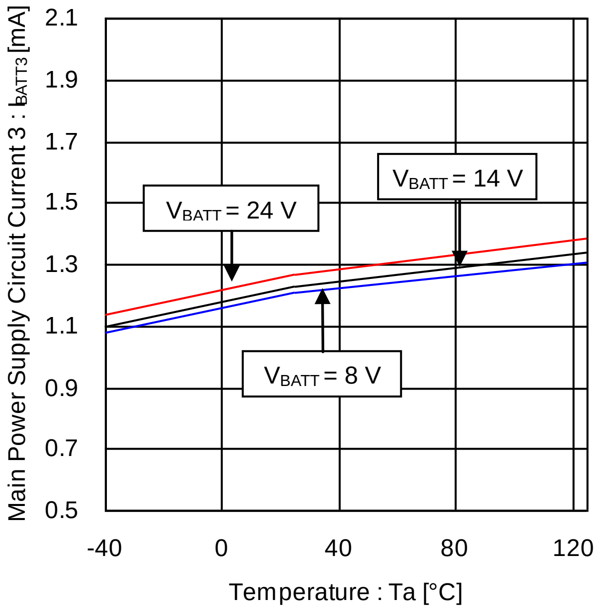


Figure 6. Main Power Supply Circuit Current 3 vs Temperature
(FET_G switching operation, INA = 10 kHz, Duty = 50 %)

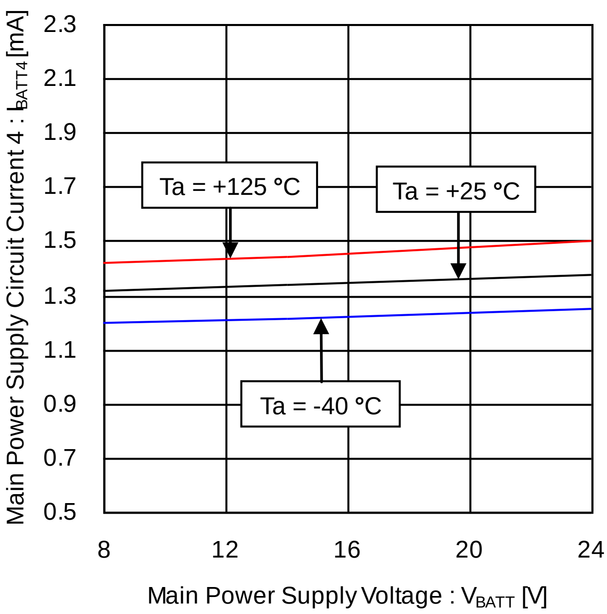


Figure 7. Main Power Supply Circuit Current 4 vs Main Power Supply Voltage
(FET_G switching operation, INA = 20 kHz, Duty = 50 %)

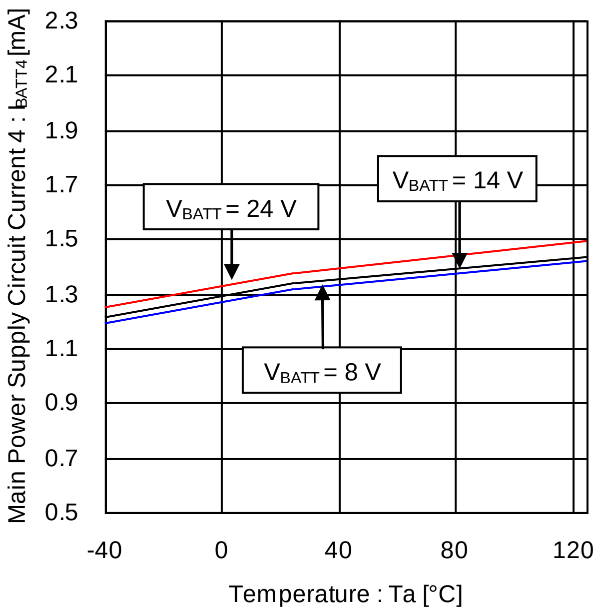


Figure 8. Main Power Supply Circuit Current 4 vs Temperature
(FET_G switching operation, INA = 20 kHz, Duty = 50 %)

Typical Performance Curves - continued
(Reference data)

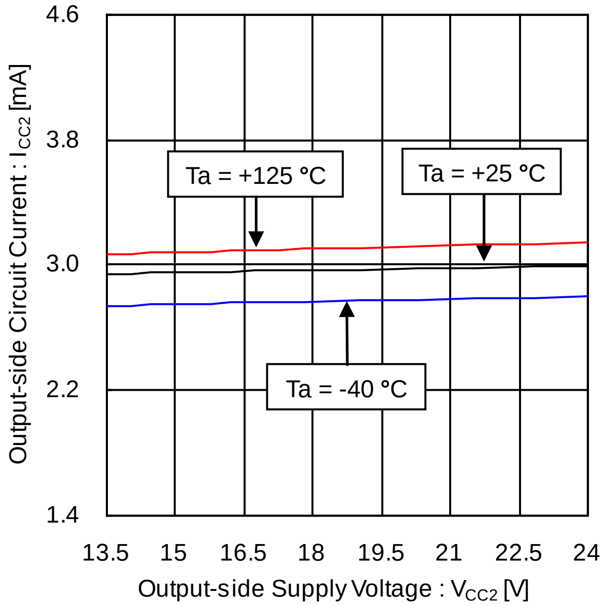


Figure 9. Output-side Circuit Current vs Output-side Supply Voltage

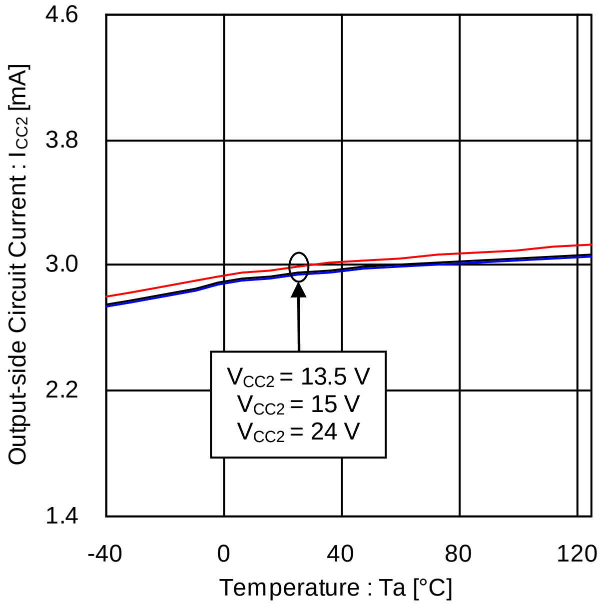


Figure 10. Output-side Circuit Current vs Temperature

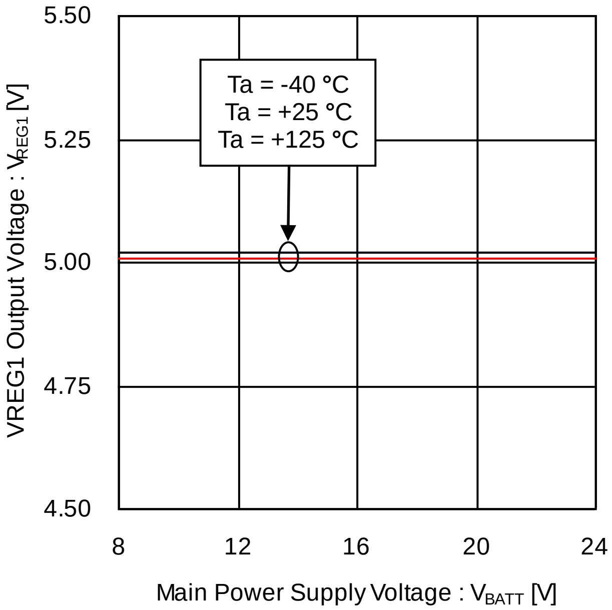


Figure 11. VREG1 Output Voltage vs Main Power Supply Voltage

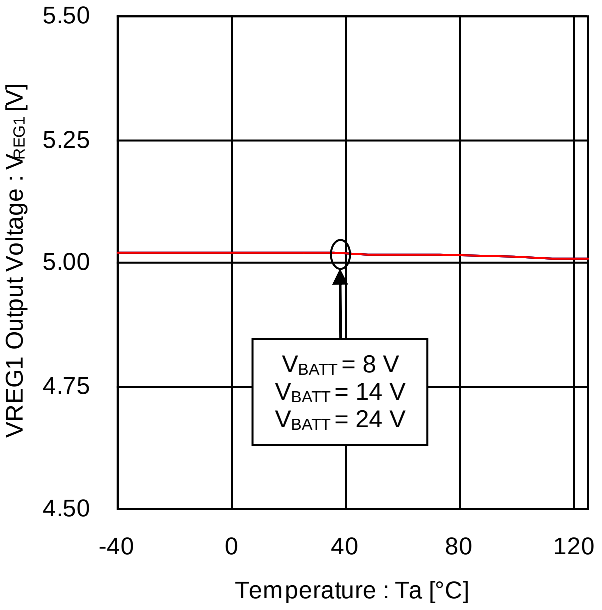


Figure 12. VREG1 Output Voltage vs Temperature

Typical Performance Curves - continued

(Reference data)

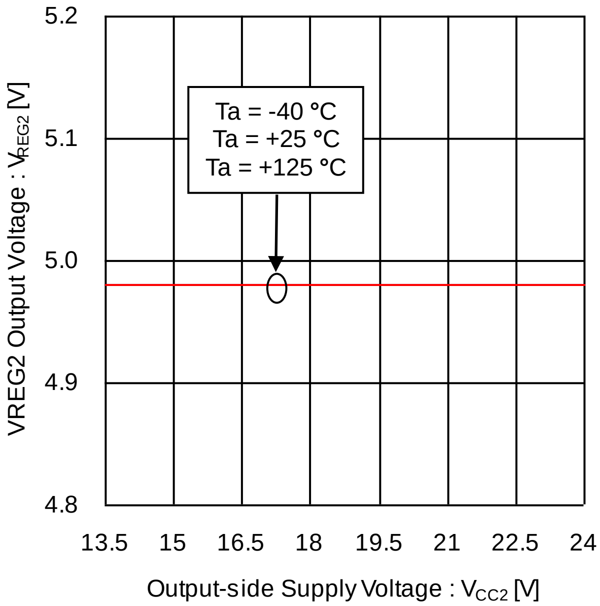


Figure 13. VREG2 Output Voltage vs Output-side Supply Voltage

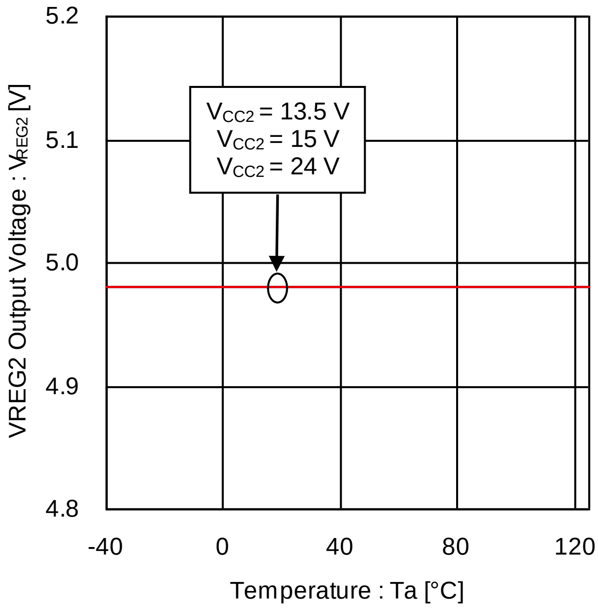


Figure 14. VREG2 Output Voltage vs Temperature

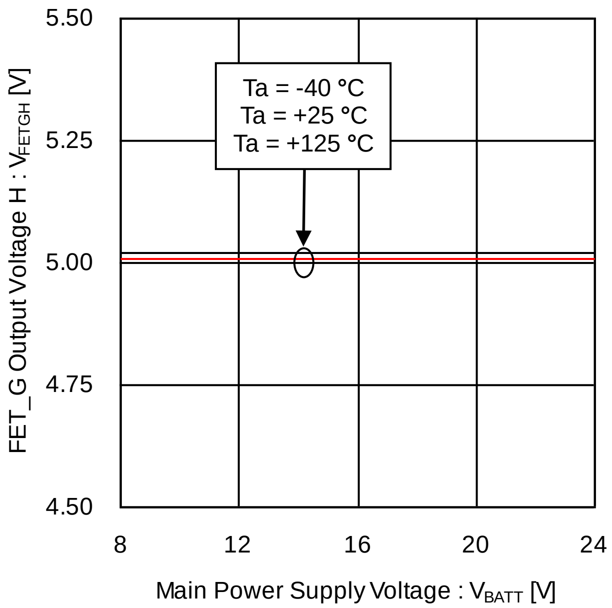


Figure 15. FET_G Output Voltage H vs Main Power Supply Voltage (I_{FET_G} = 0 A)

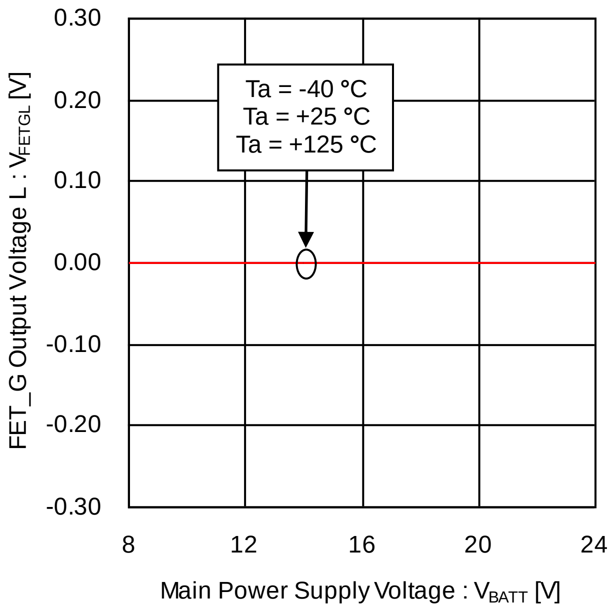


Figure 16. FET_G Output Voltage L vs Main Power Supply Voltage (I_{FET_G} = 0 A)

Typical Performance Curves - continued
(Reference data)

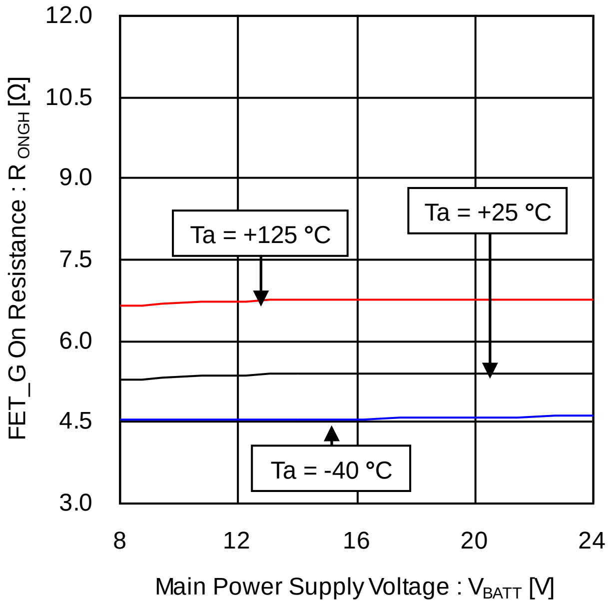


Figure 17. FET_G On Resistance vs Main Power Supply Voltage (Source-side)

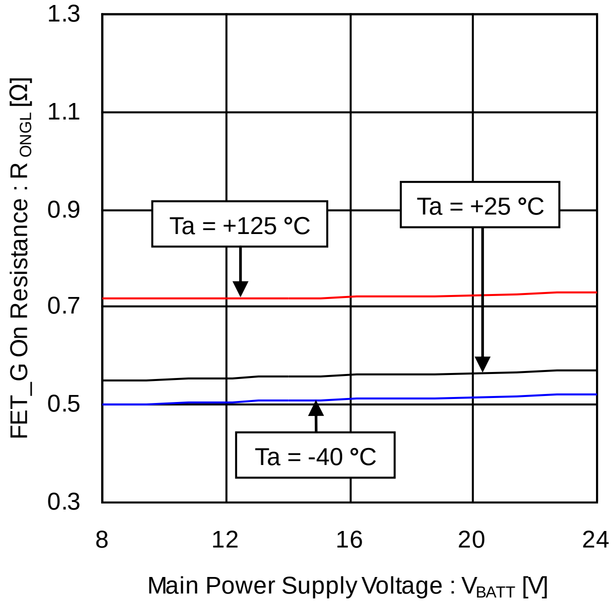


Figure 18. FET_G On Resistance vs Main Power Supply Voltage (Sink-side)

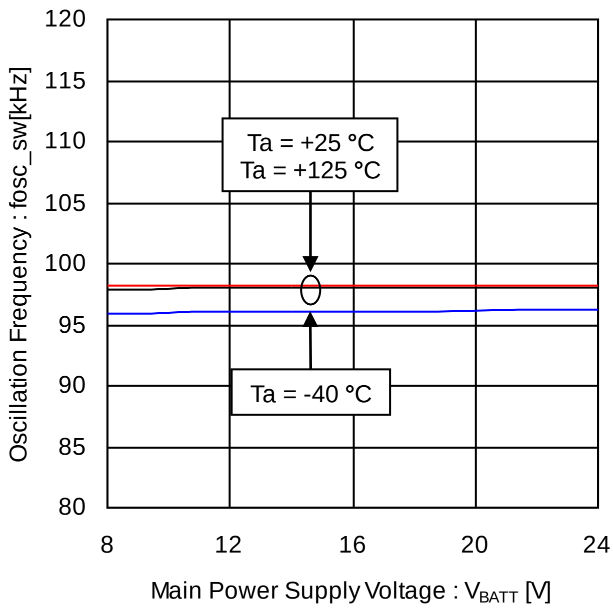


Figure 19. Oscillation Frequency vs Main Power Supply Voltage

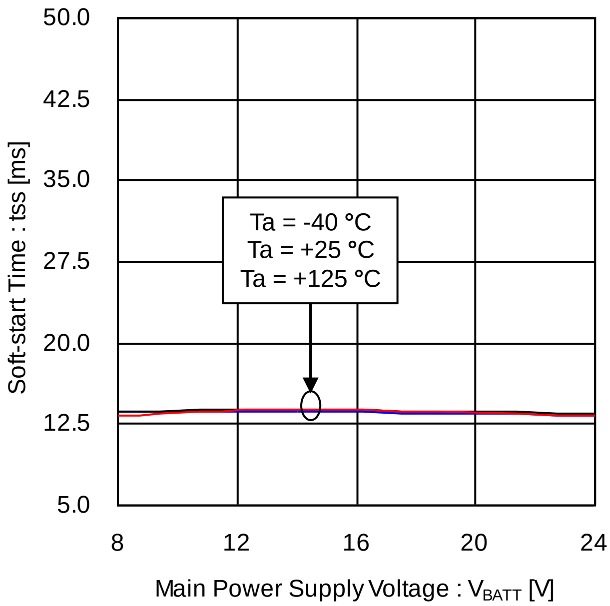


Figure 20. Soft-start Time vs Main Power Supply Voltage

Typical Performance Curves - continued
(Reference data)

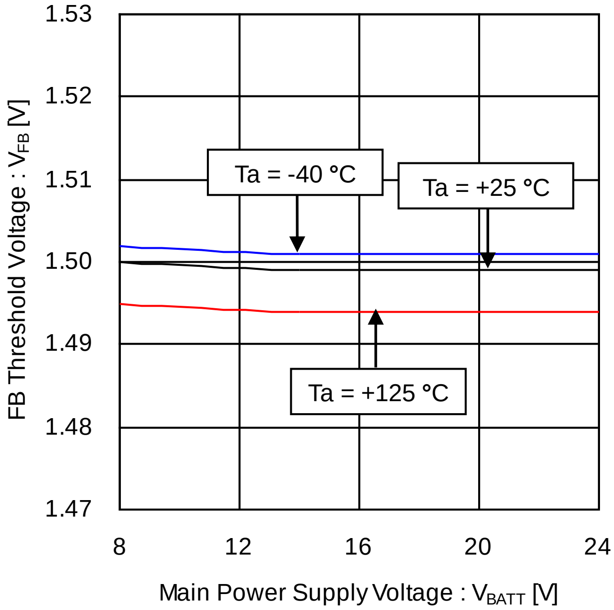


Figure 21. FB Threshold Voltage vs Main Power Supply Voltage

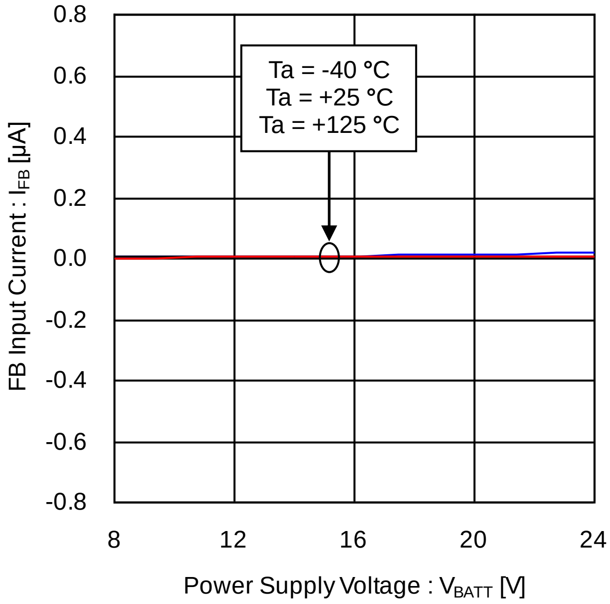


Figure 22. FB Input Current vs Main Power Supply Voltage (FB = 5 V)

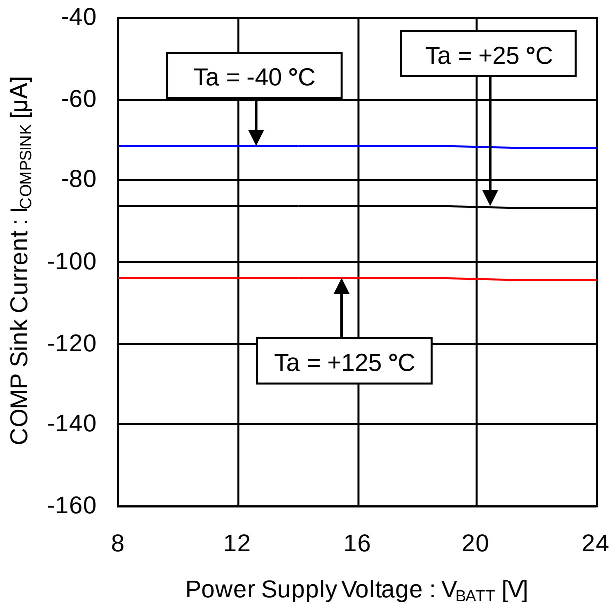


Figure 23. COMP Sink Current vs Main Power Supply Voltage

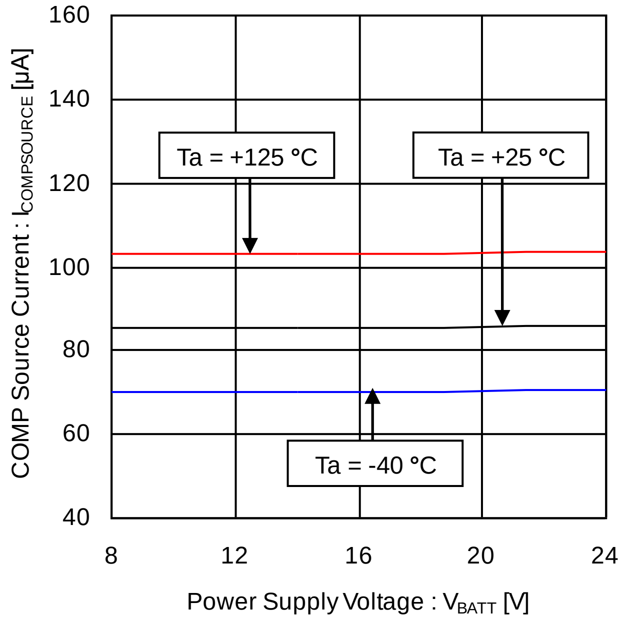


Figure 24. COMP Source Current vs Main Power Supply Voltage

Typical Performance Curves - continued

(Reference data)

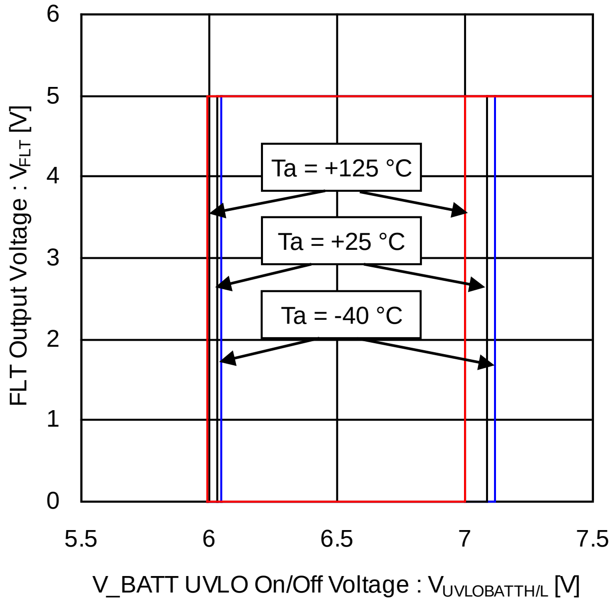


Figure 25. FLT Output Voltage vs V_BATT UVLO On/Off Voltage

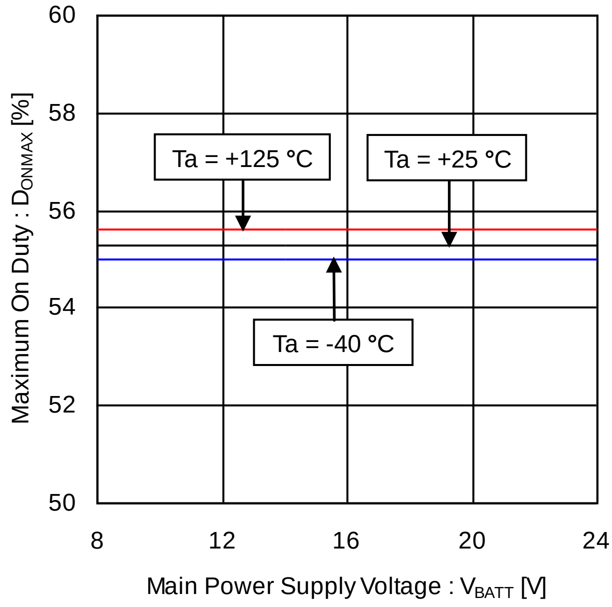


Figure 26. Maximum On Duty vs Main Power Supply Voltage

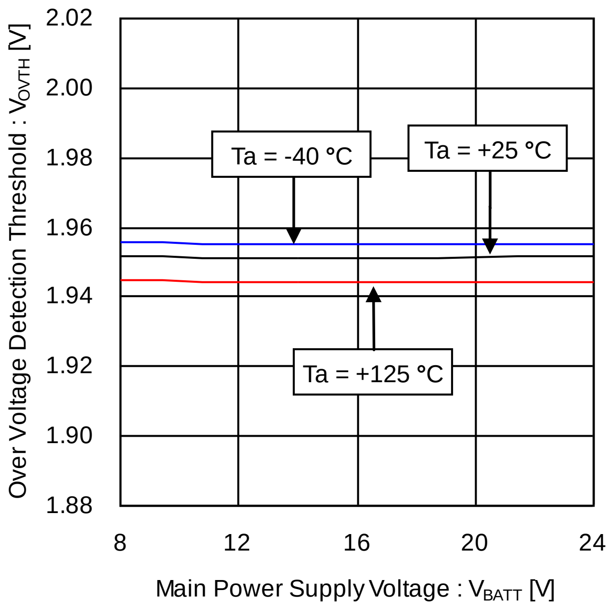


Figure 27. Over Voltage Detection Threshold vs Main Power Supply Voltage

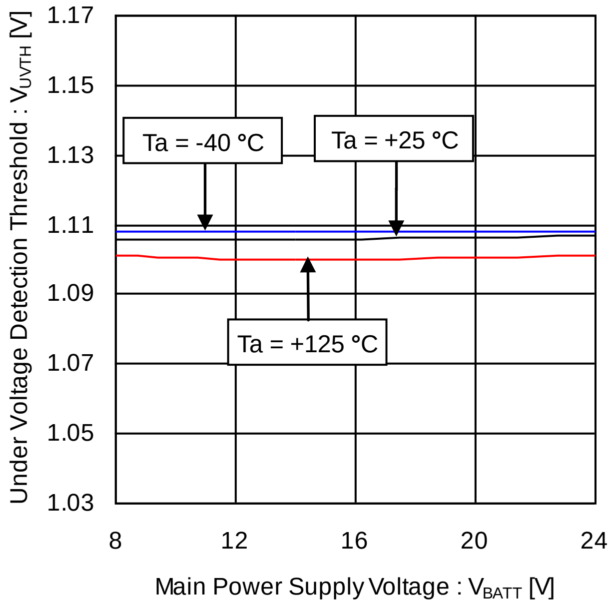


Figure 28. Under Voltage Detection Threshold vs Main Power Supply Voltage

Typical Performance Curves - continued
(Reference data)

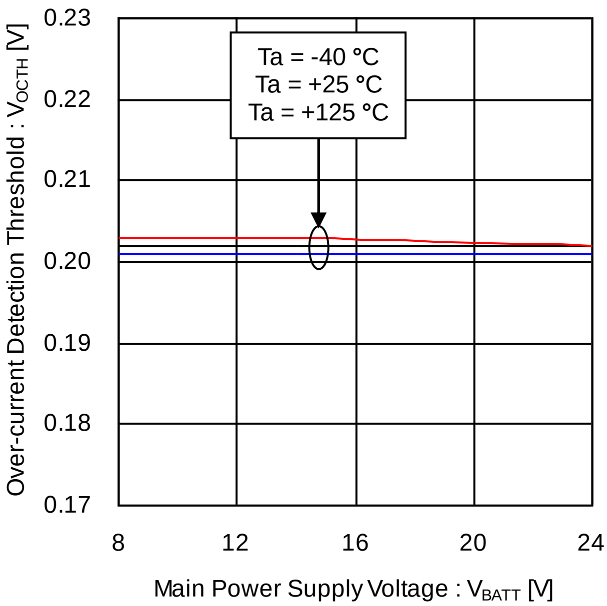


Figure 29. Over-current Detection Threshold vs Main Power Supply Voltage

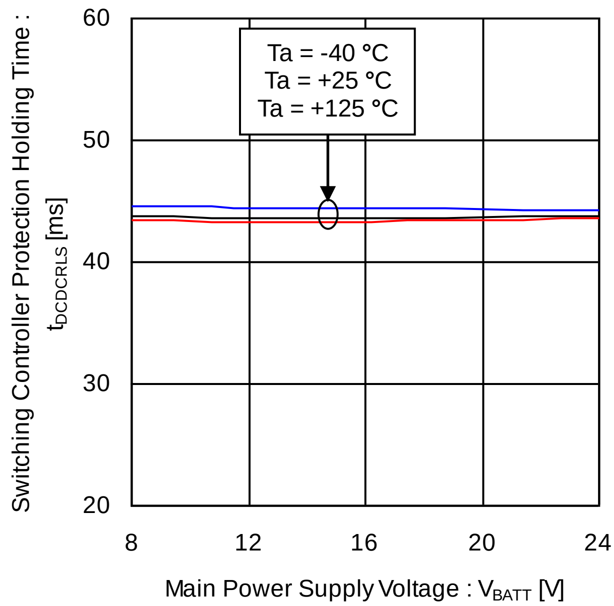


Figure 30. Switching Controller Protection Holding Time vs Main Power Supply Voltage

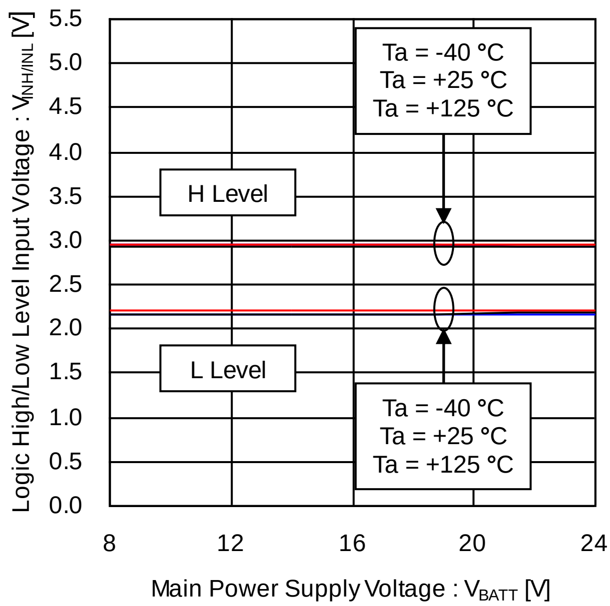


Figure 31. Logic High/Low Level Input Voltage vs Main Power Supply Voltage (INA, INB, GRSEL)

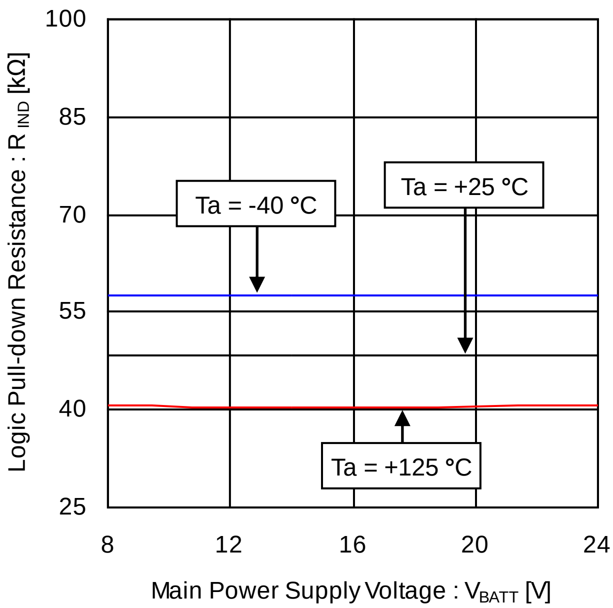


Figure 32. Logic Pull-down Resistance vs Main Power Supply Voltage (INA, INB, GRSEL)

Typical Performance Curves - continued

(Reference data)

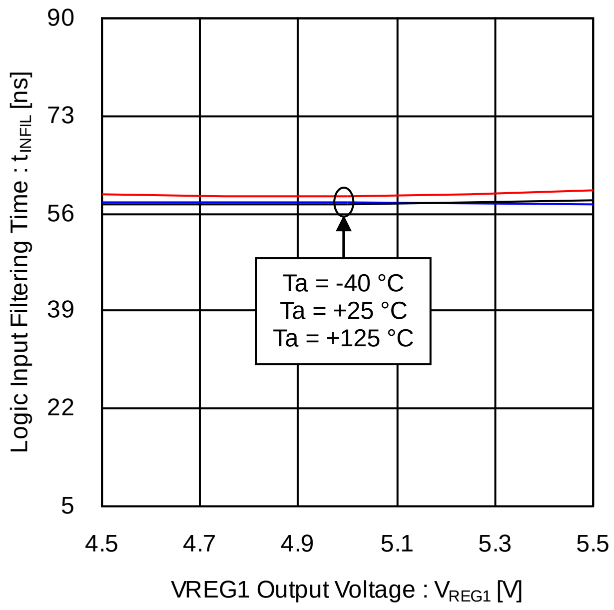


Figure 33. Logic Input Filtering Time vs VREG1 Output Voltage (INA, INB)

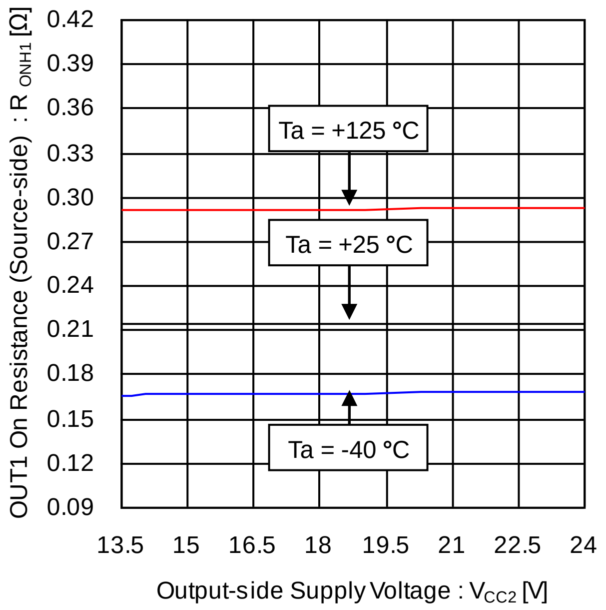


Figure 34. OUT1 On Resistance (Source-side) vs Output-side Supply Voltage (I_{OUT1} = 40 mA)

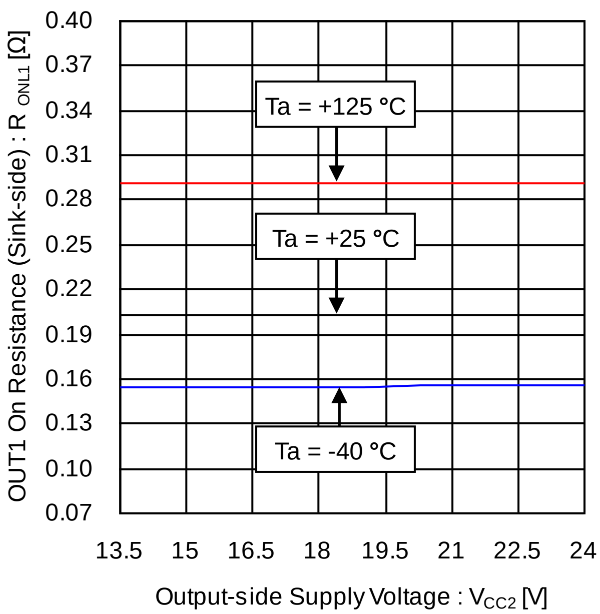


Figure 35. OUT1 On Resistance (Sink-side) vs Output-side Supply Voltage (I_{OUT1} = 40 mA)

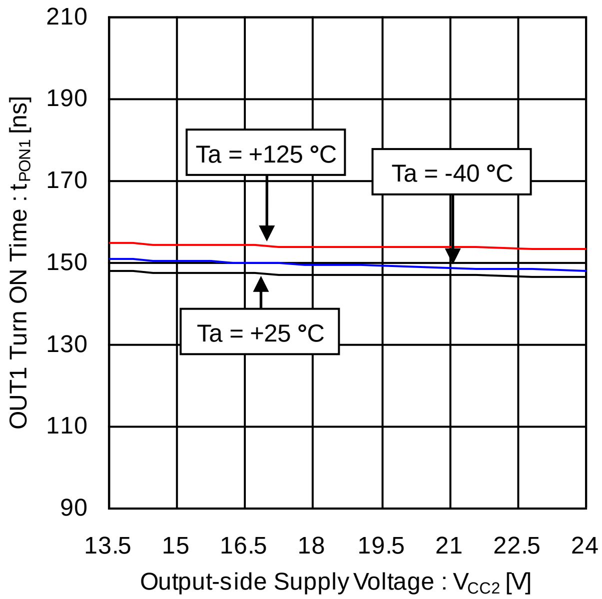


Figure 36. OUT1 Turn ON Time vs Output-side Supply Voltage

Typical Performance Curves - continued

(Reference data)

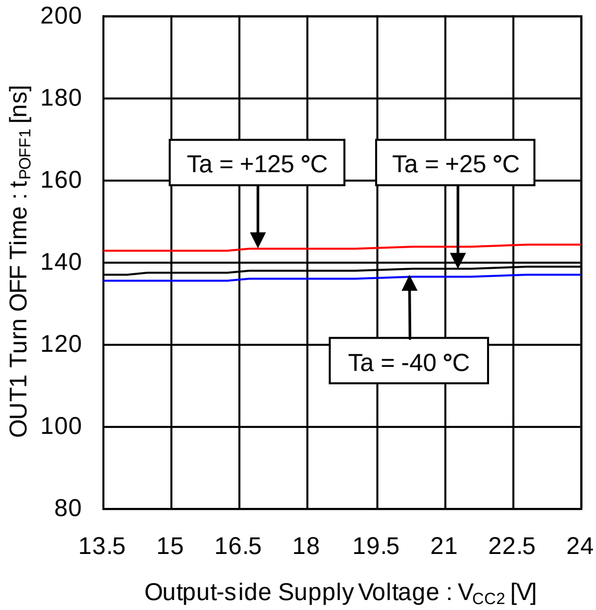


Figure 37. OUT1 Turn OFF Time vs Output-side Supply Voltage

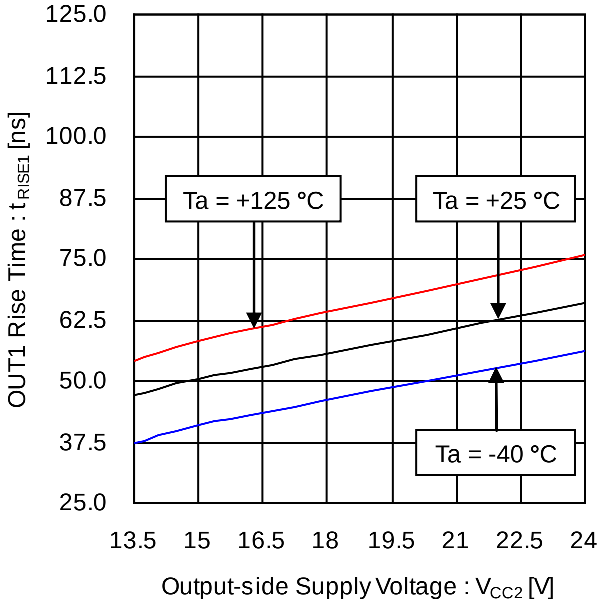


Figure 38. OUT1 Rise Time vs Output-side Supply Voltage (Load = 4.7 Ω + 1 nF)

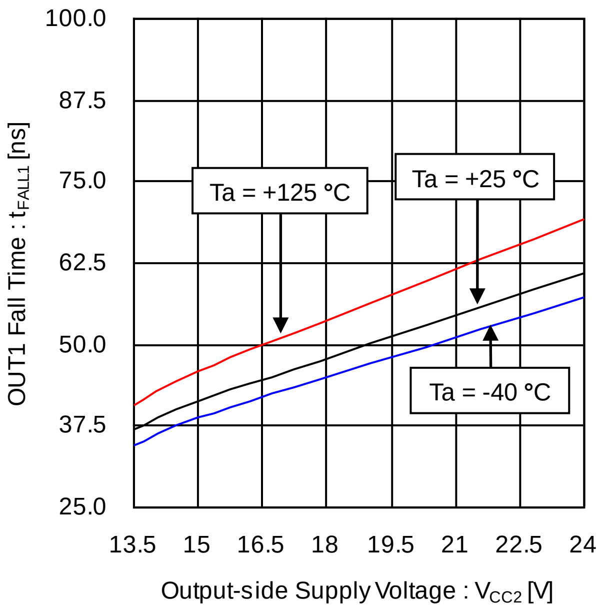


Figure 39. OUT1 Fall Time vs Output-side Supply Voltage (Load = 4.7 Ω + 1 nF)

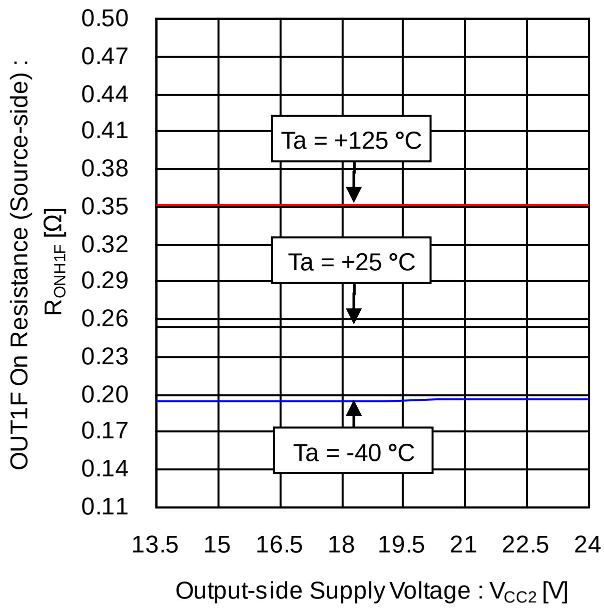


Figure 40. OUT1F On Resistance (Source-side) vs Output-side Supply Voltage (I_{OUT1F} = 40 mA)

Typical Performance Curves - continued
(Reference data)

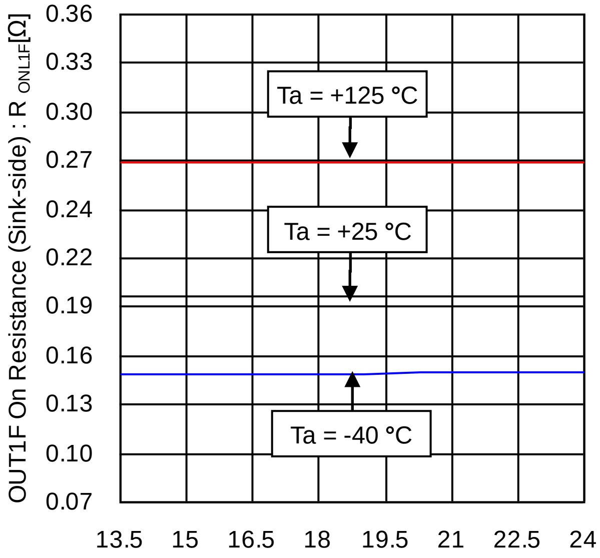


Figure 41. OUT1F On Resistance (Sink-side) vs Output-side Supply Voltage (I_{OUT1F} = 40 mA)

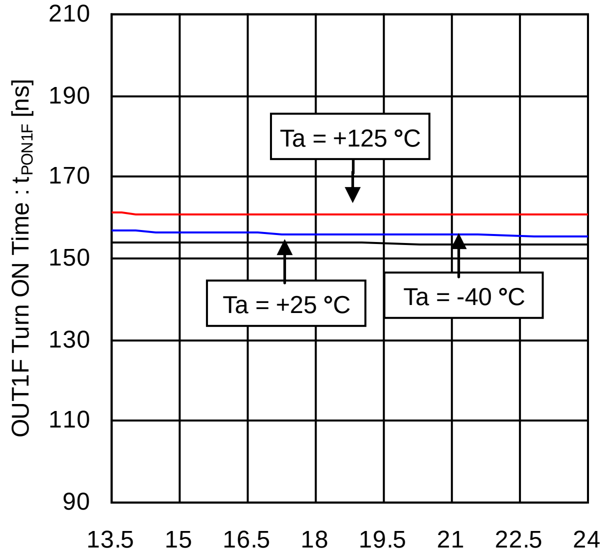


Figure 42. OUT1F Turn ON Time vs Output-side Supply Voltage

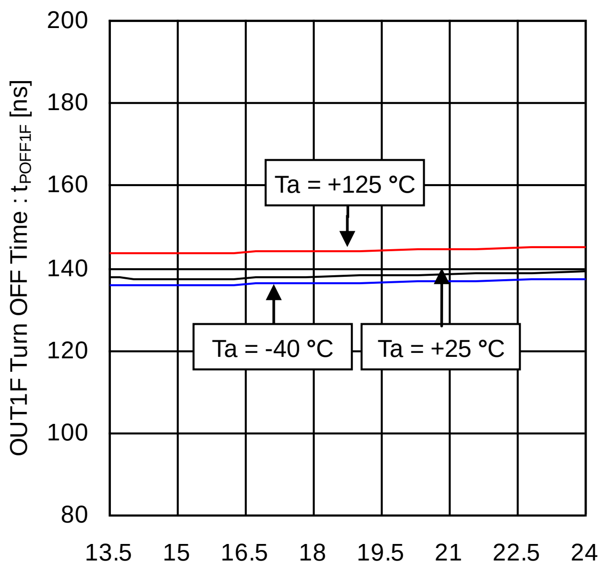


Figure 43. OUT1F Turn OFF Time vs Output-side Supply Voltage

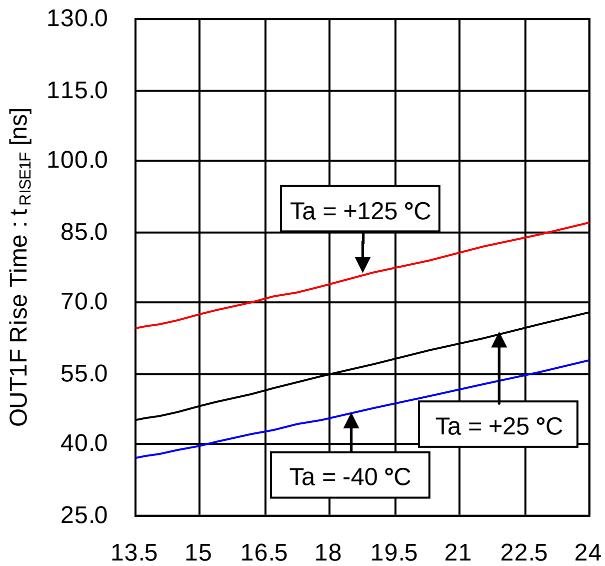


Figure 44. OUT1F Rise Time vs Output-side Supply Voltage (Load = 4.7 Ω + 1 nF)

Typical Performance Curves - continued
(Reference data)

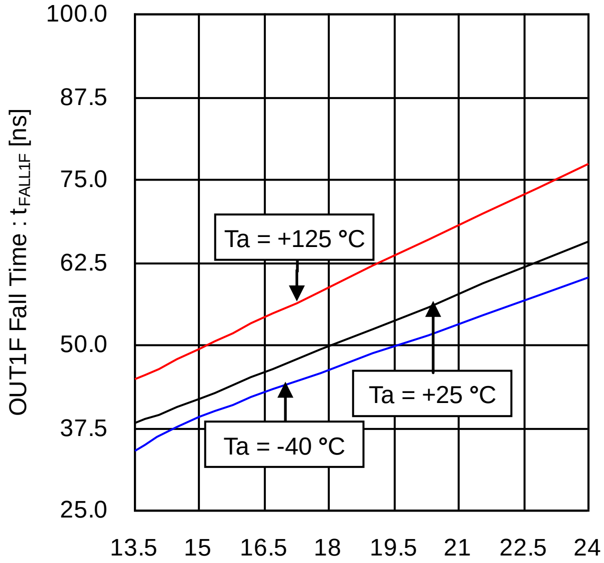


Figure 45. OUT1F Fall Time vs Output-side Supply Voltage (Load = 4.7 Ω + 1 nF)

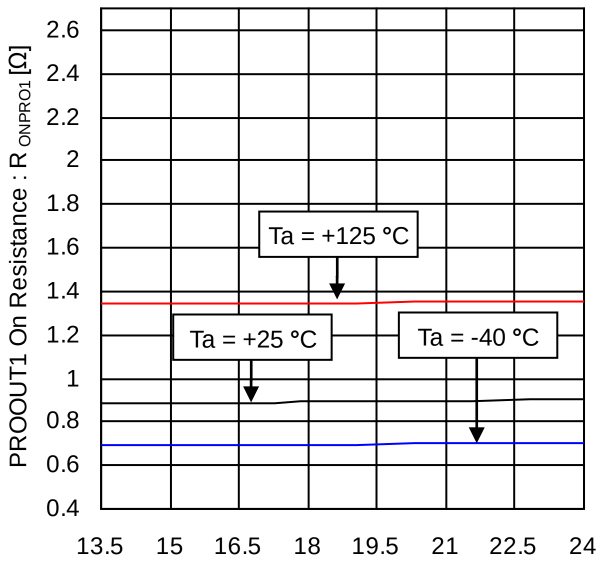


Figure 46. PROOUT1 On Resistance vs Output-side Supply Voltage ($I_{PROOUT1}$ = 40 mA)

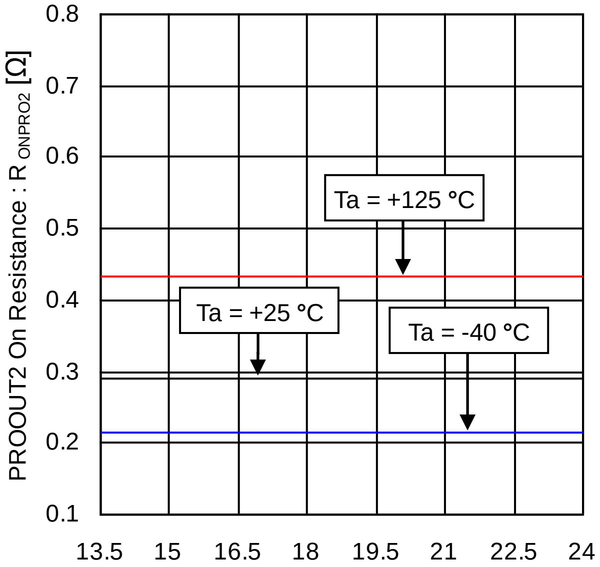


Figure 47. PROOUT2 On Resistance vs Output-side Supply Voltage ($I_{PROOUT2}$ = 40 mA)

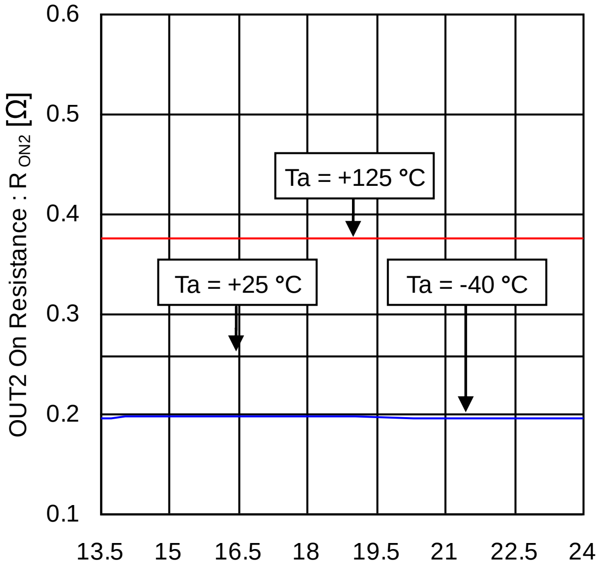


Figure 48. OUT2 On Resistance vs Output-side Supply Voltage (I_{OUT2} = 40 mA)

Typical Performance Curves - continued

(Reference data)

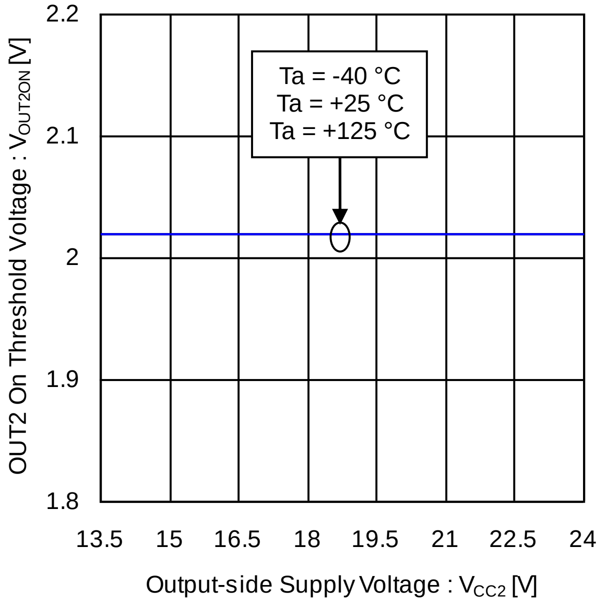


Figure 49. OUT2 On Threshold Voltage vs Output-side Supply Voltage

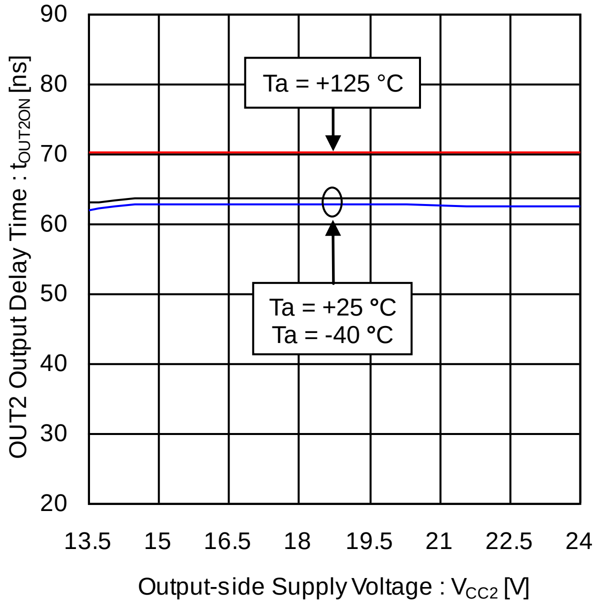


Figure 50. OUT2 Output Delay Time vs Output-side Supply Voltage

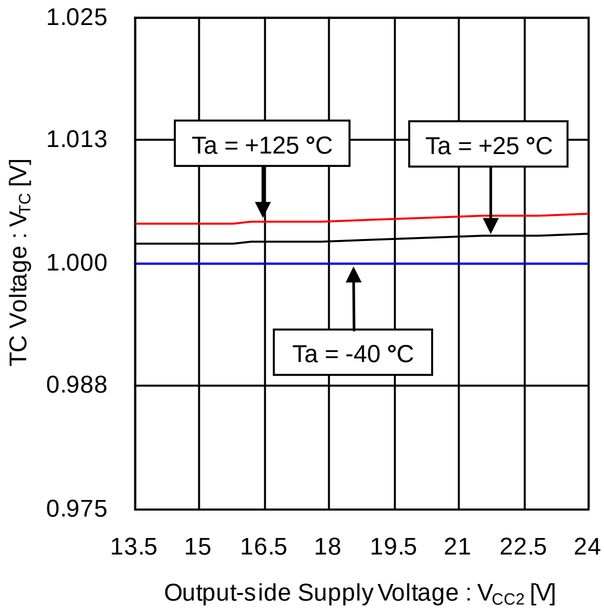


Figure 51. TC Voltage vs Output-side Supply Voltage

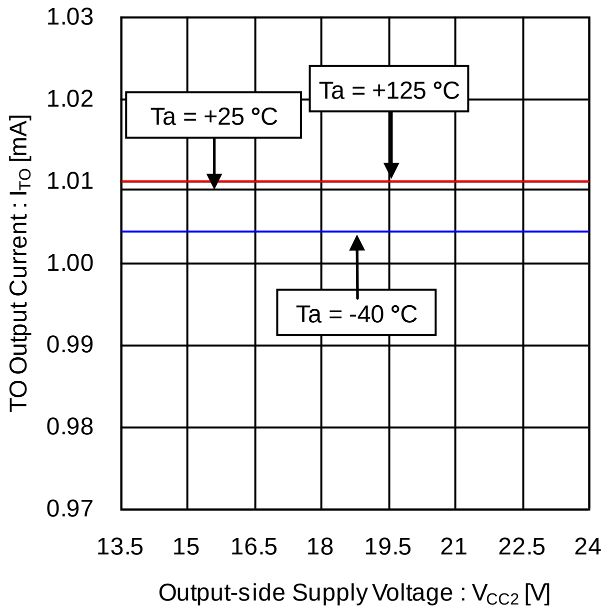


Figure 52. TO Output Current vs Output-side Supply Voltage (R_{TC} = 10 kΩ)

Typical Performance Curves - continued
(Reference data)

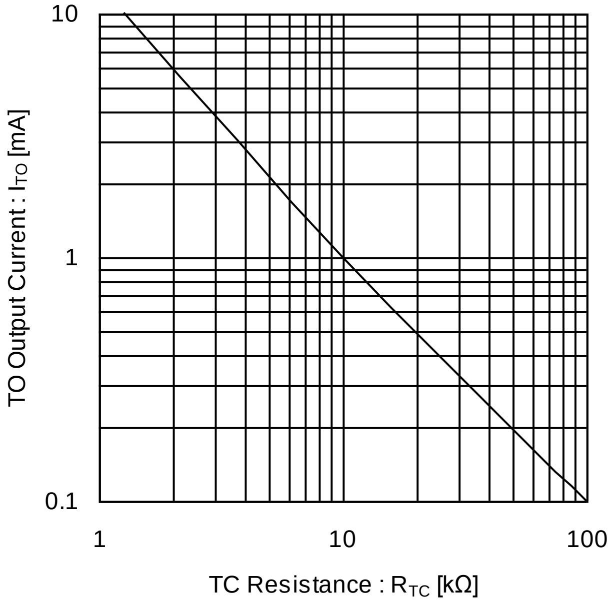


Figure 53. TO Output Current vs TC Resistance

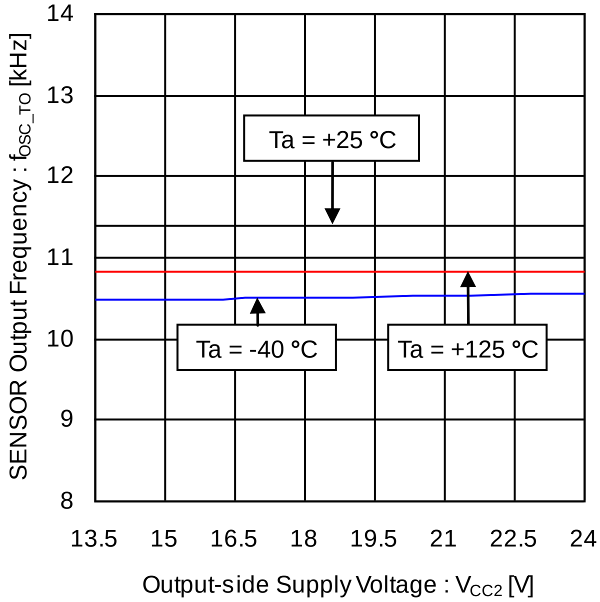


Figure 54. SENSOR Output Frequency vs Output-side Supply Voltage

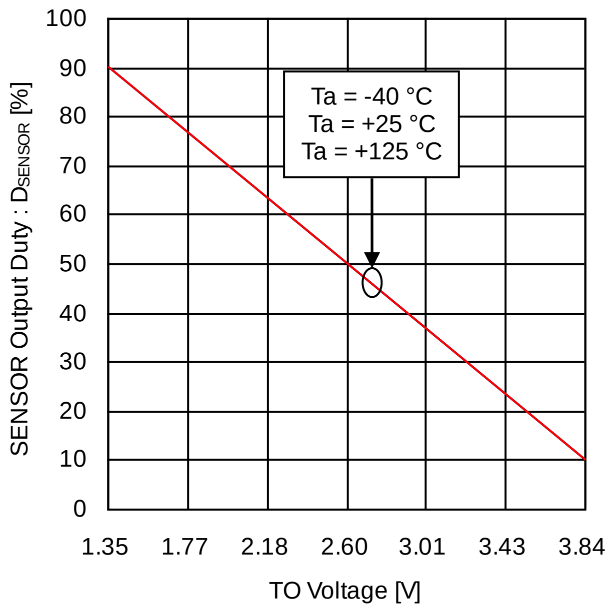


Figure 55. SENSOR Output Duty vs TO Voltage

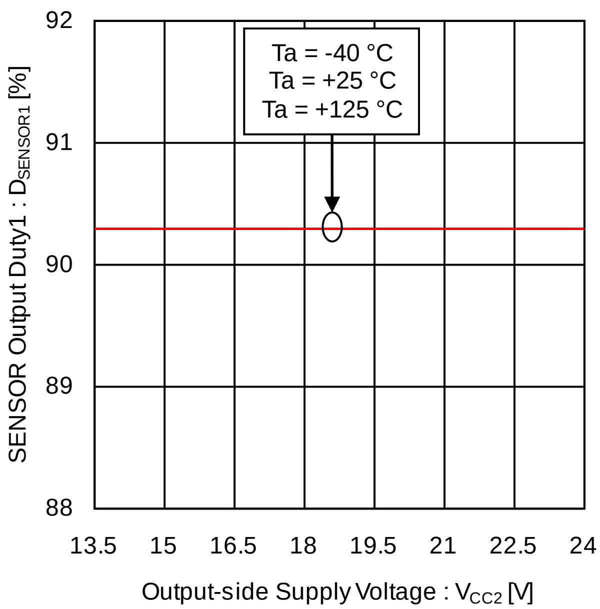


Figure 56. SENSOR Output Duty1 vs Output-side Supply Voltage (V_{TO} = 1.35 V)

Typical Performance Curves - continued

(Reference data)

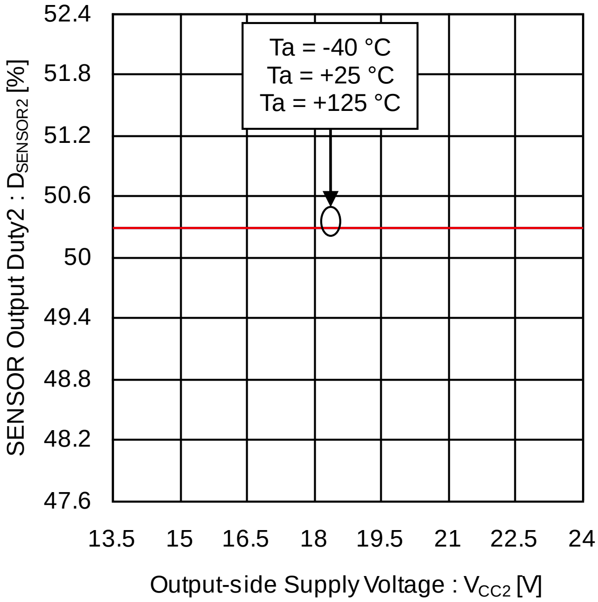


Figure 57. SENSOR Output Duty2 vs Output-side Supply Voltage (V_{TO} = 2.59 V)

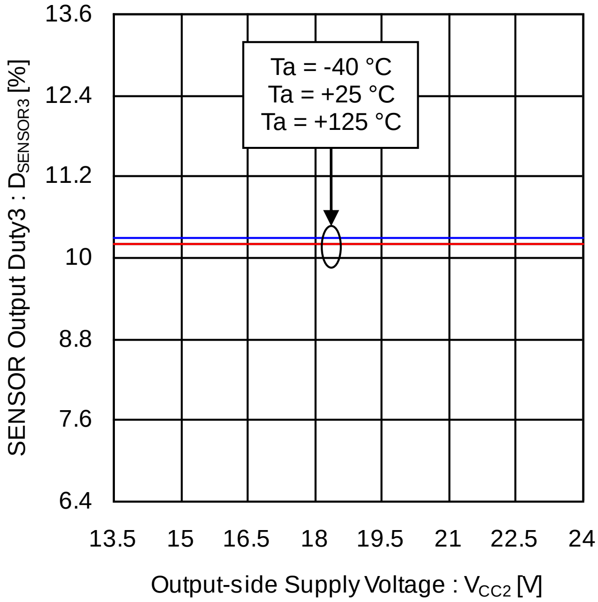


Figure 58. SENSOR Output Duty3 vs Output-side Supply Voltage (V_{TO} = 3.84 V)

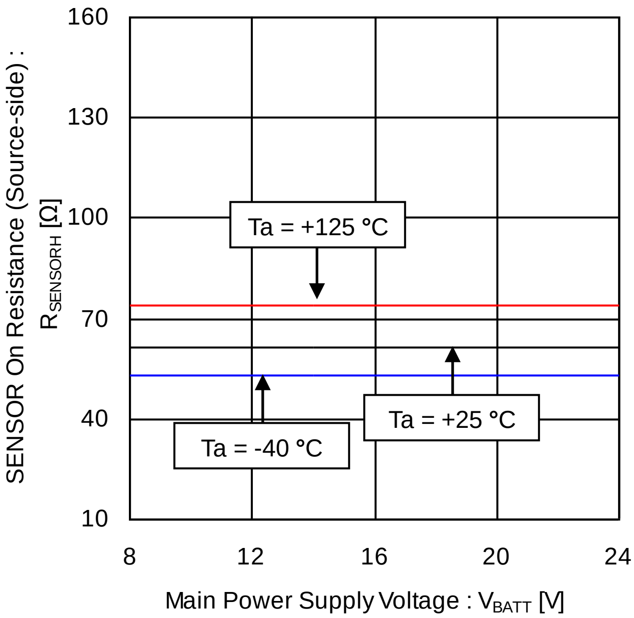


Figure 59. SENSOR On Resistance (Source-side) vs Main Power Supply Voltage

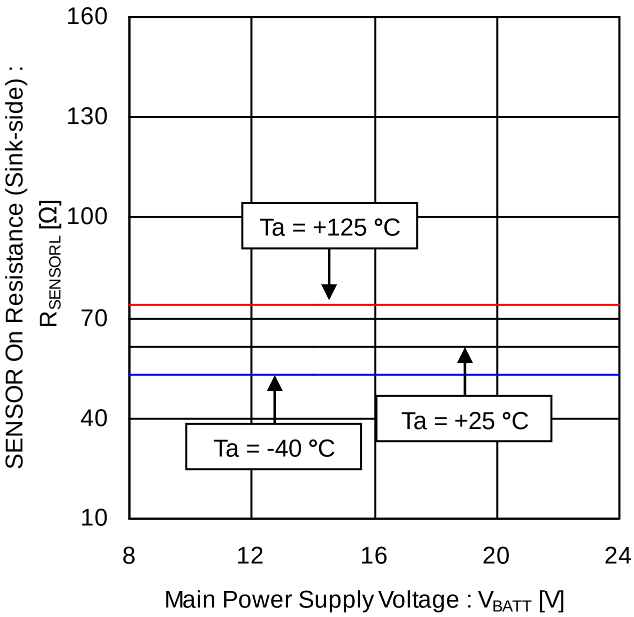


Figure 60. SENSOR On Resistance (Sink-side) vs Main Power Supply Voltage

Typical Performance Curves - continued
(Reference data)

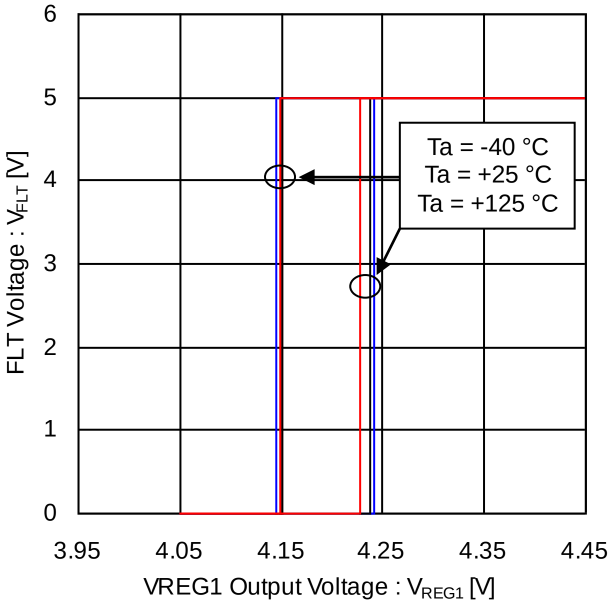


Figure 61. FLT Voltage vs VREG1 Output Voltage
(VREG1 UVLO On/Off Voltage)

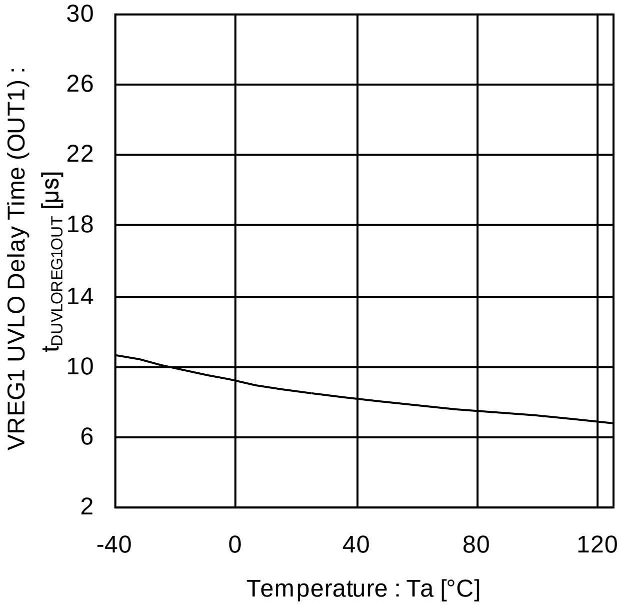


Figure 62. VREG1 UVLO Delay Time (OUT1)
vs Temperature

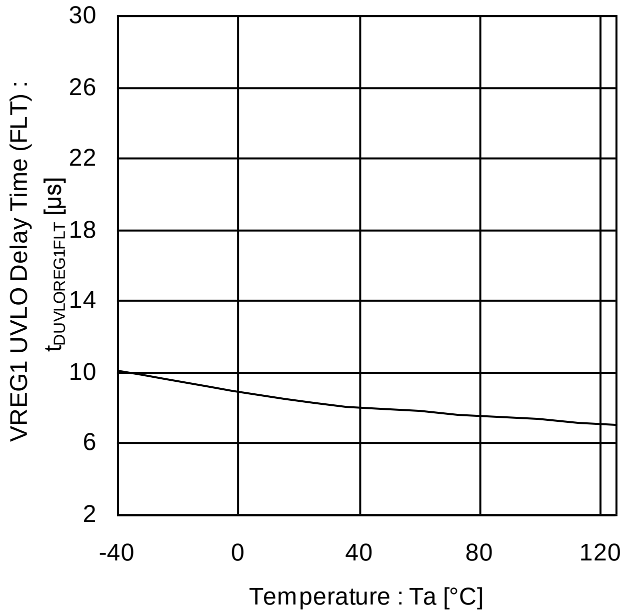


Figure 63. VREG1 UVLO Delay Time (FLT)
vs Temperature

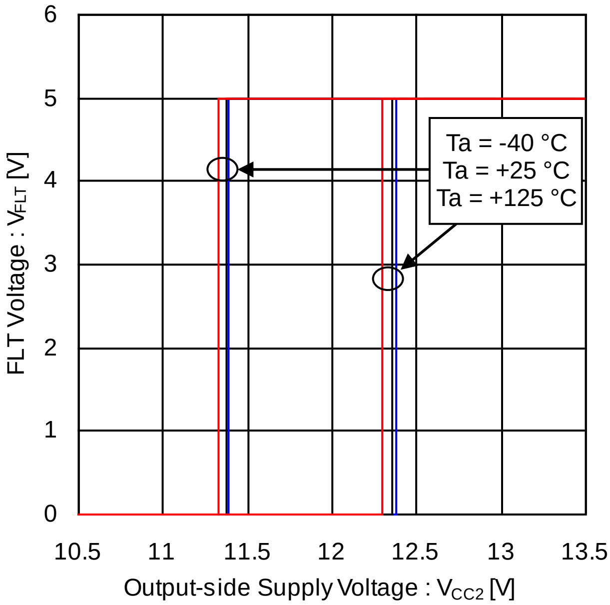


Figure 64. FLT Voltage vs Output-side Supply Voltage
(Output-side UVLO On/Off Voltage)

Typical Performance Curves - continued
(Reference data)

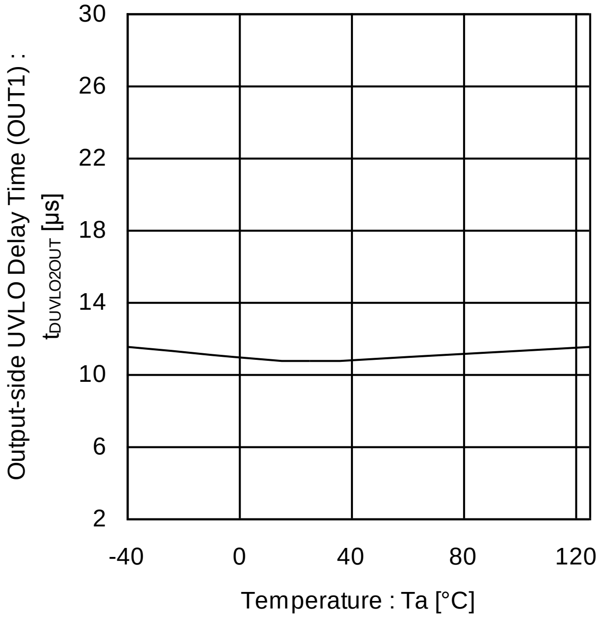


Figure 65. Output-side UVLO Delay Time (OUT1) vs Temperature

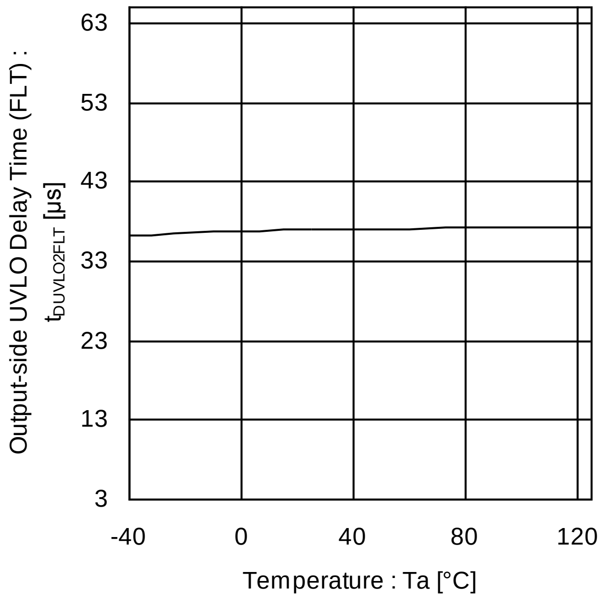


Figure 66. Output-side UVLO Delay Time (FLT) vs Temperature

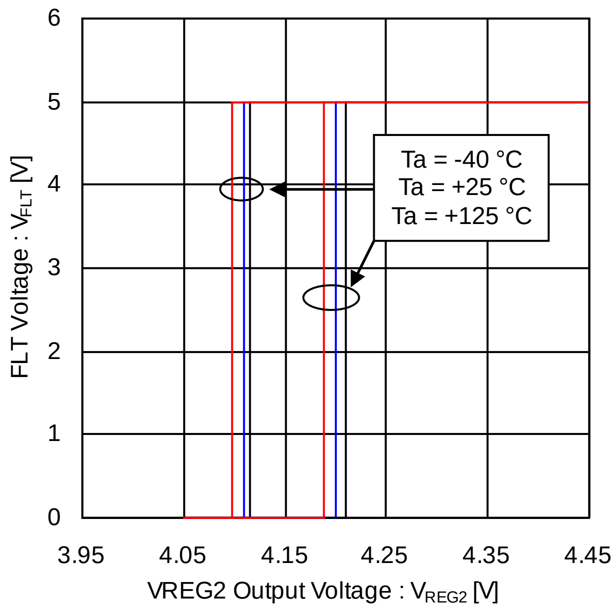


Figure 67. FLT Voltage vs VREG2 Output Voltage (VREG2 UVLO On/Off Voltage)

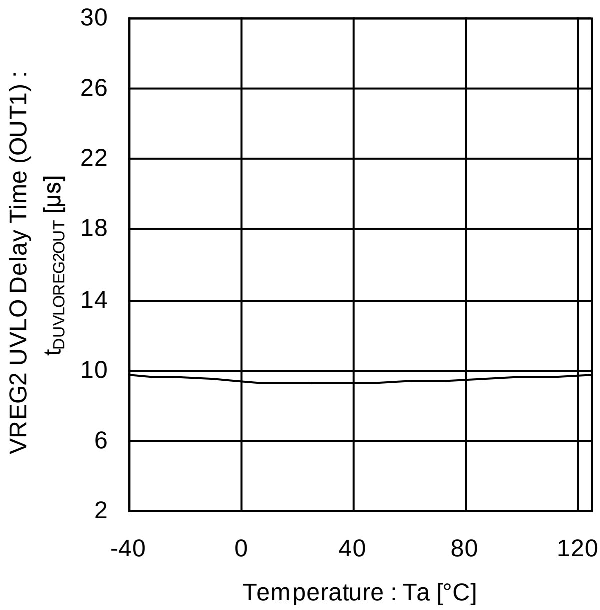


Figure 68. VREG2 UVLO Delay Time (OUT1) vs Temperature

Typical Performance Curves - continued
(Reference data)

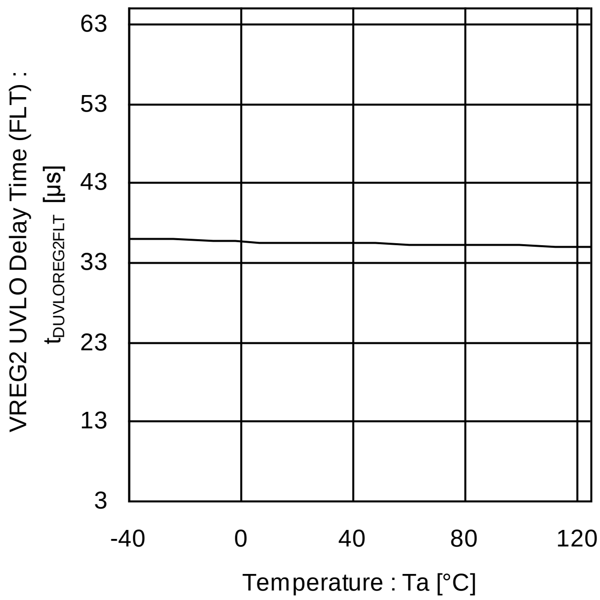


Figure 69. VREG2 UVLO Delay Time (FLT) vs Temperature

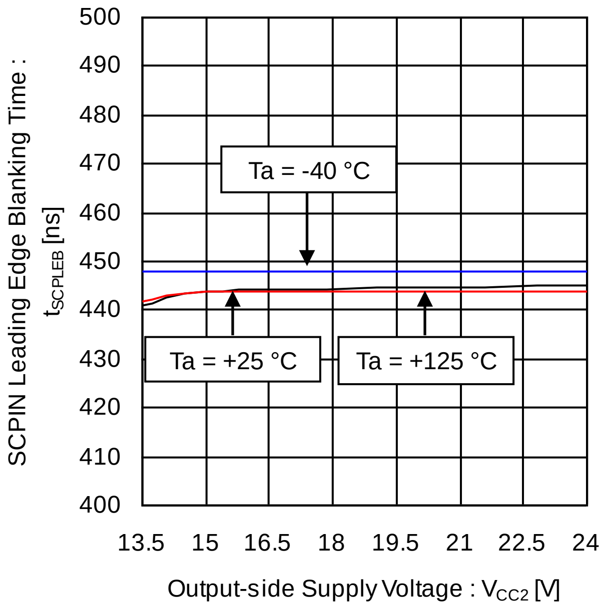


Figure 70. SCPIN Leading Edge Blanking Time vs Output-side Supply Voltage

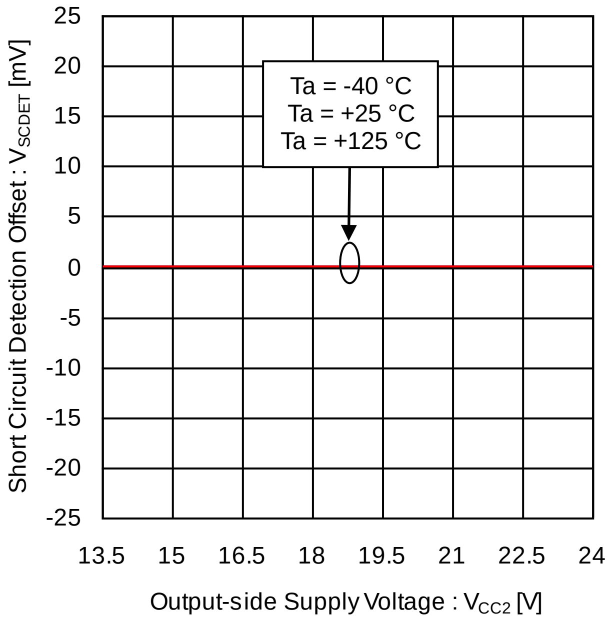


Figure 71. Short Circuit Detection Offset vs Output-side Supply Voltage

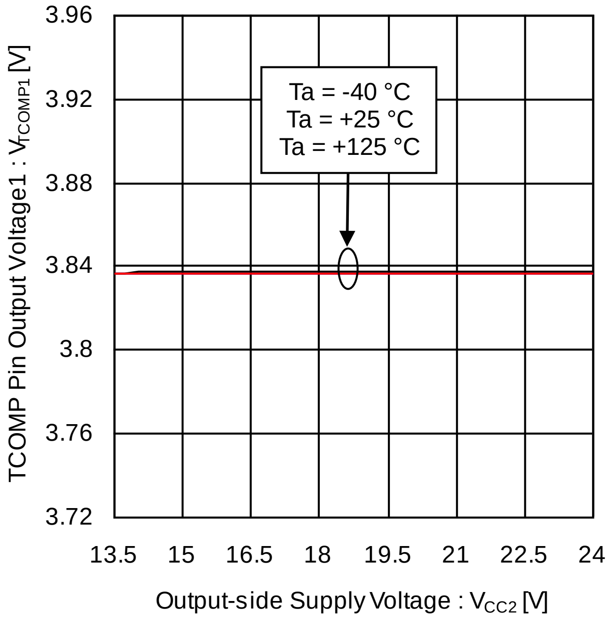


Figure 72. TCOMP Pin Output Voltage1 vs Output-side Supply Voltage (V_{TO} = 3.84 V)

Typical Performance Curves - continued
(Reference data)

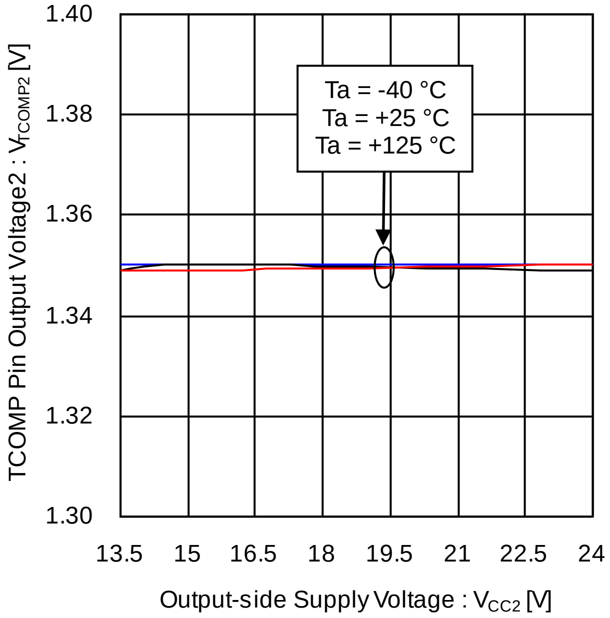


Figure 73. TCOMP Pin Output Voltage2 vs Output-side Supply Voltage (V_{TO} = 1.35 V)

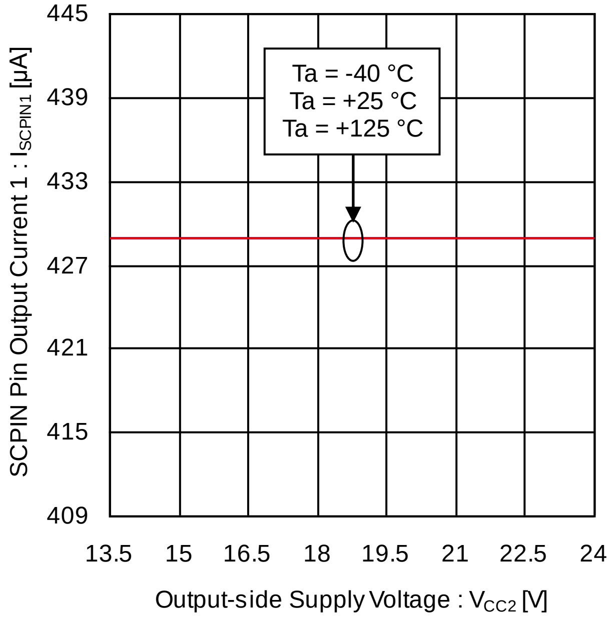


Figure 74. SCPIN Pin Output Current 1 vs Output Side Supply Voltage (V_{TO} = 3.84 V, R_{TCOMP} = 9 kΩ)

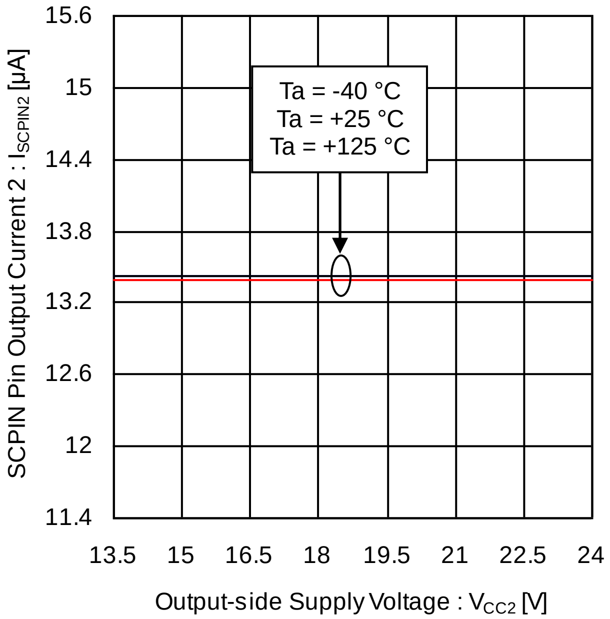


Figure 75. SCPIN Pin Output Current 2 vs Output-side Supply Voltage (V_{TO} = 1.35 V, R_{TCOMP} = 100 kΩ)

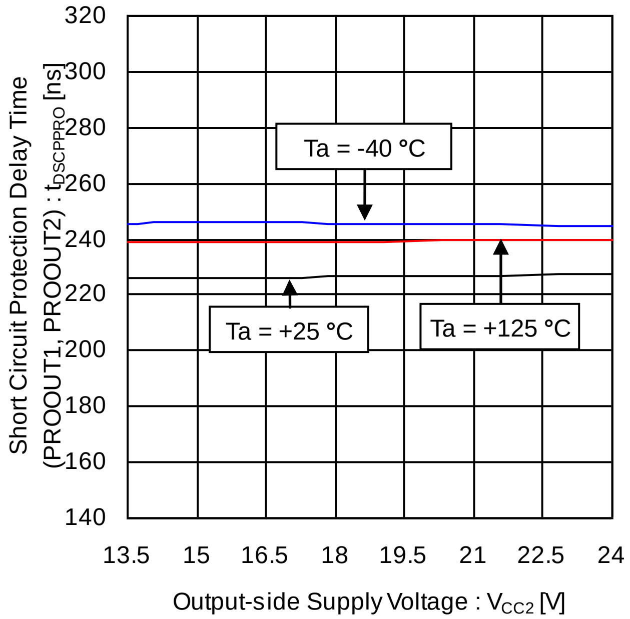


Figure 76. Short Circuit Protection Delay Time (PROOUT1, PROOUT2) vs Output-side Supply Voltage

Typical Performance Curves - continued
(Reference data)

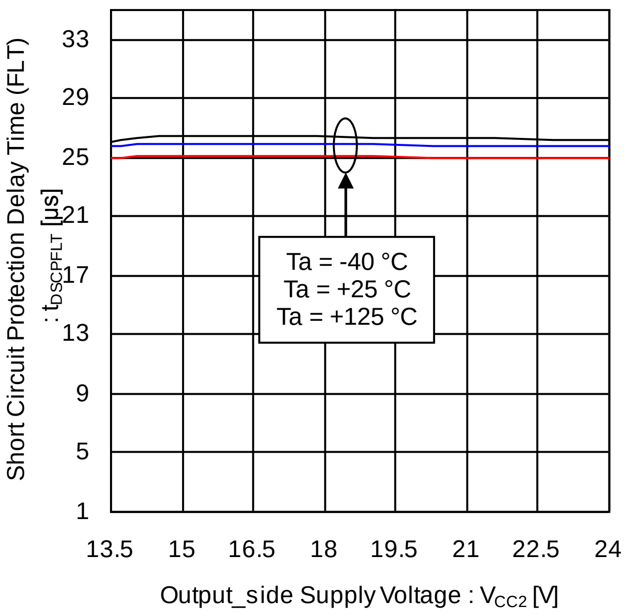


Figure 77. Short Circuit Protection Delay Time (FLT) vs Output-side Supply Voltage

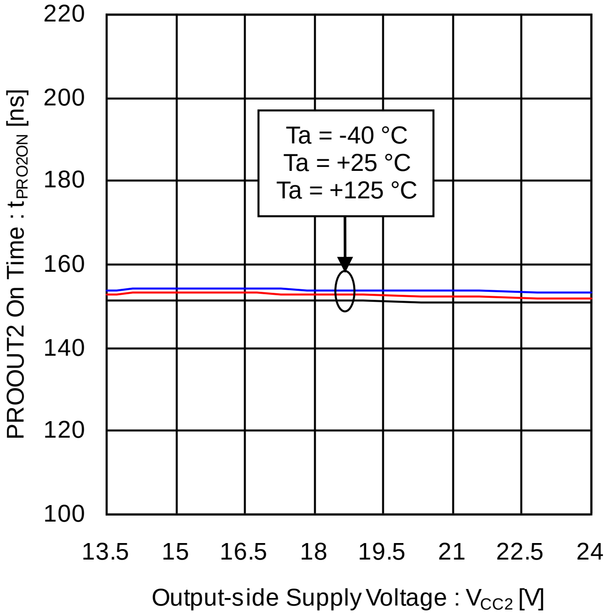


Figure 78. PROOUT2 On Time vs Output-side Supply Voltage

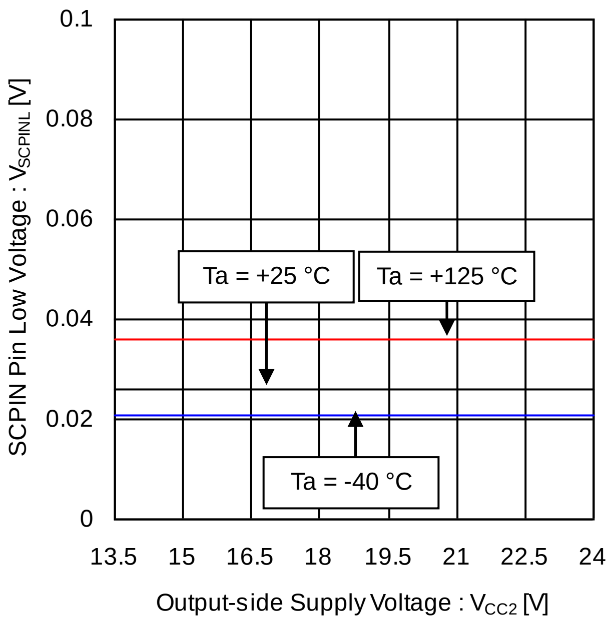


Figure 79. SCPIN Pin Low Voltage vs Output-side Supply Voltage
(I_{SCPIN} = 1 mA)

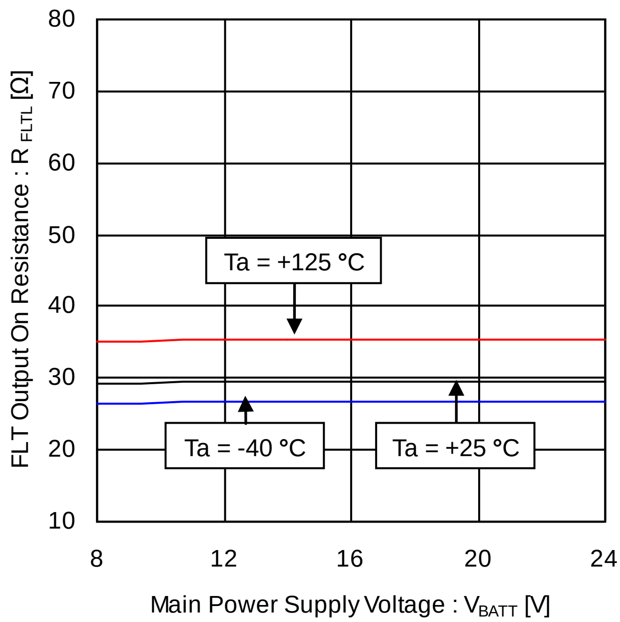


Figure 80. FLT Output On Resistance vs Main Power Supply Voltage

Typical Performance Curves - continued
(Reference data)

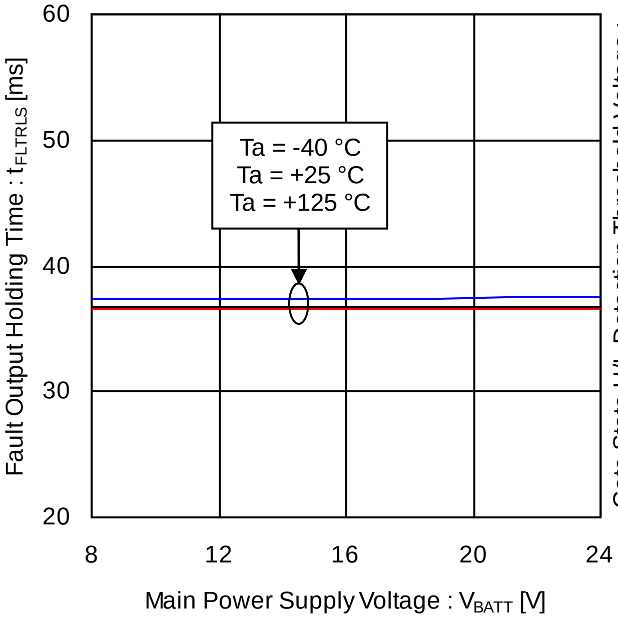


Figure 81. Fault Output Holding Time vs Main Power Supply Voltage

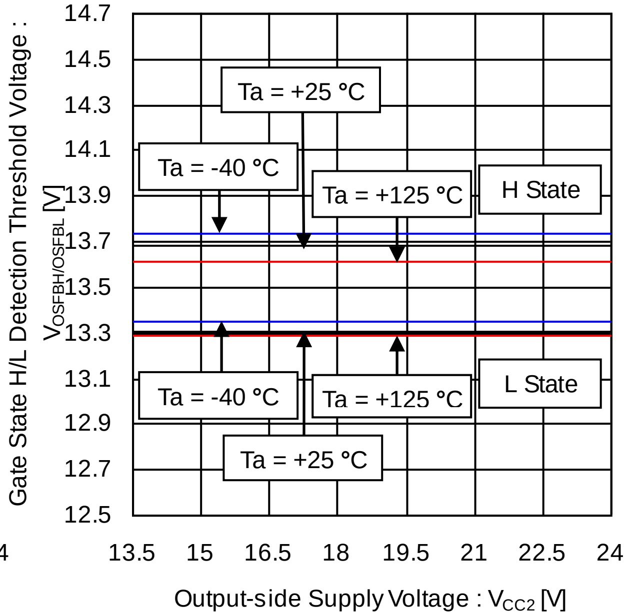


Figure 82. Gate State H/L Detection Threshold Voltage vs Output-side Supply Voltage

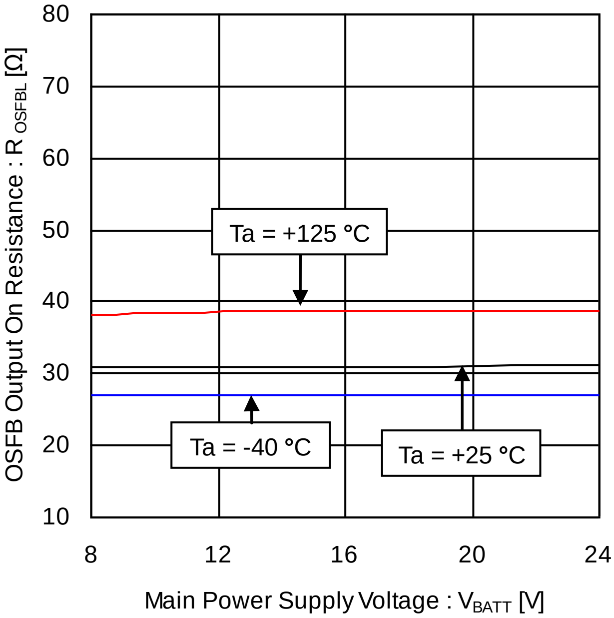


Figure 83. OSFB Output On Resistance vs Main Power Supply Voltage

Description of Pins and Cautions on Layout of Board

1. V_BATT (Main power supply pin)
   This is the main power supply pin. Connect a bypass capacitor between the V_BATT pin and the GND1 pin in order to suppress voltage variations.

2. VREG1 (Input-side internal power supply pin)
   This is the internal power supply pin on the input-side. Be sure to connect a bypass capacitor between the VREG1 pin and the GND1 pin in order to prevent oscillation and suppress voltage variation due to the driving current of the internal transformer.

3. GND1 (Input-side ground pin)
   This pin is the ground pin on the input-side.

4. VCC2 (Output-side power supply pin)
   This is the power supply pin on the output-side. To reduce voltage fluctuations due to the output current, connect a bypass capacitor between the VCC2 pin and the GND2 pin.

5. VREG2 (Output-side internal power supply pin)
   This is the internal power supply pin on the output-side. Be sure to connect a bypass capacitor between the VREG2 pin and the GND2 pin in order to prevent oscillation and suppress voltage variation due to the driving current of the internal transformer.

6. GND2 (Output-side ground pin)
   This is the ground pin on the output-side. Connect the GND2 pin to the emitter/source of output device.

7. INA, INB (Control input pin), GRSEL (Gate resistance switching pin)
   These are pins for determining the output logic. The OUT1F pin holds the previous state after GRSEL is switched and until the next the OUT1 pin is switched.

GRSEL	INB	INA	OUT1	OUT1F
L	L	L	L	Hi-Z
L	L	H	H	Hi-Z
L	H	L	L	Hi-Z
L	H	H	L	Hi-Z
H	L	L	L	L
H	L	H	H	H
H	H	L	L	L
H	H	H	L	L

8. FLT (Fault output pin)
   The FLT pin is an open drain pin that sends a fault signal when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated).

State	FLT
While in normal operation	Hi-Z
When a Fault occurs (UVLO/SCP)	L

9. OSFB (Output pin for monitoring gate condition)
   The OSFB pin is an open drain pin that outputs L when the gate theory of output element being monitored by the PROOUT1 pin is H. However, the OSFB pin becomes Hi-Z when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated).

Status	PROOUT1 (input)	OSFB
While in normal operation	H	L
	L	Hi-Z
When a Fault occurs (UVLO / SCP)	X	Hi-Z

X: Don't care

10. SENSOR (Temperature information output pin)
    This is a pin outputs the voltage of the TO pin converted to Duty cycle.

11. FB (Error amplifier inverting input pin for switching controller)
    This is a voltage feedback pin of the switching controller. This pin combine with voltage monitoring at overvoltage protection function and under voltage protection function for switching controller. When overvoltage or under voltage protection is activated, switching controller will be at OFF state (the FET_G pin outputs L). When the switching controller protection holding time $t_{DCDCRLS}$ is completed, the protection function will be released. Under voltage function is not activated during soft-start. Connect it to the VREG1 pin when the switching controller is not used.

Description of Pins and Cautions on Layout of Board – continued

12. COMP (Error amplifier output pin for switching controller)
This is the gain control pin of the switching controller. Connect a phase compensation capacitor and resistor. When the switching controller is not used, connect it to the GND1 pin.

13. FET_G (MOS FET for transformer drive control pin for switching controller)
This is a MOS FET for transformer drive control pin for switching controller. Leave it open when the switching controller is not used.

14. SENSE (Current feedback resistor connection pin for switching controller)
This is a pin connected to the resistor of the switching controller current feedback. This pin combines with current detection at overcurrent restriction function for switching controller. When overcurrent restriction is activated, switching controller will be at OFF state (the FET_G pin outputs Low), and the overcurrent restriction function will be released in the next switching period. When the switching controller is not used, connect it to the VREG1 pin.

15. OUT1, OUT1F (Output pin)
The OUT1 pin and the OUT1F pin are gate driving pins.

16. OUT2 (Miller clamp pin)
This is the miller clamp pin for preventing a rise of gate voltage due to miller current of output element. It also functions as a pin for monitoring gate voltage for miller clamp and the OUT2 pin voltage become not more than V_{OUT2ON} (Typ 2.0 V), miller clamp function operates. The OUT2 pin should be connect to the GND2 pin when miller clamp function is not used.

17. PROOUT1 (Soft turn off pin for short circuit protection / Gate voltage input pin), PROOUT2 (Fast turn off pin for short circuit protection)
They are pins for soft turn off of output element when short-circuit protection is activated. Both the PROOUT1 pin and the PROOUT2 pin turn on for t_{PRO2ON} from short circuit detection. After t_{PRO2ON}, only the PROOUT1 pin turns on. Leave the PROOUT2 pin open when the fast turn off function is not used. It also functions as the PROOUT1 pin for monitoring gate voltage for output state feedback function.

18. SCPIN (Short circuit detection pin), SCPTH (Short circuit detection threshold setting pin)
The SCPIN pin and the SCPTH pin are current detection pins for short circuit protection. When the SCPIN pin voltage becomes the SCPTH pin voltage, or more, the short circuit protection function is activated. Built-in MOSFET between the SCPIN pin and the GND2 pin for discharging electric charge of external filter when the OUT1 pin is L state. In the open state, the IC may possibly malfunction. To avoid this risk, apply voltage to SCPTH pin even when not using the short circuit protection function and connect the SCPIN pin to the GND2 pin.

19. TCOMP (Temperature compensation pin of short circuit detection voltage)
The TCOMP pin connects a resistor that sets the SCPIN pin output current according to TO pin voltage.

20. TC (Resistor connection pin for setting constant current)
The TC pin is a resistor connection for setting the constant current output. If an arbitrary resistance value is connected between the TC pin and the GND2 pin, it is possible to set the constant current value output from the TO1 pin.

21. TO (Constant current output / sensor voltage input pin)
The TO pin is constant current output / voltage input pins. It can be used as a sensor input by connecting an element with arbitrary impedance between the TO pin and the GND2 pin.

Description of Functions and Examples of Constant Setting

1. Fault Status Output

This function is used to set a fault signal from the FLT pin when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated) and hold the fault signal until fault output holding time (t_{FLTRLS}) is completed.

Status	FLT pin
Normal	Hi-Z
Fault occurs	L

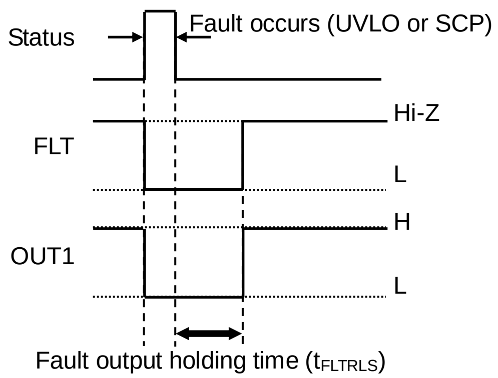


Figure 84. Fault Status Output Timing Chart

Description of Functions and Examples of Constant Setting - continued

2. Under Voltage Lockout (UVLO) Function

The BM60060FV-C incorporates the under voltage lockout (UVLO) function on V_BATT, VCC2, VREG1 and VREG2. When the power supply voltage drops to the UVLO ON voltage, the OUT1 pin and the FLT pin will both output the "L" signal and the OUT1F pin becomes the "Hi-Z" state. However, if V_BATT or VREG1 voltage drops to the UVLO ON voltage when the OUT1F pin is "L", the OUT1F pin holds "L" state. When the power supply voltage rises to the UVLO OFF voltage, UVLO will be reset after the fault output holding time t_{FLTRLS} is completed. However, if the INA pin is "L" or the INB pin is "H", when UVLO reset timing, the OUT1F pin holds the previous state until the next the OUT1 pin is switched even if the GRSEL pin is H. In addition, to prevent malfunction due to noise, filtering time are set on both V_BATT, VCC2, VREG1 and VREG2.

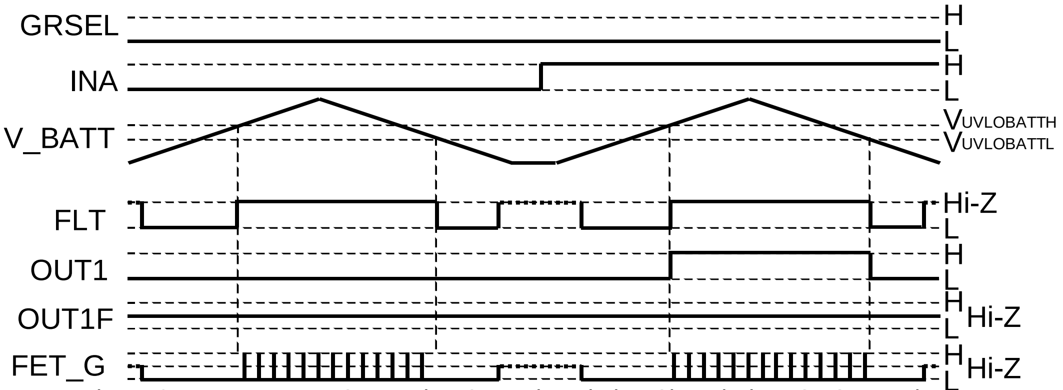


Figure 85. V_BATT UVLO Function Operation Timing Chart (When GRSEL = L)

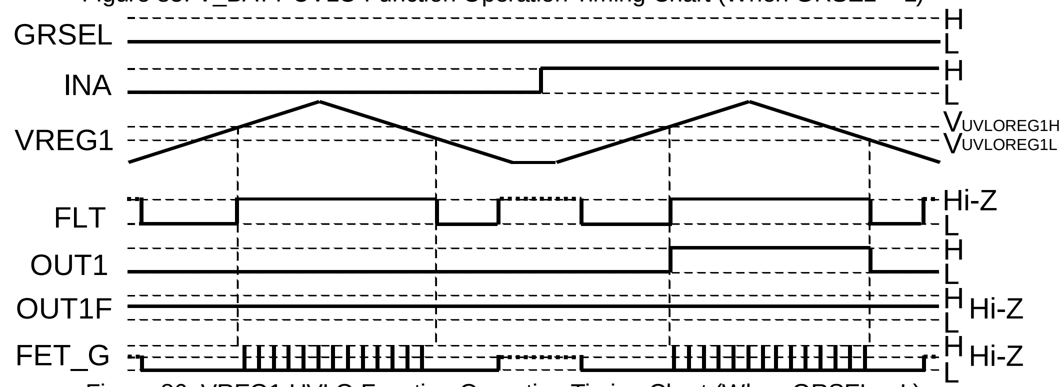


Figure 86. VREG1 UVLO Function Operation Timing Chart (When GRSEL = L)

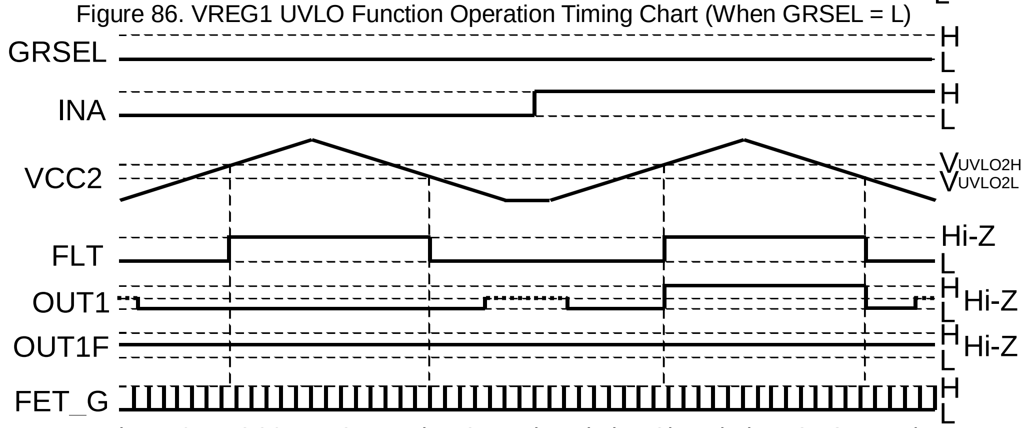


Figure 87. VCC2 UVLO Function Operation Timing Chart (When GRSEL = L)

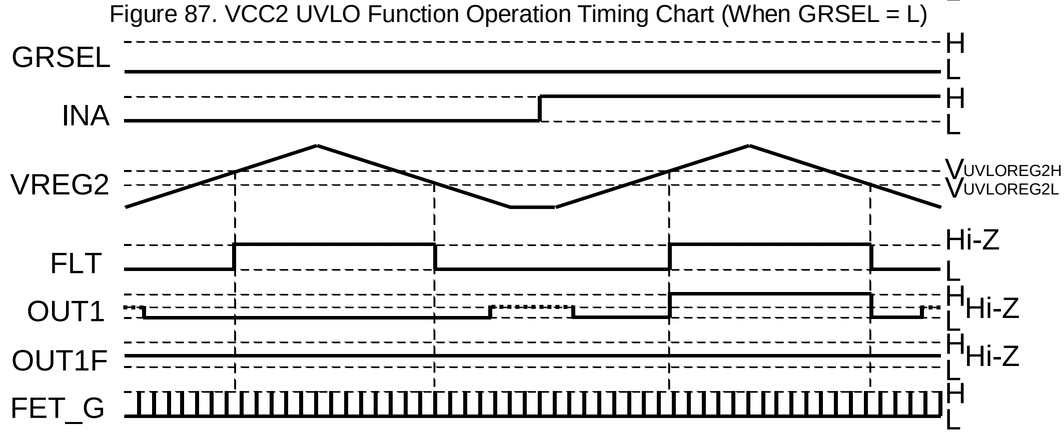


Figure 88. VREG2 UVLO Function Operation Timing Chart (When GRSEL = L)

2. Under Voltage Lockout (UVLO) Function – continued

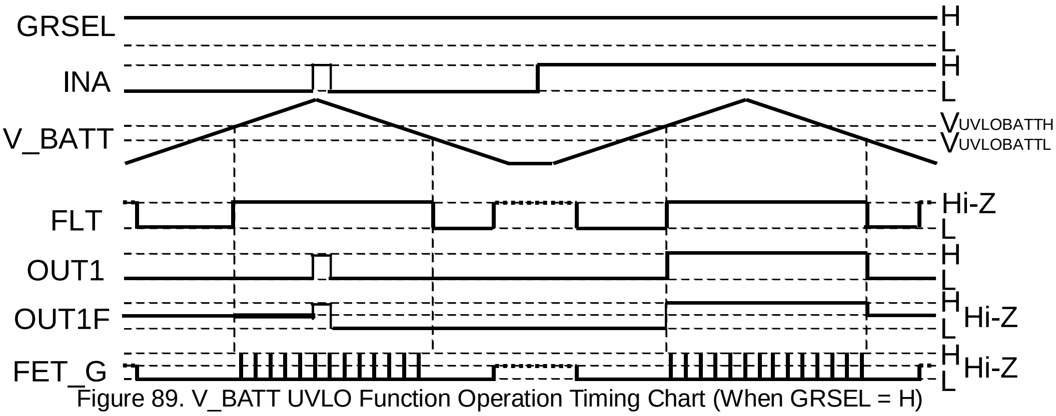


Figure 89. V_BATT UVLO Function Operation Timing Chart (When GRSEL = H)

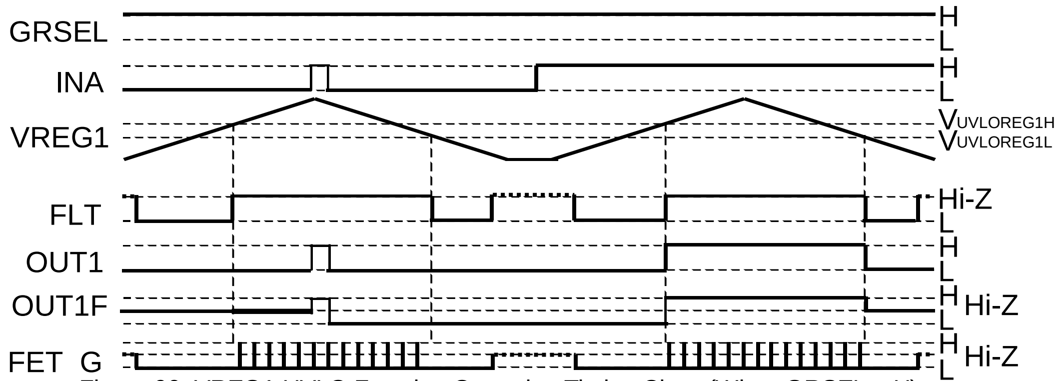


Figure 90. VREG1 UVLO Function Operation Timing Chart (When GRSEL = H)

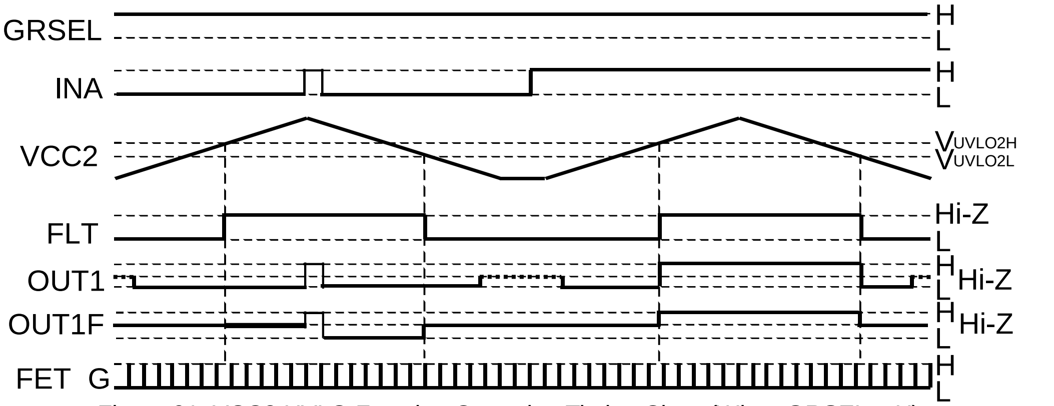


Figure 91. VCC2 UVLO Function Operation Timing Chart (When GRSEL = H)

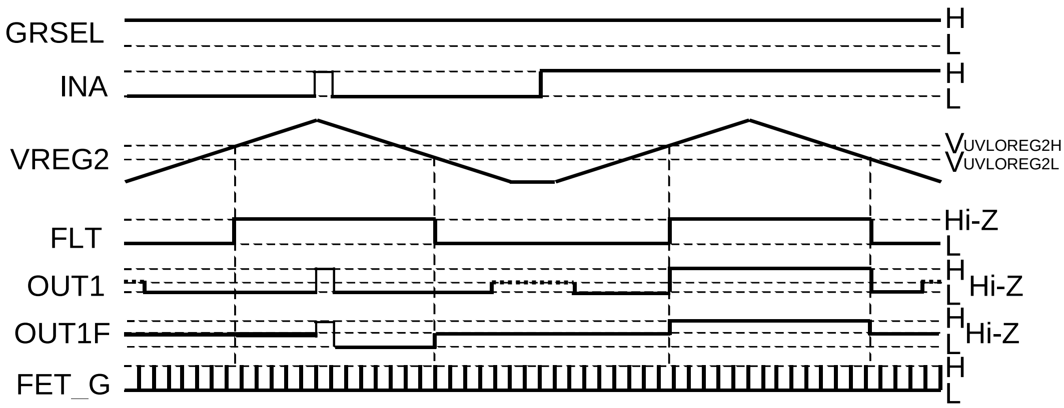


Figure 92. VREG2 UVLO Function Operation Timing Chart (When GRSEL = H)

Description of Functions and Examples of Constant Setting - continued

3. Short Circuit Protection (SCP) Function

Continuing the state where the SCPIN pin voltage ≥ the SCPTH pin voltage for $t_{DSCPPRO}$ or more, the short circuit protection function is activated. Once the function is activated, the OUT1 pin and the OUT1F pin become "Hi-Z" state and both the PROOUT1 pin and the PROOUT2 pin turn on (Fast Turn Off). After t_{PRO2ON} since the short circuit detection, the PROOUT2 pin turns off (Soft Turn Off). Furthermore, when the SCPIN pin voltage < the SCPTH pin voltage and the OUT2 pin voltage < V_{OUT2ON}, the OUT1 pin and the OUT2 pin become L. In additional, the FLT pin becomes L after $t_{DSCPFLT}$ since the short circuit protection function is activated. Finally, when the fault output holding time t_{FLTRLS} is completed, the SCP function will be released and the FLT pin becomes "Hi-Z". The PROOUT1 pin hold L state until the OUT1 pin becomes H.

This IC has a built-in temperature characteristics correction function for short circuit detection voltage. Since the SCPIN pin outputs current I_{SCPIN} according to the TO pin voltage, the IC is capable of correcting the temperature characteristics for short circuit detection voltage using voltage drop of resistor $R_{SCPCOMP}$ connected to the SCPIN pin in series. The SCPIN pin output current I_{SCPIN} can be formulated as:

$$I_{SCPIN}\,[\text{mA}] = V_{TO}\,[\text{V}] \,/\, R_{TCOMP}\,[\text{k}\Omega]$$

Therefore, short circuit detection voltage V_{SC} can be formulated as:

$$V_{SC}\,[\text{V}] = V_{SCPTH}\,[\text{V}] - V_{TO}\,[\text{V}] \times R_{SCPCOMP}\,[\text{k}\Omega] \,/\, R_{TCOMP}\,[\text{k}\Omega]$$

Still more, built-in MOSFET between the SCPIN pin and the GND2 pin for discharging electric charge of external filter when OUT1 is L state. This MOSFET turns off after t_{SCPLEB} since the OUT1 pin becomes H. And this MOSFET immediately turns on after the OUT1 pin becomes L. Also, this MOSFET immediately turns on after short circuit detection.

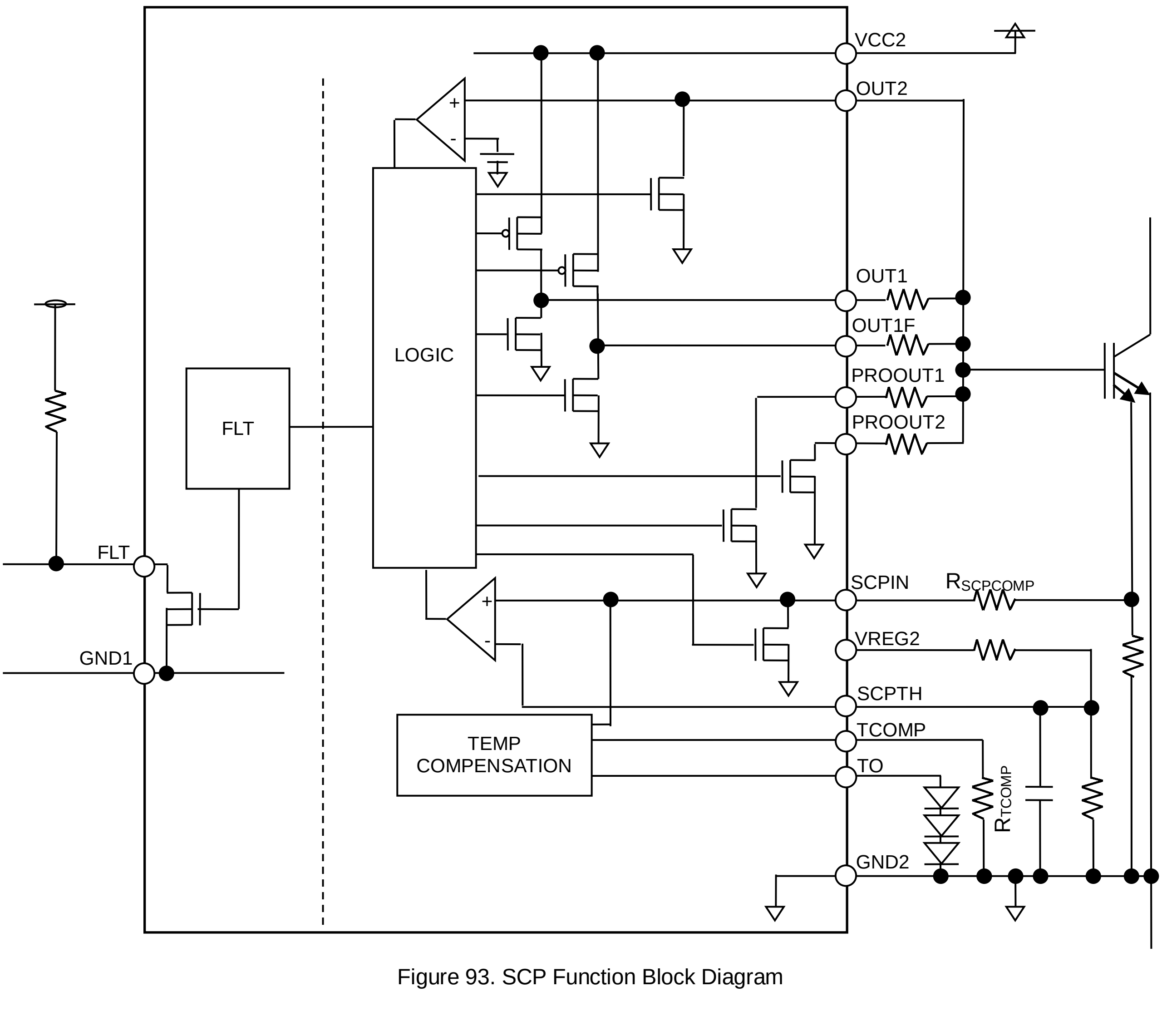


Figure 93. SCP Function Block Diagram

3. Short Circuit Protection (SCP) Function – continued

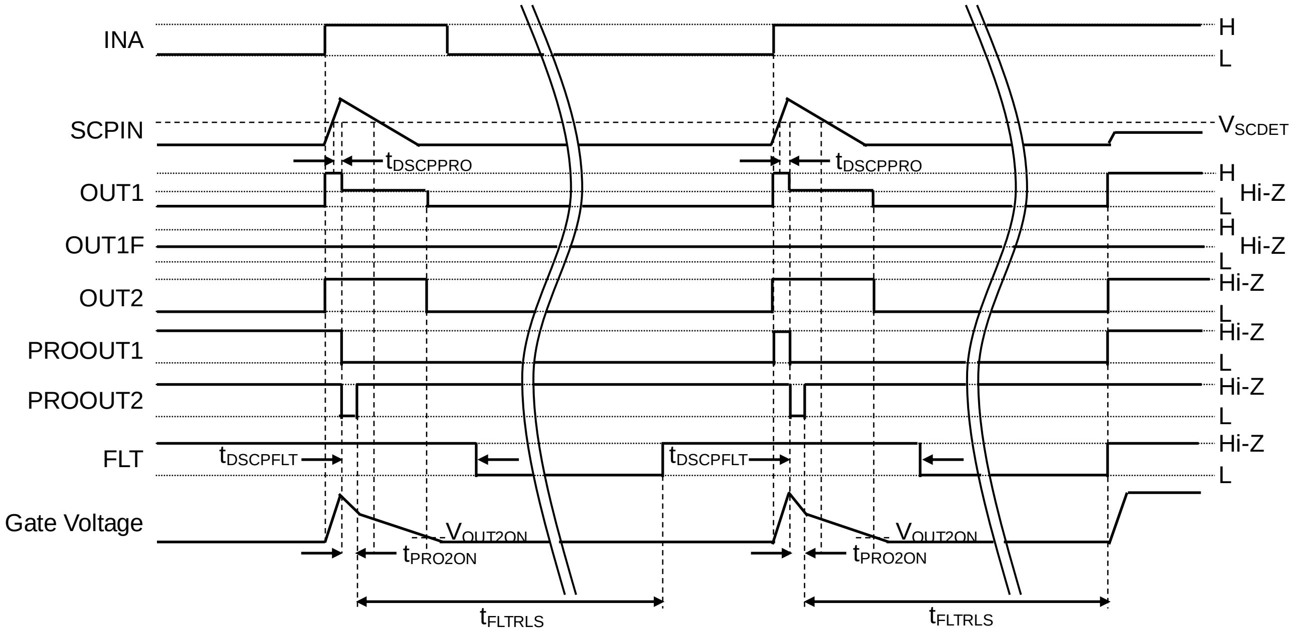
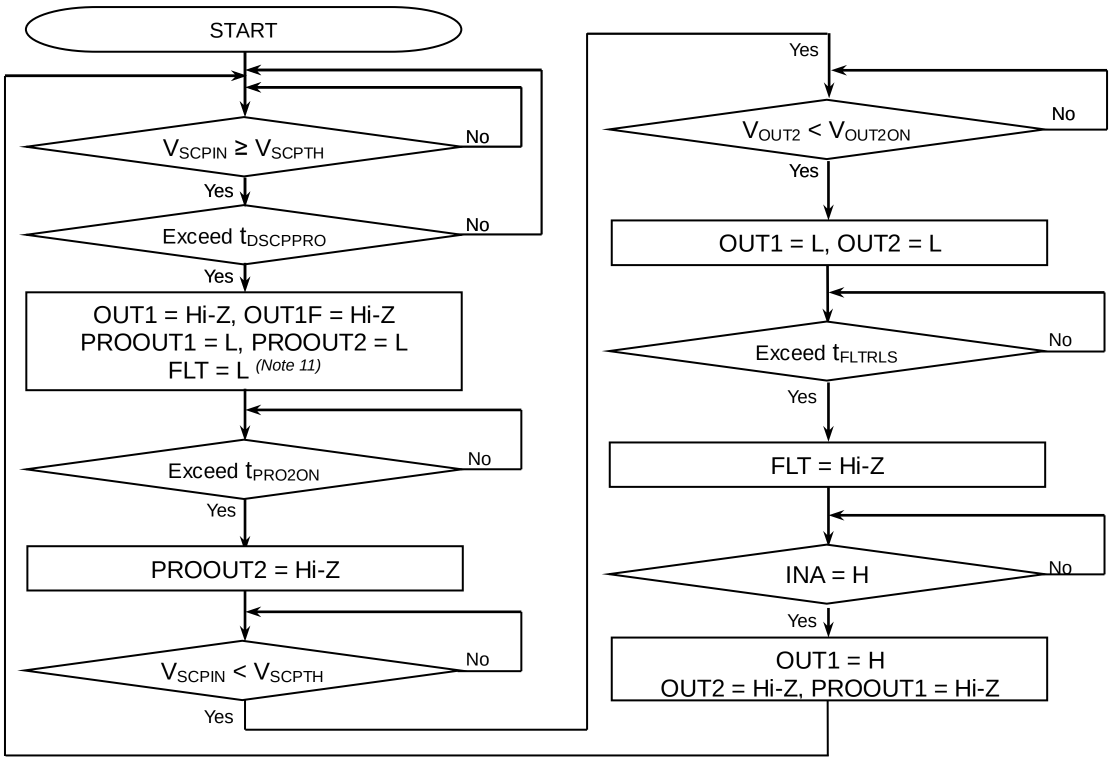


Figure 94. SCP Function Operation Timing Chart (When GRSEL = L)



(Note 11) The FLT pin becomes "L" after $t_{DSCPFLT}$

Figure 95. SCP Function Operation Status Transition Diagram (When GRSEL = L)

3. Short Circuit Protection (SCP) Function – continued

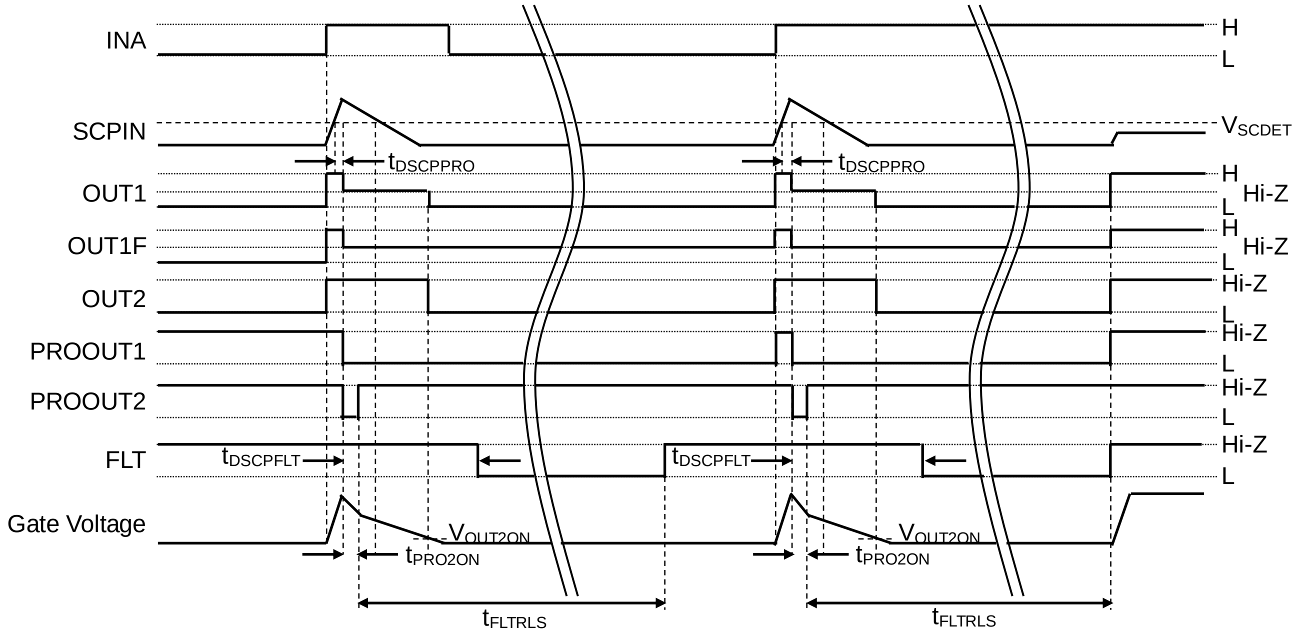
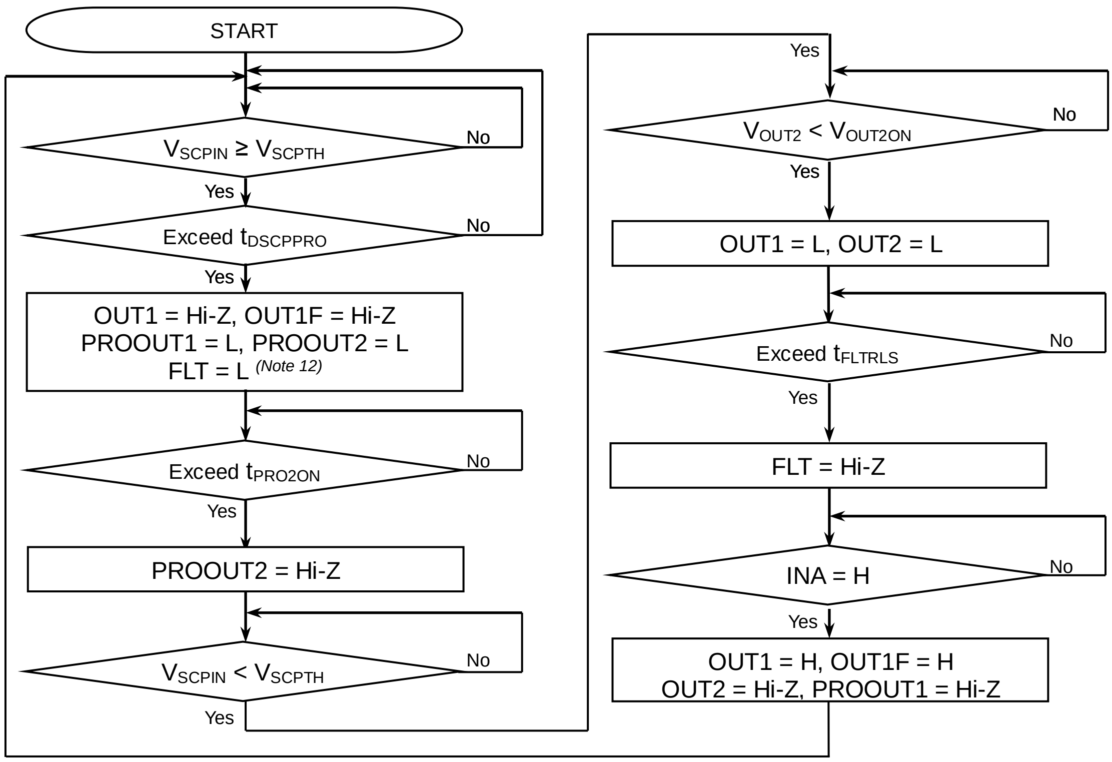


Figure 96. SCP Function Operation Timing Chart (When GRSEL = H)



(Note 12) The FLT pin becomes "L" after $t_{DSCPFLT}$

Figure 97. SCP Function Operation Status Transition Diagram (When GRSEL = H)

Description of Functions and Examples of Constant Setting - continued

4. Miller Clamp (MC) Function

When the OUT1 pin = L and the OUT2 pin voltage < V_{OUT2ON}, internal MOS of the OUT2 pin is turned ON and miller clamp function operates. After miller clamp function operates, the OUT2 pin keeps L state until the OUT1 pin goes H again. While the short circuit protection function is activated, miller clamp function operates when the OUT2 pin voltage < V_{OUT2ON}.

Short Circuit	OUT1	OUT2 (Input)	OUT2 (Output)
Not detected	H	X	Hi-Z
	L	Not less than V_{OUT2ON}	Hi-Z
	L	less than V_{OUT2ON}	L
Detected	Hi-Z	Not less than V_{OUT2ON}	Hi-Z
	Hi-Z	less than V_{OUT2ON}	L

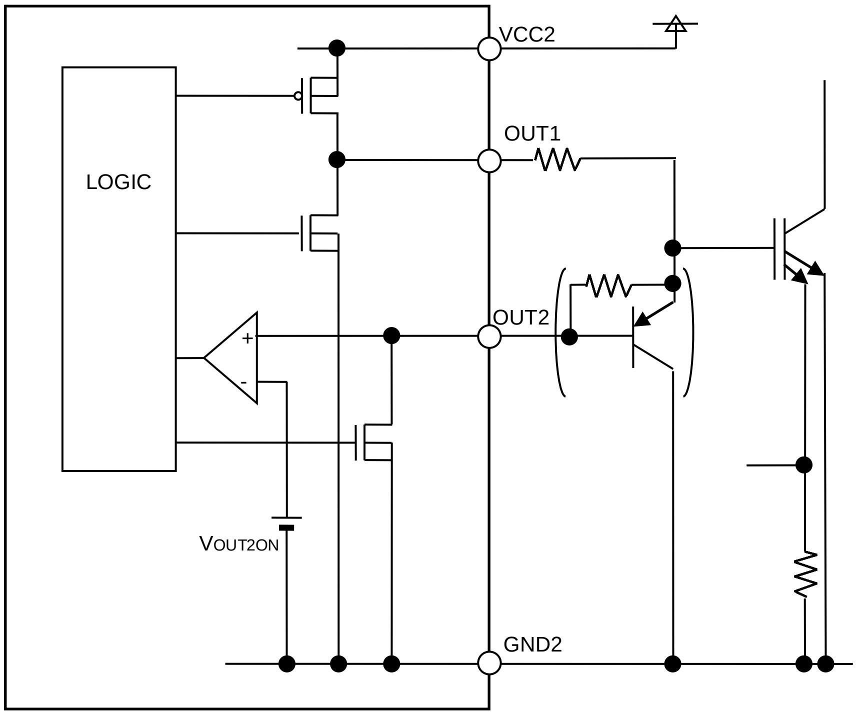


Figure 98. Miller Clamp Function Block Diagram

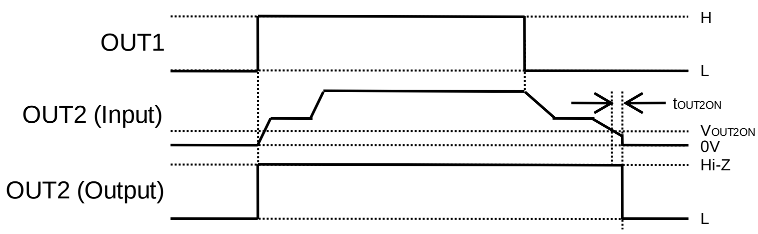


Figure 99. Miller Clamp Function Operation Timing Chart

Description of Functions and Examples of Constant Setting - continued

5. Gate Resistance Switching Function

When the GRSEL pin is L, the OUT1 pin alone outputs the theory according to the input of the INA pin and INB pin, and the OUT1F pin becomes Hi-Z. When the GRSEL pin is H, the OUT1 pin and the OUT1F pin output the theory according to the input of the INA pin and INB pin. The OUT1F pin holds the previous state until next switching of the OUT1 pin after the GRSEL pin is switched.

GRSEL	INB	INA	OUT1	OUT1F
L	L	L	L	Hi-Z
L	L	H	H	Hi-Z
L	H	L	L	Hi-Z
L	H	H	L	Hi-Z
H	L	L	L	L
H	L	H	H	H
H	H	L	L	L
H	H	H	L	L

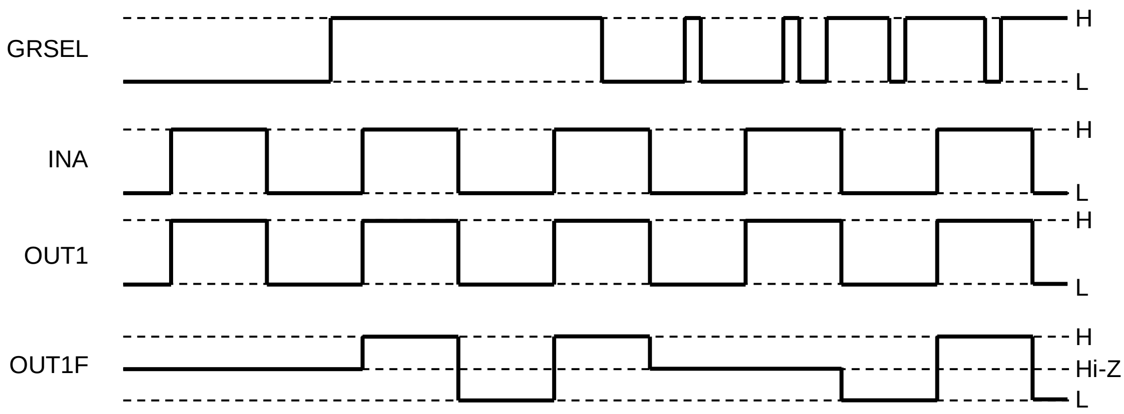


Figure 100. Gate Resistance Switching Function Operation Timing Chart

6. Output State Feedback Function

When the output element gate state being monitored at the PROOUT1 pin is H, the OSFB pin becomes L. However, when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated), the OSFB pin becomes Hi-Z.

State	PROOUT1 Input	OSFB
Normal operation	H	L
	L	Hi-Z
Fault occurs	X	Hi-Z

X: Don't care

Description of Functions and Examples of Constant Setting - continued

7. Switching Controller

(1) Basic action

This IC has a built-in switching controller which repeats ON/OFF synchronizing with internal clock. When V_BATT voltage is supplied (V_{BATT} > $V_{UVLOBATTH}$ and VREG1 > $V_{UVLOREG1}$), the FET_G pin starts switching by soft-start. Output voltage is determined by the following equation by external resistance and winding ratio "n" of flyback transformer (n = V_{OUT2} side winding number/V_{OUT1} side winding number)

$$V_{OUT} = V_{FB} \times \{(R1+R2)/R2\} \times n \text{ [V]}$$

(2) MAX DUTY

When, for example, output load is large, and voltage level of the SENSE pin does not reach current detection level, output is forcibly turned OFF by Maximum On Duty (D_{ONMAX}).

(3) Over voltage protection function, under voltage protection function

The switching controller has protection function as overvoltage protection (OVP) and under voltage protection (UVP). OVP and UVP monitor the voltage of the FB pin. When the protection function is activated, switching controller will be OFF state (the FET_G pin outputs Low). The switching controller protection holding time ($t_{DCDCRLS}$) is completed, the protection function will be released. Under voltage function is not activated during soft-start.

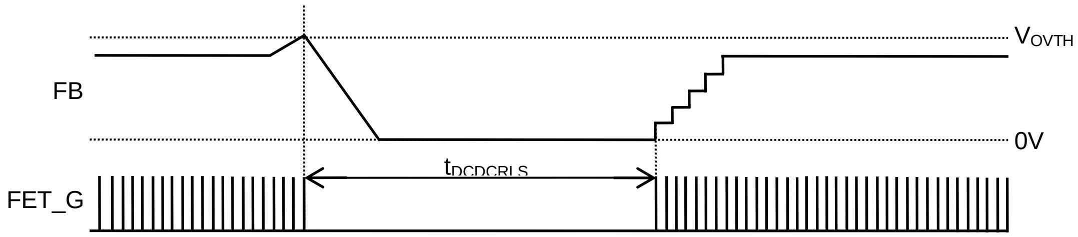


Figure 101. Over Voltage Protection Function Operation Timing Chart

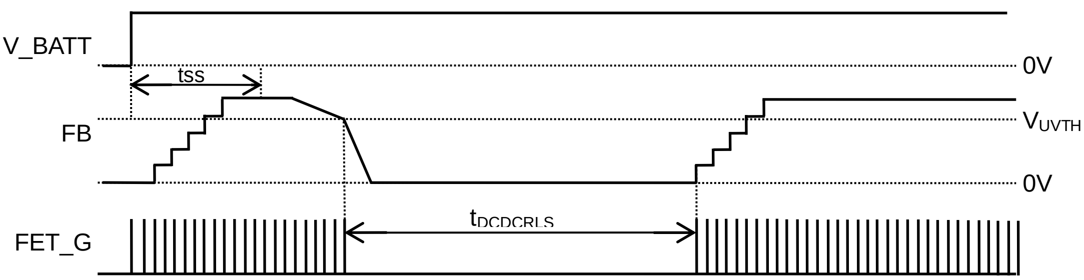


Figure 102. Under Voltage Protection Function Operation Timing Chart

(4) Overcurrent restriction function

The switching controller has overcurrent restriction function that monitors the SENSE pin voltage. When overcurrent restriction is activated, switching controller will be at OFF state (FET_G = L), and the overcurrent restriction function will be released in the next switching period.

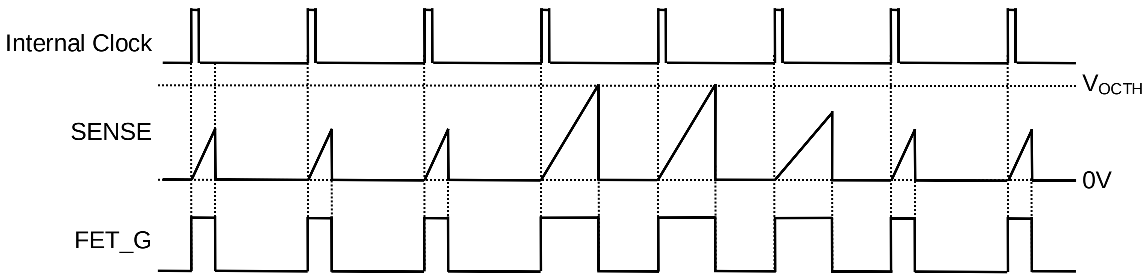


Figure 103. Overcurrent Restriction Function Operation Timing Chart

7. Switching Controller – continued

(5) Pin conditions when switching controller is not used

Implement pin setting as shown below when switching power supply is not used.

Pin Number	Pin Name	Treatment Method
22	FB	Connect to VREG1
23	COMP	Connect to GND1
24	V_BATT	Connect power supply
25	VREG1	Connect capacitor
26	FET_G	No connection
27	SENSE	Connect to VREG1

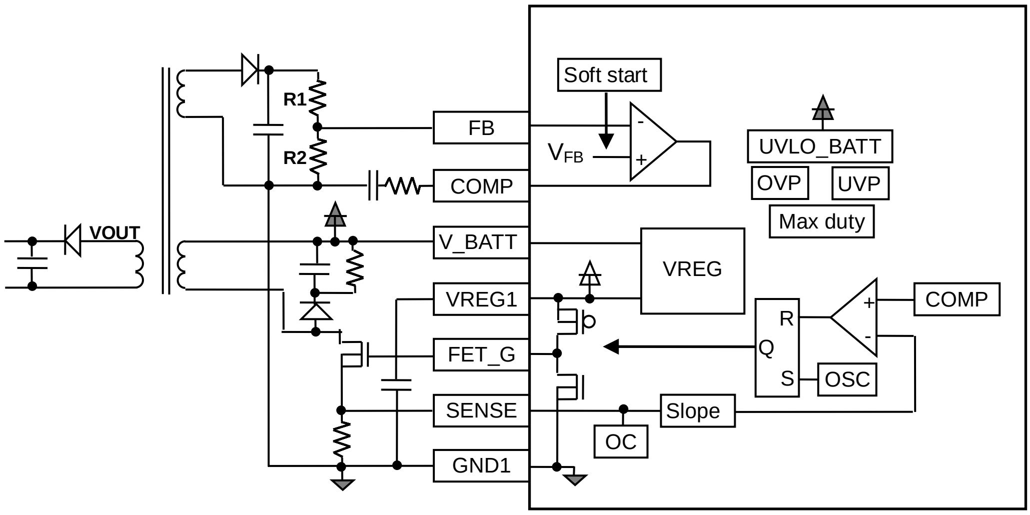


Figure 104. Block Diagram of switching controller

Description of Functions and Examples of Constant Setting - continued

8. Temperature Monitor Function

This IC has a built-in constant current circuit and constant current is supplied from the TO pin. This current value I_{TO} can be adjusted in accordance with the resistance value connected between the TC pin and the GND2 pin. Furthermore, the TO pin has voltage input function, and outputs signal of the TO pin voltage converted to Duty from the SENSOR pin.

Constant Current Value $I_{TO}[\mathrm{mA}] = 10 \times V_{TC}[\mathrm{V}] \,/\, R_{TC}[\mathrm{k\Omega}]$

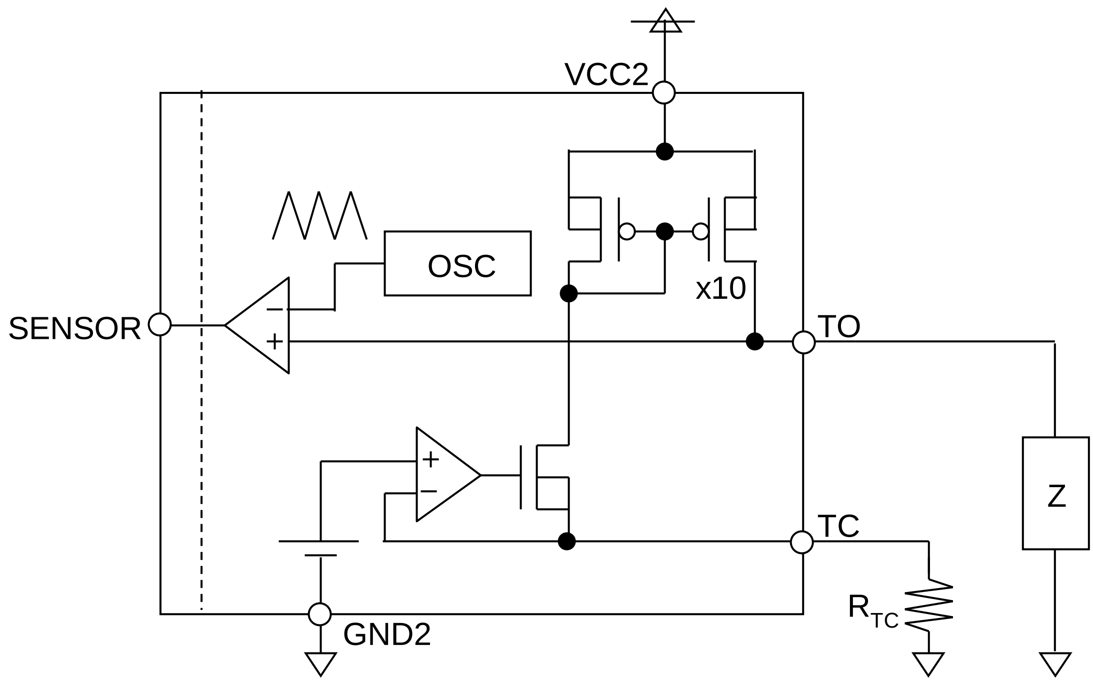


Figure 105. Block Diagram of Temperature Monitor Function

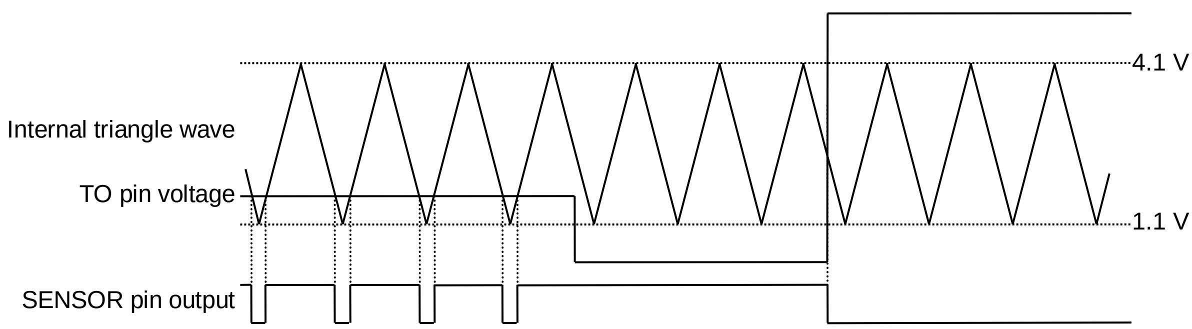
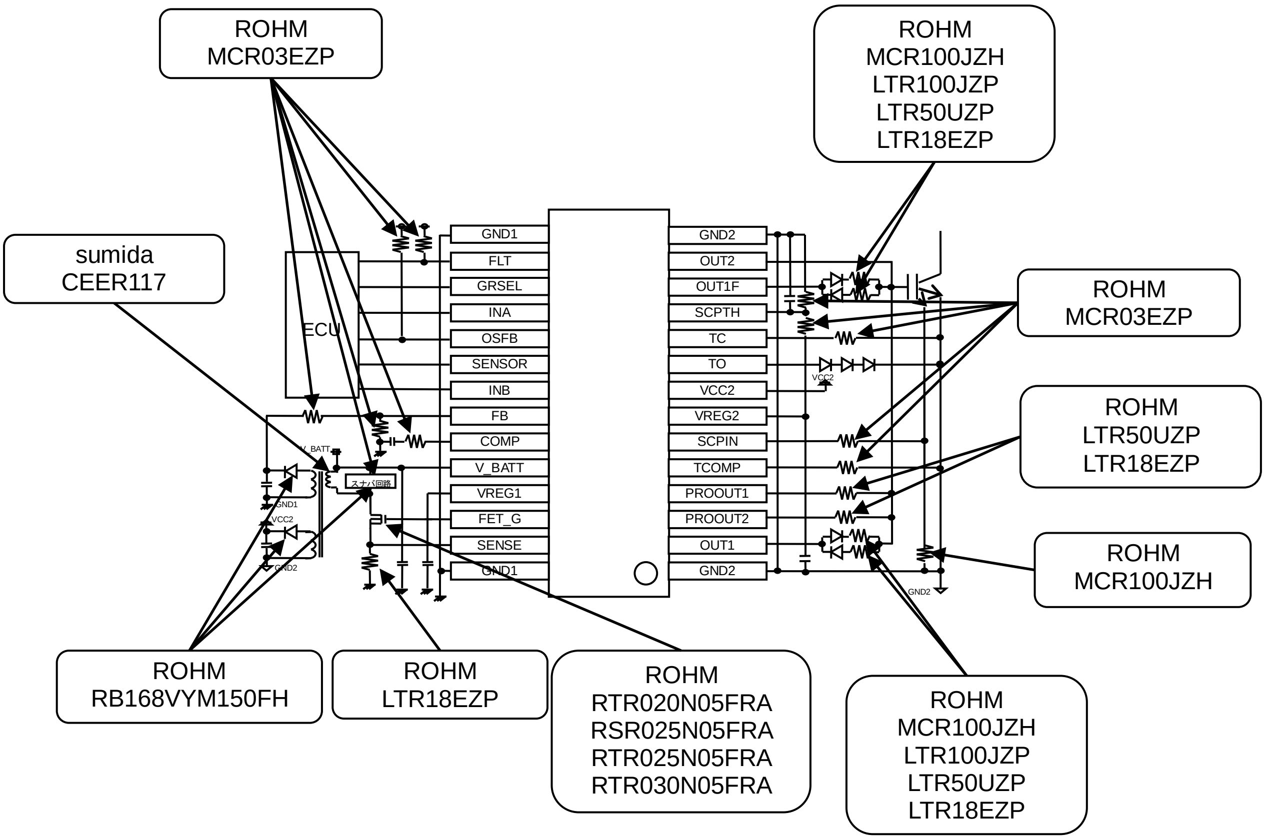


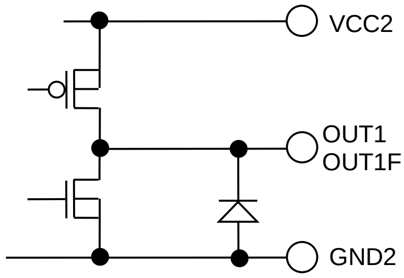
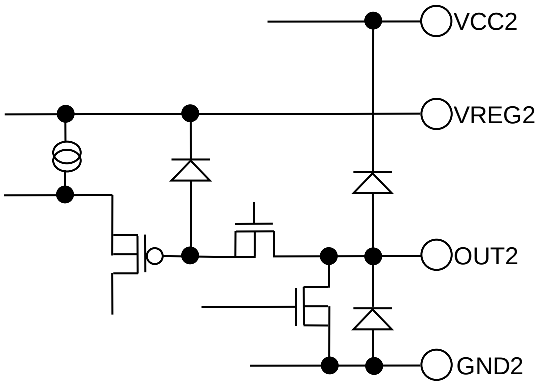
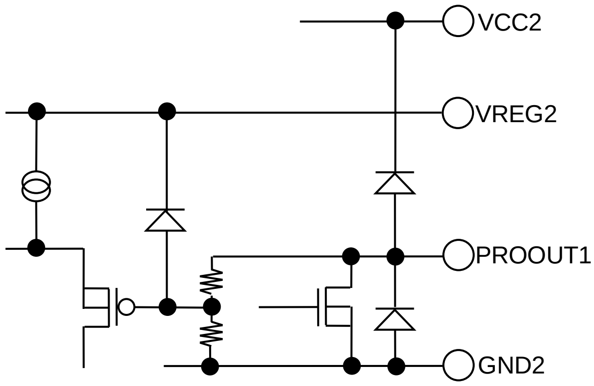
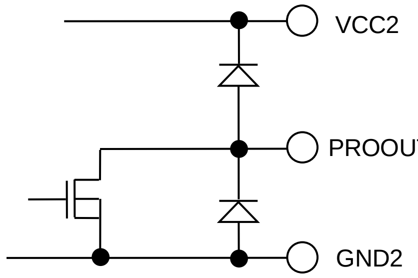
Figure 106. Temperature Monitor Function Timing Chart

Selection of Components Externally Connected

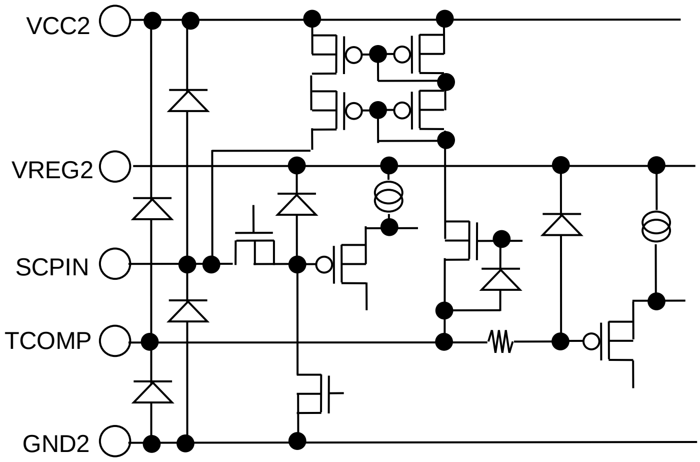
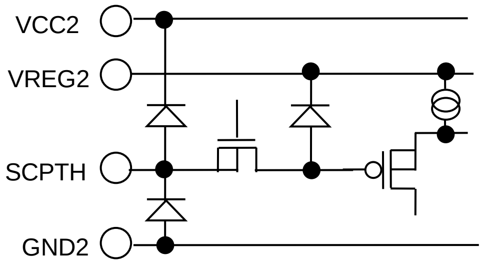
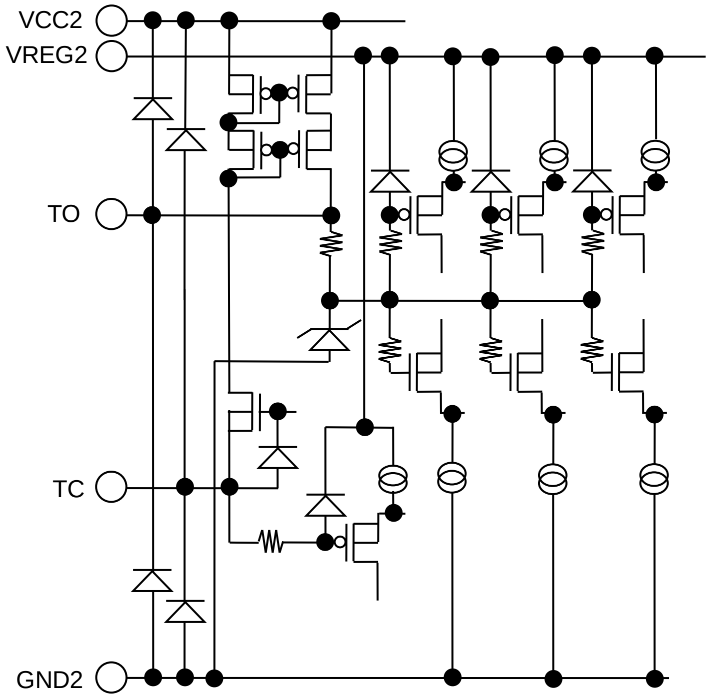
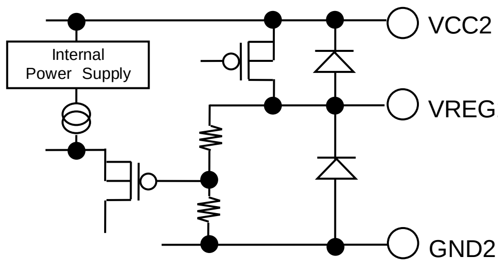
The following components are recommended for external components.



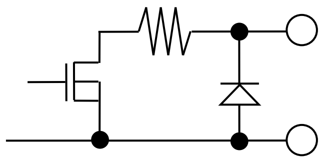
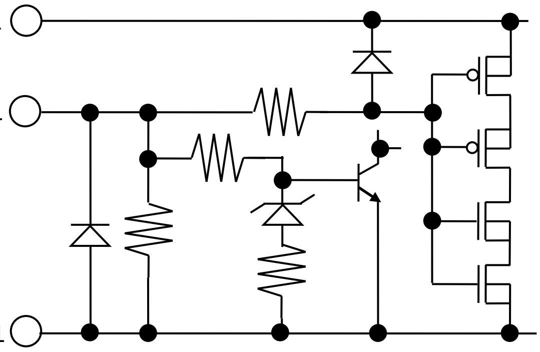
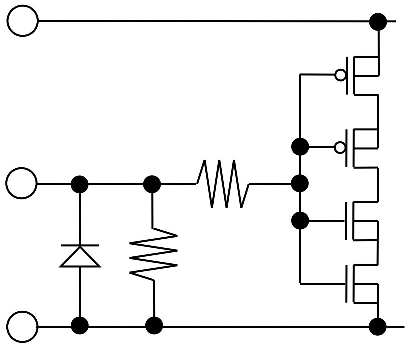
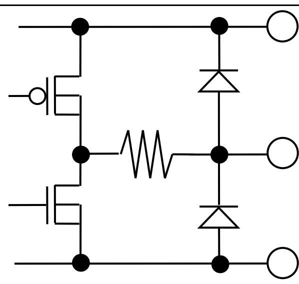
I/O Equivalent Circuits

<table>
<tr><th rowspan="2">Pin No.</th><th>Pin Name</th><th rowspan="2">Input Output Equivalent Circuit Diagram</th></tr>
<tr><th>Pin Function</th></tr>
<tr><td rowspan="2">2</td><td>OUT1</td><td rowspan="4">
</td></tr>
<tr><td>Output pin</td></tr>
<tr><td rowspan="2">12</td><td>OUT1F</td></tr>
<tr><td>Output pin</td></tr>
<tr><td rowspan="2">13</td><td>OUT2</td><td rowspan="2">
</td></tr>
<tr><td>Miller clamp pin</td></tr>
<tr><td rowspan="2">4</td><td>PROOUT1</td><td rowspan="2">
</td></tr>
<tr><td>Soft turn off pin for short circuit protection / Gate voltage input pin</td></tr>
<tr><td rowspan="2">3</td><td>PROOUT2</td><td rowspan="2">
</td></tr>
<tr><td>Fast turn off pin for short circuit protection</td></tr>
</table>

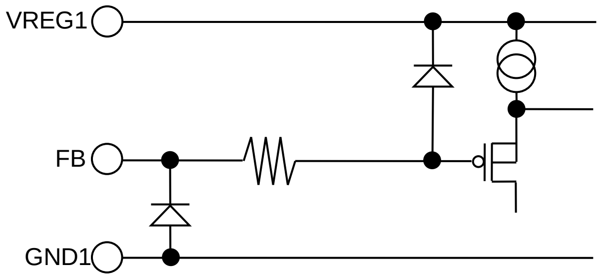
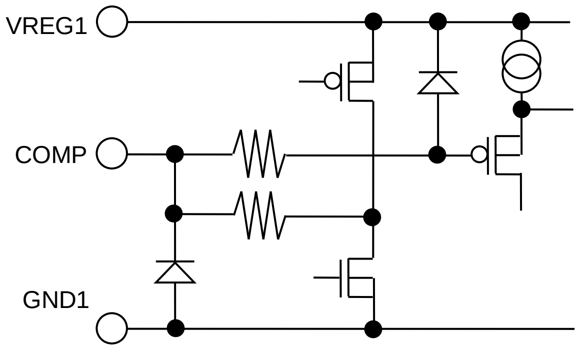
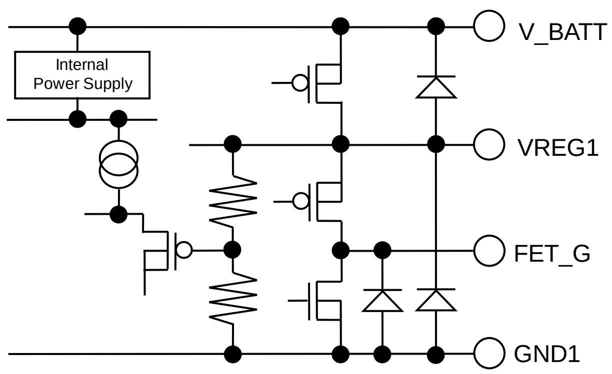
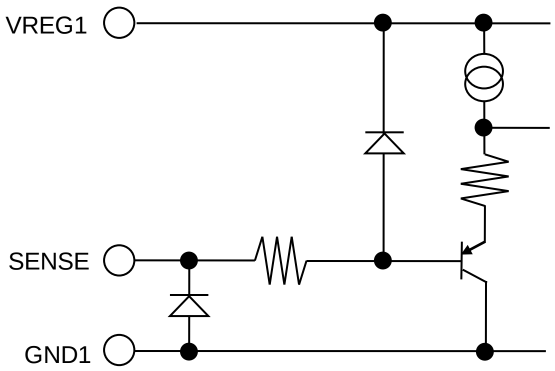
I/O Equivalence Circuits - Continued

Pin No.	Pin Name	Pin Function	Input Output Equivalent Circuit Diagram
5	TCOMP	Temperature compensation pin of short circuit detection voltage	
6	SCPIN	Short circuit detection pin	
11	SCPTH	Short circuit detection threshold setting pin	
9	TO	Constant current output pin / Sensor voltage input pin	
10	TC	Constant current setting resistor connection pin	
7	VREG2	Output-side internal power supply pin	

I/O Equivalence Circuits - Continued

<table>
<tr><td rowspan="2">Pin No.</td><td>Pin Name</td><td rowspan="2">Input Output Equivalent Circuit Diagram</td></tr>
<tr><td>Pin Function</td></tr>
<tr><td rowspan="2">16</td><td>FLT</td><td rowspan="4">
</td></tr>
<tr><td>Fault output pin</td></tr>
<tr><td rowspan="2">19</td><td>OSFB</td></tr>
<tr><td>Output state feedback output pin</td></tr>
<tr><td rowspan="2">17</td><td>GRSEL</td><td rowspan="2">
</td></tr>
<tr><td>Gate resistance switching pin</td></tr>
<tr><td rowspan="2">18</td><td>INA</td><td rowspan="4">
</td></tr>
<tr><td>Control input pin</td></tr>
<tr><td rowspan="2">21</td><td>INB</td></tr>
<tr><td>Control input pin</td></tr>
<tr><td rowspan="2">20</td><td>SENSOR</td><td rowspan="2">
</td></tr>
<tr><td>Temperature information output pin</td></tr>
</table>

I/O Equivalence Circuits - Continued

<table>
<tr><th rowspan="2">Pin No.</th><th>Pin Name</th><th rowspan="2">Input Output Equivalent Circuit Diagram</th></tr>
<tr><th>Pin Function</th></tr>
<tr><td rowspan="2">22</td><td>FB</td><td rowspan="2"></td></tr>
<tr><td>Error amplifier inverting input pin for switching controller</td></tr>
<tr><td rowspan="2">23</td><td>COMP</td><td rowspan="2"></td></tr>
<tr><td>Error amplifier output pin for switching controller</td></tr>
<tr><td rowspan="2">25</td><td>VREG1</td><td rowspan="4"></td></tr>
<tr><td>Input-side internal power supply pin</td></tr>
<tr><td rowspan="2">26</td><td>FET_G</td></tr>
<tr><td>MOS FET for transformer drive control pin for switching controller</td></tr>
<tr><td rowspan="2">27</td><td>SENSE</td><td rowspan="2"></td></tr>
<tr><td>Current feedback resistor connection pin for switching controller</td></tr>
</table>

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC
This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

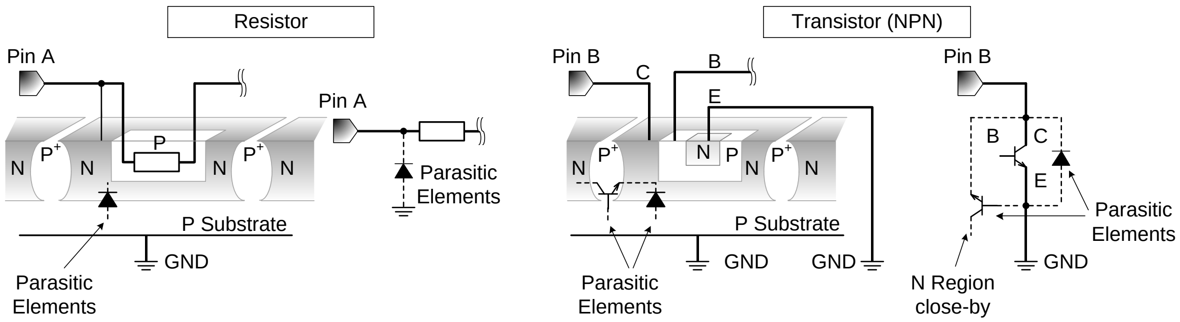
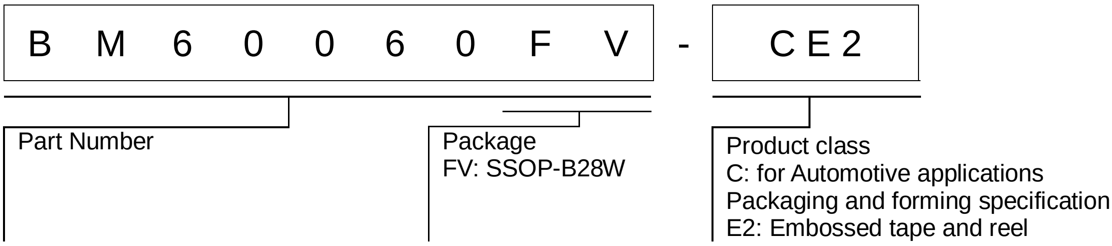


Figure 107. Example of IC Structure

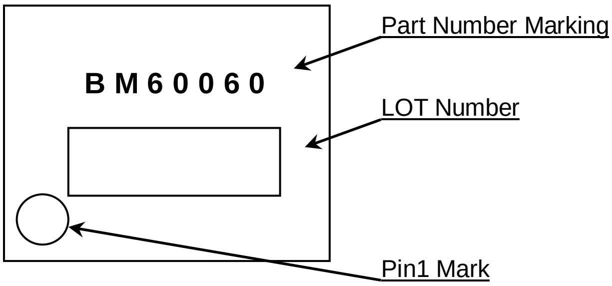
11. Ceramic Capacitor
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information



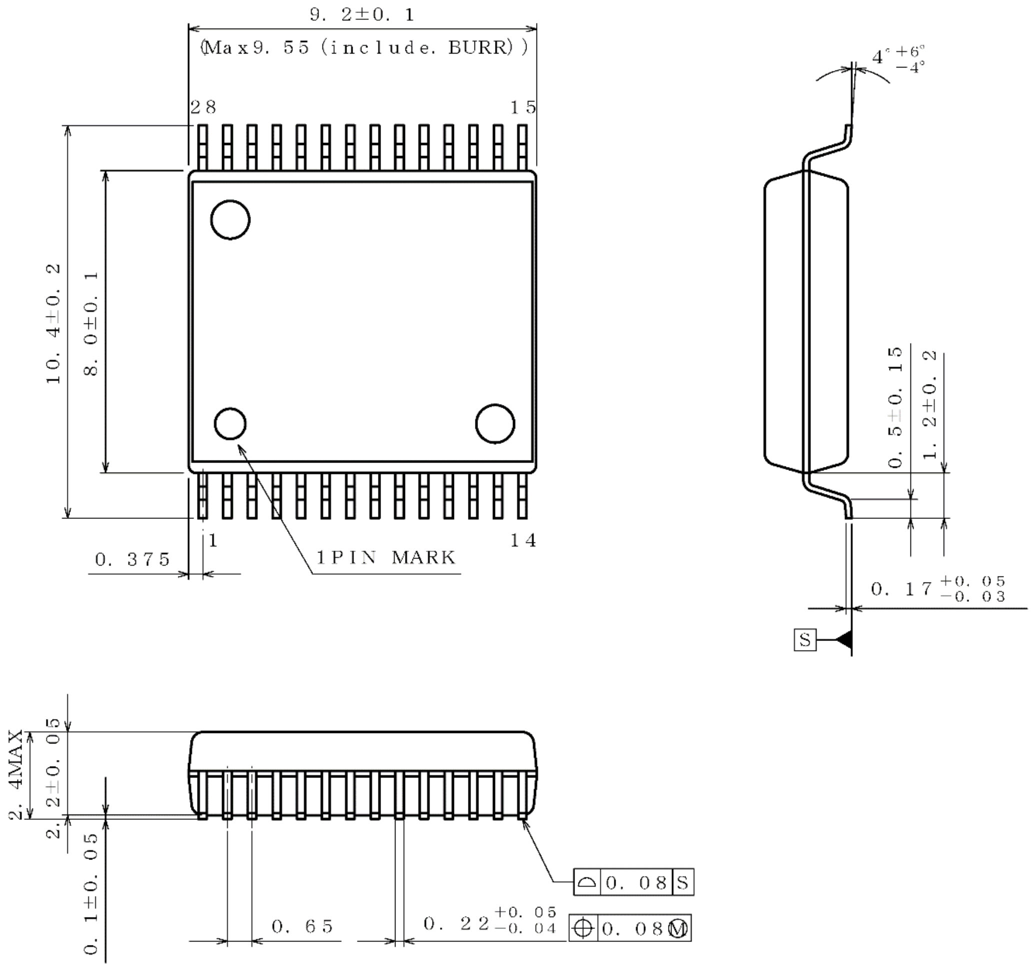
Marking Diagrams

SSOP-B28W (TOP VIEW)



Physical Dimension and Packing Information

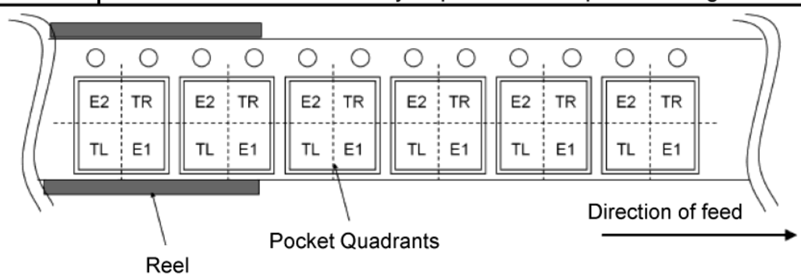
Package Name	SSOP-B28W



(UNIT : mm)
PKG : SSOP−B28W
Drawing No. EX072−5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
13.Mar.2019	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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