Product Change Notification - SYST-13VHLJ680

Date:

15 Nov 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:

Notification subject:

ERRATA - dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Silicon Errata and Document Clarification Document Revision

Notification text:

SYST-13VHLJ680

Microchip has released a new Product Documents for the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Sil Err and DS Cla of devices. If you are using one of these devices please read the document located at dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Sil Err and DS Cla.

Notification Status: Final

Description of Change: Added new data sheet clarification 5 (Pin Diagrams).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 Nov 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Sil Err and DS Cla

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.
If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

DSPIC33FJ32GS406-50I/MR
DSPIC33FJ32GS406-50I/PT
DSPIC33FJ32GS406-E/PT
DSPIC33FJ32GS406-I/MR
DSPIC33FJ32GS406-I/PT
DSPIC33FJ32GS406T-50I/MR
DSPIC33FJ32GS406T-50I/PT
DSPIC33FJ32GS406T-E/PT
DSPIC33FJ32GS406T-I/PT
DSPIC33FJ32GS606-50I/MR
DSPIC33FJ32GS606-50I/PT
DSPIC33FJ32GS606-E/MR
DSPIC33FJ32GS606-E/PT
DSPIC33FJ32GS606-E/PTV02
DSPIC33FJ32GS606-I/MR
DSPIC33FJ32GS606-I/PT
DSPIC33FJ32GS606-I/PTD23
DSPIC33FJ32GS606T-50I/MR
DSPIC33FJ32GS606T-50I/PT
DSPIC33FJ32GS606T-E/PT
DSPIC33FJ32GS606T-E/PTV02
DSPIC33FJ32GS606T-I/PT
DSPIC33FJ32GS606T-I/PTC01
DSPIC33FJ32GS606T-I/PTC04
DSPIC33FJ32GS606T-I/PTD23
DSPIC33FJ32GS608-50I/PT
DSPIC33FJ32GS608-E/PT
DSPIC33FJ32GS608-I/PT
DSPIC33FJ32GS608T-50I/PT
DSPIC33FJ32GS608T-E/PT
DSPIC33FJ32GS608T-I/PT
DSPIC33FJ32GS608T-I/PTC05
DSPIC33FJ32GS610-50I/PF
DSPIC33FJ32GS610-50I/PT
DSPIC33FJ32GS610-E/PF
DSPIC33FJ32GS610-E/PT
DSPIC33FJ32GS610-I/PF
DSPIC33FJ32GS610-I/PT
DSPIC33FJ32GS610T-50I/PF
DSPIC33FJ32GS610T-50I/PT
DSPIC33FJ64GS406-50I/MR
DSPIC33FJ64GS406-50I/PT
DSPIC33FJ64GS406-E/MR
DSPIC33FJ64GS406-E/PT
DSPIC33FJ64GS406-I/MR
DSPIC33FJ64GS406-I/PT

DSPIC33FJ64GS406T-50I/MR
DSPIC33FJ64GS406T-50I/PT
DSPIC33FJ64GS406T-E/PT
DSPIC33FJ64GS406T-I/PT
DSPIC33FJ64GS606-50I/MR
DSPIC33FJ64GS606-50I/PT
DSPIC33FJ64GS606-50I/PTVAO
DSPIC33FJ64GS606-E/MR
DSPIC33FJ64GS606-E/MRVAO
DSPIC33FJ64GS606-E/PT
DSPIC33FJ64GS606-I/MR
DSPIC33FJ64GS606-I/PT
DSPIC33FJ64GS606-I/PTD22
DSPIC33FJ64GS606T-50I/MR
DSPIC33FJ64GS606T-50I/PT
DSPIC33FJ64GS606T-50I/PTC01
DSPIC33FJ64GS606T-50I/PTV01
DSPIC33FJ64GS606T-50I/PTVAO
DSPIC33FJ64GS606T-E/PT
DSPIC33FJ64GS606T-E/PTD22
DSPIC33FJ64GS606T-E/PTV01
DSPIC33FJ64GS606T-E/PTV03
DSPIC33FJ64GS606T-E/PTV04
DSPIC33FJ64GS606T-E/PTV06
DSPIC33FJ64GS606T-I/PT
DSPIC33FJ64GS606T-I/PTD22
DSPIC33FJ64GS608-50I/PT
DSPIC33FJ64GS608-E/PT
DSPIC33FJ64GS608-I/PT
DSPIC33FJ64GS608-I/PTC03
DSPIC33FJ64GS608T-50I/PT
DSPIC33FJ64GS608T-I/PT
DSPIC33FJ64GS608T-I/PTV05
DSPIC33FJ64GS610-50I/PF
DSPIC33FJ64GS610-50I/PT
DSPIC33FJ64GS610-E/PF
DSPIC33FJ64GS610-E/PT
DSPIC33FJ64GS610-I/PF
DSPIC33FJ64GS610-I/PT
DSPIC33FJ64GS610T-50I/PF
DSPIC33FJ64GS610T-50I/PT
DSPIC33FJ64GS610T-E/PF
DSPIC33FJ64GS610T-I/PF

dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 family devices that you have received conform functionally to the current Device Data Sheet (DS70000591**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on Page 15, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and Device ID and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A0	A1	A2
dsPIC33FJ32GS406	0x4000	0x3000	0x3001	0x3002
dsPIC33FJ32GS606	0x4002			
dsPIC33FJ32GS608	0x4004			
dsPIC33FJ32GS610	0x4006			
dsPIC33FJ64GS406	0x4001			
dsPIC33FJ64GS606	0x4003			
dsPIC33FJ64GS608	0x4005			
dsPIC33FJ64GS610	0x4007			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
ECAN	WAKIF bit	1.	The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.	X	X	X
Reserved	—	2.	—	—	—	—
SPI	$\overline{SS1}$ Pin	3.	The $\overline{SS1}$ pin function does not work.	X	X	X
JTAG	Boundary Scan	4.	The boundary scan cells for the RD3 and RD13 pins are swapped.	X	X	X
PWM	Secondary Master Time Base Synchronization	5.	The external time base synchronization output pin, SYNCO2, does not work.	X	X	X
Interrupts	Exit from Doze Mode on Interrupt	6.	An interrupt with a priority level lower than the CPU priority level will trigger the dsPIC® DSC device to exit the Doze mode, but an interrupt request will not be generated.	X	X	X
ADC	Current Consumption in Sleep Mode	7.	If the ADC module is in an enabled state when the device enters Sleep mode, the Power-Down Current (I_{PD}) of the device may exceed the device data sheet specifications.	X	X	X
PWM	External Period Reset Mode (XPRES)	8.	When using the External Period Reset mode, PWM period will get reset immediately if the Reset signal is active at the end of the PWM On time.	X	X	X
PWM	PWM Module Enable	9.	A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module.	X	X	X
ECAN	Error Interrupt Flag	10.	The ERRIF status bit does not get set when a CAN error condition occurs.	X	X	X
SPI	Framed Master Mode	11.	When the SPI module is configured in Framed Master mode and the Frame Sync Pulse Edge Select bit (FRMDLY) is set to '1', transmitting a word and then buffering another word in the SPIxBUF register before the transmission has completed, results in an incomplete transmission of the first data word.	X	X	X
I^2C	Slave Mode	12.	When operating the I^2C module in Slave mode, intermittent address and data receive errors may be detected.	X		
PWM	SWAP	13.	When the PWM SWAP feature is enabled, the user-defined dead time is ignored during the Fault or current-limit condition.	X	X	X
PWM	External Period Reset Mode (XPRES)	14.	When using the External Period Reset in True Independent Output mode, the external Reset signal only resets the PWMxH signal.	X	X	X
CPU	`div.sd` Instruction	15.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X	X	X
CPU	Interrupt Disable	16.	When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
UART	TX Interrupt	17.	A transmit (TX) Interrupt may occur before the data transmission is complete.	X	X	X
Reserved	—	18.	—	—		
PWM	—	19.	In Master time base mode, writing to the period register and any other timing parameter of the PWM module will cause the update of the other timing parameter to take effect one PWM cycle after the period update is effective.	X	X	X
PWM	PWM Module Enable	20.	If the PWM Clock Divider Select Register, PTCON2, is not equal to zero, the PWM module may or may not initialize from an override state.	X	X	X
JTAG	Flash Programming	21.	JTAG Flash programming is not supported.	X	X	X
ECAN	DMA	22.	Write collisions on DMA-enabled ECAN™ peripheral do not generate DMAC error traps.	X	X	X
PWM	Current-Limit Mode	23.	A <8 ns glitch may be observed on the PWM pins when the PWM is interrupted by a Current-Limit/ Fault event.	X	X	X
Core	ICD and Device Programming	24.	Device debugging is not functional when using the PGEC3/PGED3 clock/data pins.	X	X	X
PWM	Dead-Time Compensation	25.	If the ALTDTR register value is greater than 512 counts, the actual dead-time compensation could be limited to 512 counts during a Current-Limit/Fault operation.	X	X	X
PWM	External Period Reset	26.	Feature not functional when PWM outputs are swapped.	X	X	X
PWM	Immediate Update	27.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X	X
I/O	Open-Drain	28.	Configuring RG3 for open-drain output also configures RD3.	X	X	X
PWM	Redundant/ Push-Pull Output Mode	29.	Changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to one PWM clock.	X	X	X
PWM	Master Time Base Mode	30.	Changes to the PHASEx register may result in missing dead time.	X	X	X
PWM	Trigger Compare Match	31.	First PWM/ADC trigger event on TRIGx/STRIGx match may not occur under certain conditions.	X	X	X
PWM	Push-Pull Mode	32.	Period register writes may produce back-to-back pulses under certain conditions.	X	X	X
QEI	Index Pulse Reset	33.	POSxCNT may not rollover/underflow correctly due to index match handling in specific applications.	X	X	X
I^2C	Slave Mode	34.	Clock stretching may not occur when enabled.	X	X	X
UART	Transmit Mode	35.	TRMT bit is set before the Shift register is empty.	X	X	X
PWM	Clock	36.	PWM output will exhibit jitter with some PWM clock divider settings.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The shaded column in the "Affected Silicon Revisions" table included in each issue indicates that the issue applies to the most current revision of silicon (**A2**).

1. Module: ECAN

The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.

When the device wakes up from Sleep due to CAN bus activity, the ECAN module is placed in operational mode. The ECAN event interrupt occurs due to the WAKIF flag. Trying to clear the flag in the Interrupt Service Routine (ISR) may not be sufficient. The WAKIF bit being set will not cause repetitive Interrupt Service Routine execution.

Work around

Although the WAKIF bit does not clear, the device Sleep and ECAN Wake function continue to work as expected. If the ECAN event is enabled, the CPU will enter the Interrupt Service Routine due to the WAKIF flag getting set. The application can maintain a secondary flag, which tracks the device Sleep and wake events.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

2. Module: Reserved

The issue in the previous version of the document has been removed.

3. Module: SPI

The $\overline{ASS1}$ pin is provided as an alternative pin for the slave select function of the SPI1 module. However, the alternate slave select function ($\overline{ASS1}$) on this pin does not work. All other functions multiplexed on the same pin work as expected.

Work around

Use the $\overline{SS1}$ pin for the slave select function.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

4. Module: JTAG

The boundary scan cells for the RD3 and RD13 pins are swapped. When running the boundary scan test, an input to the RD3 pin excites the RD13 pin, and vice versa.

This erratum does not affect any other functionality on the RD3 and RD13 pins.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

5. Module: PWM

The SYNCO2 pin can be used to transmit synchronization pulses to generate an identical PWM time base on another device. However, the SYNCO2 function does not work as expected. As a result of this erratum, the secondary master time base cannot be used for synchronizing a slave device.

All other functions multiplexed on the same pin work as expected.

Work around

A spare PWMxL/PWMxH pin can be used as the synchronization source output instead of the SYNCO2 pin using the following procedure:

1. Configure the spare PWMxL/PWMxH pin to operate on the same time base, period and phase as the synchronizing (or reference) PWM channel.
2. Set up the duty cycle for the spare PWMxL/PWMxH pin to the desired pulse width for the synchronization signal (typically 100 ns at the highest PWM resolution).
3. Connect the spare PWMxL/PWMxH pin to the synchronization input of the slave PWM generator.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

6. Module: Interrupts

When the dsPIC® DSC device is operating in Doze mode, any interrupt should trigger the device to exit Doze mode and generate an Interrupt Request (IRQ) regardless of the Interrupt Priority Level (IPL). However, if the Interrupt Priority Level is lower than the CPU priority level, the interrupt request will not be generated. As a result, the CPU will not detect that it has exited Doze mode.

Work around

Any interrupt that is expected to wake the CPU from Doze mode must be configured for an Interrupt Priority Level higher than the CPU priority level. This work around can be implemented in software right before the device enters Doze mode and reverted to the desired priority level after it wakes up from Doze mode.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

7. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a `PWRSAV #0` instruction, the device Power-Down Current (I_{PD}) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work around

In order to remain within the I_{PD} specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a `PWRSAV #0` instruction.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

8. Module: PWM

The External Period Reset mode is used to reset the PWM period when the selected Reset signal is asserted during the Off time of the PWM. If the Reset signal remains active during and after the PWM On time, the Reset signal must be ignored.

However, the Reset signal is not ignored at the end of the PWM On time. Therefore, the PWM period will be reset immediately after the end of the PWM On time.

Work around

Ensure that the External Period Reset signal is asserted during the PWM Off time and deasserted before the end of the PWM On time.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

9. Module: PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to assign pin ownership to the PWM module and then enabling it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before actual switching of the PWM outputs begins. This glitch may cause momentary turn ON of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

Work around

Follow the given sequence to avoid any glitches from appearing on the PWM outputs at the time of enabling.

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.
2. Assign pin ownership to the GPIO module by configuring the PENH bit (IOCONx[15]) = 0 and the PENL bit (IOCONx[14]) = 0.
3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT[1:0] bit field in the IOCONx register.
4. Override the PWM outputs by setting the OVRENH bit (IOCONx[9]) = 1 and the OVRENL bit (IOCONx[8]) = 1.
5. Enable the PWM module by setting the PTEN bit (PTCON[15]) = 1.
6. Remove the PWM overrides by making the OVRENH bit (IOCONx[9] = 0 and the OVRENL bit (IOCONx[8]) = 0.
7. Ensure a delay of at least one full PWM cycle.
8. Assign pin ownership to the PWM module by setting the PENH bit (IOCONx[15]) = 1 and the PENL bit (IOCONx[14]) = 1.

The code in Example 1 illustrates the use of this work around.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

EXAMPLE 1: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING

```
TRISAbits.TRISA4 = 1;      // Configure PWM1H/RA4 as digital input
                           // Ensure output is in safe state using pull-up or
                           // pull-down resistors
TRISAbits.TRISA3 = 1;      // Configure PWM1L/RA3 as digital input
                           // Ensure output is in safe state using pull-up or
                           // pull-down resistors

IOCON1bits.PENH = 0;       // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;       // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;     // Configure override state of the PWM outputs to
                           // desired safe state.

IOCON1bits.OVRENH = 1;     // Override PWM1H output
IOCON1bits.OVRENL = 1;     // Override PWM1L output

PTCONbits.PTEN = 1;        // Enable PWM module

IOCON1bits.OVRENH = 0;     // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;     // Remove override for PWM1L output

Delay(x);                  // Introduce a delay greater than one full PWM cycle

IOCON1bits.PENH = 1;       // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;       // Assign pin ownership of PWM1L/RA3 to PWM module
```

10. Module: ECAN

The ERRIF status flag (CxINTF[5]) does not get set when a CAN error condition occurs. However, the corresponding CxIF interrupt flag will get set on a CAN error condition, and an interrupt will be correctly generated if enabled.

Work around

Do not inspect the state of the ERRIF bit to determine if a CAN error interrupt has occurred. Instead, inspect the individual error condition status flags: TXBO, TXBP, RXBP, TXWAR, RXWAR and EWARN (CxINTF[13:8]).

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

11. Module: SPI

When the SPI module is configured in Framed Master mode and the Frame Sync Pulse Edge Select bit (FRMDLY) is set to '1', transmitting a word and then buffering another word in the SPIxBUF register, before the transmission has completed, results in an incomplete transmission of the first data word. Only the first 15 bits from the first data word are transmitted, followed by the Sync Pulse and the complete second word.

Work around

Between the two back-to-back SPI operations, add a delay to ensure that the first word is fully transmitted before the second word is written to the SPIxBUF register, as shown in Example 2.

EXAMPLE 2:

```
SPI1BUF = 0x0001;

while (SPI1STATbits.SPITBF);

    asm ("REPEAT #50");.
    asm ("NOP");

// The number of NOPs depends on the SPI
// clock prescalers

SPI1BUF = 0x0002;
```

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

12. Module: I²C

When operating the I²C module in Slave mode, intermittent address and data receive errors may be detected.

For example, any one of the eight bits received in the transaction may be received incorrectly. As a result of this erroneous reception, the slave device may send an incorrect Acknowledge/Not Acknowledge, or the data may be received incorrectly.

On devices that exhibit this issue, the rate of erroneous receptions may be up to 0.05% of all address and data transactions.

Work around

1. Implement Bit-Banged I²C

   Software controlled (bit-banged) I²C slave communication can be implemented. This work around ensures that all receive errors will be eliminated from the I²C communication.

2. Implement Redundant Transmissions

   The I²C master device can be programmed to transmit the same address/data packet multiple times. After receiving all redundant transmissions, the slave can compare the data received, and detect and correct receive errors by performing a majority detect on all bits of the transmission.

3. Master Address Resend for Address Errors and Checksums or Parity Bits for Data Errors

   Configure the I²C master device to resend address bytes upon reception of an invalid NACK. With this work around, the I²C slave device that incorrectly sent a NACK will be provided additional opportunities to receive the correct address. Using multiple resends can reduce the occurrence of incorrect address receptions by the slave.

   Checksums and parity bits can be used for detecting and/or correcting data receive errors on the I²C slave device.

Affected Silicon Revisions

A0	A1	A2					
X							

13. Module: PWM

The PWM SWAP bit allows the user-assigned application to connect the PWMxH signal to the PWMxL pin, and the PWMxL signal to the PWMxH pin. When the SWAP bit is set and Current-Limit mode or Fault mode is enabled, the user-defined dead time is ignored during the Fault condition and the PWM pins default to their defined state, as specified by the FLTDATx and CLDATx bits in the IOCONx register.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

14. Module: PWM

When using the External Period Reset in True Independent Output mode, the external Reset signal should reset the time bases of the PWMxH and PWMxL signals. However, the External Period Reset signal does not affect the PWMxL signal.

This issue is not exhibited in Complementary, Redundant or Push-Pull PWM modes.

Work around

The PWMxH channel of a spare PWM generator can be configured identically to that of the PWMxL channel mentioned above. The same current-limit signal should be selected for this spare PWM generator.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

15. Module: CPU

When using the Signed 32-By-16-Bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

16. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for '`n`'.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

17. Module: UART

When using UTXISEL[1:0] = `01` (interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete, hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

18. Module: Reserved

The issue in a previous version of the document was removed.

19. Module: PWM

The high-speed PWM module can operate with variable period, duty cycle, dead-time and phase values. The master period and other timing parameters can be updated in the same PWM cycle. With immediate updates disabled, the new values should take effect at the start of the next PWM cycle.

As a result of this erratum, the updated master period takes effect on the next PWM cycle, while the update of the additional timing parameter is delayed by one PWM cycle. The parameters affected by this erratum are as follows:

Master Period Registers: Update effective on the next PWM cycle:

1. PTPER: if MTBS (PWMCONx[3]) = 0
2. STPER: if MTBS = 1

Additional PWM Timing Parameters: Update effective one PWM cycle after master period update:

1. Duty cycle: PDCx, SDCx and MDC registers
2. Phase: PHASEx or SPHASEx registers
3. Dead-time: DTRx and ALTDTRx registers and dead-time compensation signals
4. Clearing of Current-Limit and Fault conditions, and application of External Period Reset signal

Work around

If the application requires the master period and other parameters to be updated at the same time, enable both immediate updates:

- EIPU (PTCON[10]) = 1 to enable immediate period updates
- IUE (PWMCONx[0]) = 1 to enable immediate updates of additional parameters listed above

Enabling immediate updates will allow updates to the master period and the other parameter to take effect immediately after writing to the respective registers.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

20. Module: PWM

If the PWM Clock Divider Select register, PTCON2, is not equal to zero, the PWM module may or may not initialize from an override state (OVRENH (IOCONx[9]) = 1 or OVRENL (IOCONx[8]) = 1).

Work around

When configuring the Override Enable bits (OVRENL/OVRENH) in the PWMx I/O Control register, IOCONx, set these bits implicitly via word format and not explicitly via bit format.

For example:

```
IOCONx = IOCONx & 0xFCFF;
```

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

21. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

22. Module: ECAN

When DMA is used with the ECAN peripheral, and the CPU and DMA write to a CAN Special Function Register (SFR) at the same time, the DMAC error trap is not occurring, nor is the PWCOLx bits of the DMAPWC SFR or the DMACERR bit of the INTCON1 SFR being set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

Work around

None. However, under normal circumstances, this situation should never arise. When DMA is used with the ECAN peripheral, the application should not be writing to the ECAN SFRs.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

23. Module: PWM

The PWM current-limit operation allows the PWM module to set/reset the output signals when a specific current-limit is detected with the minimum latency delay. When operating the PWM module in Complementary mode (PMOD[1:0] = 00), positive dead-time and with Current-Limit/Fault enabled, it is possible to observe a <8 ns pulse glitch on the complementary output after the current limit or Fault is detected. This glitch will be present prior to the implementation of the dead time.

Work around

In order to avoid the <8 ns glitch to be propagated into the MOSFET gate driver, a low-pass filter (e.g., resistor-capacitor network) should be implemented between the dsPIC DSC PWM output pin and the gate driver input pin.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

24. Module: Core

Device debugging is not functional when using the PGEC3/PGED3 clock/data pins.

Work around

Use PGEC1/PGED1 or PGEC2/PGED2 clock/data pins for debugging functionality.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

25. Module: PWM

If the ALTDTRx register value is greater than 512 counts, the actual dead-time compensation between PWMxH and PWMxL could be truncated to the equivalent of ALTDTRx = 512 counts during a Current-Limit/Fault operation. The dead time works as expected, even with ALTDTRx register values greater than 512 counts during normal operation (not in Current-Limit or Fault).

Work around

Change the value of the PWM input clock prescaler, PCLKDIV[2:0] (PTCON2[2:0]), that allows the use of an ALTDTRx value lower than 512 counts.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

26. Module: PWM

External Period Reset (enabled by XPRES (PWMCONx[1])) is not functional when the PWM outputs are swapped using the SWAP bit (IOCONx[1]).

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

27. Module: PWM

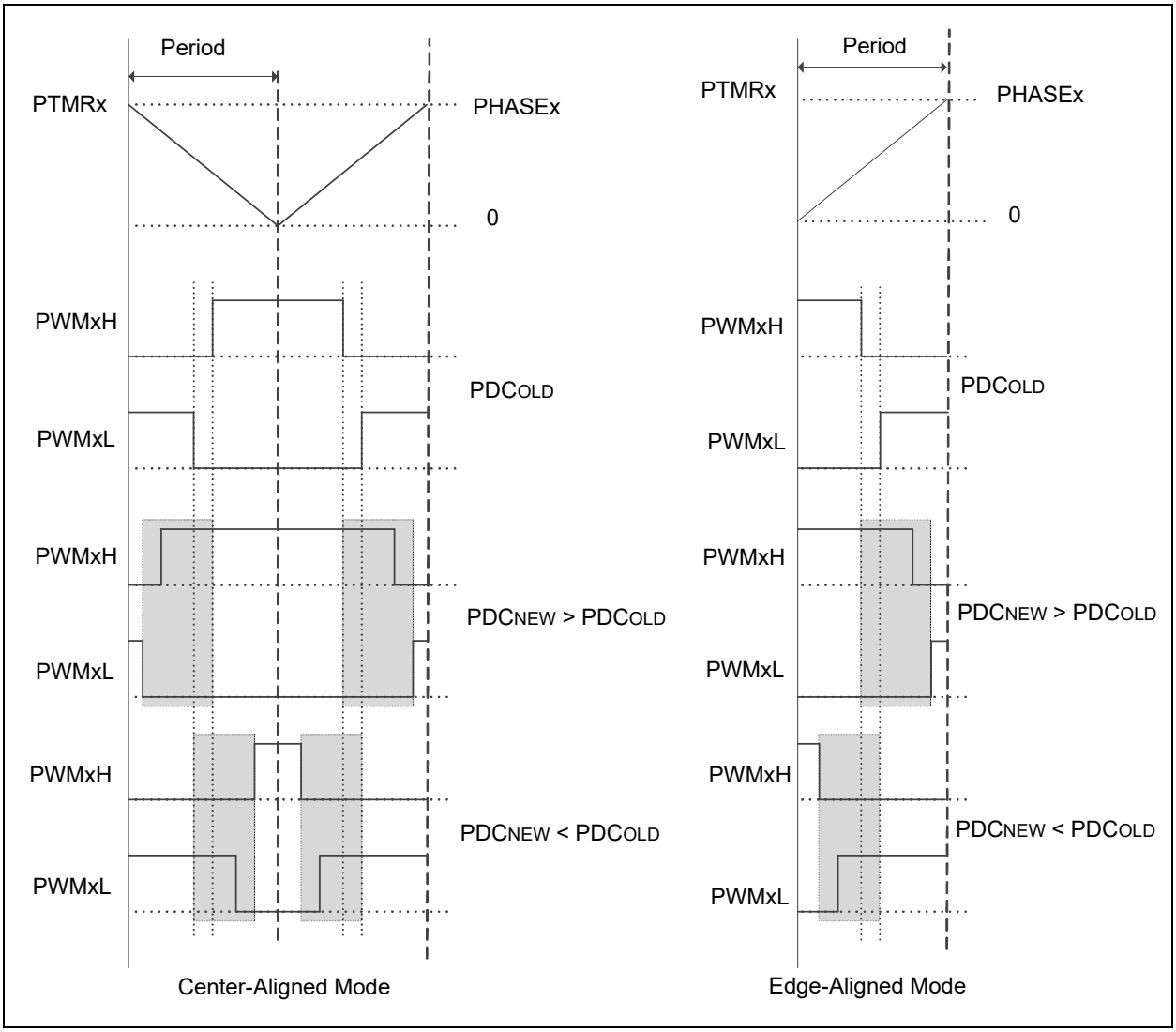
The PWMx generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWMx generator is configured to operate in Complementary mode with the independent time base or master time base;
- Immediate update is enabled; and
- The value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDCOLD, newly calculated duty cycle, PDCNEW, and the point at which the write to the Duty Cycle register occurs within the PWMx time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDCNEW, at a point of time when the PWMx time base is counting a value that is in between PDCNEW and PDCOLD. Additionally, writing to the Duty Cycle register close to the instant of time where dead time is being applied may result in reduced dead time, effective on the PWMxH and PWMxL transition edges.

In Figure 1 (following page), if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

FIGURE 1: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES



Work around

None. However, in most applications the duty cycle update timing can be controlled using the TRIGx trigger or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

28. Module: I/O

Configuring RG3 as an open-drain output (ODCG[3] = 1) will also place RD3 in open-drain configuration. The Open-Drain Control bit for RD3 (OCDC[3]) has no effect on the configuration of RD3 under these circumstances.

Work around

None.

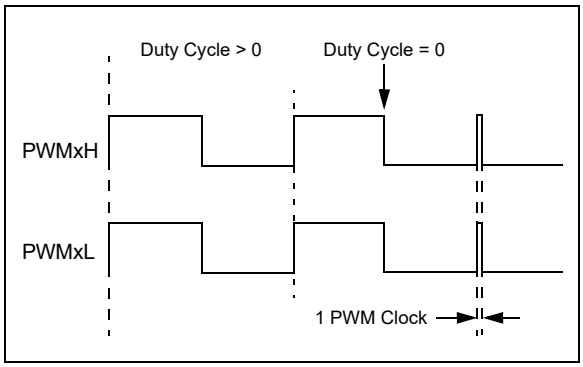
Affected Silicon Revisions

A0	A1	A2					
X	X	X					

29. Module: PWM

In Redundant Output mode (IOCONx[11:10] = 01) and Push-Pull Output mode (IOCONx[11:10] = 10), with the Immediate Update Enable bit disabled (PWMCONx[0] = 0), when the Duty Cycle register is updated from a non-zero value to zero, a glitch pulse of a width equal to one PWM clock will appear at the next PWM period boundary, as shown in Figure 2 (for the Redundant Output mode). The Duty Cycle register refers to the PDCx register if PWMCONx[8] = 0 or the MDC register if PWMCONx[8] = 1.

FIGURE 2: ISSUE EXAMPLE FOR REDUNDANT OUTPUT MODE



Work around

If the application requires a zero duty cycle output, there are two possible work around methods:

1. Use the PWM override feature to override the PWM output to a low state instead of writing to the Duty Cycle register. In order to switch back to a non-zero duty cycle output, turn off the PWM override. The override-on and override-off events must be timed close to the PWM period boundary if the IOCONx register has been configured with IOCONx[0] = 0 (i.e., output overrides through the OVDDAT[1:0] bits occur on the next CPU clock boundary).
2. Enable the Immediate Update Enable bit (PWMCONx[0] = 1) while configuring the PWMx module (i.e., before enabling the PWMx module, PTCON[15] = 1). With the Immediate Update enabled, writes to the Duty Cycle register can have an immediate effect on the PWM output. Therefore, the duty cycle write operations must be timed close to the PWM period boundary in order to avoid distortions in the PWM output.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

30. Module: PWM

In Edge-Aligned PWM mode with Master Time Base (PWMCONx[9] = 0) and the Immediate Update Enable bit disabled (PWMCONx[0] = 0), after enabling the PWMx module (PTCON[15] = 1), changes to the PHASEx register, such that PHASEx < DTRx or PHASEx > PDCx, will result in missing dead time at the PWMxH-PWMxL transition that will occur at the next master period boundary.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

31. Module: PWM

The triggers generated by the PWMx Primary Trigger Compare Value register (TRIGx) and the PWMx Secondary Trigger Compare Value register (STRIGx) will not trigger at the point defined by the TRIGx/STRIGx register values on the first instance for the configurations listed below. Subsequent trigger instances are not affected.

- Trigger compare values for TRIGx, STRIGx are less than eight counts,
- Trigger Output Divider bits, TRGDIV[3:0] (TRGCONx[15:12]), are greater than '0',
- Trigger Postscaler Start Enable Select bits, TRGSTRT[5:0] (TRGCONx[5:0]), are equal to '0'.

Work around

Configure the PWMx Primary Trigger Compare Value Register (TRIGx) and PWMx Secondary Trigger Compare Value Register (STRIGx) values to be equal to or greater than eight.

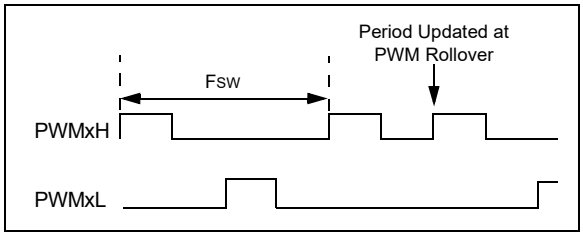
Affected Silicon Revisions

A0	A1	A2					
X	X	X					

32. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx[11:10] = 10) with the Enable Immediate Period Update bit enabled (PTCON [10] = 1), a write to the Period register that coincides with the period rollover event may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins (Figure 3).

FIGURE 3:



Work around

Ensure that the update to the PWM Period register occurs away from the PWM rollover event by setting the EIPU bit (PTCON[10] = 1). Use either the PWM Special Event Trigger (SEVTCMP) or the PWM Primary Trigger (TRIGx) to generate a PWM Interrupt Service Routine (ISR) near the start of the PWM cycle. This ISR will ensure that period writes do not occur near the PWM period rollover event.

For additional information, please refer to silicon issue 19 (PWM).

Affected Silicon Revisions

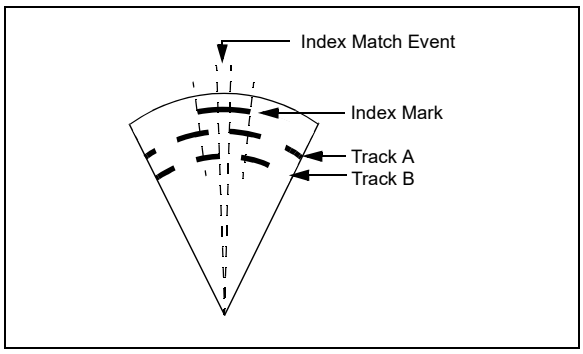
A0	A1	A2					
X	X	X					

33. Module: QEI

When the QEI module is used in 4x mode with Index Pulse Reset (QEIM[2:0] = 110), the value of the POSxCNT register may not transition (rollover or underflow) from zero to the maximum count value as expected.

This issue is most likely to be seen in specific motor applications using a rotation encoder with an ungated index pulse, operating at near zero speed and/or in the presence of mechanical vibration. In these applications, the encoder may change direction and incrementally rock back and forth. If this happens with the encoder positioned in the vicinity of its index mark, the module will detect the first index match event as the encoder rotates into the index match event area, but not subsequent events if it drifts into and out of that position but stays within the index mark area (Figure 4). If the encoder count increments or decrements in only one direction, the index match will only occur once.

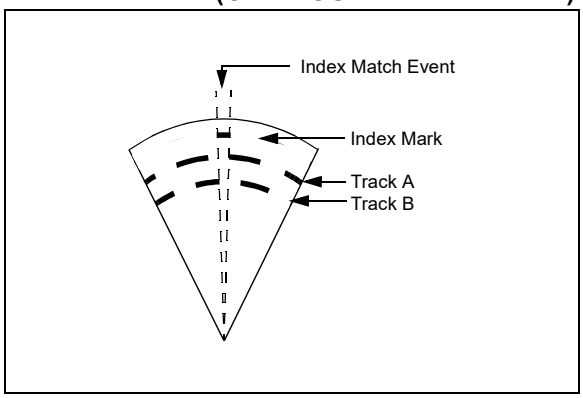
FIGURE 4: ENCODER IN THE SECTOR AROUND THE INDEX MARK



As a result of this, the value of POSxCNT may leave its expected range of 0 to maximum count (defined as the number of encoder pulses per revolution, minus 1), resulting in erroneous reporting of the rotor's position.

This issue is not seen when the encoder uses an index mark that is one encoder count in width (Figure 5).

FIGURE 5: ENCODER IN THE SECTOR AROUND THE INDEX MARK (ONE COUNT WIDTH INDEX)



Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

34. Module: I²C

In Slave mode, clock stretching may not occur during address detect, even when it has been enabled (STREN = 1). As a result, the SCLREL bit may not be cleared upon address reception when the R/$\overline{W}$ bit is '0'. This is seen in both 7-Bit and 10-Bit Addressing modes.

Work around

User software should read the Acknowledged address from the receive buffer before the data byte is received. User software also needs to configure the slave interrupt priority, such that, the interrupt latency time should be less (before the reception of the data byte).

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

35. Module: UART

In Transmit mode, the TRMT bit may be set before the Shift register is empty. In back-to-back transmission, if the data are loaded into the UxTXREG register when the TRMT bit is set, the new byte transmission starts immediately and the Stop bit may be abbreviated, as shown in the condition below:

- When BRGH (UxMODE[3]) = 1, the Stop bit may be shortened by 1/4 of a bit clock
- When BRGH (UxMODE[3]) = 0, the Stop bit may be shortened by 1/16th of a bit clock

Work around

- Use the UTXBF flag instead of the TRMT bit when loading new data into the UxTXREG

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

36. Module: PWM

The PWM output will exhibit jitter under the following conditions:

When the PWM clock divider has the value of 1, 5 or 6 (PCLKDIV[2:0] (PTCON2[2:0]) = 0b001, 0b101 or 0b110), and the three Least Significant bits of the PWM Period register (PTPER or PHASEx), the Duty Cycle register (MDC or PDCx) or Phase-Shift register (PHASEx) are non-zero.

Work around

Use PWM clock dividers other than 1, 5 or 6.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000591**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: 50 MIPS Power-Down Current (I_{PD})

In **Section 28.0 "50 MIPS Electrical Characteristics"**, a new table has been added, Table 28-4, showing the Power-Down Current for the DC Characteristics. Subsequent tables have been renumbered accordingly.

TABLE 28-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Power-Down Current (I_{PD})						
MDC60d	320	850	µA	-40°C	3.3V	50 MIPS
MDC60a	320	850	µA	+25°C		
MDC60b	320	850	µA	+85°C		

2. Module: Table 1: dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Controller Families

In Table 1, the I/O pin count for the dsPIC33FJXXGSXX6 devices (64-pin) should be 53 instead of 58, as shown in the table.

The I/O pin count for the dsPIC33FJXXGSXX8 devices (80-pin) should be 69 instead of 74, as shown in the table.

3. Module: Table 24-2: dsPIC33F Configuration Bits Description

In Table 24-2, the end addresses for the BSS[2:0] bits selection should be read as follows:

When BSS[2:0] = x10, the boot program Flash segment ends at 0x0007FE.

When BSS[2:0] = x01, the boot program Flash segment ends at 0x001FFE.

When BSS[2:0] = x00, the boot program Flash segment ends at 0x003FFE.

4. Module: Special Features

In Table 24-1, the FWDT (bit 5) is changed from Unimplemented to Reserved for development tools and must be programmed as '1'. Bit 6 and bit 7 of the FCMP register are added with Note 3. The changes are shown below in **bold**.

TABLE 24-1: DEVICE CONFIGURATION REGISTER MAP

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	—	—	—	—	BSS[2:0]			BWRP
0xF80002	RESERVED	—	—	—	—	—	—	—	—
0xF80004	FGS	—	—	—	—	—	GSS[1:0]		GWRP
0xF80006	FOSCSEL	IESO	—	—	—		FNOSC[2:0]		
0xF80008	FOSC	FCKSM[1:0]		—	—	—	OSCIOFNC	POSCMD[1:0]	
0xF8000A	FWDT	FWDTEN	WINDIS	**Reserved(1)**	WDTPRE	WDTPOST[3:0]			
0xF8000C	FPOR	—	ALTQIO	ALTSS1	—	—	FPWRT[2:0]		
0xF8000E	FICD	Reserved(1)	Reserved(1)	JTAGEN	—	—	—	ICS[1:0]	
0xF80010	FCMP	**—(3)**	**—(3)**	CMPPOL1(2)	HYST1[1:0](2)		CMPPOL0(2)	HYST0[1:0](2)	

Legend: — = unimplemented bit, read as '0'.

Note 1: These bits are reserved for use by development tools and must be programmed as '1'.

2: These bits are reserved on dsPIC33FJXXXGS406 devices and always read as '1'.

3: — = unimplemented bit, read as '1'.

5. Module: Pin Diagrams

All pin diagrams with AN9/DACOUT/RB9 have the following note added to the pin.

Note: At device power-up (POR), a pulse with an amplitude around 2V and a duration greater than 20 ms may be observed on this device pin, independent of pull-down resistors. It is recommended to not use this pin as an output driver unless the circuit being driven can endure this active duration.

APPENDIX A: REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document; issued for revision A0. Includes silicon issues 1 (ECAN), 2 (SPI), 3 (SPI) 4 (JTAG), 5 (PWM) and 6 (Interrupts).

Rev B Document (6/2010)

Removed silicon issue 2 (SPI) and marked its location as reserved.

Updated the work around in silicon issue 5 (PWM).

Added silicon issues 7 (ADC), 8 (PWM) and 9 (PWM) and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

Rev C Document (11/2010)

Updated the Device IDs in Table 1 for the following devices:

- dsPIC33FJ32GS606
- dsPIC33FJ32GS608
- dsPIC33FJ32GS610
- dsPIC33FJ64GS406
- dsPIC33FJ64GS606
- dsPIC33FJ64GS608

Added silicon issue 10 (ECAN).

Rev D Document (3/2011)

Added silicon issue 11 (SPI).

Rev E Document (4/2011)

Added silicon issue 12 (I^2C).

Rev F Document (6/2011)

Updated current silicon revision to A1 throughout the document.

Updated silicon issue 8 (PWM).

Removed the words High-Speed from the title of issue 9 (PWM).

Added silicon issues 13 and 14 (PWM), and silicon issue 15 (CPU).

Rev G Document (11/2011)

Added silicon issues 16 (CPU), 17 (UART), 18 (PWM) and 19 (PWM).

Rev H Document (5/2012)

Removed data sheet clarification 1.

Updated silicon issue 9 (PWM).

Added silicon issues 20 (PWM), 21 (JTAG) and 22 (ECAN).

Rev J Document (2/2013)

Modified the PWM Clock Divider Select register name from PTCON to PTCON2. Added silicon issues 23 (PWM), 24 (Core) and 25 (PWM). Added data sheet clarification 1 (Electrical Characteristics).

Rev K Document (9/2013)

Removed existing silicon issue 18 (PWM) and marked its location as reserved.

Added new silicon issues 26-27 (PWM) and 28 (I/O).

Corrected “PTCON” to “PTCON2” in silicon issue 20 (PWM).

Corrected the module for issue 24 from “PGEC3/PGED3” to “Core”, to conform with standard nomenclature practice (the issue itself is unchanged).

Other minor typographic corrections.

Rev L Document (9/2014)

Updated document to include silicon revision A2. Adds all existing silicon issues to revision A2, with the exception of issue 12 (I^2C).

Added new silicon issues 29 through 32 (PWM) and 33 (QEI) for all silicon revisions.

Removed data sheet clarification 1 as this was fixed in the latest data sheet.

Rev M Document (1/2015)

Added new silicon issue 34 (I^2C).

Rev N Document (11/2015)

Updated silicon issue 34 (I^2C) updated.

Rev P Document (2/2016)

Added new silicon issue 35 (UART).

Added new data sheet clarifications 1 (50 MIPS Power-Down Current (IPD)), 2 (Table 1: dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 Controller Families) and 3 (Table 24-2: dsPIC33F Configuration Bits Description).

Rev Q Document (9/2019)

Added new silicon issue 36 (PWM).

Added new data sheet clarification 4 (Special Features).

Rev R Document (11/2019)

Added new data sheet clarification 5 (Pin Diagrams).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-5224-5268-3

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820