Click here for production status of specific part numbers.

MAX40027

Dual 280ps High-Speed Comparator, Ultra-Low Dispersion with LVDS Outputs

General Description

The MAX40027 is a single-supply, dual high-speed comparator with a typical propagation delay of 280ps. The overdrive dispersion is extremely low (25ps, typ.), making these comparators ideal for time-of-flight, distance-measurement applications.

The input common mode range of 1.5V to V_{DD} + 0.1V is compatible with the output swings of several widely used high-speed trans-impedance amplifiers, such as the MAX40658, MAX40660, and MAX40661.

The output stage is LVDS (Low-Voltage Differential Signaling), which helps to minimize power dissipation and interfaces directly with many FPGAs and CPUs. Complementary outputs help in suppression of common-mode noise on each output line.

The MAX40027 is offered in a tiny, space-saving, 3mm x 2mm, 12-pin TDFN package with side-wettable flanks, and meets AEC-Q100 automotive qualification requirements. The MAX40027 operates over the -40°C to +125°C temperature range and runs from a 2.7V to 3.6V supply voltage.

Applications

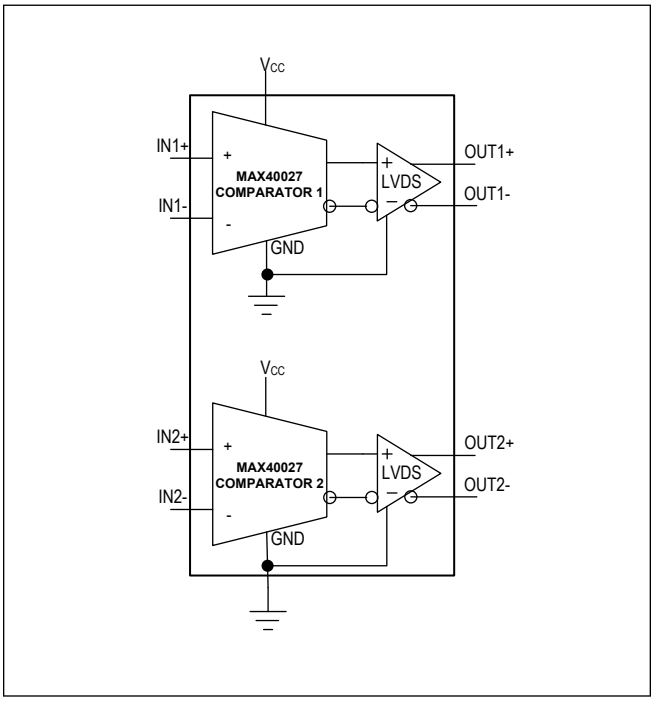
- Automotive ADAS
- Distance Sensing in LiDAR, RADAR, and SONAR
- Time-of-Flight Sensors
- High-Speed Differential Line Receivers
- High-Speed Triggering in Oscilloscopes
- Communications
- Oscillators
- Threshold Detectors
- High-Speed Level-Shifting
- Test and Measurement

Benefits and Features

- Fast Propagation Delay: 280ps, Typ
- Low Overdrive Dispersion: 25ps (V_{OD} = 10mV to 1V)
- Supply Voltage 2.7V to 3.6V
- 45.9mW at 2.7V Supply (Each Comparator)
- Power-Efficient LVDS Outputs
- -40°C to +125°C Temperature Range
- Automotive AEC-Q100 Qualified
- Small, 3mm x 2mm TDFN Package with Side-Wettable Flanks

Ordering Information appears at end of data sheet.

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +3.6V
IN1+, IN1-, IN2+, IN2- to GND ..... -0.3V to V_{CC} + 0.3V
OUT1+, OUT1-, OUT2+, OUT2- to GND..... -0.3V to V_{CC} + 0.3V
OUT1+ to OUT1-, or OUT2+ to OUT2- ..... -0.5V to +0.5V
Current Into Any Pin (Continuous) 10mA
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 15.94mW/°C above +70°C.) 1274.90mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN

Package Code	TD1232MY+1
Outline Number	21-100369
Land Pattern Number	90-100136
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	62.75°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.27°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = 3.3V, V_{CM} = 2.5V, R_{LOAD} = 100Ω, connected from OUTx+ to OUTx-, T_A = -40ºC to +125ºC)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 2)	V_{CC}	Guaranteed by PSRR specification	2.7		3.6	V
Supply Current (Per Comparator)	I_{CC}			17	23	mA
Power-Up Time	t_{ON}	Measured using supply current >75% of final value		20		µs
Power Supply Rejection Ratio (Note 2)	PSRR	2.7V ≤ V_{CC} ≤ 3.6V	50	80		dB
Input Common Mode Range (Note 2)	V_{CM}	Guaranteed by CMRR specification	1.5		V_{CC} + 0.1	V
Input Offset Voltage (Note 2)	V_{OS}	Over the input common mode range		0.5	5	mV
Common Mode Rejection Ratio (Note 2)	CMRR	Over the input common mode range	52	80		dB
Input Hysteresis (Note 2)	V_{HYS}			1.5		mV

Electrical Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 2.5V, R_{LOAD} = 100Ω, connected from OUTx+ to OUTx-, T_A = -40ºC to +125ºC)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Current	I_B	Over the input common mode range. Inputs shorted together.			1.3	10	µA
Input Offset Current	I_{OS}	V_{INx+} = V_{INx-}			0.1	4	µA
Input Capacitance	C_{IN}	Either input, over entire Input common mode range			2		pF
Output Differential Voltage	$V_{OUTDIFF}$	$\lvert V_{OUTx+} - V_{OUTx-} \rvert$		247	350	454	mV
Output Differential Voltage Match		$\lvert V_{OUTx+} - V_{OUTx-} \rvert$		-50		+50	mV
Output Common-Mode Voltage	V_{CMOUT}	Either output polarity		1.125	1.23	1.375	V
Output Common-Mode Voltage Match		Either output polarity		-50		+50	mV
Output Common-Mode Transient		Either output transition polarity			18		mVp-p
Output Short-Circuit Current	I_{SC}	Either output shorted to ground, either polarity				24	mA
		Outputs shorted together, either polarity		-12		+12	
Propagation Delay	t_{PD}	20mV overdrive			270		ps
		100mV overdrive			280		
		200mV overdrive			280		
Jitter	t_{JITTER}	Measured using square wave with Rise and Fall Time = 150ps, 100mV overdrive			2		ps
Overdrive Dispersion	$t_{OD-disp}$	10mV to 1V			25		ps
		20mV to 100mV			10		
Rise Time	t_R	From 25% to 75% output swing.	C_L = 1pF		150		ps
Fall Time	t_F	From 75% to 25% output swing.	C_L = 1pF		165		ps
Output Skew		Measured using square wave with Rise and Fall Time = 150ps, 100mV overdrive	Propagation Delay difference between OUTx+ and OUTx-		10		ps
Maximum Toggle Rate	T_R	V_{OUT} = 550mV, V_{OD} = 100mV			3		Gbps
Minimum Pulse Width					330		ps

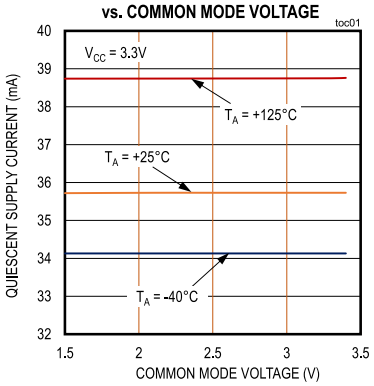
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Specifications are guaranteed by design and characterization and not production tested.

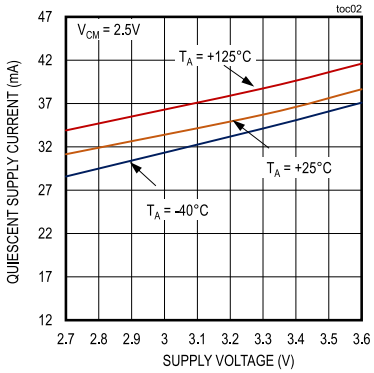
Typical Operating Characteristics

(R_{LOAD} = 100Ω, connected from OUT+ to OUT-.)

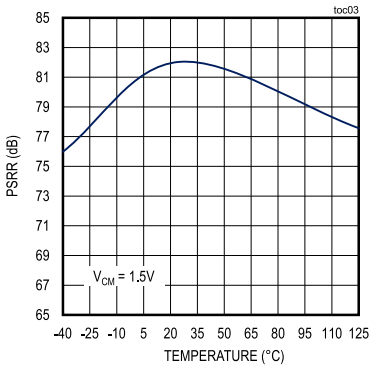
SUPPLY CURRENT vs. COMMON MODE VOLTAGE



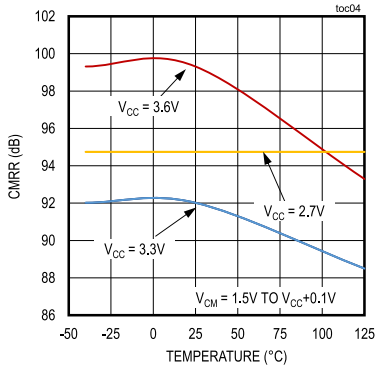
SUPPLY CURRENT vs. SUPPLY VOLTAGE



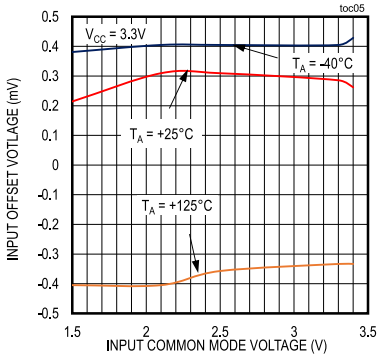
DC PSRR vs. TEMPERATURE



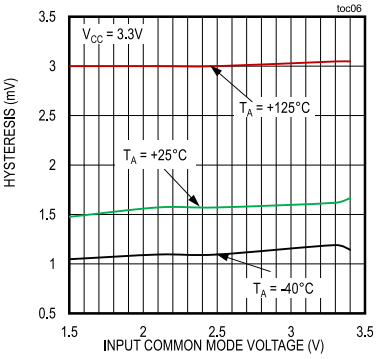
DC CMRR vs. TEMPERATURE



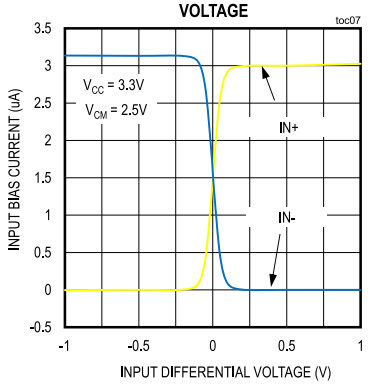
INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE VOTLAGE



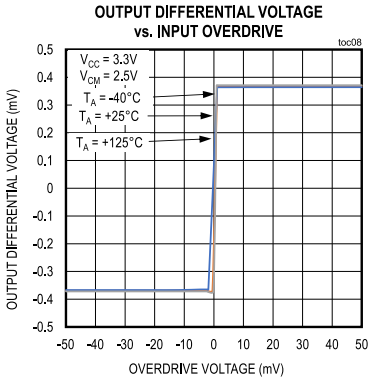
HYSTERESIS vs. INPUT COMMON MODE VOTLAGE



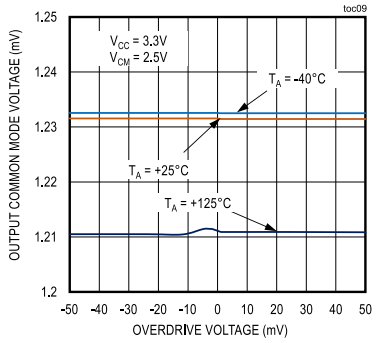
INPUT CURRENT vs. INPUT DIFFERENTIAL VOLTAGE



OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT OVERDRIVE

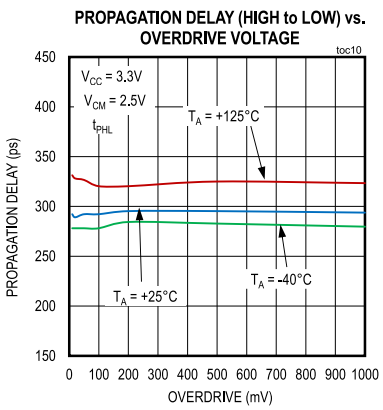


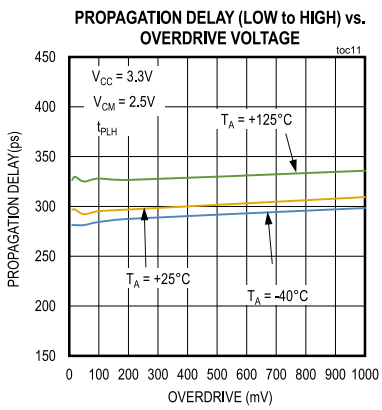
OUTPUT COMMON MODE VOTLAGE vs. INPUT OVERDRIVE

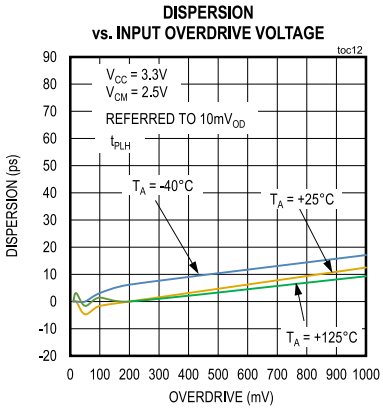


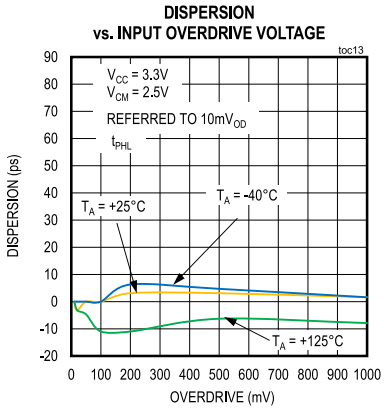
Typical Operating Characteristics (continued)

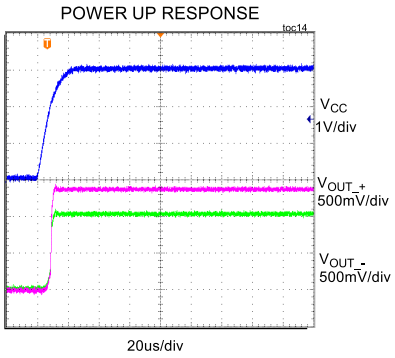
(R_{LOAD} = 100Ω, connected from OUT+ to OUT-.)





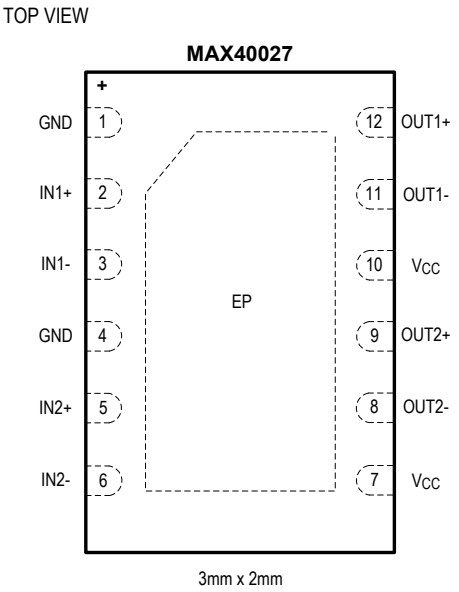






Pin Configuration

12 SWTDFN-EP



Pin Description

PIN	NAME	FUNCTION
1, 4	GND	Ground. Signal and power return. Connect pins 1 and 4 together externally.
2	IN1+	Comparator 1 Non-Inverting Input
3	IN1-	Comparator 1 Inverting Input
5	IN2+	Comparator 2 Non-Inverting Input
6	IN2-	Comparator 2 Inverting Input
7, 10	V_{CC}	Positive Supply. Connect pins 7 and 10 together externally.
8	OUT2-	Comparator 2 Inverting LVDS Output. Connect a 100Ω termination resistor between OUT2- and OUT2+. OUT2- is at logic-low if V_{IN2+} is at higher voltage compared to V_{IN2-}.
9	OUT2+	Comparator 2 Non-Inverting LVDS Output. Connect a 100Ω termination resistor between OUT2+ and OUT2-. OUT2+ is at logic-high if V_{IN2+} is at higher voltage compared to V_{IN2-}.
11	OUT1-	Comparator 1 Inverting LVDS Output. Connect a 100Ω termination resistor between OUT1- and OUT1+. OUT1- is at logic-low if V_{IN1+} is at higher voltage compared to V_{IN1-}.
12	OUT1+	Comparator 1 Non-Inverting LVDS Output. Connect a 100Ω termination resistor between OUT1+ and OUT1-. OUT1+ is at logic-high if V_{IN1+} is at higher voltage compared to V_{IN1-}.
EP	Exposed Pad	Exposed Pad. This pad must be connected to ground.

Detailed Description

The MAX40027 is a single-supply, dual high-speed comparator with a typical propagation delay of 280ps. The overdrive dispersion is extremely low (25ps, typ.), making these comparators ideal for time-of-flight distance measurement applications.

The input common-mode range of 1.5V to V_{CC} + 0.1V is compatible with the outputs of several widely used high-speed transimpedance amplifiers, such as the MAX40658, MAX40660, and MAX40661. The output stage is LVDS, which helps to minimize power dissipation and interfaces directly with many modern FPGAs and CPUs.

The MAX40027 operates from a +2.7V to +3.6V power supply voltage, while typically consuming only 17mA quiescent current per comparator at 3.3V. The MAX40027 is available in space-saving, 12-pin TDFN package.

LVDS Outputs

Each LVDS output has a switched 3.25mA current source. The outputs are differentially terminated with an external 100Ω resistor, which produces a ±350mV differential output. The power delivered to the 100Ω load resistor is only 1.1mW while enabling transmission data rates up to a few hundreds of Megabits per second. The output common-mode voltage is maintained at 1.23V on both outputs, and is independent of power supply voltage. The fully differential LVDS outputs provide high-speed, digital-signalling with reduced EMI compared to single-ended outputs.

System Timing Definitions

Table 1. Timing Definitions

SYMBOL	SPECIFICATION	DESCRIPTION
V_{OD}	Overdrive Voltage	Differential voltage applied across inputs during test.
t_{PDH}	Propagation Delay High on OUTx+	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output low-to-high transition on OUTx+.
t_{PDL}	Propagation Delay Low on OUTx-	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output high-to-low transition on OUTx-.
Δt_{PDHO}	Propagation Delay Skew on High	Difference in propagation delay on output transition from low to high on OUTx+ to propagation delay from high to low on OUTx-.
Δt_{PDLO}	Propagation Delay Skew on Low	Difference in propagation delay on output transition from high to low on OUTx+ to propagation delay from low to high on OUTx-.
t_R	Output Rise Time	Time taken by either OUTx+ or OUTx- to rise from 25% of final output voltage to 75% of final output voltage.
t_F	Output Fall Time	Time taken by either OUTx+ or OUTx- to fall from 75% of final output voltage to 25% of final output voltage.
$t_{PD\overline{L}}$	Propagation Delay Low on OUT-	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output high-to-low transition on OUTx-.
$t_{PD\overline{H}}$	Propagation Delay High on OUT-	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output low-to-high transition on OUTx-.
t_{PDHD}	Differential Propagation Delay High	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output differential signal across OUTx+ to OUTx- while switching low to high.
t_{PDLD}	Differential Propagation Delay Low	Propagation delay measured from the time the differential input signal changes polarity (± input V_{OS}) to the 50% point in the output differential signal across OUTx+ to OUTx- while switching high to low.
V_{OH}	Output Voltage High	Comparator output high state voltage level.
V_{OL}	Output Voltage Low	Comparator output low state voltage level.

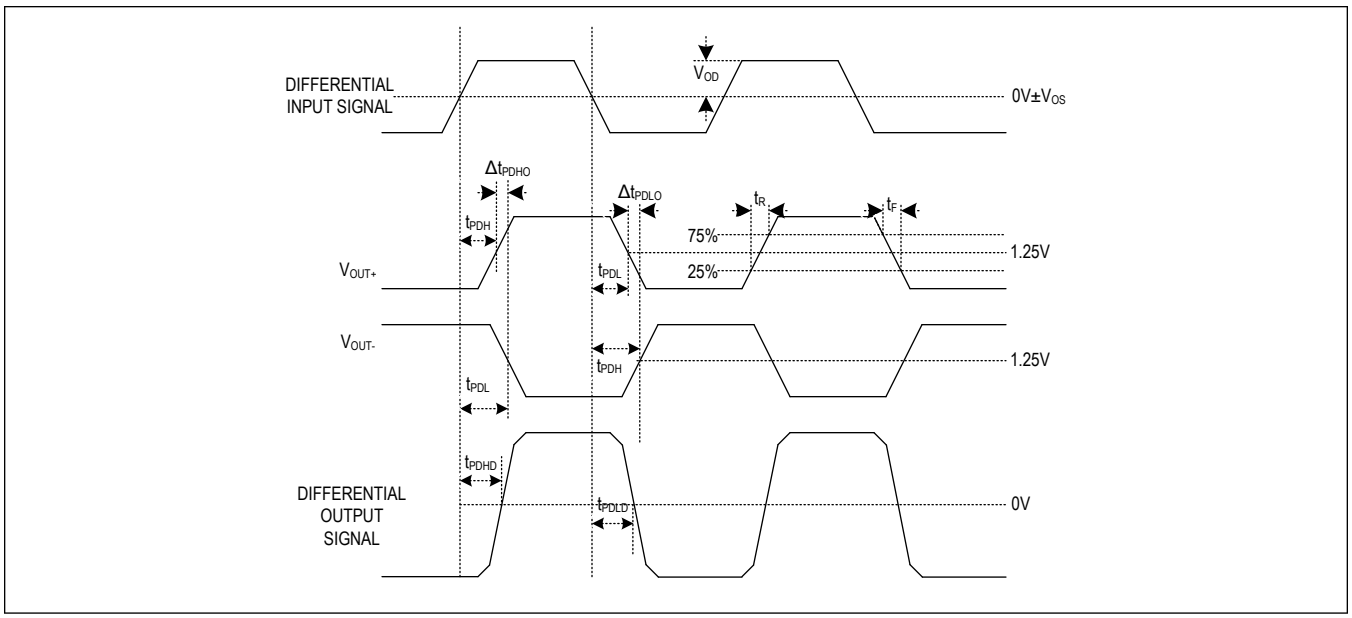


Figure 1. System Timing Diagram

Propagation Delay

The propagation delay is defined as the delay between the differential comparator input voltage changing polarity and the output(s) reaching the midpoint of the high-to-low or low-to-high transition. The low-to-high propagation delay is t_{PDH} on OUTx+ and $t_{\overline{PDH}}$ on OUTx-, whereas the high-to-low propagation delay is t_{PDL} on OUTx+ and $t_{\overline{PDL}}$ on OUTx-. These high-to-low and low-to-high timing parameters will differ slightly due to mismatches between the two complementary outputs. As a result, this difference in propagation delay is considered to be a skew for a given combination of low-to-high transitions on OUTx+ and high-to-low transitions on OUTx-.

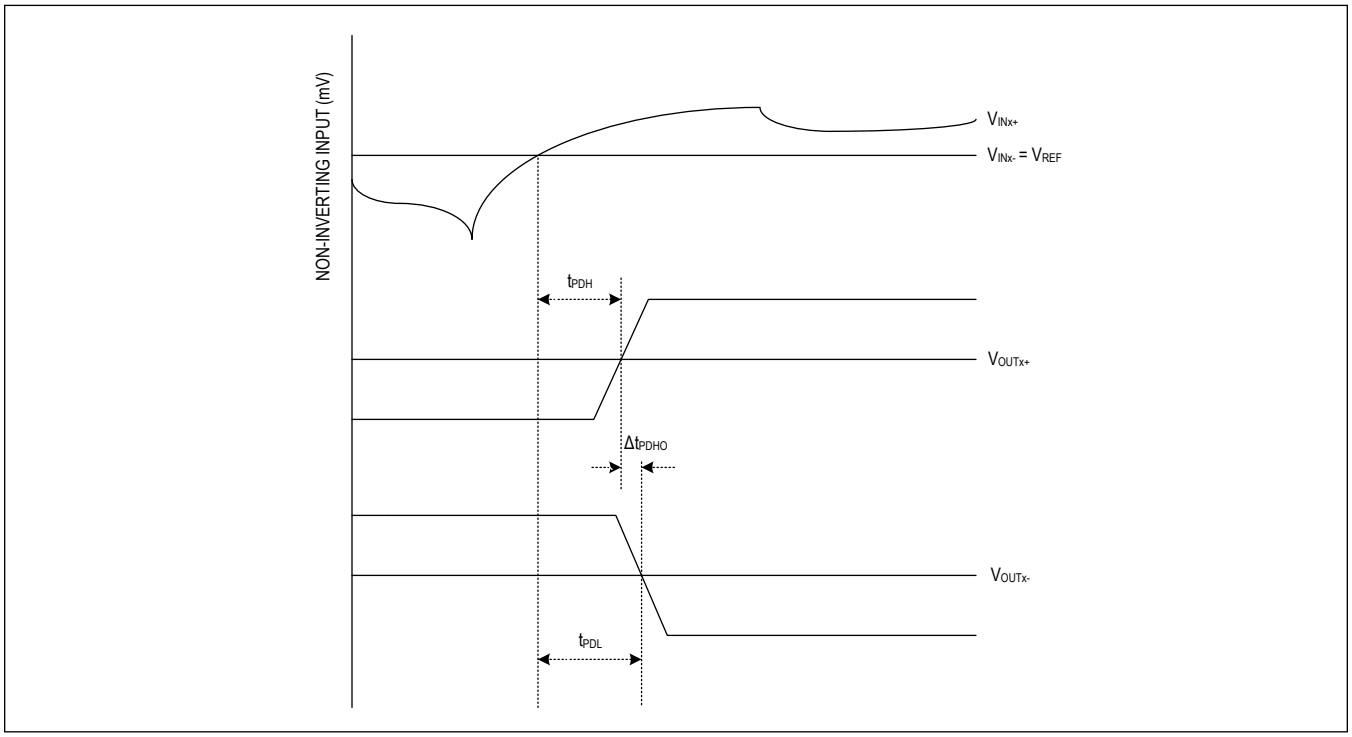


Figure 2. Propagation Delay

Propagation Delay Dispersion

Dispersion, or variation of the propagation delay under different conditions, is affected by the amount of overdrive voltage applied to the comparator inputs. As can be seen in the Typical Operating Characteristics, the dispersion is typically under 25ps for 10mV to 1V, a wide range of input overdrive values.

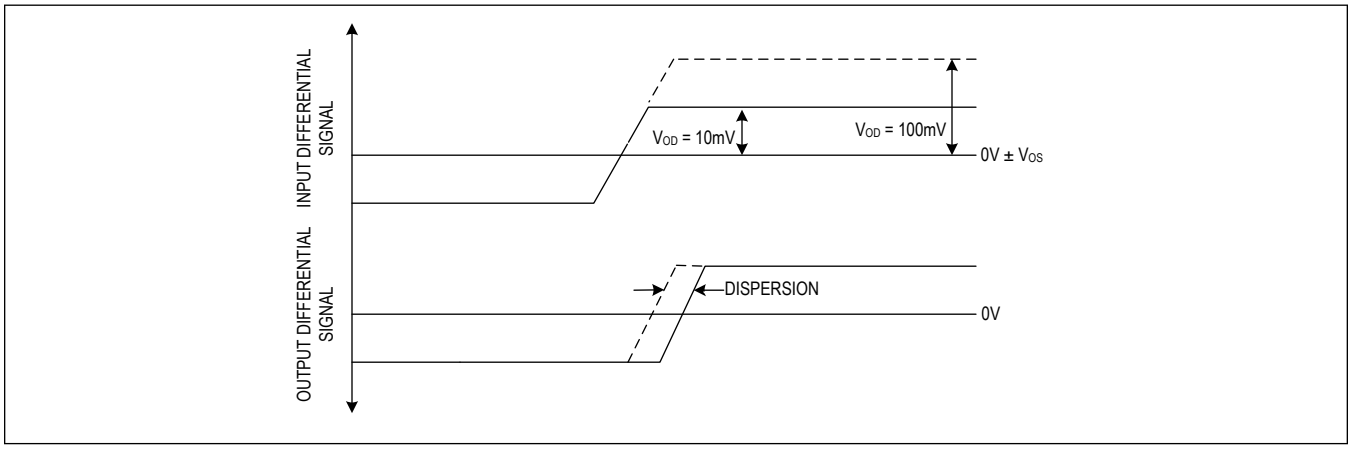


Figure 3. Amplitude Overdrive Dispersion

Dispersion is also affected by the input slew rate. As the slew rate of the input signal changes, the propagation delay also changes. The dispersion is typically under 15ps from 0.4V/µs to 1V/µs input slew rates.

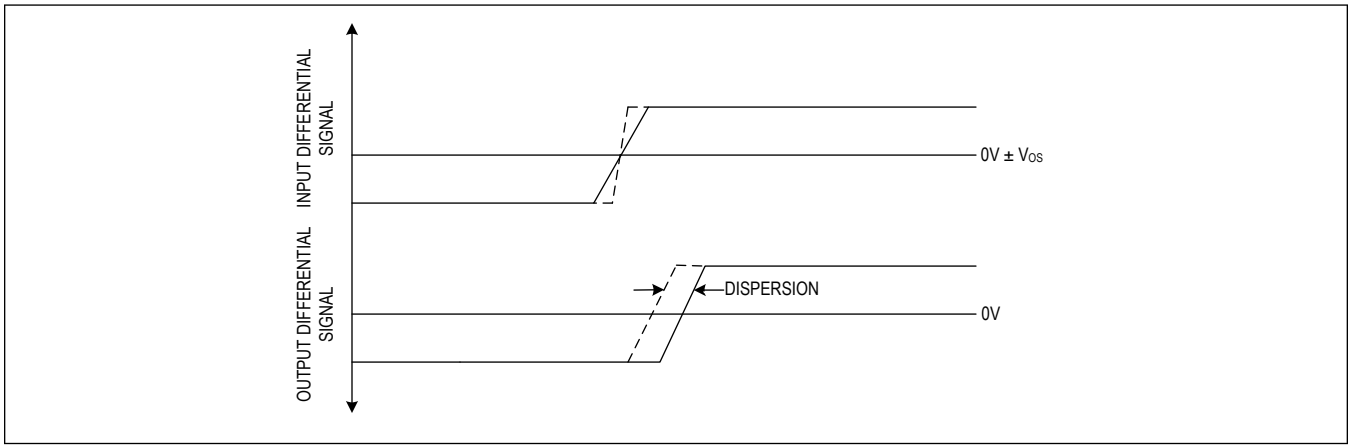


Figure 4. Slew Rate Dispersion

Hysteresis

Adding a small amount hysteresis to a comparator in a noisy environment is useful when input signals are slow-moving and have small noise levels superimposed on them. However, hysteresis must be used carefully when signals are small because it can cause valid signals to be ignored. Figure 5 shows the input signal and output response for a comparator with hysteresis applied.

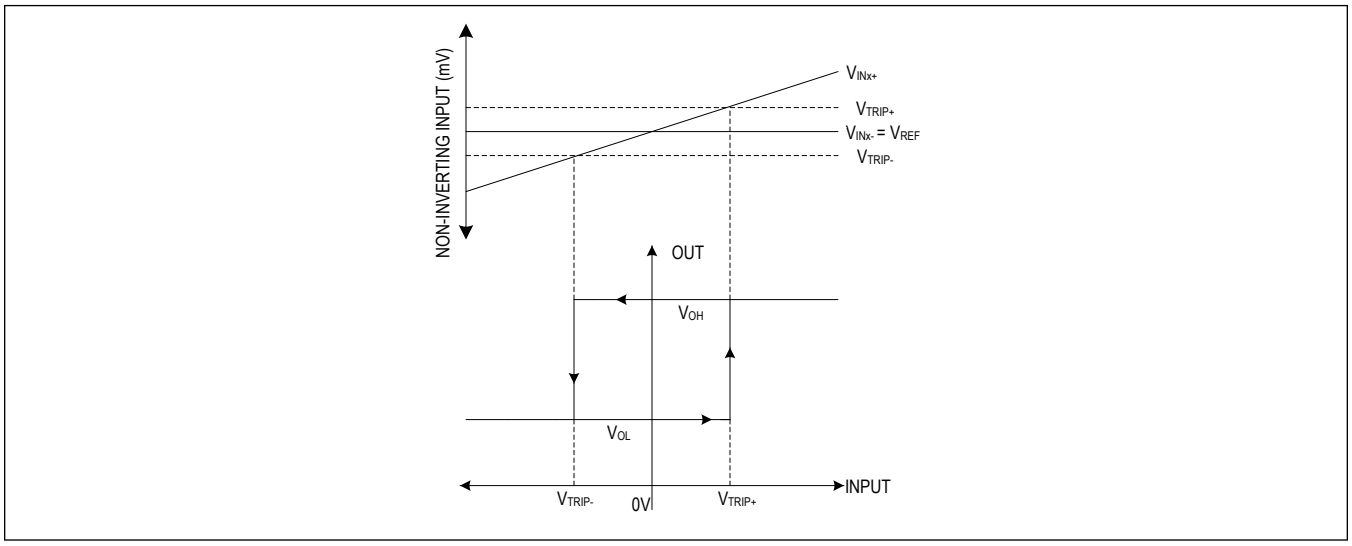


Figure 5. Hysteresis Transfer Function

The MAX40027 has fixed internal 1.5mV hysteresis, which improves its usefulness for detecting larger differential input signals in the presence of noise. This helps to avoid the external components and potential stability degradation associated with external positive feedback paths.

Input Stage Circuitry

The MAX40027 includes internal protection circuitry that prevents damage to the precision input stage from large differential input voltages.This protection circuitry consists of two groups of two front-to-back diodes between INx+ and INx-, as well as two 50Ω resistors (Figure 6). The diodes limit the differential voltage applied to the comparator's internal circuitry to no more than $2(V_F)$, where V_F is the diode's forward-voltage drop (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2(V_F)$), this protection circuitry increases the input bias current at INx+ (source) and INx- (sink).

$$\text{INPUT CURRENT} = \frac{\left(V_{INx+} - V_{INx-}\right) - 2 \times V_F}{2 \times 50}$$

Input currents with large differential input voltages should not be confused with input bias currents (I_B). As long as the differential input voltage is less than $2(V_F)$, this input current is less than $2I_B$.

The input circuitry allows the MAX40027's input common-mode range to extend 100mV beyond the positive power-supply rail. The output remains in the correct logic state if one or both inputs are within the common-mode range. Taking either input outside the common-mode range causes the input to saturate and the propagation delay to increase.

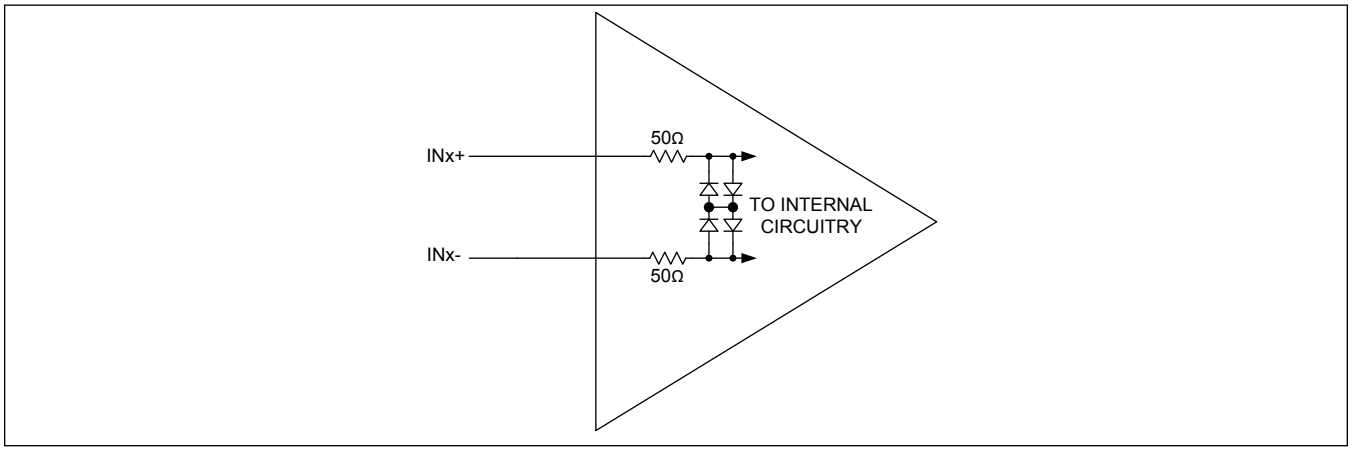


Figure 6. Input Stage Circuitry

Applications Information

Critical Layout Guidelines

Some critical layout guidelines are listed below.

- Use a PC board with a low-impedance ground plane.
- Mount one or more 10nF ceramic capacitors between GND and V_{CC}, as close to the pins as possible. Multiple bypass capacitors help to reduce the effect of trace impedance and capacitor ESR.
- Choose bypass capacitors for minimum inductance and ESR.
- Use a 100Ω termination resistor for the LVDS output, connected directly between OUTx+ and OUTx-, if practical. If the destination LVDS inputs can't be located adjacent to the outputs, use a 100Ω microstrip between the output pins and the termination resistor, which should be close to the LVDS inputs of the FPGA or other destination component. This will avoid the creation of stub beyond the termination resistor, which will cause reflections. The added length of the differential trace has less degrading affects than added stub length.
- Ensure that there is no parasitic coupling between the inputs and the outputs. Such coupling serves as feedback, and can result in oscillation.
- Minimize any parasitic layout inductance.
- It is recommended to use higher performance substrate materials (for example, Rogers).
- A differential micro-strip is the recommended layout for the MAX40027 with terminations done close to the device inputs and outputs. Care must be taken to avoid unwanted stubs by removing ground below the traces that are not part of the 50Ω termination line leading into input pins. The parasitic capacitance created between traces and ground slow down and even distort the signals by creating reflections on the path.
- Prevent cross coupling by routing one channel inputs and outputs on the top layer, and the other channel inputs and outputs on the bottom layer.
- Below is an example from the MAX40027EVKIT#, where ground has been etched/removed underneath a stub as shown in the layer below top layer.

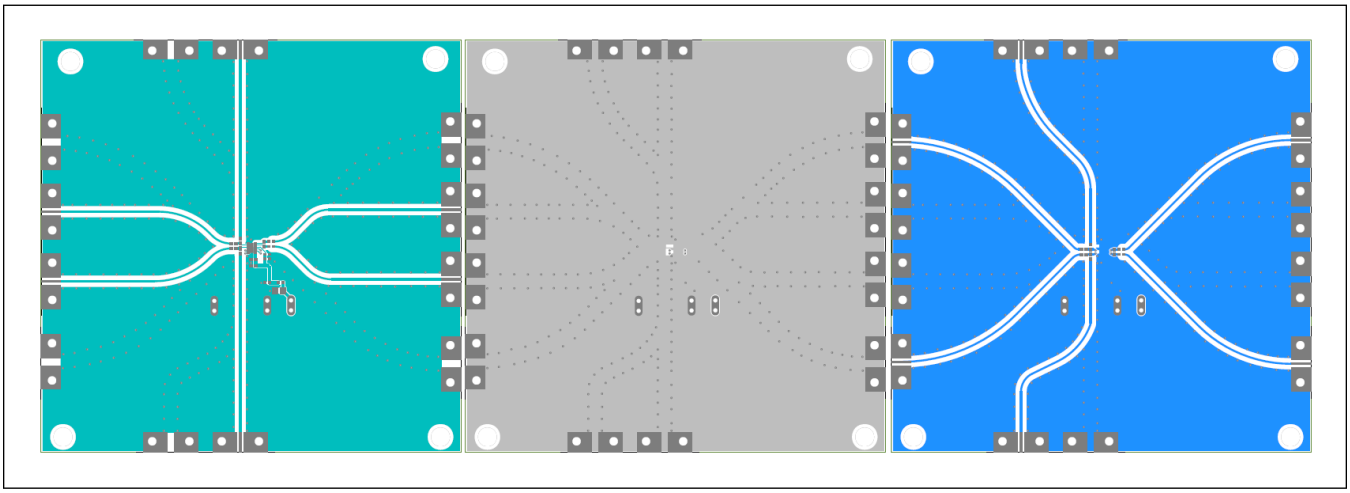


Figure 7. Layout Guidelines—Ground Keep-Out to Avoid Stubs.

Input Slew Rate

With slower slew rates, when the input voltage is near the threshold any parasitic feedback paths can cause oscillation. In addition, the comparator's input noise will cause the output to undergo transitions. Eliminating feedback paths will stop oscillation. To avoid noise-induced chattering, the input slew rate should be greater than 1V/µs.

Typical Application Circuits

Receiver Section of Differential Time-of-Flight Measurement Circuit:

In Figure 8, the photodiode, shown at the far right, converts light incident upon it into current that drives the input of the MAX40660 Transimpedance Amplifier (TIA). The MAX40660 then converts photodiode current to voltage, amplifies it, and passes a replica of the incident light to input of the high-speed comparator. By default, the MAX40660 has -200mV differential output offset voltage when there is no input current. This offset can be adjusted using the MAX40660's offset pin. The MAX40027 produces differential output pulses whenever an incident light pulse has intensity sufficient to change the polarity of the comparator input signal.

Receiver Section of Single-Ended Time-of-Flight Measurement Circuit:

Figure 9 has a single-ended output configuration on the transimpedance amplifier, which drives one input of the comparator. This functionality is the same as that of the differential configuration discussed above, except that the threshold voltage can be adjusted by selecting the values of R1 and R2.

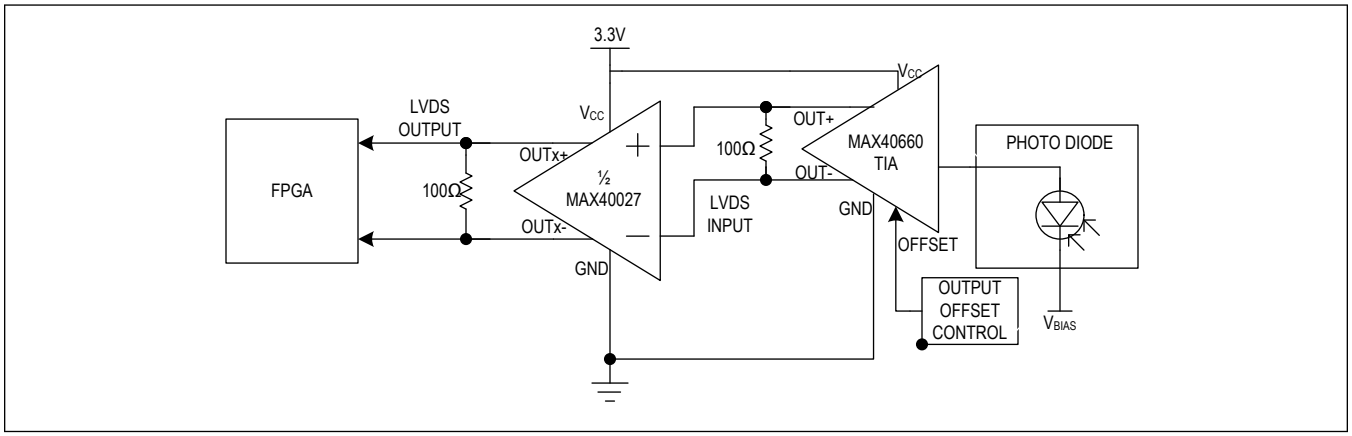


Figure 8. Differential-Ended Output Receiver

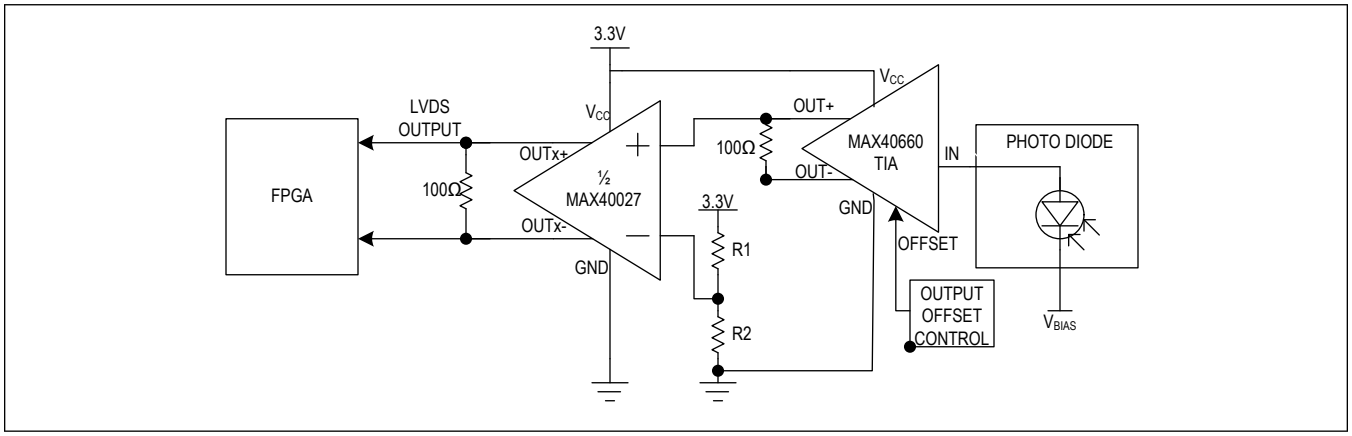


Figure 9. Single-Ended Output Receiver

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	TOP MARK	HYSTERESIS
MAX40027ATC/VY+T	-40°C to +125°C	12-SWTDFN-EP	AHG	1.5mV

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V denotes an automotive qualified part.

Y = Side-wettable package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial Release	—