April 2002

National Semiconductor

CLC5957
12-Bit, 70 MSPS Broadband Monolithic A/D Converter

General Description

The CLC5957 is a monolithic 12-bit, 70MSPS analog-to-digital converter. The device has been optimized for use in IF-sampled digital receivers and other applications where high resolution, high sampling rate, wide dynamic range, low power dissipation, and compact size are required. The CLC5957 features differential analog inputs, low jitter differential universal clock inputs, a low distortion track-and-hold with 0-300MHz input bandwidth, a bandgap voltage reference, data valid clock output, TTL compatible CMOS (3.3V or 2.5V) programmable output logic, and a proprietary 12-bit multi-stage quantizer. The CLC5957 is fabricated on the ABIC-V 0.8 micron BiCMOS process.

The CLC5957 features a 74dBc spurious free dynamic range (SFDR) and a 67dB signal to noise ratio (SNR). The wideband track-and-hold allows sampling of IF signals to greater than 250MHz. The part produces two-tone, dithered, SFDR of 83dBFS at 75MHz input frequency. The differential analog input provides excellent common mode rejection, while the differential universal clock inputs minimize jitter. The 48-pin TSSOP package provides an extremely small footprint for applications where space is a critical consideration. The CLC5957 operates from a single +5V power supply. Operation over the industrial temperature range of -40˚C to +85˚C is guaranteed. National Semiconductor tests each part to verify compliance with the guaranteed specifications.

Features

- 70MSPS
- Wide dynamic range:
  - — SFDR: 74dBc
  - — SFDR with dither: 85dBFS
  - — SNR: 67dB
- IF sampling capability
- Input bandwidth = 0-300MHz
- Low power dissipation: 640mW
- Very small package: 48-pin TSSOP
- Single +5V supply
- Data valid clock output
- Programmable output levels: 3.3V or 2.5V

Applications

- Cellular base stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

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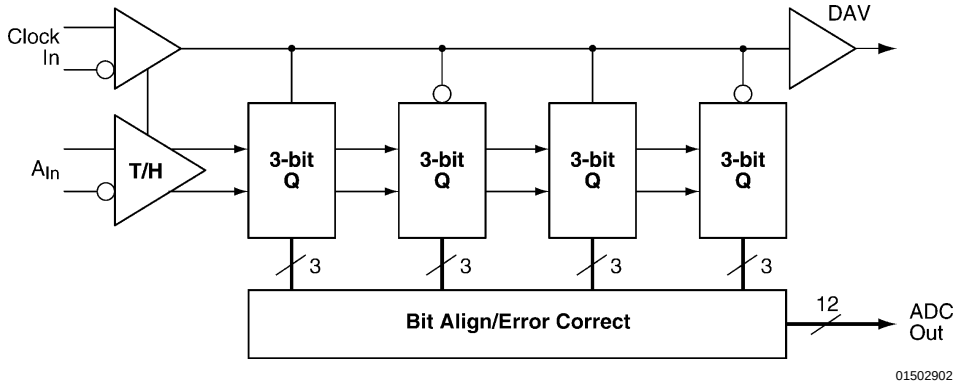
Block Diagram



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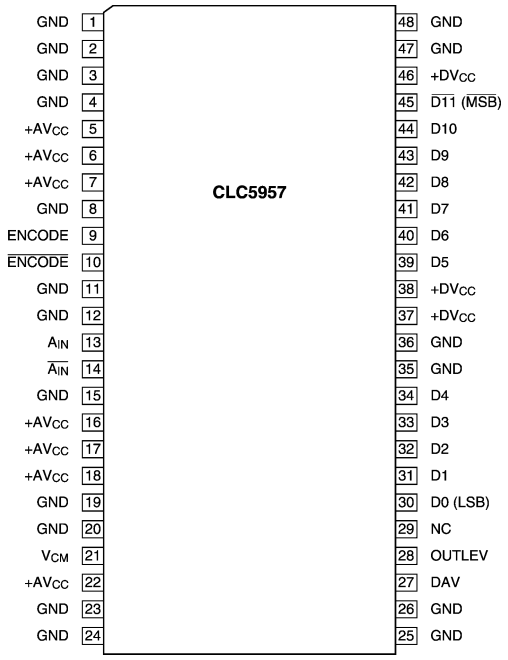
Pin Configuration



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Ordering Information

CLC5957MTD	48-Pin TSSOP
CLC5957MTDX	48-Pin TSSOP (Taped Reel)
CLC5957PCASM	Evaluation Board

Pin Descriptions

Pin Name	Pin No.	Description
A_{IN} / $\overline{A_{IN}}$	13, 14	Differential input with a common mode voltage of +2.4V. The ADC full scale input is 1.024 V_{PP} on each of the complimentary input signals.
ENCODE / $\overline{\text{ENCODE}}$	9, 10	Differential clock where ENCODE initiates a new data conversion cycle on each rising edge. Logic for these inputs are a 50% duty cycle universal differential signal (>200mV). The clock input is internally biased to $V_{CC}/2$ with a termination impedance of 2.5kΩ.
V_{CM}	21	Internal common mode voltage reference. Nominally +2.4V. Can be used for the input common mode voltage. This voltage is derived from an internal bandgap reference. V_{CM} should be buffered when driving any external load. Failure to buffer this signal can cause errors in the internal bias currents.
D0–$\overline{\text{D11}}$	30–34, 39–45	Digital data outputs are CMOS and TTL compatible. D0 is the LSB and $\overline{\text{D11}}$ is the MSB. MSB is inverted. Output coding is two's complement. Current limited to source/sink 2.5mA typical.
GND	1–4, 8, 11, 12, 15, 19, 20, 23–26, 35, 36, 47, 48	Circuit ground.
$+AV_{CC}$	5–7, 16–18, 22	+5V power supply for the analog section. Bypass to ground with a 0.1 µF capacitor.
$+DV_{CC}$	37, 38, 46	+5V power supply for the digital section. Bypass to ground with a 0.1 µF capacitor.
NC	29	No connect. May be left open or grounded.
DAV	27	Data Valid Clock. Data is valid on rising edge. Current limited to source/sink 5mA typical.
OUTLEV	28	Output Logic 3.3V or 2.5V option. Open = 3.3V, GND = 2.5V.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage (V_{CC})	−0.5V to +6V
Differential Voltage between any two Grounds	<100 mV
Analog Input Voltage Range	GND to V_{CC}
Digital Input Voltage Range	−0.5V to +V_{CC}
Output Short Circuit Duration (one-pin to ground)	Infinite
Junction Temperature (Note 7)	175˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec.
ESD tolerance	
human body model	2000V
machine model	200V

Recommended Operating Conditions

Positive Supply Voltage (V_{CC})	+5V ±5%
Analog Input Voltage Range	2.048 V_{PP} diff.
Operating Temperature Range	−40˚C to +85˚C

Package Thermal Resistance (Note 7)

Package	θ_{JA}	θ_{JC}
48-Pin TSSOP	56˚C/W	16˚C/W

Reliability Information

Transistor Count	5000

Converter Electrical Characteristics

The following specifications apply for AV_{CC} = DV_{CC} = +5V, 66MSPS. **Boldface limits apply for T_A = T_{min} = −40˚C to T_{max} = +85˚C,** all other limits T_A = 25˚C (Note 3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
BW	Large-Signal Bandwidth	A_{IN} = −3 dBFS		300		MHz
	Overvoltage Recovery Time	A_{IN} = 1.5 FS (0.01%)		12		ns
t_A	Effective Aperture Delay			−0.41		ns
t_{AJ}	Aperture Jitter			0.3		ps(rms)
NOISE AND DISTORTION						
SNR *(Note 2)	Signal-to-Noise Ratio (without 50 harmonics)	f_{IN} = 5 MHz, A_{IN} = −1dBFS		67		dBFS
		f_{IN} = 25 MHz, A_{IN} = −1dBFS*	**60**	66		dBFS
		f_{IN} = 75 MHz, A_{IN} = −3dBFS		65		dBFS
		f_{IN} = 150 MHz, A_{IN} = −15dBFS		66		dBFS
		f_{IN} = 250 MHz, A_{IN} = −15dBFS		66		dBFS
SFDR	Spurious-Free Dynamic Range	f_{IN} = 5 MHz, A_{IN} = −1dBFS		74		dBc
		f_{IN} = 25 MHz, A_{IN} = −1dBFS*	**60**	74		dBc
		f_{IN} = 75 MHz, A_{IN} = −3dBFS		72		dBc
		f_{IN} = 150 MHz, A_{IN} = −15dBFS		69		dBc
		f_{IN} = 250 MHz, A_{IN} = −15dBFS		65		dBc
	Spurious-Free Dynamic Range (dithered)	f_{IN} = 19 MHz, A_{IN} = −6dBFS		85		dBFS
IMD	Intermodulation Distortion	f_{IN1} = 149.84 MHz, f_{IN2} = 149.7 MHz, A_{IN} = −10dBFS		68		dBFS
		f_{IN1} = 249.86 MHz, f_{IN2} = 249.69 MHz, A_{IN} = −10dBFS		58		dBFS
	Intermodulation Distortion (dithered)	f_{IN1} = 74 MHz, f_{IN2} = 75 MHz, A_{IN} = −12dBFS		83		dBFS
DC ACCURACY AND PERFORMANCE						
DNL	Differential Non-Linearity	f_{IN} = 5MHz, A_{IN} = −1dBFS		±0.65		LSB
INL	Integral Non-Linearity	f_{IN} = 5MHz, A_{IN} = −1dBFS		±1.5		LSB
	Offset Error (Note 2)		**−30**	0	**30**	mV
	Gain Error			1.2		% FS
V_{REF}	Reference Voltage (Note 2)		2.2	2.37	2.6	V
	No Missing Codes (Note 2)	f_{IN} = 5MHz, A_{IN} = -1dBFS	Guaranteed			

Converter Electrical Characteristics (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V, 66MSPS. **Boldface limits apply for T_A = T_{min} = −40˚C to T_{max} = +85˚C,** all other limits T_A = 25˚C (Note 3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INPUTS						
V_{IN}	Analog Diff Input Voltage Range			2.048		V_{PP}
R_{IN} (SE)	Analog Input Resistance (Single-Ended)			500		Ω
R_{IN} (Diff)	Analog Input Resistance (Differential)			1000		Ω
C_{IN}	Analog Input Capacitance (Single-ended)			2		pF
ENCODE INPUTS (UNIVERSAL)						
V_{IH}	Logic Input High Voltage (Note 4),(Note 5)				5	V
V_{IL}	Logic Input Low Voltage(Note 4),(Note 5)		0			V
	Differential Input Swing (Note 4),(Note 5)		0.2			V
DIGITAL OUTPUTS						
V_{OL}	Logic Output Low Voltage (Note 2)			0.01	0.4	V
V_{OH}	Logic Output High Voltage (Note 2)	OUTLEV = 1 (open)	3.2	3.5	3.8	V
		OUTLEV = 0 (GND)	2.4	2.7	3.0	V
TIMING (Note 6)						
	Maximum Conversion Rate (ENCODE) (Note 2)		**70**	75		MSPS
	Minimum Conversion Rate (ENCODE)			10		MSPS
t_P	Pulse Width High (ENCODE) (Note 4)	50% threshold	**7.1**			ns
t_M	Pulse Width Low (ENCODE) (Note 4)	50% threshold	**7.1**			ns
t_{DNV}	ENCODE falling edge to DATA not valid (Note 4)		**8.3**			ns
t_{DGV}	ENCODE falling edge to DATA guaranteed valid (Note 4)				**17.8**	ns
t_{DAV}	Rising ENCODE to rising DAV delay (Note 4)	50% threshold	**8.3**		**12.6**	ns
t_S	DATA setup time before rising DAV (Note 4)		**t_M−2.4**			ns
t_H	DATA hold time after rising DAV (Note 4)		**t_P−1.6**			ns
	Pipeline latency				**3.0**	clk cycle

Converter Electrical Characteristics (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V, 66MSPS. **Boldface limits apply for T_A = T_{min} = −40˚C to T_{max} = +85˚C,** all other limits T_A = 25˚C (Note 3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER REQUIREMENTS						
I_{CC}	Total Operating Supply Current (Note 2)			128	**150**	mA
	Power Dissipation (Note 2)			640	**750**	mW
	Power Supply Rejection Ratio			64		dB

Note 1: "Absolute Maximum Ratings" are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 2: These parameters are guaranteed by test.

Note 3: Typical specifications are based on the mean test values of deliverable converters from the first three diffusion lots.

Note 4: Values guaranteed based on characterization and simulation.

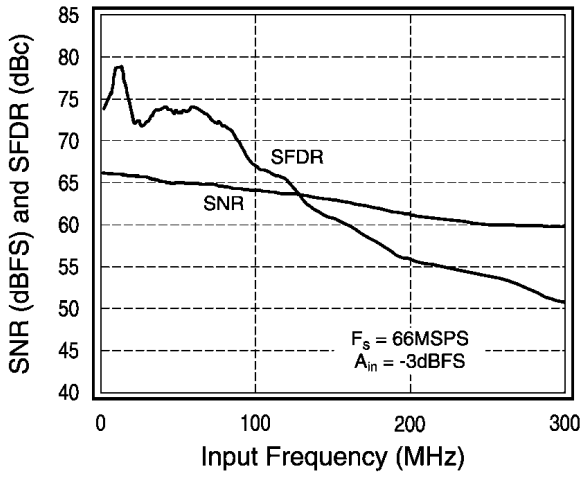
Note 5: See page 14, Figure 3 for ENCODE inputs circuit.

Note 6: C_L = 7pF DATA; 10pF DAV.

Note 7: The absolute maximum junction ($T_J$max) temperature for this device is 175˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D$max = ($T_J$max – T_A)/θ_{JA}. For the 48-pin TSSOP, θ_{JA} is 56˚C/W, so $P_D$max = 2.68W at 25˚C and 1.6W at the maximum operating ambient temperature of 85˚C. Note that the power dissipation of this device under normal operation will typically be about 650 mW (640 mW quiescent power + 10 mW due to 1 TTL load on each digital output). The values of absolute maximum power dissipation will only be reached when the CLC5957 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Typical Performance Characteristics (AV_{CC} = DV_{CC} = +5V)

SNR and SFDR vs. Input Frequency



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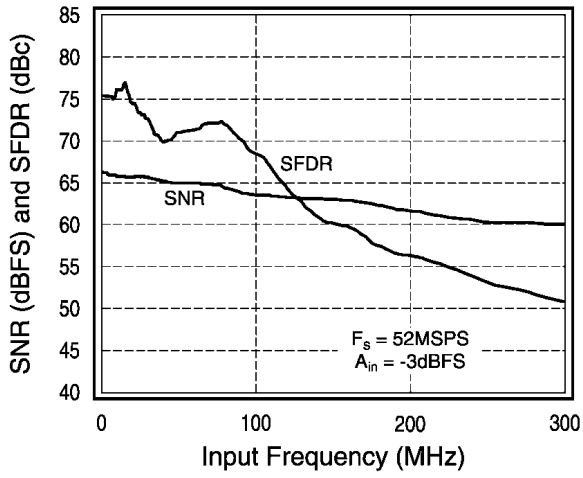
SNR and SFDR vs. Input Frequency



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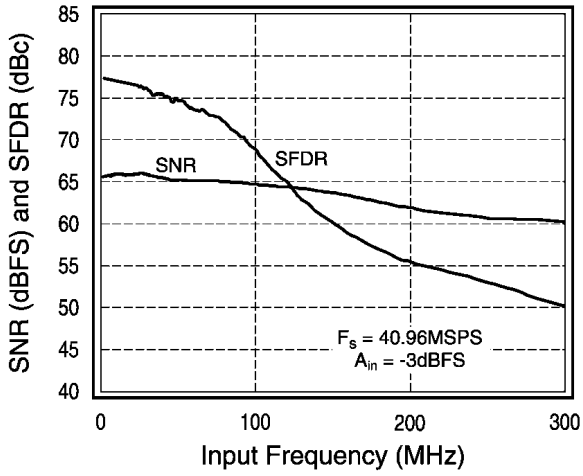
SNR and SFDR vs. Input Frequency



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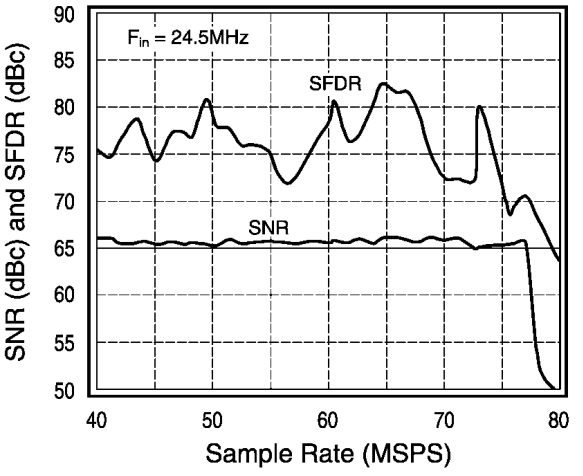
SNR and SFDR vs. Sample Rate



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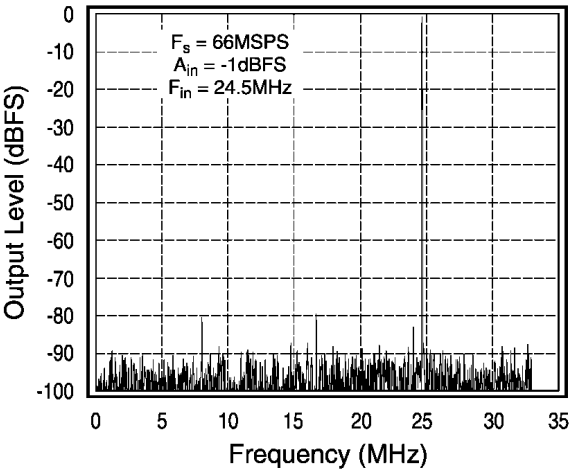
Single Tone Output Spectrum



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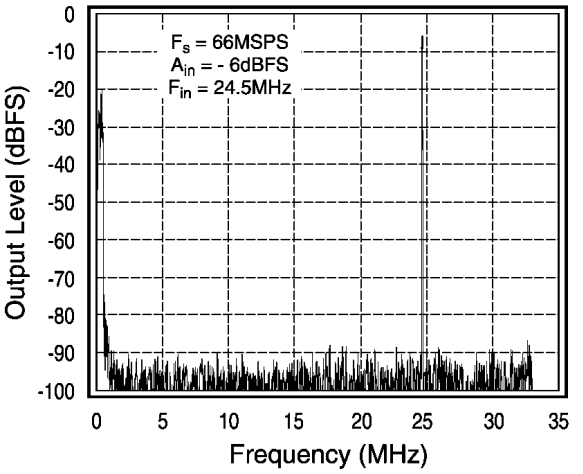
Single Tone Output Spectrum (w/Dither)



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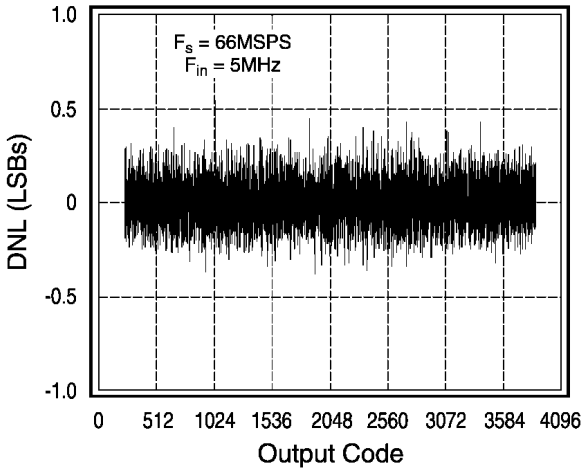
Typical Performance Characteristics (AV_{CC} = DV_{CC} = +5V) (Continued)

Differential Non-Linearity



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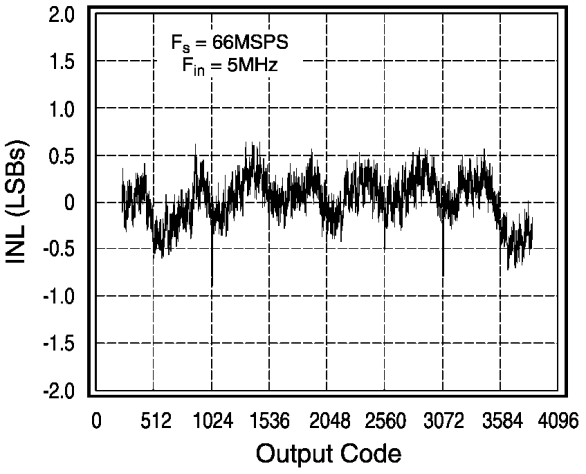
Integral Non-Linearity



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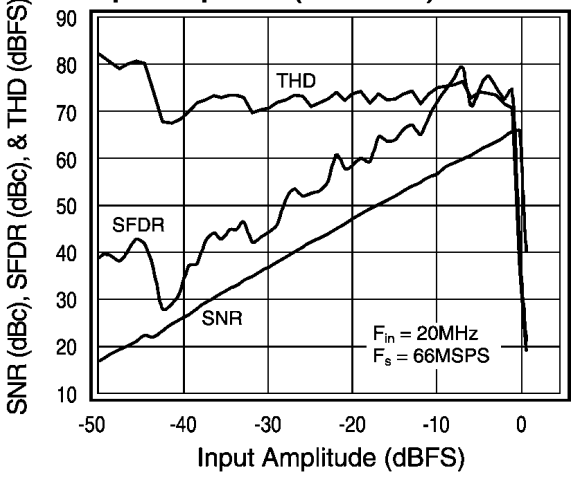
SNR and SFDR vs. Input Amplitude (w/o Dither)



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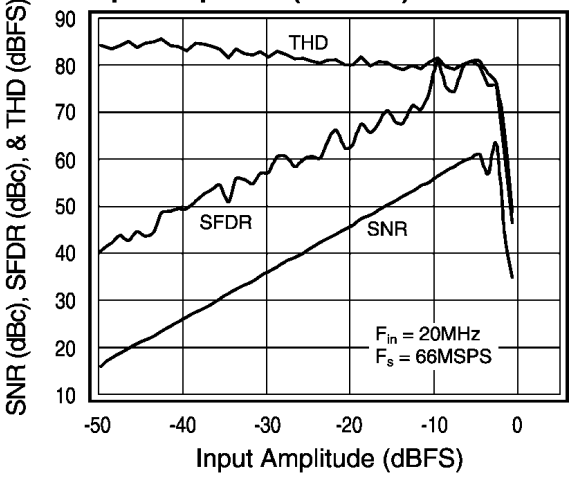
SNR and SFDR vs. Input Amplitude (w/Dither)



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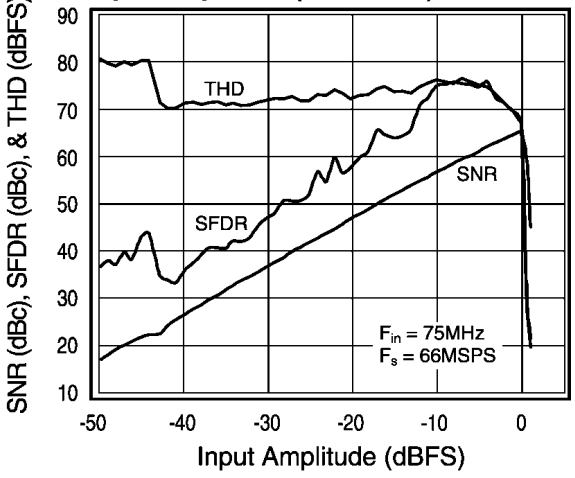
SNR and SFDR vs. Input Amplitude (w/o Dither)



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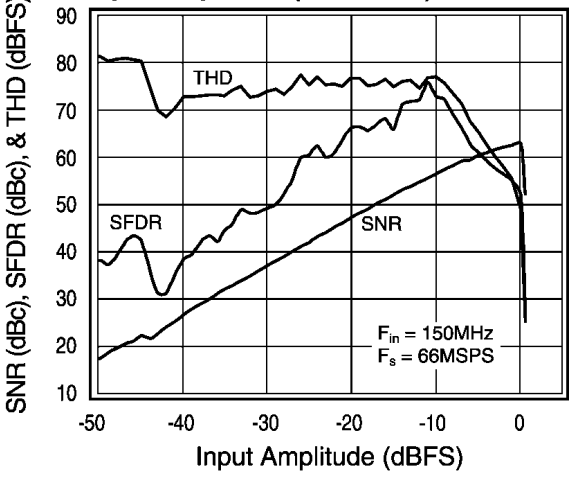
SNR and SFDR vs. Input Amplitude (w/o Dither)



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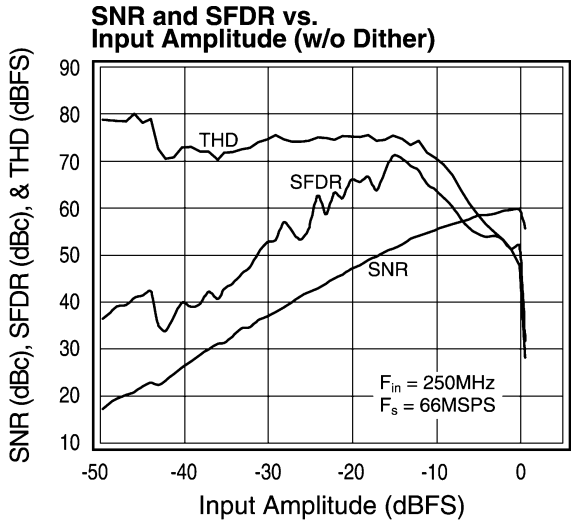
Typical Performance Characteristics (AV_{CC} = DV_{CC} = +5V) (Continued)



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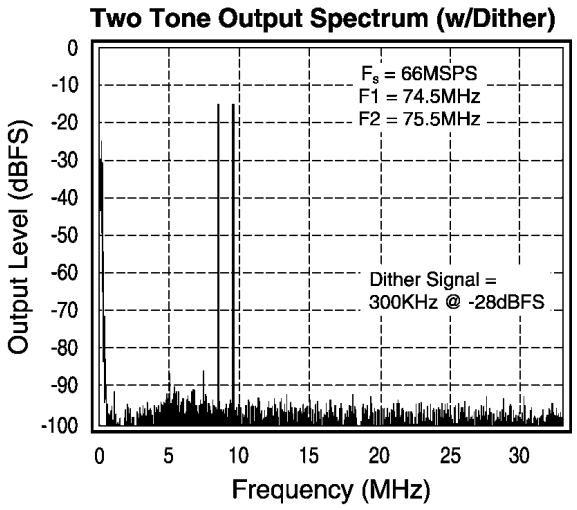

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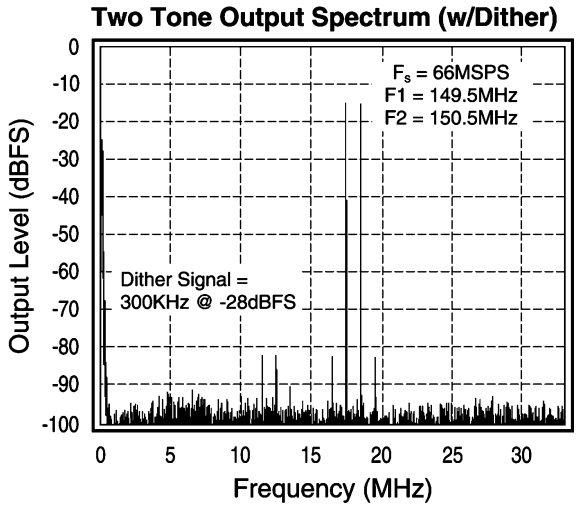

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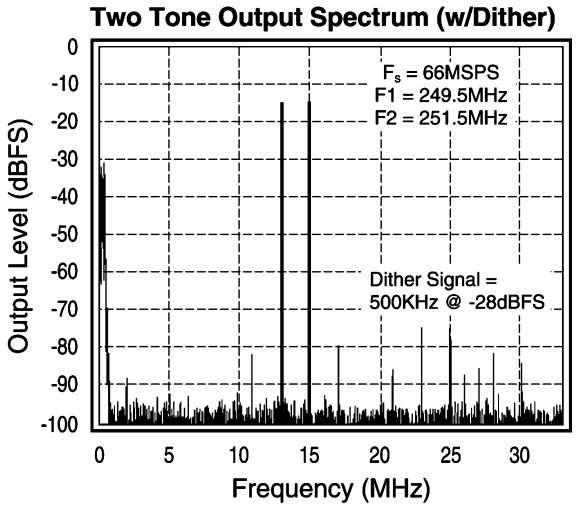

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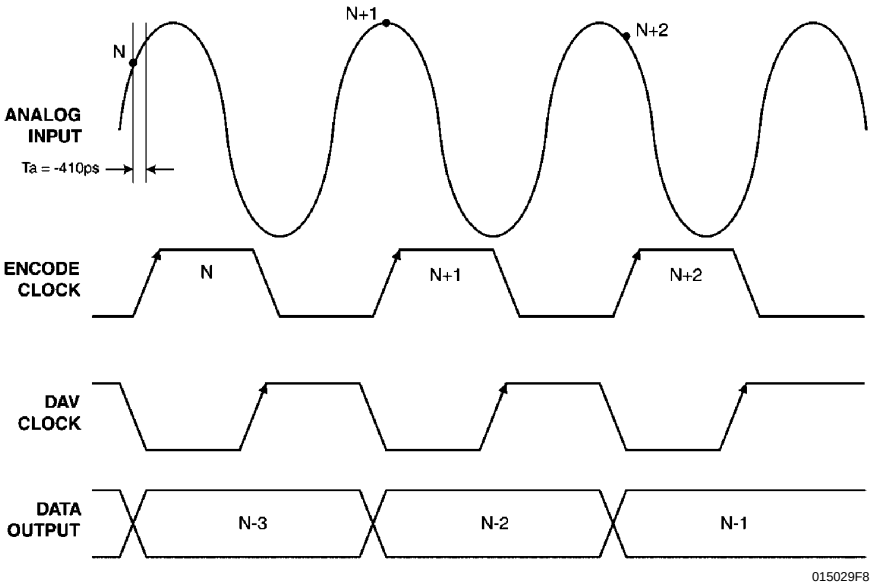
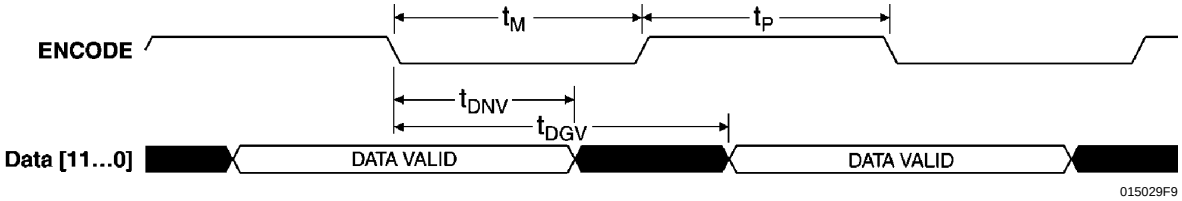
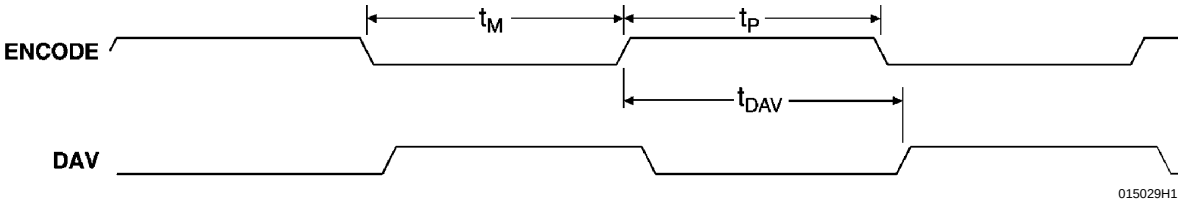
Timing Diagrams



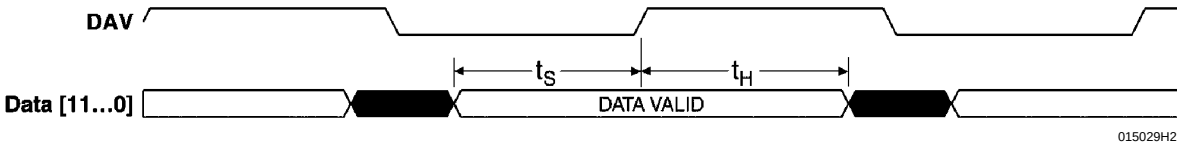
CLC5957 APERTURE DELAY Diagram



CLC5957 ENCODE to Data Timing Diagram

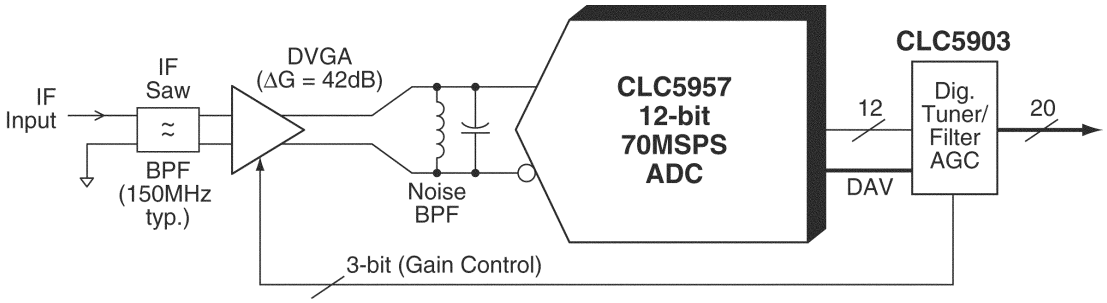


CLC5957 ENCODE to DAV Timing Diagram



CLC5957 DAV to Data Timing Diagram

Single IF Down Converter (Diversity Receiver Chipset)



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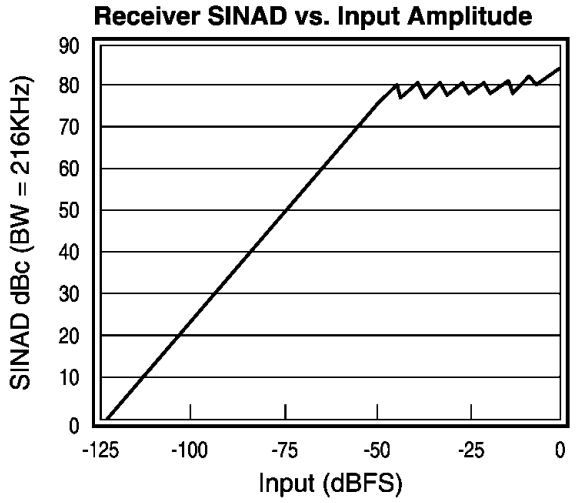

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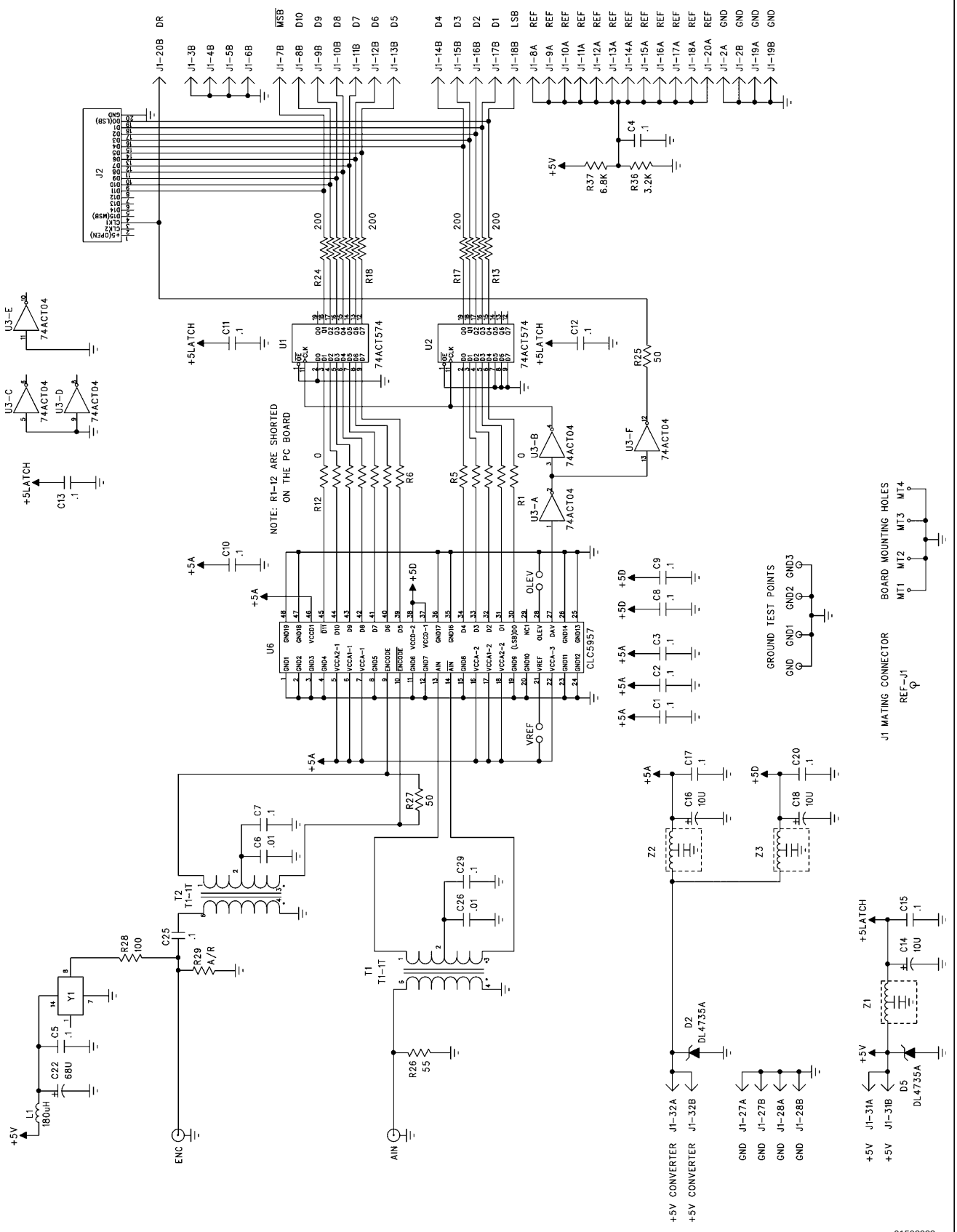
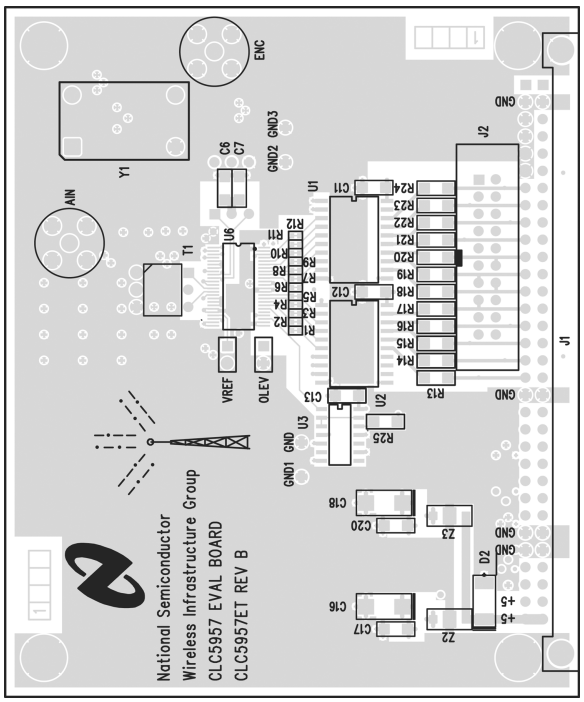
Evaluation Board



Evaluation Board Schematic

Evaluation Board (Continued)



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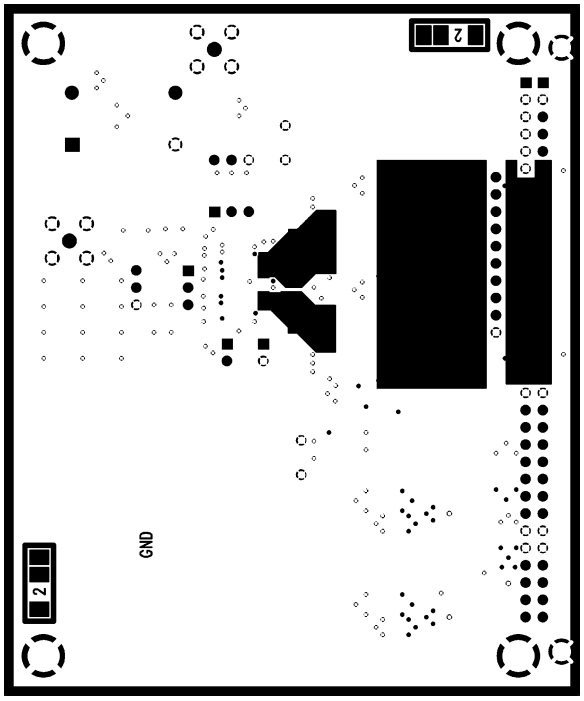
CLC5957PCASM Layer 1



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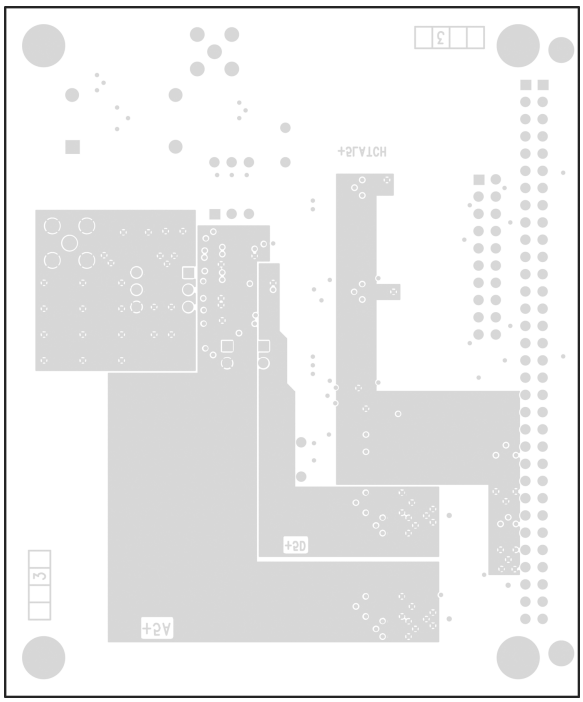
CLC5957PCASM Layer 2

Evaluation Board (Continued)



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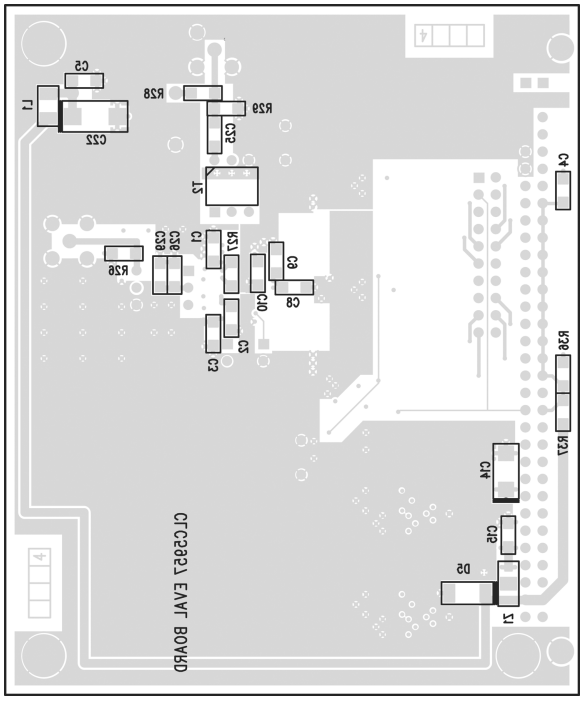
CLC5957PCASM Layer 3



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CLC5957PCASM Layer 4

CLC5957 Applications

Analog Inputs and Bias

Figure 1 depicts the analog input and bias scheme. Each of the differential analog inputs are internally biased to a nominal voltage of 2.40V DC through a 500Ω resistor to a low impedance buffer. This enables a simple interface to a broadband RF transformer with a center-tapped output winding that is decoupled to the analog ground. If the application requires the inputs to be DC coupled, the V_{CM} output can be used to establish the proper common-mode input voltage for the ADC. The V_{CM} voltage reference is generated from an internal bandgap source that is very accurate and stable.

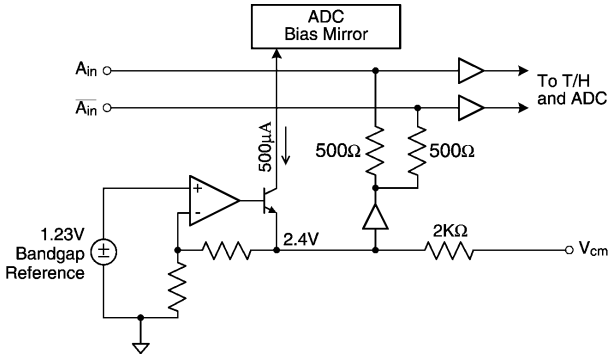


FIGURE 1. CLC5957 Bias Scheme

The V_{CM} output may also be used to power down the ADC. When the V_{CM} pin is pulled above 3.5V, the internal bias mirror is disabled and the total current is reduced to less than 10mA. *Figure 2* depicts how this function can be used. The diode is necessary to prevent the logic gate from altering the ADC bias value.

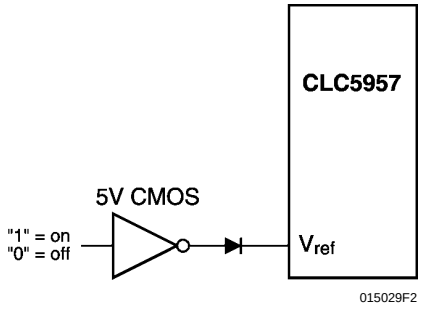


FIGURE 2. Power Shutdown Scheme

ENCODE Clock Inputs

The CLC5957's differential input clock scheme is compatible with all commonly used clock sources. Although small differential and single-ended signals are adequate, for best aperture jitter performance a low noise differential clock with a high slew rate is preferred. As depicted in *Figure 3*, both ENCODE clock inputs are internally biased to $V_{CC}/2$ through a pair of 5kΩ resistors. The clock input buffer operates with any common-mode voltage between the supply and ground.

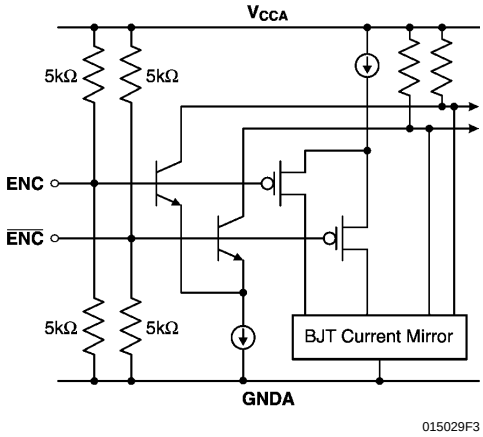


FIGURE 3. CLC5957 ENCODE Clock Inputs

The internal bias resistors simplify the clock interface to another center-tapped transformer as depicted in *Figure 4*. A low phase noise, RF synthesizer of moderate amplitude ($1 - 4V_{PP}$) can drive the ADC through this interface.

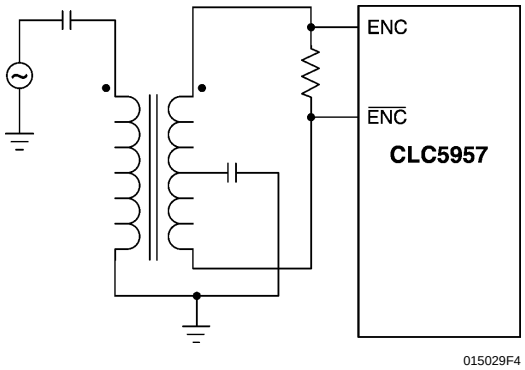


FIGURE 4. Transformer Coupled Clock Scheme

Figure 5 shows the clock interface scheme for square wave clock sources.

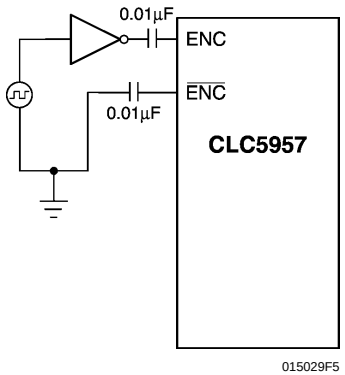


FIGURE 5. TTL, 3V CMOS or 5V CMOS Clock Scheme

CLC5957 Applications (Continued)

Digital Outputs and Level Select

Figure 6 depicts the digital output buffer and bias used in the CLC5957. Although each of the twelve output bits uses a controlled current buffer to limit supply transients, it is recommended that parasitic loading of the outputs is minimized. Because these output transients are harmonically related to the analog input signal, excessive loading will degrade ADC performance at some frequencies.

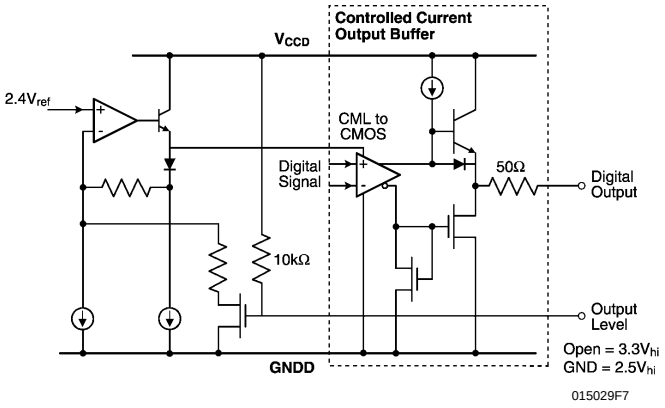


FIGURE 6. CLC5957 Digital Outputs

The logic high level is slaved to the internal 2.4V reference. The OUTLEV control pin selects either a 3.3V or 2.5V logic high level. An internal pull up resistor selects the 3.3V level as the default when the OUTLEV pin is left open. Grounding the OUTLEV pin selects the 2.5V logic high level.

To ease user interface to subsequent digital circuitry, the CLC5957 has a data valid clock output (DAV). In order to match delays over IC processing variables, this digital output also uses the same output buffer as the data bits. The DAV clock output is simply a delayed version of the ENCODE input clock. Since the ADC output data change is slaved to the falling edge of the ENCODE clock, the rising DAV clock edge occurs near the center of the data valid window (or eye) regardless of the sampling frequency.

Minimum Conversion Rate

This ADC is optimized for high-speed operation. The internal bipolar track and hold circuits will cause droop errors at low sample rates. The point at which these errors cause a degradation of performance is listed on the specification page as the minimum conversion rate. If a lower sample rate is desired, the ADC should be clocked at a higher rate, and the output data should be decimated. For example, to obtain a 10MSPS output, the ADC should be clocked at 20MHZ, and every other output sample should be used. No significant power savings occurs at lower sample rates, since most of the power is used in analog circuits rather than digital circuits.

CLC5957 Evaluation Board

Description

The Evaluation board for the CLC5957 allows for easy test and evaluation of the product. The part may be ordered with all components loaded and tested. The order number is the CLC5957PCASM. The user supplies an analog input signal, encode signal and power to the board and is able to take latched 12-bit digital data out of the board.

ENCODE Input (ENC)

The ENCODE input is an SMA connector with a termination of 50Ω. The encode signal is converted to an AC coupled, differential clock signal centered between V_{CC} and ground. The user should supply a sinusoidal or square wave signal of $> 200mV_{PP}$ and $< 4\ V_{PP}$ with a 50% duty cycle. The duty cycle can vary from 50% if the minimum clock pulse width times are observed. A low jitter source will be required for IF-sampled analog input signals to maintain best performance.

CLC5957 Clock Option

The CLC5957 evaluation board is configured for use with an optional crystal clock oscillator source. The component Y1 may be loaded with a 'Full-sized', HCMOS type, crystal oscillator.

Analog Input (AIN)

The analog input is an SMA connector with a 50Ω termination. The signal is converted from single to differential by a transformer with a 5 to 260MHz bandwidth and approximately one dB loss. Full scale is approximately 11dBm or $2.2V_{PP}$. It is recommended that the source for the analog input signal be low jitter, low noise and low distortion to allow for proper test and evaluation of the CLC5957.

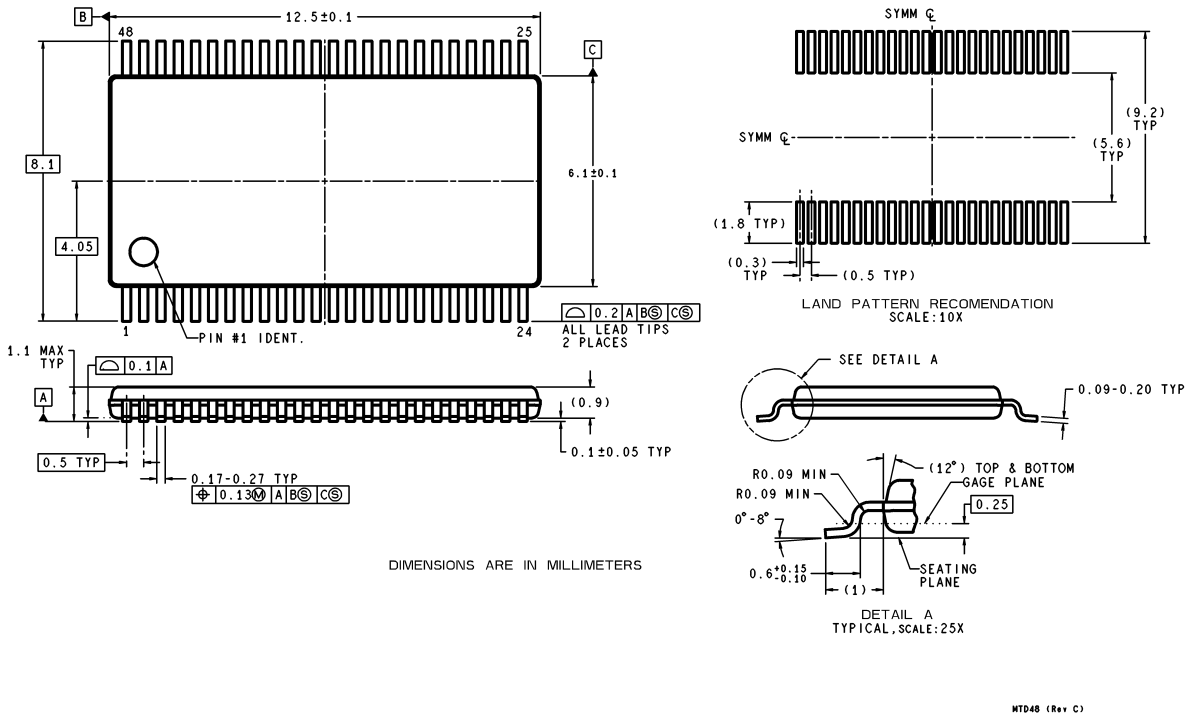
Supply voltages (J1 pins 31 A&B and 32 A&B)

The CLC5957PCASM is powered from a single 5V supply connected from the referenced pins on the Eurocard connector. The recommended supplies are low noise linear supplies.

Digital Outputs (J1 pins 7B ($\overline{\text{MSB}}$, $\overline{\text{D11}}$) through 18B (LSB) and 20B (Data Valid))

The digital outputs are provided on the Eurocard connector. The outputs are buffered by 5V CMOS latches with 50Ω series output resistors. The rising edge of Data Valid may be used to clock the output data into data collection cards or logic analyzers. The board has a location for the HP 01650-63203 termination adapter for HP 16500 logic analyzers to simplify connection to the analyzer.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead TSSOP (Millimeters Only)
Order Number CLC5957MTD
NS Package Number MTD48

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