Product Change Notification - SYST-11ALNE662

Date:

12 Feb 2020

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:

Notification subject:

ERRATA - dsPIC33CH512MP508 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-11ALNE662

Microchip has released a new Product Documents for the dsPIC33CH512MP508 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33CH512MP508 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added silicon issue 21 (I2C).
Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 12 Feb 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

dsPIC33CH512MP508 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.
If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

DSPIC33CH256MP205-E/M4
DSPIC33CH256MP205-E/PT
DSPIC33CH256MP205-H/M4
DSPIC33CH256MP205-H/PT
DSPIC33CH256MP205-I/M4
DSPIC33CH256MP205-I/PT
DSPIC33CH256MP205T-E/M4
DSPIC33CH256MP205T-E/PT
DSPIC33CH256MP205T-I/M4
DSPIC33CH256MP205T-I/PT
DSPIC33CH256MP206-E/MR
DSPIC33CH256MP206-E/PT
DSPIC33CH256MP206-E/PTVAO
DSPIC33CH256MP206-H/MR
DSPIC33CH256MP206-H/PT
DSPIC33CH256MP206-I/MR
DSPIC33CH256MP206-I/PT
DSPIC33CH256MP206T-E/MR
DSPIC33CH256MP206T-E/PT
DSPIC33CH256MP206T-E/PTV01
DSPIC33CH256MP206T-I/MR
DSPIC33CH256MP206T-I/PT
DSPIC33CH256MP208-E/PT
DSPIC33CH256MP208-H/PT
DSPIC33CH256MP208-I/PT
DSPIC33CH256MP208T-E/PT
DSPIC33CH256MP208T-I/PT
DSPIC33CH256MP505-E/M4
DSPIC33CH256MP505-E/PT
DSPIC33CH256MP505-H/M4
DSPIC33CH256MP505-H/PT
DSPIC33CH256MP505-I/M4
DSPIC33CH256MP505-I/PT
DSPIC33CH256MP505T-E/M4
DSPIC33CH256MP505T-E/PT
DSPIC33CH256MP505T-I/M4
DSPIC33CH256MP505T-I/PT
DSPIC33CH256MP506-E/MR
DSPIC33CH256MP506-E/PT
DSPIC33CH256MP506-H/MR
DSPIC33CH256MP506-H/PT
DSPIC33CH256MP506-I/MR
DSPIC33CH256MP506-I/PT
DSPIC33CH256MP506T-E/MR
DSPIC33CH256MP506T-E/PT
DSPIC33CH256MP506T-I/MR

DSPIC33CH256MP506T-I/PT
DSPIC33CH256MP508-E/PT
DSPIC33CH256MP508-E/PTVAO
DSPIC33CH256MP508-H/PT
DSPIC33CH256MP508-I/PT
DSPIC33CH256MP508T-E/PT
DSPIC33CH256MP508T-E/PTVAO
DSPIC33CH256MP508T-I/PT
DSPIC33CH512MP205-E/M4
DSPIC33CH512MP205-E/PT
DSPIC33CH512MP205-H/M4
DSPIC33CH512MP205-H/PT
DSPIC33CH512MP205-I/M4
DSPIC33CH512MP205-I/PT
DSPIC33CH512MP205T-E/M4
DSPIC33CH512MP205T-E/PT
DSPIC33CH512MP205T-I/M4
DSPIC33CH512MP205T-I/PT
DSPIC33CH512MP206-E/MR
DSPIC33CH512MP206-E/PT
DSPIC33CH512MP206-H/MR
DSPIC33CH512MP206-H/PT
DSPIC33CH512MP206-I/MR
DSPIC33CH512MP206-I/PT
DSPIC33CH512MP206T-E/MR
DSPIC33CH512MP206T-E/PT
DSPIC33CH512MP206T-I/MR
DSPIC33CH512MP206T-I/PT
DSPIC33CH512MP208-E/PT
DSPIC33CH512MP208-H/PT
DSPIC33CH512MP208-I/PT
DSPIC33CH512MP208T-E/PT
DSPIC33CH512MP208T-I/PT
DSPIC33CH512MP505-E/M4
DSPIC33CH512MP505-E/PT
DSPIC33CH512MP505-H/M4
DSPIC33CH512MP505-H/PT
DSPIC33CH512MP505-I/M4
DSPIC33CH512MP505-I/PT
DSPIC33CH512MP505T-E/M4
DSPIC33CH512MP505T-E/PT
DSPIC33CH512MP505T-I/M4
DSPIC33CH512MP505T-I/PT
DSPIC33CH512MP506-E/MR
DSPIC33CH512MP506-E/MRC01
DSPIC33CH512MP506-E/PT
DSPIC33CH512MP506-H/MR
DSPIC33CH512MP506-H/PT
DSPIC33CH512MP506-I/MR

DSPIC33CH512MP506-I/PT
DSPIC33CH512MP506T-E/MR
DSPIC33CH512MP506T-E/PT
DSPIC33CH512MP506T-I/MR
DSPIC33CH512MP506T-I/PT
DSPIC33CH512MP508-E/PT
DSPIC33CH512MP508-E/PTC01
DSPIC33CH512MP508-E/PTVAO
DSPIC33CH512MP508-H/PT
DSPIC33CH512MP508-I/PT
DSPIC33CH512MP508T-E/PT
DSPIC33CH512MP508T-E/PTVAO
DSPIC33CH512MP508T-I/PT

dsPIC33CH512MP508

dsPIC33CH512MP508 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CH512MP508 family devices that you have received conform functionally to the current Device Data Sheet (DS70005371**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CH512MP508 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on Page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CH512MP508 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision
		A0
Devices with CAN FD		
dsPIC33CH256MP505	0x7D42	0x0000
dsPIC33CH512MP505	0x7D52	
dsPIC33CH256MP506	0x7D43	
dsPIC33CH512MP506	0x7D53	
dsPIC33CH256MP508	0x7D44	
dsPIC33CH512MP508	0x7D54	
Devices with No CAN FD		
dsPIC33CH256MP205	0x7D02	0x0000
dsPIC33CH512MP205	0x7D12	
dsPIC33CH256MP206	0x7D03	
dsPIC33CH512MP206	0x7D13	
dsPIC33CH256MP208	0x7D04	
dsPIC33CH512MP208	0x7D14	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A0
I²C	Interrupt	1.	In Slave mode, incorrect interrupt generated with DHEN = 1.	X
I²C	Error	2.	False bus collision error generated.	X
I²C	Idle	3.	SFRs are reset in Idle mode.	X
I²C	SMBus 3.0	4.	When Configuration bit, SMBEN (FDEVOPT<10>) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X
Oscillator	HS, XT	5.	The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early.	X
UART	FERR	6.	The FERR bit will not get set if one Stop bit is received.	X
UART	OERR	7.	The 9th byte received will not be available to be read.	X
UART	TXWRE	8.	TXWRE bit (UxSTAH<7>) cannot be cleared once it gets set.	X
UART	Address Detect	9.	When writing to UxP1 with UTXBRK = 1, content of P1 will not get transmitted.	X
UART	Address Detect	10.	In Address Detect mode, content of P1 is not transmitted on writing to P1 with UTXBRK = 1.	X
UART	Sleep	11.	When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.	X
UART	Smart Card	12.	Wait time interrupt flag is set when the last character transmitted has the bit, LAST = 0.	X
MBIST	MBISTDONE	13.	After executing a Reset, the MBISTDONE bit will always be set.	X
CPU	FLIM Instruction	14.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X
CPU	MAXAB/MINAB Instructions	15.	When the operands are of different signs, the MAXAB, MINAB and MINZAB instructions may not output the correct value.	X
CPU	div.sd Instruction	16.	When using the signed 32-by-16-bit division instruction, div.sd, the Overflow bit is not getting set when an overflow occurs.	X
SCCP/ MCCP	Clock Source	17.	Using FOSC as the clock source may cause synchronization issues.	X
I/O	POR	18.	Spike on I/O at POR.	X
DMA	ADC Triggers	19.	DMA is triggered continuously from ADC.	X
PWM	Time Base Capture	20.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X
I²C	I²C	21.	All instances of I²C may exhibit errors and should not be used.	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: I²C

In Slave mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Slave interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Slave interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0							
X							

2. Module: I²C

In Slave mode, a false bus collision event is generated when the bus collision is enabled (SBCDE = 1) and a Stop bit is received.

Work around

None.

Affected Silicon Revisions

A0							
X							

3. Module: I²C

In Slave mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0							
X							

4. Module: I²C

When selecting SMBus 3.0 operation using Configuration bit, SMBEN (FDEVOPT<10>), the Voltage Input High (V_{IH}) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

Affected Silicon Revisions

A0							
X							

5. Module: Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Then switch to the POSC source.

Affected Silicon Revisions

A0							
X							

6. Module: UART

When the UART is operating with STSEL<1:0> = 2 (two Stop bits sent, two checked at receive) and STPMD = 0, the FERR bit will not get set if one Stop bit is received.

Work around

Use STPSEL = 3 instead of STSEL = 2. When operating with STSEL = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

A0							
X							

7. Module: UART

When the receive buffer overflows, the 9th byte received will get lost and cannot be read.

Work around

Do not allow the OERR bit to get set by reading the received data byte on each byte reception.

Affected Silicon Revisions

A0							
X							

8. Module: UART

Once the TX Write Transmit Error Status bit (TXWRE, UxSTAH<7>) gets set, the TXWRE bit cannot be cleared by a single clear instruction.

Work around

Use multiple clear instructions in a loop until the TXWRE bit gets cleared.

Affected Silicon Revisions

A0							
X							

9. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

A0							
X							

10. Module: UART

In Address Detect mode, the content of P1 is not transmitted on writing to P1 with UTXBRK = 1.

Work around

Write P1 a second time after waiting for the Break transmission to start.

Affected Silicon Revisions

A0							
X							

11. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

A0							
X							

12. Module: UART

In Smart Card T = 1 mode, the Wait time interrupt flag is set when the last character transmitted has the bit, LAST = 0.

Work around

Ignore WTC interrupt events on non-last bytes.

Affected Silicon Revisions

A0							
X							

13. Module: MBIST

After a Reset, the MBISTDONE status bit will be set regardless of a BIST test being executed. If a BIST is requested and executed, the MBISTDONE bit will set as expected.

Work around

None.

Affected Silicon Revisions

A0							
X							

14. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

A0							
X							

15. Module: CPU

When operating on signed operands of different sign values, the output for MAXAB, MINAB and MINZAB instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

A0							
X							

16. Module: CPU

When using the Signed 32-by-16-Bit Division instruction, div.sd, the Overflow bit may not always get set when an overflow occurs. This erratum only affects operations in which at least one of the following conditions is true:

- Dividend and divisor differ in sign,
- Dividend > 0x3FFFFFFF or
- Dividend < 0xC0000000

Work around

The application software must perform both the following actions to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.

b) If the dividend and divisor differ in sign (e.g., dividend is negative and divisor is positive), then after executing the div.sd instruction or the compiler built-in function, __builtin_divsd(), inspect the sign of the resultant quotient. If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

A0							
X							

17. Module: SCCP/MCCP

When FOSC is selected as the clock source using the CLKSEL<2:0> bits (CCPxCON1L<10:8>), unexpected operation may occur. For proper SCCP/MCCP input clock synchronization, do not use FOSC as the CCP clock source.

Work around

Use any of the other available clock sources in CLKSEL<2:0>.

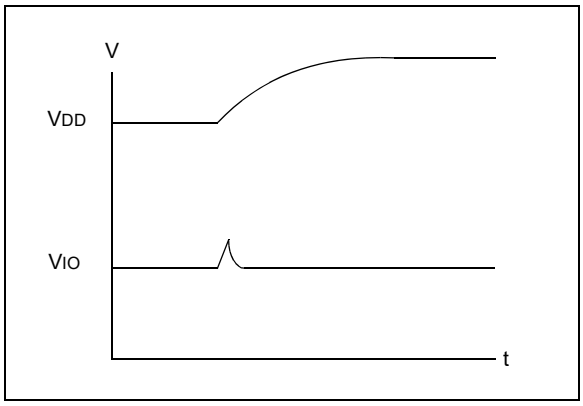
Affected Silicon Revisions

A0							
X							

18. Module: I/O

During a fast device power-up, when the VDD ramp is less than 4 mS, the I/O pins may drive up to 100 µA current for a duration of up to 10 µS (Figure 1-1).

FIGURE 1-1: I/O RAMP



Work around

1. Slow down the VDD ramp time (greater than 4 mS for VDD to ramp 0V to 3.3V).
2. Ensure the circuitry that is connected to the pins can endure this pulse.

   Example applications affected may include complementary power switches, where a transient current shoot-through might occur. High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® device to avoid the current shoot-through. This behavior is specific to each device and not affected by aging.

Affected Silicon Revisions

A0							
X							

19. Module: DMA

The DMA receives multiple continuous triggers from the ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

A0							
X							

20. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status Flag, CAP, will not set again.

Work around

Read the PWM Generator x Capture (PGxCAP) register as soon as possible to avoid the condition. Poll the CAP bit and read the PGxCAP value within the associated PWM Generator (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event which triggered the time base capture.

Affected Silicon Revisions

A0							
X							

21. Module: I²C

All instances of I²C/SMBus may exhibit errors and should not be used. When operating I²C/SMBus in a noisy environment, the I²C module may exhibit various errors. These errors may include, but are not limited to, corrupted data, unintended interrupts or the I²C bus getting hung up due to injected noise. Examples of system noise include, but are not limited to, PWM outputs or other pins toggled at high speed adjacent to the I²C pins. Both Master and Slave I²C/SMBus modes may exhibit this issue.

Work around

If I²C is required, use a software I²C implementation. An example I²C software library is available from Microchip:

www.microchip.com/dsPIC33C_I2C_SoftwareLibrary

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005371**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2018)

Initial version of this document; issued for revision A0.

Rev B Document (7/2019)

Removes original silicon errata issues 6 (PWM) and 18 (CPU). The issues are no longer relevant and were removed.

Updates silicon errata issue 18 (I/O)

Adds silicon errata issues 19 (DMA) and 20 (PWM).

Rev C Document (9/2019)

Updates device data sheet reference to the current revision D.

Rev D Document (2/2020)

Adds silicon issue 21 (I2C).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-5224-5605-6

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820