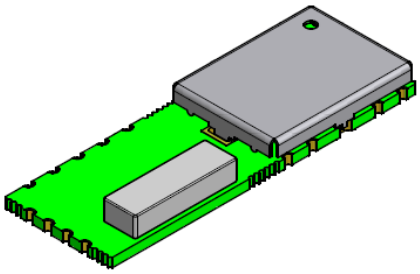

REV 1.2

TECHNICAL DESCRIPTION

Fastrax UC322 OEM GPS Receiver module

This document describes the electrical connectivity, operation and application notes of the Fastrax UC322 OEM GPS receiver module.

February 1, 2008

Fastrax Ltd.

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CHANGE LOG

Rev.	Notes	Date
1.0	Initial document	2007-10-05
1.1	Spelling corrections, PCB rev B: changed GPIO13 to GPIO2, added chapter 6.5, updated protocol configuration Table 3.	2007-12-05
1.2	Added chapter 6.6, suggestion on plastic cover distance to antenna >1mm	2008-02-01

CONTENTS

COMPLEMENTARY READING

The following Fastrax reference documents are complementary reading for this document.

Ref. #	File name	Document name
1	GSC3LTProductInsert.pdf	GSC3LT Brochure
2	NMEA Reference Manual.pdf	NMEA Reference Manual
3	SiRF Binary Protocol Reference Manual.pdf	SiRF Binary Protocol Reference Manual

1. GENERAL DESCRIPTION

The Fastrax UC322 is an OEM GPS receiver module, which uses the state of the art SiRF single chip receiver GSC3LT *(ref 1)* having high navigation sensitivity -159dBm. The UC322 receiver provides low power 90mW and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations.

The module provides complete signal processing from embedded GPS antenna to serial data output in NMEA (or SiRF binary) messages. The embedded antenna has good radiation gain, which leads to solid GPS signal levels. The antenna operation is optimized for 50-110mm ground plane width.

Small module size 10.4x30.0x2.9mm together with surface mount and reflow soldering allows easy and cost effective integration to various applications. Optimum placing of the module is symmetrically at the top edge of the mother board.

The module requires only a single power supply VDD. The UC322 module interfaces to the customer's application via one serial port. Connectivity includes also a control input for Normal/Hibernate operation mode control. Serial data and all I/O signal levels are CMOS 1.8V compatible.

The module is available with two versions:

- SiRF ROM code version
- Early samples are provided with embedded flash version (4Mbit in GSC3LTf), which allows also evaluation with GSWLT3 firmware.

2. SPECIFICATIONS

2.1 General

Table 1 General Specifications

Receiver	GPS L1 C/A-code, SPS
Chip set & Sensitivity	SiRF GSC3LT -159dBm
Channels	20 physical (limited to 12 tracking by firmware)
Update rate	1 Hz default (fix rate configurable)
Supply voltage, VDD	+3.25V…+5.5 V
Supply voltage, VDD ripple max	300mVpp @ f<10kHz & 3mVpp @ f>100kHz
Power consumption, VDD	90 mW typical @ 3.3V
Power consumption, VDD	65 uW typical @ 3.3V (during Hibernate state)
Operating temperature range	-30ºC…+85ºC (1)
Serial port protocol (default)	NMEA 3.01 (switchable to SiRF binary)
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	4800 baud (configurable)
I/O signal levels	CMOS VCC=1.8V compatible: low state 0.0…0.25xVCC; high state 0.75…1.0xVCC
I/O sink/source capability	+/- 2 mA max.
Embedded antenna gain	2.8dBi (linear pol.) @ 80mm ground plane width
PPS output accuracy	+/- 1us

Note (1): Operation at the temperature range -40…+85C is accepted but the TTFF and other GPS performance may degrade.

2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	300	mW
Supply voltage, VDD	-0.3	+5.5	V
Voltage on any input connection	-0.3	+2.1V	V
RF input level	-	+15	dBm

3. OPERATION

3.1 Operating modes

After power up the receiver boots from the internal flash memory for normal operation. Modes of operation:

- Normal (Navigation) mode
    - Power management system modes
- Hibernate mode
- Programming mode

3.2 Normal mode

The UC322 receiver will start navigation automatically after power up. The power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as *Full Power* or *ON* state.

Navigation is available and any configuration settings are valid as long as the VDD power supply is active. When the VDD is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.

3.2.1 Output configuration

With ROM code version user can select the data output configuration by setting the GPIO 6 and 2 control inputs, which are read at power up according to the following table. Configuration is selected by setting GPIO 6 and 2 to low or high state at power up.

Table 3 Output configurations (GSWLT3.2.5, subject to change)

Configuration	1	2	3
GPIO6 input	low	high	low
GPIO2 input	low	low	high
Protocol	NMEA 3.01	SiRF binary	NMEA 3.01
Baud	4800,n,8,1	57600,n,8,1	57600,n,8,1
NMEA messages @1Hz	GGA, GSA, GSV@5s, RMC, VTG	-	GGA, GSA, GSV, RMC, VTG, (EE)
Binary messages @1Hz	-	2, 4, 9, 13, 18, 41, (EE)	-
GPIO1 output, no navigation	high	high	high
GPIO1 output, navigation	100ms high @ 1Hz	100ms high @ 1Hz	100ms high @ 1Hz
DGPS/SBAS	Disabled	Enabled	Enabled
Static Navigation filter	Disabled	Disabled	Enabled
Track Smoothing filter	Enabled	Enabled	Enabled
Internal DR	Disabled	Disabled	Enabled
Extended Ephemeris	Disabled	Enabled	Enabled

3.3 Power management system states

The receiver supports also SiRF operating modes for reduced average power consumption (*ref 3*) like Adaptive TricklePower™ and Push-to-Fix™ modes:

1. *Adaptive TricklePower:* In this mode the receiver stays at Full Power for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in a low power mode

to reduce power drain. TricklePower mode is configurable with SiRF binary protocol message ID151 (*ref 3*). The receiver stays once in while in Full Power automatically to collect new ephemeris and almanac data from rising satellites.

2. *Push-to-Fix*: In this mode the receiver is configured to wake up periodically, typically every 1800 sec, to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in the Hibernate mode (current drain 20uA typ.). The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >62us) after which the receiver performs Hot start and a valid fix is available within few seconds. This mode is configurable with SiRF binary protocol message ID151 (*ref 3*).

Note that position accuracy is somewhat degraded in power management modes when compared to full power operation.

3.4 Hibernate mode

Hibernate (also referenced as OFF) mode means a low quiescent power state where only the internal non-volatile RTC and RAM block is powered on. Current drain is only 20uA typ. The main supply input VDD is kept active all the time, even during Hibernate mode. The Hibernate mode is entered by host interrupt at ON_OFF control input (pulse low-high-low >62us).

The receiver wakes up from Hibernate mode and returns to Normal mode after next ON_OFF interrupt (pulse low-high-low >62us) allowing fast TTFF with either Hot or Warm start.

3.5 Programming mode

Programming mode is only available with the flash version (GSC3LTf) with the embedded 4Mbit flash memory. The ROM code version does not support programming.

Programming via HW-booting mode is utilized by forcing the BOOT control input for high state (Flash programming, Table 3) during power up. Now the GPS module boots for the UART and waits for the boot loader commands from the host (an application running on the host, SiRFFlash). It is suggested that all applications using embedded flash version should support the HW-booting by access to UART (TXA & RXA) and BOOT input signal and VDD supply On/Off control.

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to

the host without any transferring utilities that may cause failure during speed change.

Table 4 BOOT modes

BOOT mode	**BOOT** input (CMOS 1.8V)
Normal mode (Flash)	0
Flash programming (UART)	1

3.6 Procedure for re-programming the flash firmware

1. Connect UART (RXA and TXA signals) to PC via RS232 converter.

2. Set the module to UART boot mode: Power up the module to Flash programming mode according to table 4 (BOOT input high state, VCC = 1.8V). When using iTrax Evaluation kit power up the kit and toggle Prog/Reset switch to Prog position.

3. Start SiRFFlash application on PC.

4. Browse for the flash *.s file.

5. Check the Communication setting from the SiRFFlash to meet your PC serial port.

6. Press Execute at SiRFFlash. Now the flashing starts.

7. After flashing has finished, recover normal operation by toggling power VDD off-on and setting boot mode to Normal mode according to Table 4 (BOOT low state).

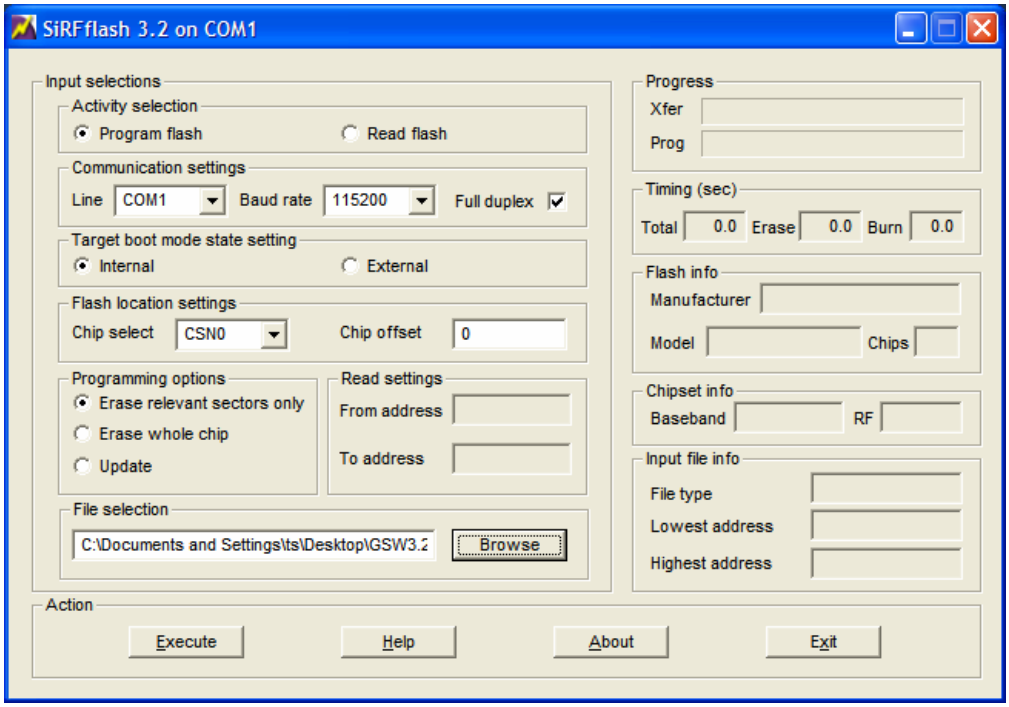

Figure 1 SiRFFlash utility settings

4. CONNECTIVITY

4.1 Connection assignments

For pin out numbering see end of this chapter.

Table 5 Connections

Contact	Signal	I/O	Signal description
1	VDD	I	Power supply input +3.25… +5.5V. Note ripple voltage spec.
2	GPIO2	I	Protocol configuration input. Pull low for default configuration. See table 3. CMOS 1.8V compatible.
3	GPIO1	O	Valid fix indicator output. CMOS 1.8V compatible.
4	1PPS	O	1 Pulse per second (1us length) output. CMOS 1.8V compatible. Can be left unconnected if not used.
5	GND	-	Ground. Connect to ground plane.
6	RXA	I	UART Port A async. input. Internal pull-up 100k resistor. CMOS 1.8V compatible. Can be left unconnected if not used.
7	TXA	O	UART Port A async. output. CMOS 1.8V compatible.
8	BOOT	I	***Flash version:*** Boot control input: 1=UART, 0=Internal flash memory. CMOS 1.8V compatible. Pull low with external pull-down resistor 220ohm… 4.7kohm. ***ROM version:*** Can be left unconnected.
9… 24	GND	-	Ground. Connect to ground plane.
25	ON_OFF	I	ON/OFF input for controlling operation between Normal/Hibernate mode. Pulse >62us, min. interval 1 sec. CMOS 1.8V compatible. Internal pull-down resistor 10kohm. Can be left unconnected if not used.
26	GND	-	Ground. Connect to ground plane.
27	GPIO6	I	Protocol configuration input. Pull low for default configuration. See table 3. CMOS 1.8V compatible.

4.2 Power supply

The UC322 module requires only one power supply VDD. If possible keep the VDD active all the time. When required use ON_OFF input for controlling Normal/Hibernate operation mode in order to keep the internal non-volatile RTC & RAM active for fastest possible TTFF.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typical VDD peak current is 45mA during acquisition. Typical VDD current in low power Hibernate mode is 20uA.

The UC322 allows about 300mVpp ripple voltage at the supply VDD below 10kHz frequency. The VDD ripple voltage should be reduced further below 3mVpp at 100kHz frequency or higher. E.g. if the battery that provides the supply for VDD is connected to a switched mode regulator operating at 100kHz, the resulting voltage ripple shall be reduced below 3mVpp by a suitable by-pass capacitor or by external low pass filter prior VDD supply input.

4.3 UART

The device supports UART communication via serial Port A. With the standard firmware the Port A is configured by default to NMEA protocol. The Port A is used also when the device is booting from the serial port for re-flashing.

I/O levels form the serial ports are CMOS 1.8V compatible, not RS232 compatible. Use an external level translator when needed to interface with 3.3V or RS232 levels.

4.4 Hibernate control input: ON_OFF

The ON_OFF control input can be used to control the receiver between Normal or Hibernate modes and also to generate interrupt in Push-to-Fix operation.

The ON_OFF interrupt is generated by rising edge of a low-high-low pulse, which should be longer than 62us (suggestion is abt. 100ms pulse length). Input level is CMOS 1.8V compatible. Do not generate ON_OFF interrupts less than 1 sec intervals. Especially take care that any multiple switch bounce pulses are filtered out.

After power up the first ON_OFF interrupt sets the module to Hibernate mode. Next ON_OFF interrupt wakes up the module for Normal

(Navigation) operation. Consequent ON_OFF interrupts switch the operation mode between Hibernate and Normal modes.

During Hibernate mode internal I/O supply is internally powered off, thus output levels are at low state and any inputs, excluding ON_OFF input, like UART RXA should be disconnected or forced to low state.

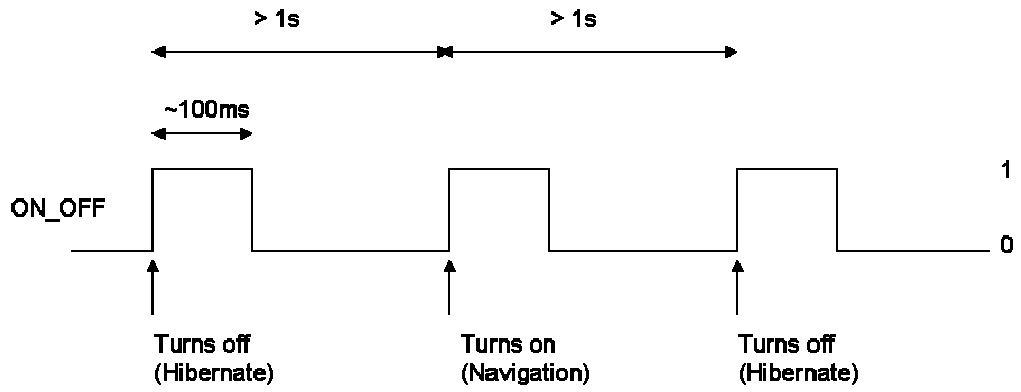

Figure 2 Suggested ON_OFF control input timing diagram.

NOTE

The ON_OFF input has 10kohm pull-down resistor. The ON_OFF input can be left unconnected if not used. Do not generate ON_OFF interrupts less than 1 sec intervals.

4.5 Boot Select input: BOOT

With ROM version the BOOT signal is unconnected and it can be left floating.

With Flash version the boot source is defined using the BOOT pin. After power up or after system reset the value is read and the boot is processed according the Table 4. If not used with flash version, pull BOOT signal to low state with 220… 4k7 resistor.

For re-programming the firmware, the BOOT pin should be kept at high state at least 500 ms during power up. Input level is CMOS 1.8V compatible.

4.6 Timing pulse: PPS

The pulse-per-second (PPS) output provides a pulse signal for timing purposes. Pulse length (high state) is about 1us synchronized to full UTC second. Output level is CMOS 1.8V compatible.

4.7 Valid fix: GPIO1

GPIO1 output can be used as a valid fix indicator. Prior to navigation the output is at high state. During valid navigation the output has 100ms high state pulse at 1Hz rate. Output level is CMOS 1.8V compatible.

4.8 Configuration select: GPIO 6 & 2

The data output configuration is defined using the GPIO 6 and 2 control inputs. After power up the value is read and the configuration is processed according the Table 3 (in previous chapter).

The GPIO 6&2 inputs should be kept valid after power up for at least 500 ms to allow the internal power-on-reset delay to settle. I/O levels are CMOS 1.8V compatible.

4.9 Mechanical outline

Module size is 10.4mm (width) x 30.0mm (length) x 2.9mm (height). General tolerance is ±0.3mm.

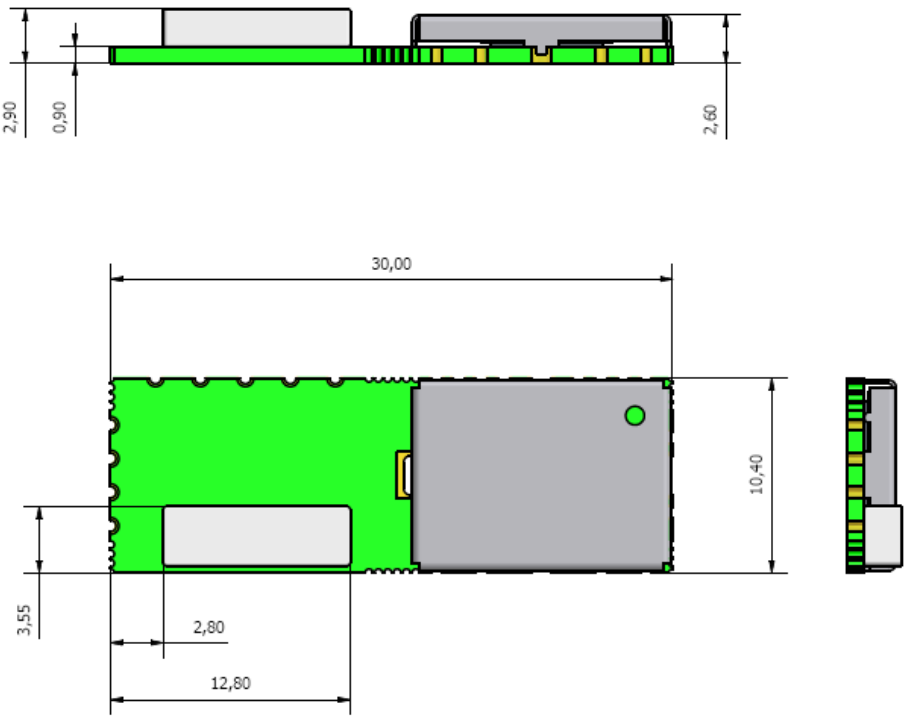

Figure 3 Mechanical outline.

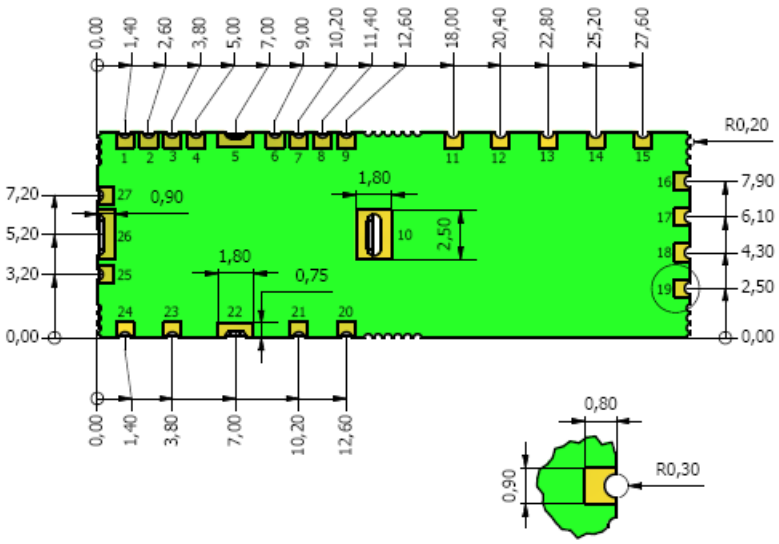

Figure 4 Mechanical outline, bottom side.

4.10 Suggested pad layout and pin numbering

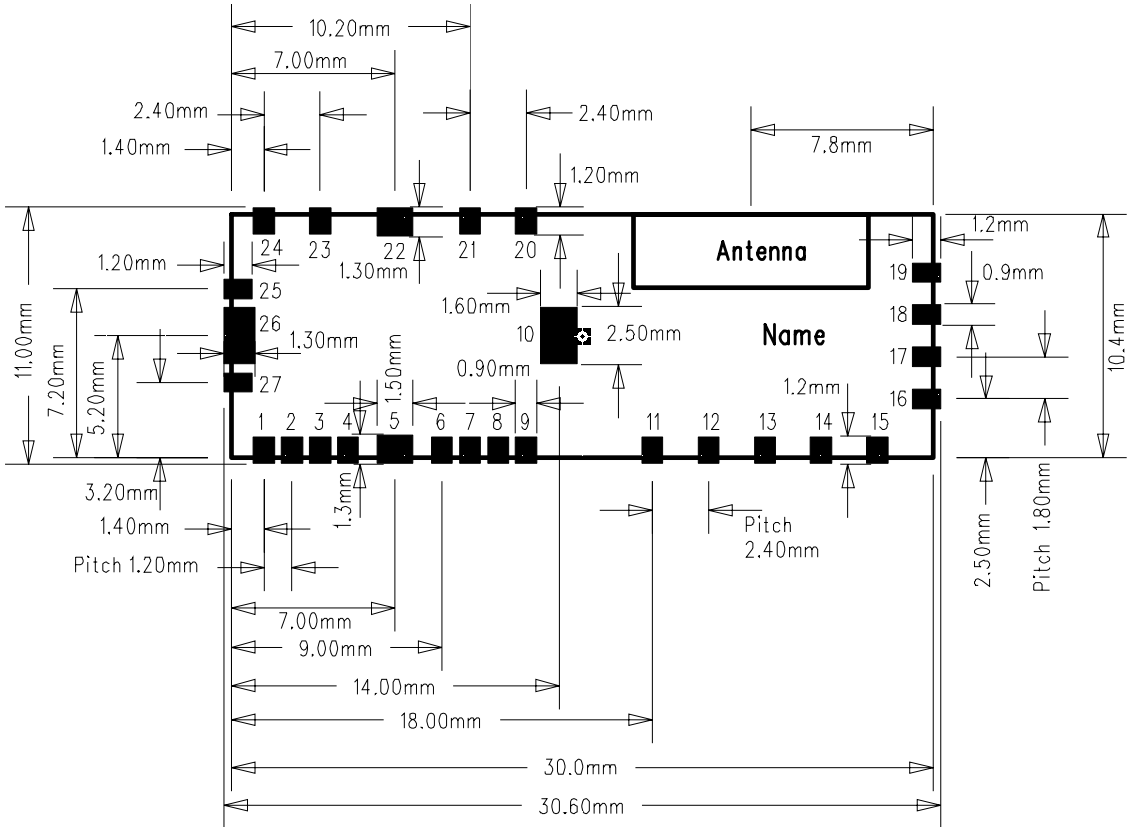

Figure 5 Suggested pad layout and pin numbering, top side.

5. MANUFACTURING

5.1 Assembly and soldering

The UC322 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads. Suggested peak reflow temperature is 250C for ten seconds (Pb-free paste). Absolute max reflow temperature is 260C for ten seconds.

5.2 Moisture sensitivity

Note that the UC322 is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be re-packed or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

5.3 Tape and reel

One reel contains TBD modules.

Picture TBD

Figure 6 Tape and reel specification

6. APPLICATION DESIGN

The intention of the following application design notes is to give guidelines for electrical and layout design of the mother board using the UC322 module.

6.1 Circuit diagram

A suggested circuit diagram for typical application with UC322 ROM version is shown in the picture below.

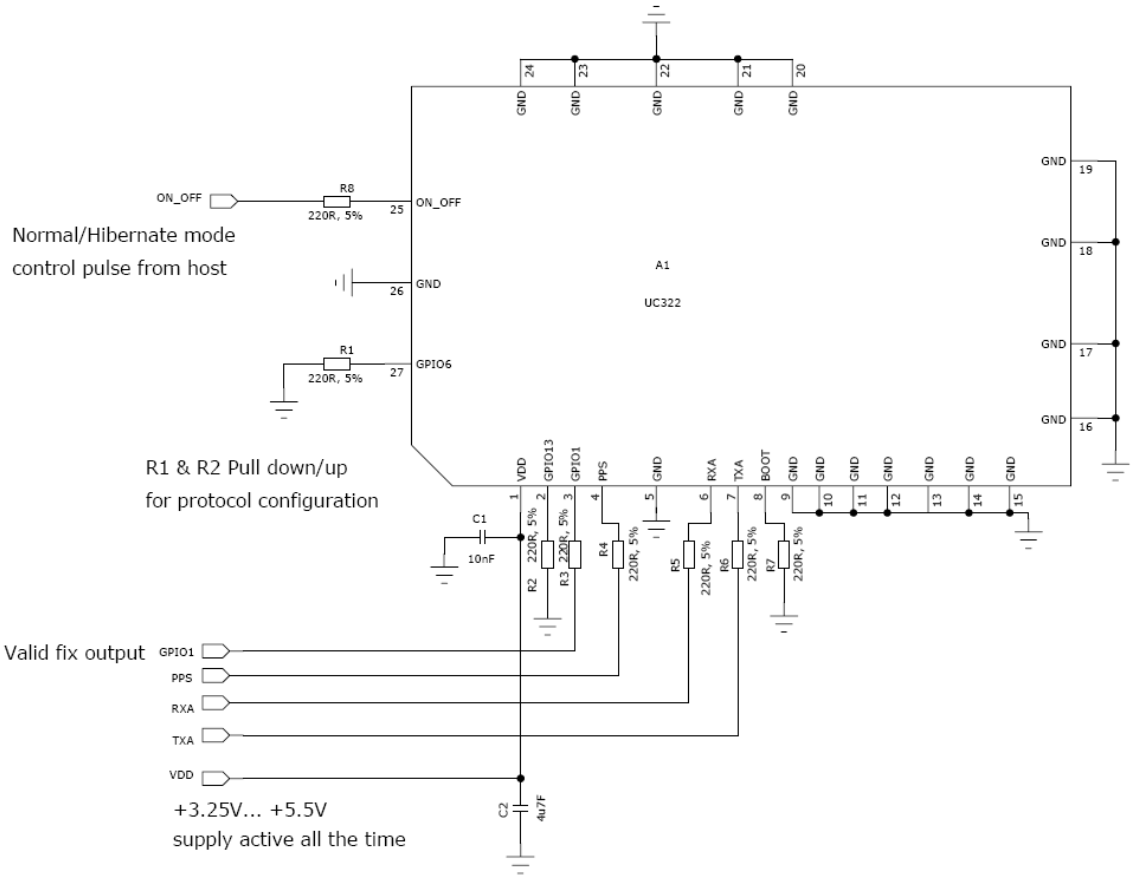

Figure 7 Application circuit diagram

6.2 Power supply

The UC322 allows direct battery supply connection. However take care that VDD ripple voltage does not exceed the VDD ripple re-

quirement. Use an external by-pass capacitor or a low pass filter for VDD supply when required to reduce excessive ripple voltage.

No back up supply is required. Instead keep the VDD supply active all the time and when needed use the ON_OFF control input for Normal/Hibernate mode control.

6.3 Embedded antenna operation

The embedded antenna of the UC322 requires a solid ground plane on the mother board, which plays a necessary part of the antenna radiation.

The UC322 module is intended to be placed horizontally at the top edge of the mother board. Place the module in such orientation where the antenna is closest to the top edge of the mother board. Optimum width for the mother board is 50… 110mm. The height of the mother board is not so critical. Main radiation beam is pointed upwards along the plane of the mother board.

The optimum placement of the module is such that the embedded antenna of the UCC322 is at the center of the top edge of the mother board. Small deviations (< 25% of the board width) from center position are acceptable. With a narrow mother board (width 50… 75mm) the antenna should be placed more closely (+/- 15%) to the center of the top edge.

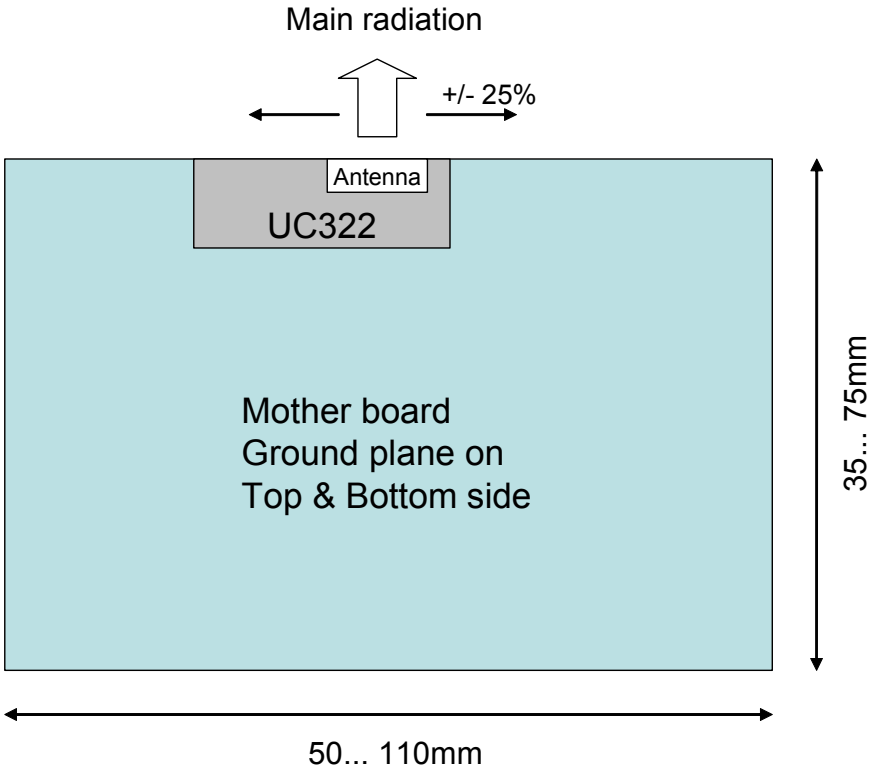

Figure 8 Suggested module location

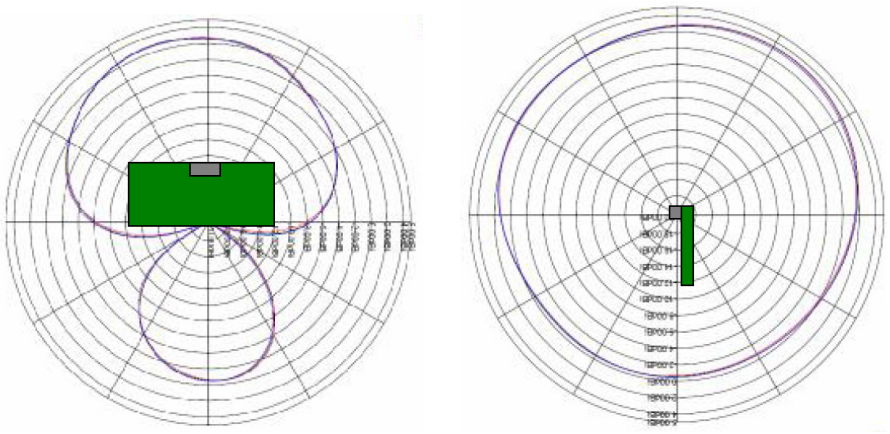

Figure 9 Radiation pattern @ 80mm ground plane width. Amplitude scale 2dB/div.

Avoid placing the antenna at the corner of the mother board. The resonance frequency of the embedded antenna may shift and the radiation efficiency will drop. Do not either place the module vertically or at the bottom side of the board.

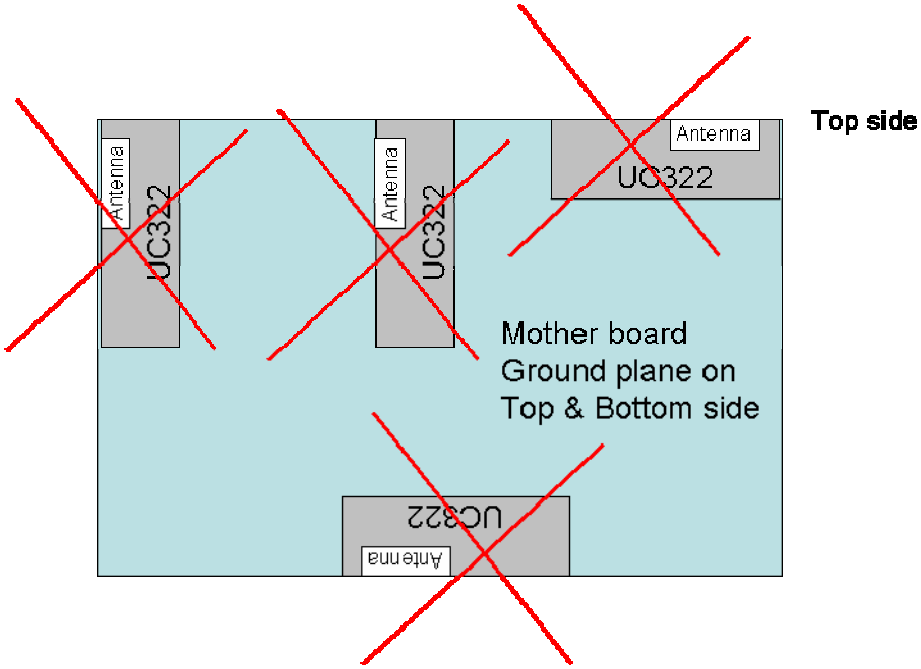

Figure 10 Avoid poor antenna location

6.4 Keep out under the embedded antenna

Use a keep out for copper, trace and via holes under the embedded antenna. Suggested keep out size is 12.8x8.0mm for all layers precisely under the embedded antenna location, see the following picture. Use multiple of GND via holes around the keep out.

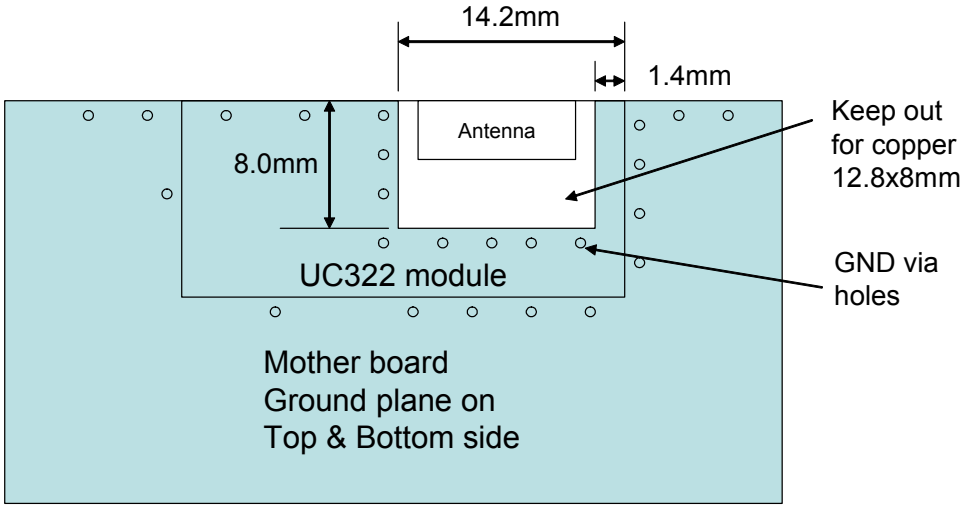

Figure 11 Keep out for copper under embedded antenna

6.5 Placing nearby components or parts

Any parts or components should be placed outside the embedded antenna copper keepout. If several components are placed nearby the UC322 or dense routing is required close to the UC322, it is a good practice to use a metal shield over the components & signal traces.

Note also that any adjacent metal planes like LCD displays or batteries should have 8mm distance to the top of the UC322.

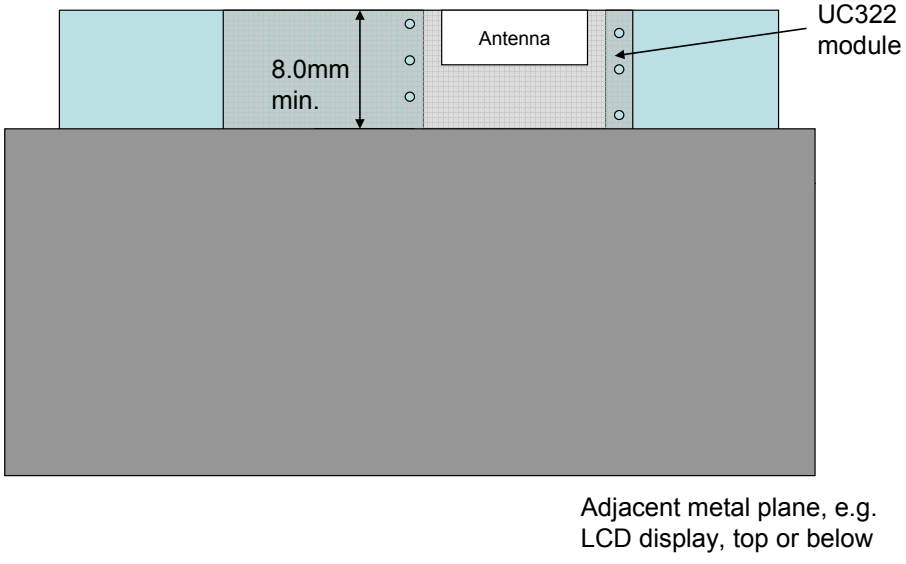

Figure 12 Distance to adjacent metal plane 8mm min.

6.6 Placing plastic cover, antenna side

The near by plastic cover has loading effect, which may shift antenna resonance frequency downwards by -50MHz. In order to avoid the loading effect, suggestion is to keep plastic cover distance to the embedded antenna >1mm. This can be implemented e.g. by making the plastic cover thinner around the embedded antenna location, i.e. making a dugout around the antenna.

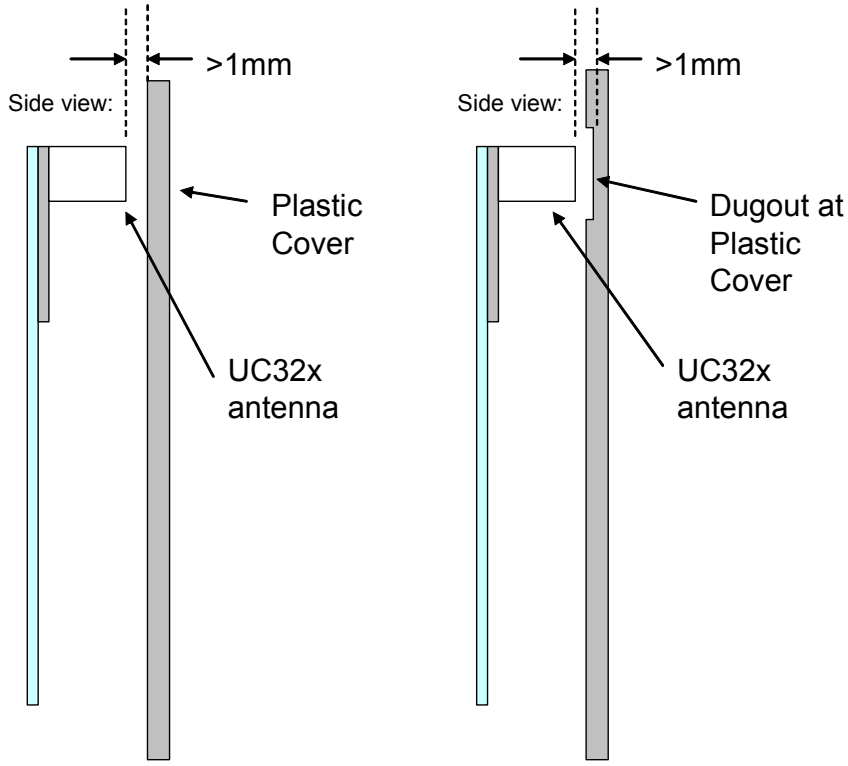

Figure 13 Distance to plastic cover >1mm

6.7 PCB layout issues

The suggested multilayer PCB build up is presented in the following table.

Table 6 Suggested PCB build up

Layer	Description

Top	Ground plane (dense component areas covered with a shield)
2	Signals
N	Signals
N+1	Ground plane
N+2	Power plane for supply nets
Bottom	Ground plane

Routing signals directly under the module should be avoided. This area should be dedicated to ground plane.

The serial resistors at the I/O should be placed very near to the module I/O pad. In this way the risk for the local oscillator leakage is minimized. Route the I/O signals further at inner layers below the ground plane.

The by-pass capacitor C1 at VDD input should be placed very close to the module with short traces to VDD I/O pad and to the ground plane. Place a GND via hole as close as possible to the capacitor. Capacitor C2 can be placed further away. Route the VDD supply net at inner layer below the ground plane.

Connect the GND soldering pads of the module to ground plane with ‘thermals’, i.e. with short traces to ground plane and to GND via holes near by. Use preferably two via holes for each GND pad.

The following pictures give an example of suggested layout rules discussed previously. This simplified example uses 4-layer PCB build up.

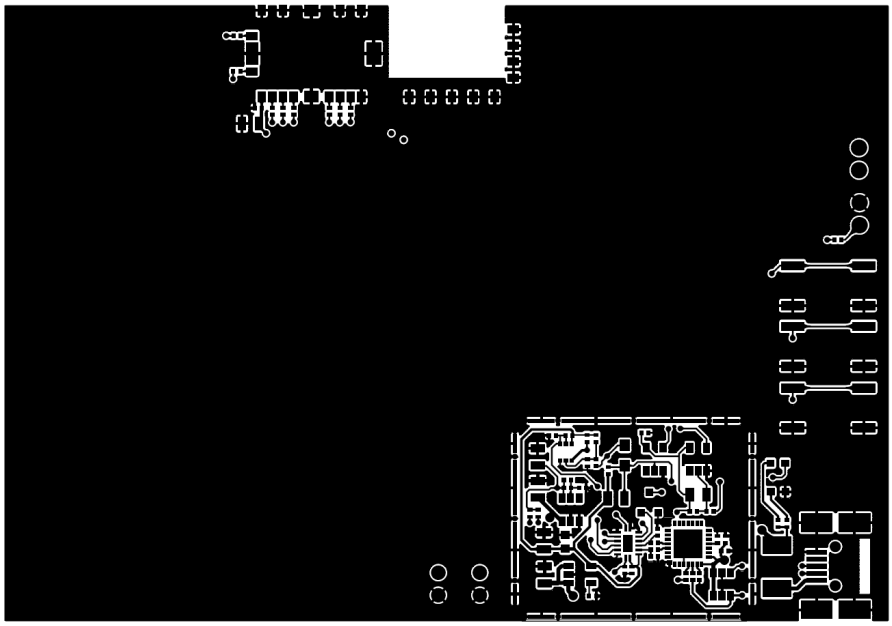

Figure 14 Example of layout, top side.

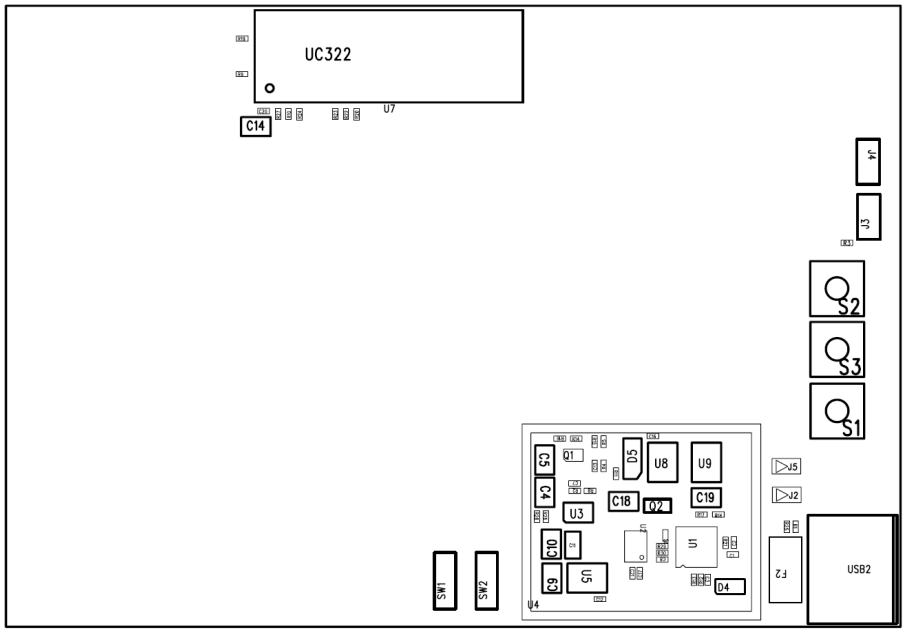

Figure 15 Example of assembly, top side.

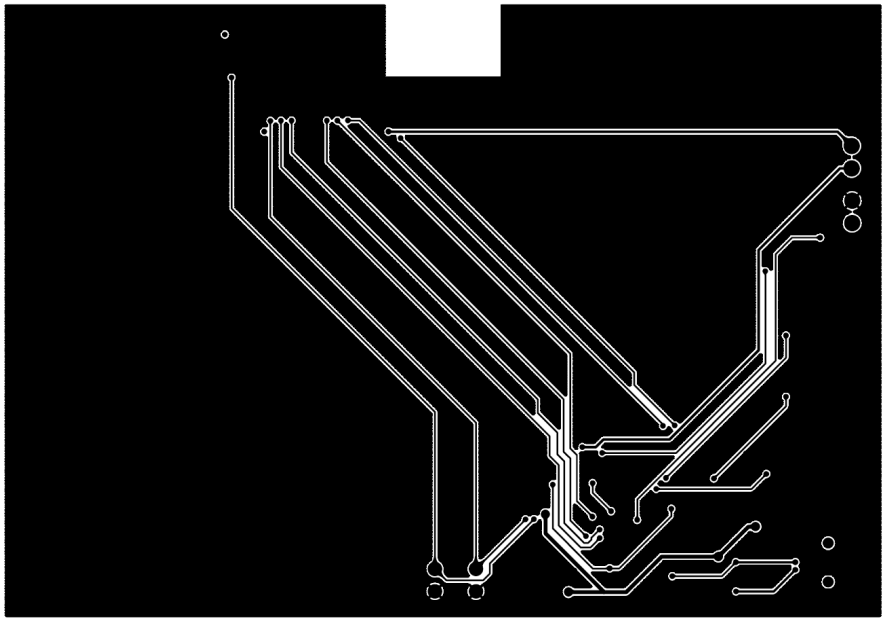

Figure 16 Example of layout, layer 2.

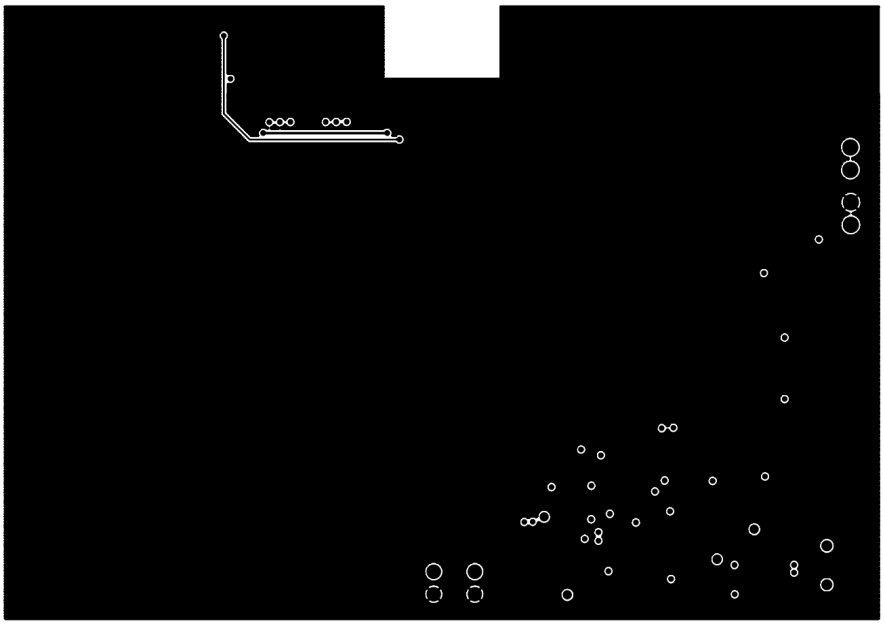

Figure 17 Example of layout, layer 3.

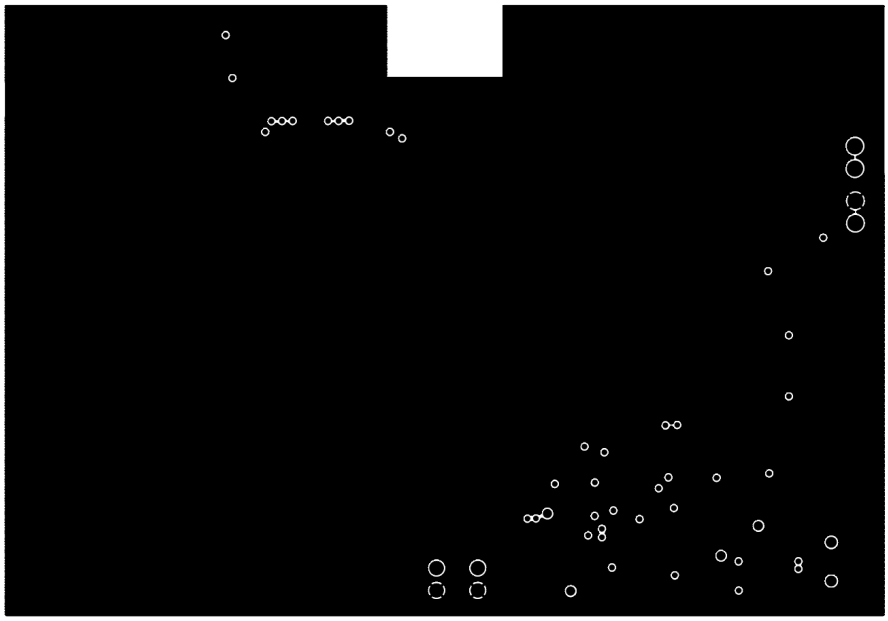

Figure 18 Example of layout, bottom side.

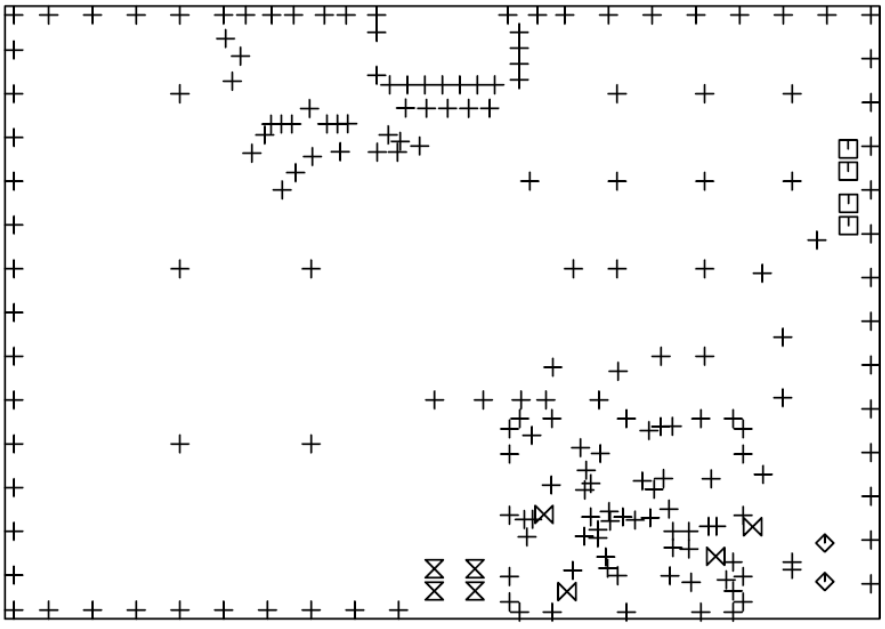

Figure 19 Example of drill drawing, top side. Note multiple GND via holes at the ground plane and at the perimeter of the PCB.

6.8 Other electronics on mother board

Signal traces on top and bottom layers should have minimum length. Route signals mainly at inner layers below the top or bottom ground plane. In this way, a solid RF ground is achieved throughout the circuit board on top and bottom sides. Several via holes should be used to connect the ground areas between different layers.

Areas with dense component placing and dense routing requirements should be covered with a metal shield, which should be connected to ground plane with multiple GND via holes. Small ground plane openings for SMT components (length few mm, like LED or push buttons) in the ground plane are OK without a shield.

Dense areas having multiple via holes may open the ground plane for wide areas, thus blind and buried via holes are suggested to be used when changing layers for internal signals and power planes.

Use a power plane layer dedicated solely for power nets. Use wide trace width or even copper plane areas to achieve low impedance for power nets. Dedicate two layers as ground planes on adjacent layers above and below.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing symmetrical copper content between layers, and adding ground copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

6.9 Avoiding EMI

Since the ground plane of the mother board plays a vital role in the antenna operation, it is essential for good GPS performance that the following measures against EMI are properly implemented:

- High speed electronics like CPU & memory bus are enclosed in a ‘Faraday shield’. The enclosure is formed by the ground planes on PCB + metal shield. Route signals at inner layers as discussed previously. Use a power plane layer for supply nets.

- Any signal that is routed outside the Faraday shield is protected against EMI noise on 1575MHz with a serial RF filter like

- a serial resistor (> 220ohm, suitable for I/O with low current) or
- with a dedicated EMI filter (or ferrite bead) suitable for higher current or
- with suitable by-pass capacitor e.g. 18pF (low impedance due to series resonance at 1575MHz).

The following picture gives a suggestion for e.g. a 6-layer PCB build up, which forms a Faraday shield together with ground planes on PCB and with the shield over high speed electronics. Buried and blind via holes are used to keep EMI signal inside ground planes. I/O signals that are routed outside the Faraday enclosure are filtered with a suitable EMI filter. Power plane layer is used for supply nets with low impedance traces/planes.

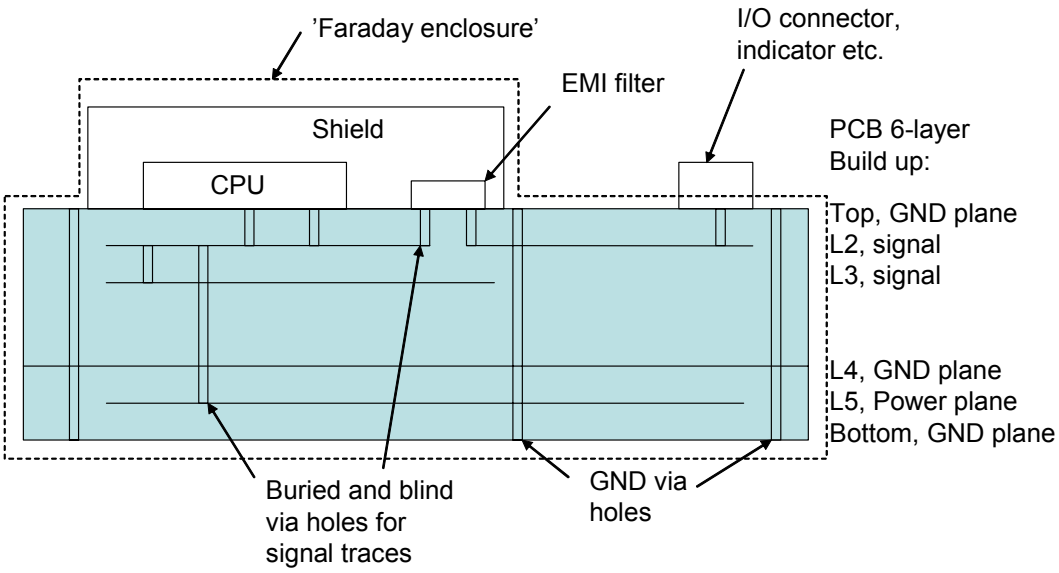

Figure 20 Avoiding EMI with Faraday enclosure, e.g. 6-layer PCB