

# DALLAS

SEMICONDUCTOR

## DS2401

Silicon Serial Number

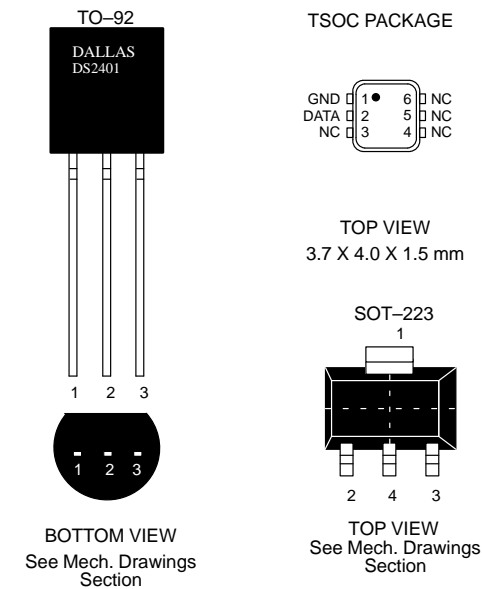
### FEATURES

- Upgrade and drop-in replacement for DS2400
  - Extended 2.8 to 6.0 voltage range
  - Multiple DS2401s can reside on a common 1-Wire™ bus
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester); guaranteed no two parts alike
- Built-in multidrop controller ensures compatibility with other MicroLAN™ products
- 8-bit family code specifies DS2401 communications requirements to reader
- Presence pulse acknowledges when the reader first applies voltage
- Low-cost TO-92, SOT-223 and TSOC surface mount packages
- Reduces control, address, and data to a single pin
- Zero standby power required
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits/s
- Pulse width measurement determines 1s or 0s
- Power derived from data line
- Applications
  - PCB Identification
  - Network Node ID
  - Equipment Registration
- Operates over industrial temperature range of -40°C to +85°C

### DESCRIPTION

The DS2401 enhanced Silicon Serial Number is a low-cost, electronic registration number that provides an absolutely unique identity which can be determined with a minimal electronic interface, typically a single port pin of a microcontroller. The DS2401 consists of a factory-

### PIN ASSIGNMENT



### PIN DESCRIPTION

#### TO-92/SOT-223

Pin 1	– Ground
Pin 2	– Data (DQ)
Pin 3	– No Connect
Pin 4	– Ground

#### TSOC

Pin 1	– Ground
Pin 2	– Data (DQ)
Pin 3	– No Connect
Pin 4–6	– No Connect

### ORDERING INFORMATION

DS2401	TO-92 Package
DS2401Z	SOT-223 Surface Mount Package
DS2401T	Tape & Reel of DS2401
DS2401Y	Tape & Reel of DS2401Z
DS2401P	TSOC Surface Mount Package
DS2401V	Tape & Reel of DS2401P

lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. Power for reading and writing the device is

derived from the data line itself with no need for an external power source. The DS2401 is an upgrade to the DS2400. The DS2401 is fully reverse-compatible with the DS2400 but provides the additional multi-drop capability that enables many devices to reside on a single data line. The familiar TO-92, SOT-223 or TSOC package provides a compact enclosure that allows standard assembly equipment to handle the device easily.

### OPERATION

The DS2401's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

### 1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS2401 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal

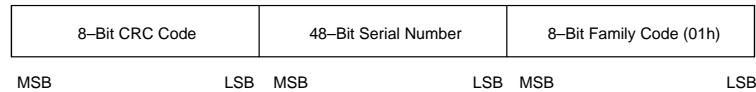
type and timing). For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

### Hardware Configuration

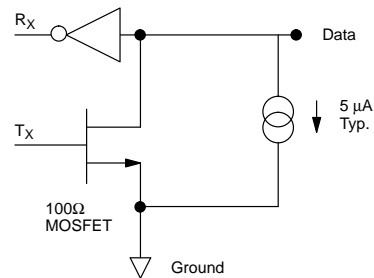
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain connection or 3-state outputs. The DS2401 is an open drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pull-up resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pull-up resistor should be approximately 5 k $\Omega$  for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3k bits per second.

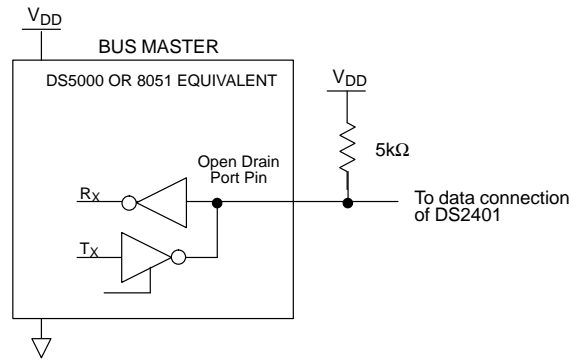
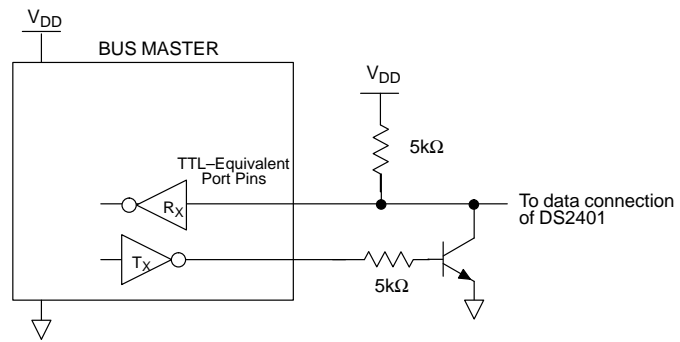
The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus **MUST** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120  $\mu$ s, one or more of the devices on the bus may be reset.

### DS2401 MEMORY MAP Figure 1



### DS2401 EQUIVALENT CIRCUIT Figure 2



**BUS MASTER CIRCUIT** Figure 3**A) Open Drain****B) Standard TTL**

## TRANSACTION SEQUENCE

The sequence for accessing the DS2401 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

## INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2401 is on the bus and is ready to operate. For more details, see the “1–Wire Signalling” section.

## ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 4):

### Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS2401’s 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2401 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The DS2401 Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS2400, which will only respond to a 0Fh command word with its 64-bit ROM data.

### Match ROM [55h] / Skip ROM [CCh]

The complete 1–Wire protocol for all Dallas Semiconductor iButtons contains a Match ROM and a Skip ROM command. (See the Book of DS19xx iButton Standards). Since the DS2401 contains only the 64-bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1–Wire bus if executed. The DS2401 does not interfere with other 1–Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (for example, a DS2401 and DS1994 on the same bus).

## Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a ROM search, including an actual example.

## 1–WIRE SIGNALLING

The DS2401 requires a strict protocol to insure data integrity. The protocol consists of four types of signalling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1 and read data. All these signals except presence pulse are initiated by the bus master.

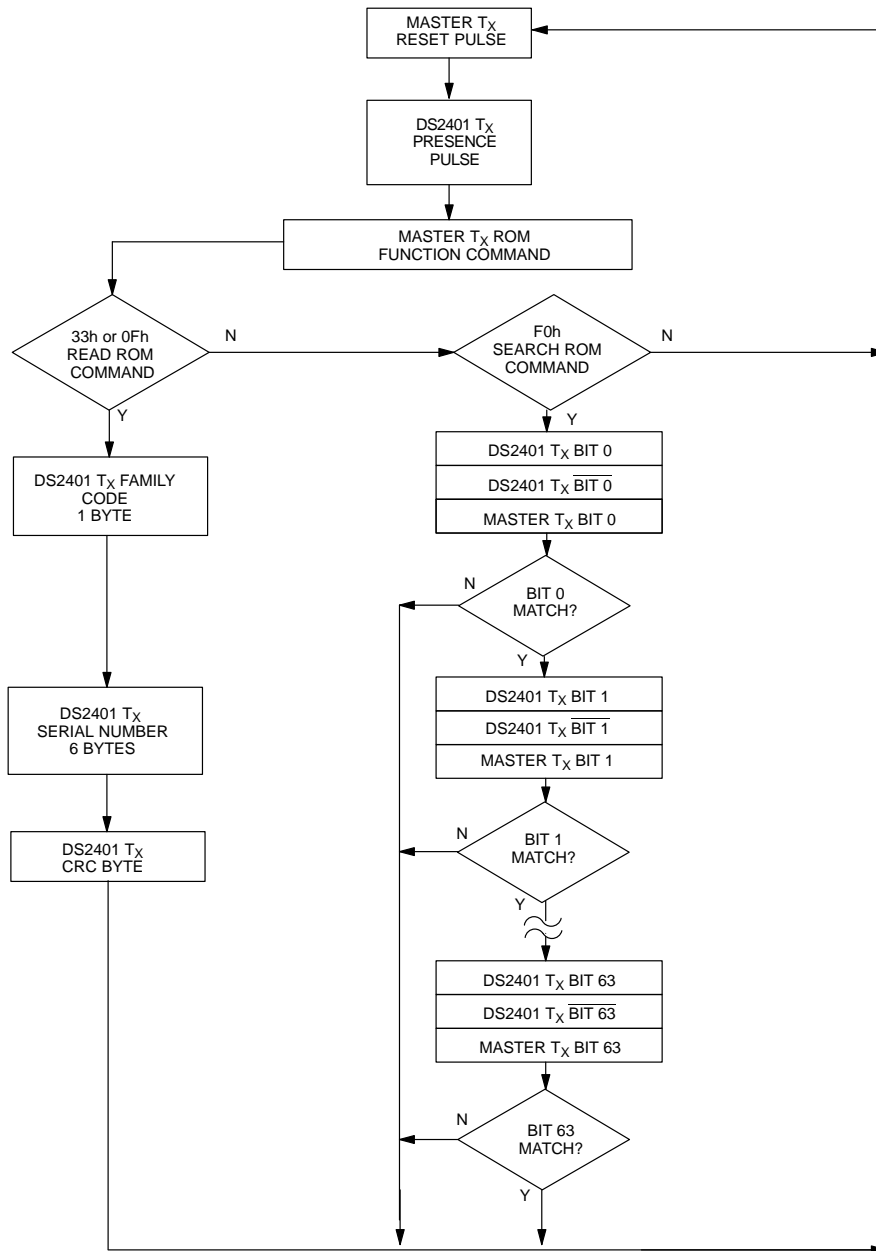
The initialization sequence required to begin any communication with the DS2401 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS2401 is ready to send or receive data given the correct ROM command.

The bus master transmits ( $T_X$ ) a reset pulse ( $t_{RSTL}$ , minimum 480  $\mu$ s). The bus master then releases the line and goes into receive mode ( $R_X$ ). The 1–Wire bus is pulled to a high state via the 5 k $\Omega$  pull-up resistor. After detecting the rising edge on the data pin, the DS2401 waits ( $t_{PDH}$ , 15–60  $\mu$ s) and then transmits the presence pulse ( $t_{PDL}$ , 60–240  $\mu$ s).

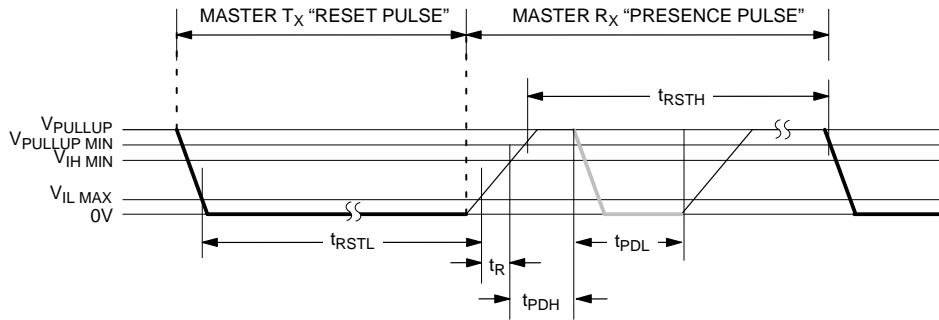
## READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2401 to the master by triggering a delay circuit in the DS2401. During write time slots, the delay circuit determines when the DS2401 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the DS2401 will hold the data line low overriding the 1 generated by the master. If the data bit is a “1”, the DS2401 will leave the read data time slot unchanged.

ROM FUNCTIONS FLOW CHART Figure 4



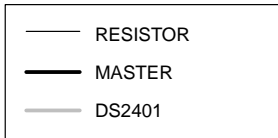
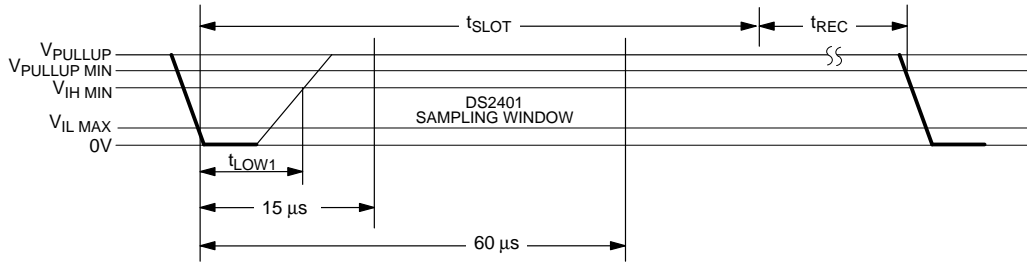
**INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 5**



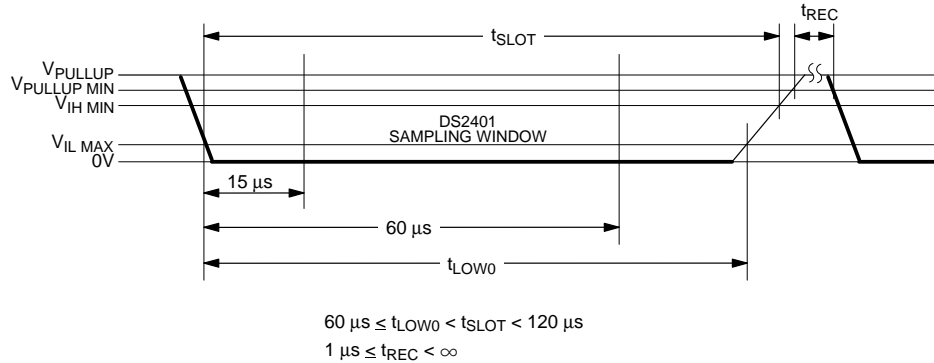
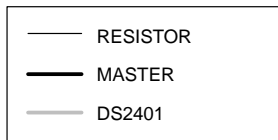
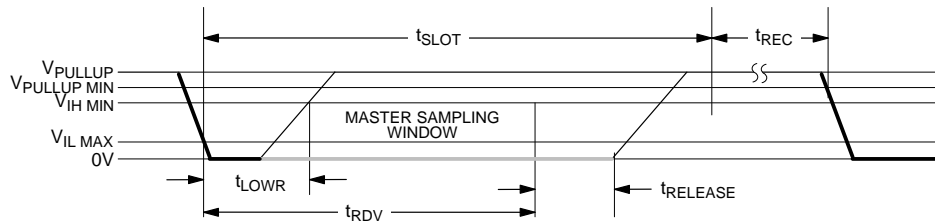
$480 \mu s \leq t_{RSTL} < \infty^*$   
 $480 \mu s \leq t_{RSTH} < \infty$  (includes recovery time)  
 $15 \mu s \leq t_{PDH} < 60 \mu s$   
 $60 \mu s \leq t_{PDL} < 240 \mu s$

\* In order not to mask interrupt signalling by other devices on the 1-Wire bus,  $t_{RSTL} + t_R$  should always be less than 960  $\mu s$ .

**READ/WRITE TIMING DIAGRAM Figure 6**  
**Write-One Time Slot**



$60 \mu s \leq t_{SLOT} < 120 \mu s$   
 $1 \mu s \leq t_{LOW1} < 15 \mu s$   
 $1 \mu s \leq t_{REC} < \infty$

**READ/WRITE TIMING DIAGRAM (cont'd) Figure 6****Write-zero Time Slot****Read-data Time Slot**

$60 \mu\text{s} \leq t_{\text{SLOT}} < 120 \mu\text{s}$   
 $1 \mu\text{s} \leq t_{\text{LOWR}} < 15 \mu\text{s}$   
 $0 \leq t_{\text{RELEASE}} < 45 \mu\text{s}$   
 $1 \mu\text{s} \leq t_{\text{REC}} < \infty$   
 $t_{\text{RDV}} = 15 \mu\text{s}$

**CRC GENERATION**

To validate the data transmitted from the DS2401, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS2401. If the two CRC values match, the transmission is error-free.

The equivalent polynomial function of this CRC is:

$$\text{CRC} = x^8 + x^5 + x^4 + 1$$

For more details, see the Book of DS19xx iButton Standards.

**LOT QUANTITIES AND CUSTOM DS2401**

The DS2401 is available in registered whole lots sealed in tamper-detecting cartons with the beginning number and range which that particular lot spans specified on

the label. Nominal lot size is 7,200 pieces with devices packed in either 500-piece bags or mounted on reels for use by automatic assembly equipment.

The DS2401 can be made available with a custom brand on the package which provides a human-readable representation of the factory-lasered 64-bit ROM code inside. Additional customization of a portion of the unique 48-bit serial number by the customer is available. Dallas Semiconductor will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your Dallas Semiconductor sales representative for more information.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**DC ELECTRICAL CHARACTERISTICS**(-40°C to +85°C;  $V_{PUP}=2.8V$  to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	$V_{IH}$	2.2		$V_{CC} + 0.3$	V	1, 6
Logic 0	$V_{IL}$	-0.3		+0.8	V	1
Output Logic Low @4 mA	$V_{OL}$			0.4	V	1
Output Logic High	$V_{OH}$		$V_{PUP}$	6.0	V	1, 2
Input Load Current	$I_L$		5		$\mu A$	3
Operating Charge	$Q_{OP}$			30	nC	7, 8

**CAPACITANCE** $(t_A = 25^\circ C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	9

**AC ELECTRICAL CHARACTERISTICS**(-40°C to +85°C;  $V_{PUP}=2.8V$  to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	$t_{SLOT}$	60		120	$\mu s$	
Write 1 Low Time	$t_{LOW1}$	1		15	$\mu s$	
Write 0 Low Time	$t_{LOW0}$	60		120	$\mu s$	
Read Data Valid	$t_{RDV}$	exactly 15			$\mu s$	
Release Time	$t_{RELEASE}$	0	15	45	$\mu s$	
Read Data Setup	$t_{SU}$			1	$\mu s$	5
Recovery Time	$t_{REC}$	1			$\mu s$	
Reset Time High	$t_{RSTH}$	480			$\mu s$	4
Reset Time Low	$t_{RSTL}$	480			$\mu s$	10
Presence Detect High	$t_{PDHIGH}$	15		60	$\mu s$	
Presence Detect Low	$t_{PDLOW}$	60		240	$\mu s$	



**NOTES:**

1. All voltages are referenced to ground.
2.  $V_{PUP}$  = external pull-up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1  $\mu$ s of this falling edge and will remain valid for 14  $\mu$ s minimum (15  $\mu$ s total from falling edge on 1-Wire bus).
6.  $V_{IH}$  is a function of the external pull-up resistor and the  $V_{CC}$  supply.
7. 30 nanocoulombs per 72 time slots @ 5.0V.
8. At  $V_{CC}=5.0V$  with a 5 k $\Omega$  pullup to  $V_{CC}$  and a maximum time slot of 120  $\mu$ s.
9. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5 k $\Omega$  resistor is used to pull up the I/O line to  $V_{CC}$ , 5  $\mu$ s after power has been applied the parasite capacitance will not affect normal communications.
10. The reset low time ( $t_{RSTL}$ ) should be restricted to a maximum of 960  $\mu$ s, to allow interrupt signalling, otherwise it could mask or conceal interrupt pulses if this device is used in parallel with a DS2404 or DS1994.