

# MOSFET - Single N-Channel

80 V, 5.9 mΩ, 84 A



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## NTTFS5D9N08H

### Features

- Max  $R_{DS(on)}$  = 5.9 mΩ at  $V_{GS} = 10$  V,  $I_D = 23$  A
- Max  $R_{DS(on)}$  = 9 mΩ at  $V_{GS} = 6$  V,  $I_D = 12$  A
- High Performance Technology for Extremely Low  $R_{DS(on)}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- DC-DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	80	V	
Gate-to-Source Voltage		$V_{GS}$	±20	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	84	A
			$P_D$	100	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	13	A
			$P_D$	2.7	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$	$I_{DM}$	535	A	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	83	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{AV} = 40$ A, $L = 0.1$ mH) (Note 3)		$E_{AS}$	80	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

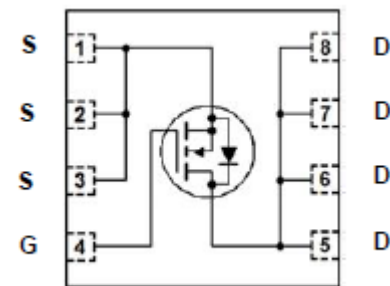
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

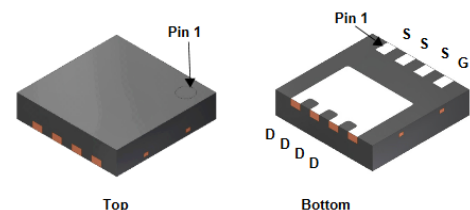
Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 1)	$R_{\theta JC}$	1.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	54.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz. Cu pad.
3.  $E_{AS}$  of 80 mJ is based on started  $T_J = 25^\circ\text{C}$ ,  $I_{AS} = 40$  A,  $V_{DD} = 80$  V,  $V_{GS} = 10$  V. 100% test at  $I_{AS} = 40$  A.

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
80 V	5.9 mΩ @ 10 V	84 A
	9 mΩ @ 6 V	



N-CHANNEL MOSFET



WDFN8  
3.3X3.3, 0.65P  
CASE 483AW

### ORDERING INFORMATION

Device	Package	Shipping†
NTTFS5D9N08HTWG	PQFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTTFS5D9N08H

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		42.91		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 120\ \mu\text{A}$	2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 120\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-6.81		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$		4.6	5.9	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 12\text{ A}$		6.6	9.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 23\text{ A}$		135		S
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		1		$\Omega$

## CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		2040		pF	
Output Capacitance	$C_{OSS}$			303			
Reverse Transfer Capacitance	$C_{RSS}$			12			
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 64\text{ V}, I_D = 11.5\text{ A}$		20		nC	
Total Gate Charge	$Q_{G(TOT)}(10V)$			31			
Gate-to-Source Charge	$Q_{GS}$			8.4			
Gate-to-Drain Charge	$Q_{GD}$			6.8			
Plateau Voltage	$V_{GP}$			4.4			V

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 6\text{ V}, V_{DS} = 64\text{ V}, I_D = 11.5\text{ A}, R_G = 2.5\ \Omega$		17.2		ns
Rise Time	$t_r$			8.7		
Turn-Off Delay Time	$t_{d(OFF)}$			21.6		
Fall Time	$t_f$			5.8		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 23\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.7		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 11.5\text{ A}$		39		ns	
Reverse Recovery Charge	$Q_{RR}$			28		nC	
Charge Time	$t_a$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 11.5\text{ A}$		21		ns	
Discharge Time	$t_b$			16		ns	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures

5. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

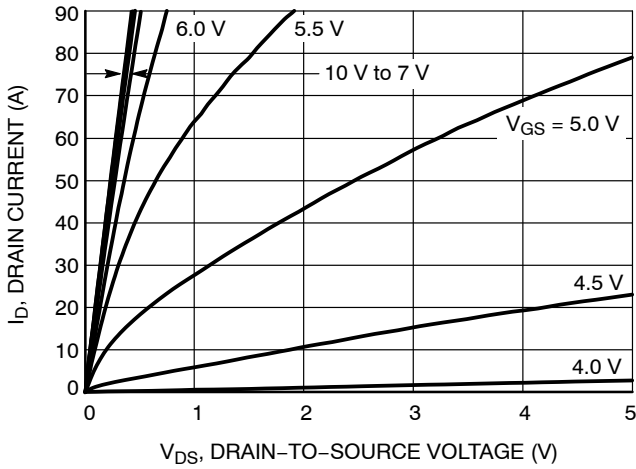


Figure 1. On-Region Characteristics

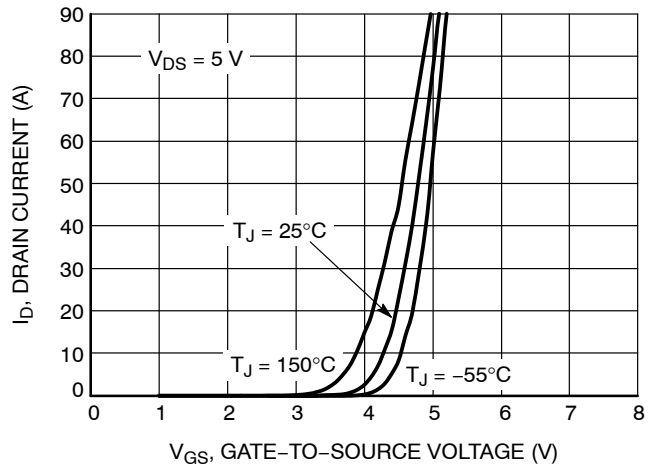


Figure 2. Transfer Characteristics

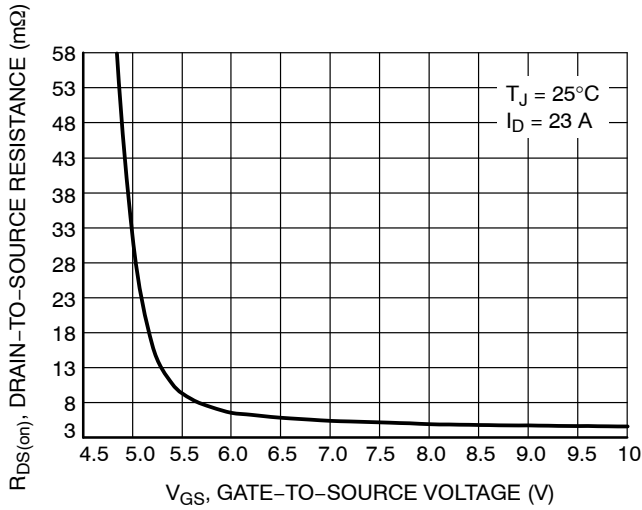


Figure 3. On-Resistance vs. Gate-to-Source Voltage

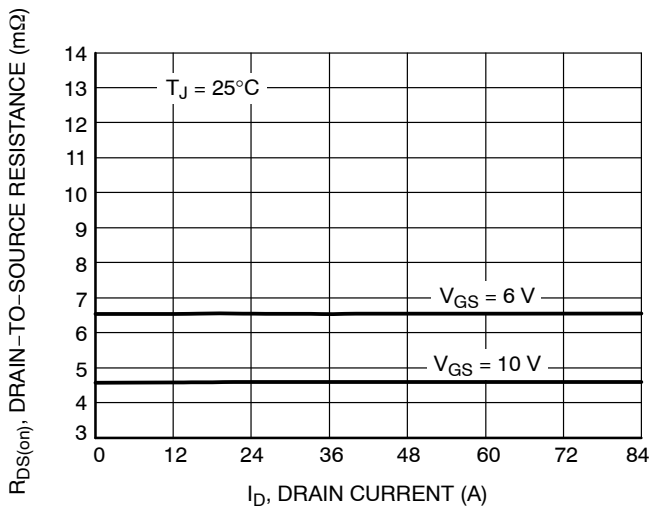


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

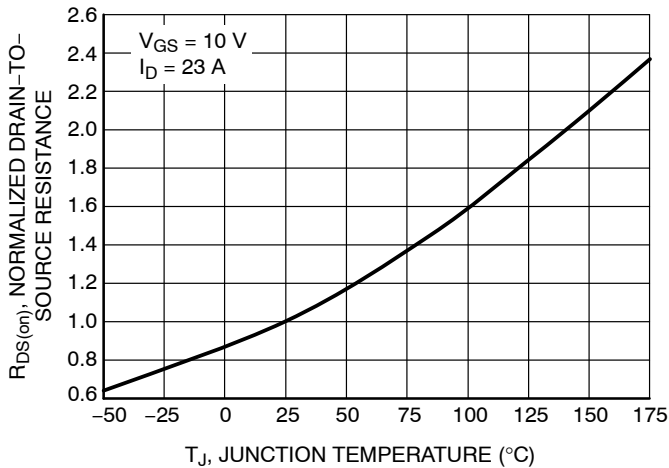


Figure 5. On-Resistance Variation with Temperature

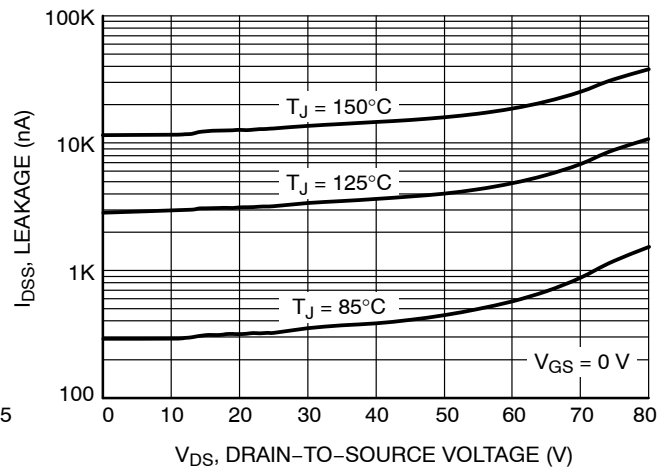


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

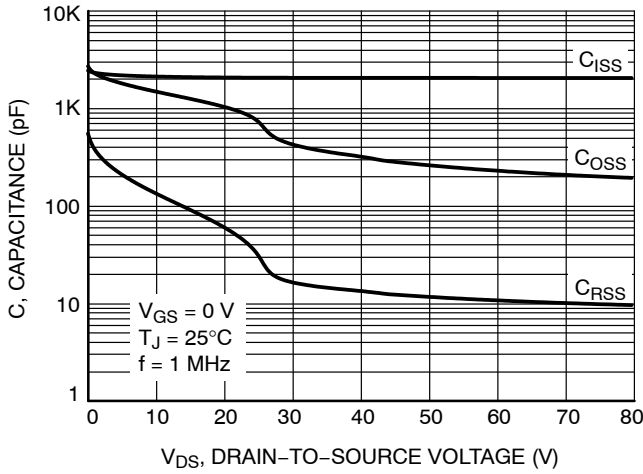


Figure 7. Capacitance Variation

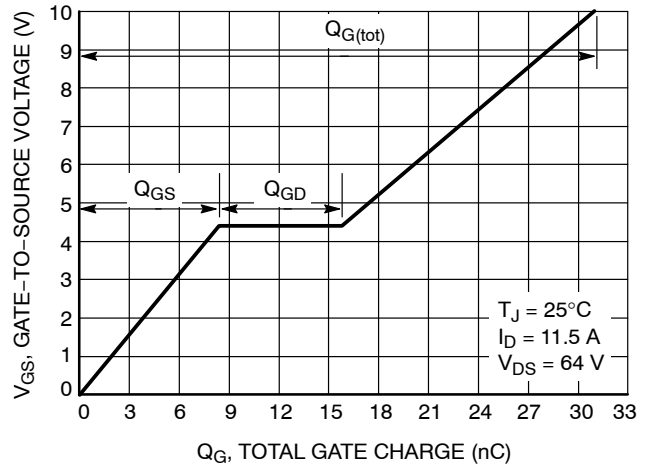


Figure 8. Gate-to-Source Voltage vs. Total Charge

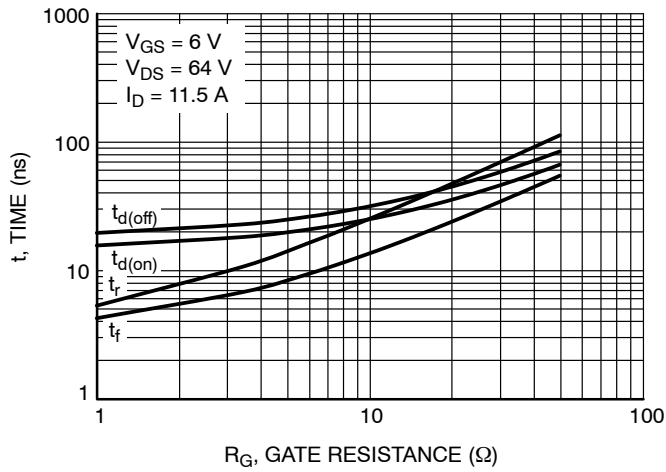


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

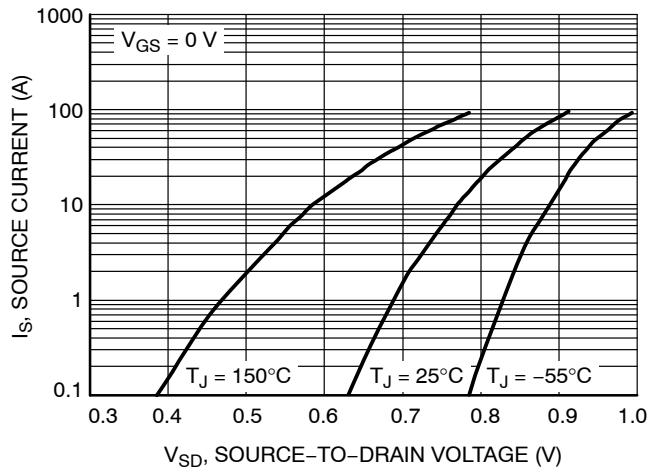


Figure 10. Diode Forward Voltage vs. Current

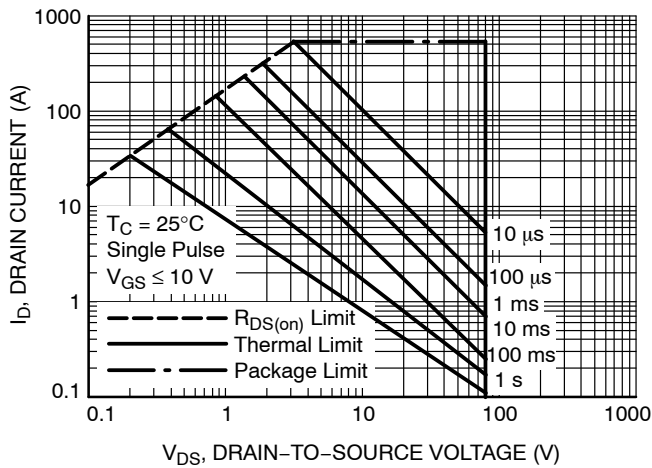


Figure 11. Maximum Rated Forward Biased Safe Operating Area

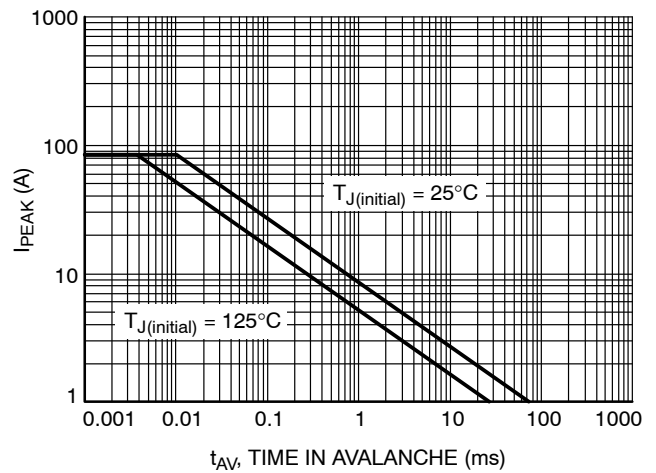


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

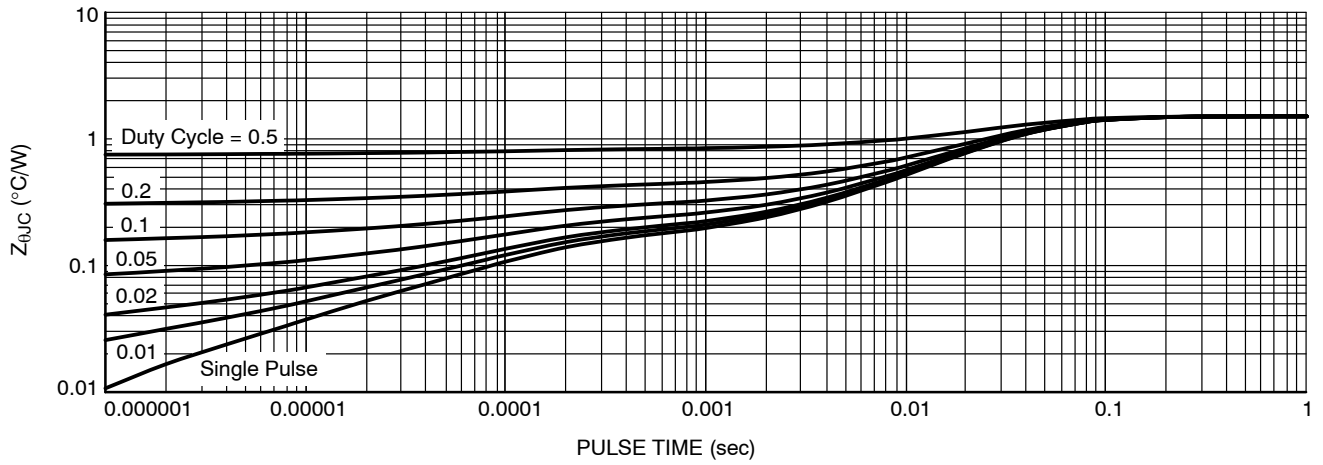
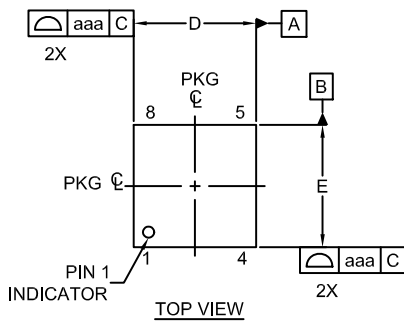


Figure 13. Transient Thermal Impedance

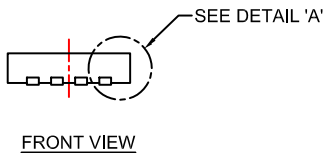
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## PACKAGE DIMENSIONS

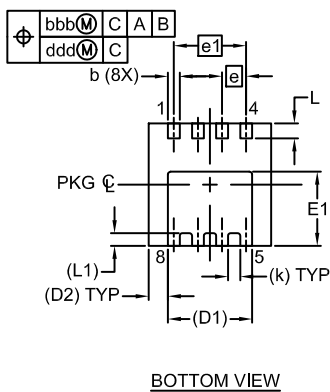
**WDFN8 3.3X3.3, 0.65P**  
**CASE 483AW**  
**ISSUE A**



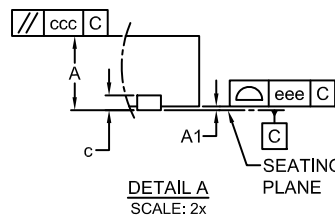
TOP VIEW



FRONT VIEW

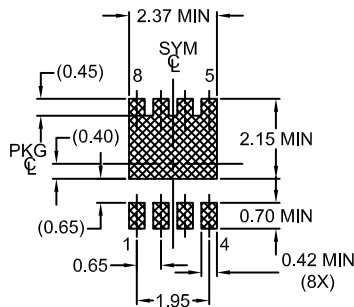


BOTTOM VIEW



DETAIL A  
SCALE: 2x

### LAND PATTERN RECOMMENDATION\*



### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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