

Vishay Siliconix

# Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	100				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0089				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0112				
I <sub>D</sub> (A)	50				
Configuration	Single				

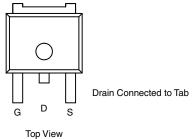
#### **FEATURES**

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization:
   For definitions of compliance please see www.vishay.com/doc?99912

N-Channel MOSFET







ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50N10-8m9L-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	100	.,	
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>	I <sub>D</sub>	50		
	T <sub>C</sub> = 125 °C		49		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	50	Α	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	200		
Single Pulse Avalanche Current	. 0.4	I <sub>AS</sub>	43		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	92	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	D	136	W	
	T <sub>C</sub> = 125 °C	$P_{D}$	45	VV	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)		$R_{thJC}$	1.1	C/ VV

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR-4 material).



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	1					ı	ı	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2.0	2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 175 °C	-	-	500		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A	-	0.0071	0.0089	Ω	
Dunin Course On Chata Basistanas		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C	-	-	0.0151		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C	-	-	0.0187		
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 10 A	-	0.0089	0.0112		
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	67	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>				2340	2950		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	1441	1810	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	]		-	124	160		
Total Gate Charge <sup>c</sup>	Qg			-	46	70		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 50 \text{ V}, I_{D} = 50 \text{ A}$	-	7.5	-	nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	1		-	10	-		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		6	12.3	18.5	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>				12	18		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, \text{ R}_L = 1 \Omega$ $I_D \cong 50 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	12	18	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	95	145		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	120	180		
Source-Drain Diode Ratings and Char-	acteristics <sup>b</sup>	•			•			
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	200	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V		-	0.8	1.5	V	

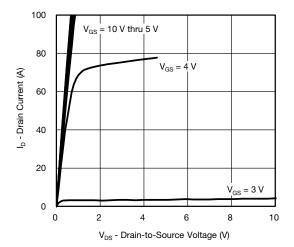
### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

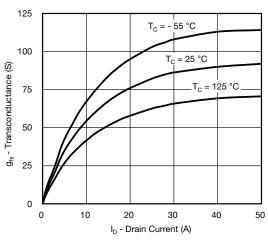
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



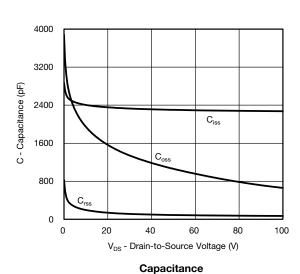
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

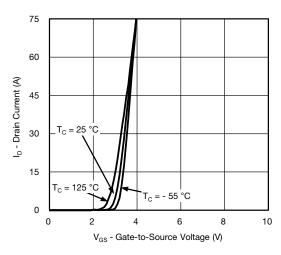


### **Output Characteristics**

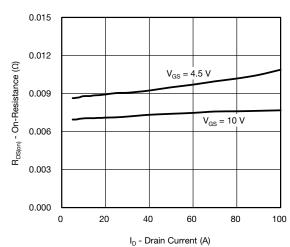


### Transconductance

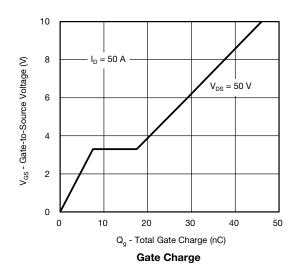




#### **Transfer Characteristics**

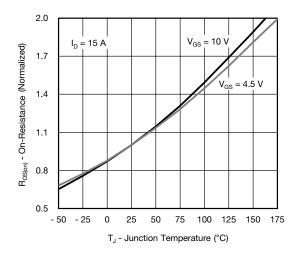


On-Resistance vs. Drain Current

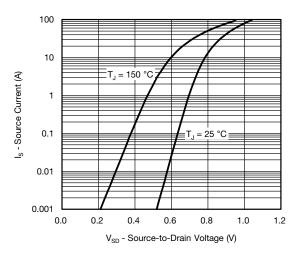




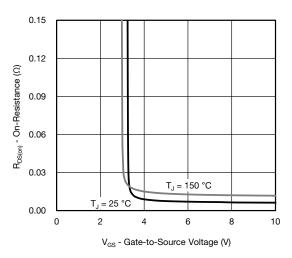
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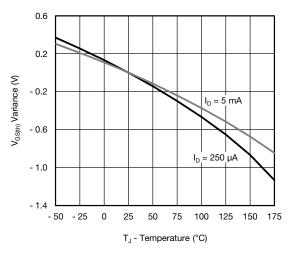
#### On-Resistance vs. Junction Temperature



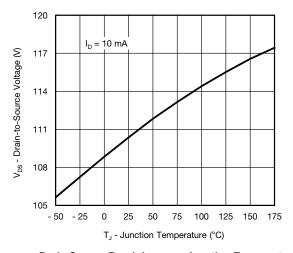
**Source Drain Diode Forward Voltage** 



On-Resistance vs. Gate-to-Source Voltage



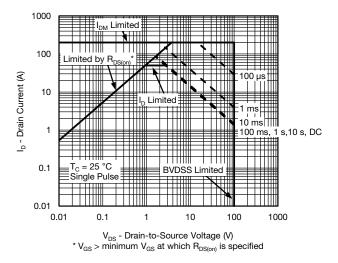
**Threshold Voltage** 



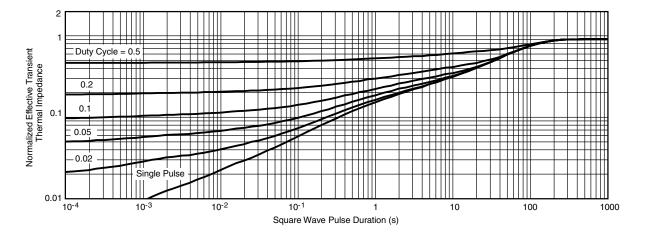
Drain Source Breakdown vs. Junction Temperature



### **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



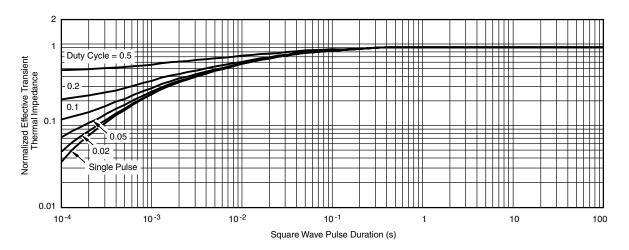
### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

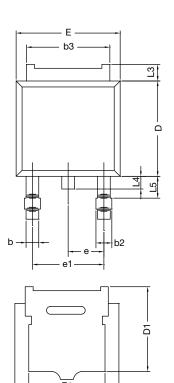
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

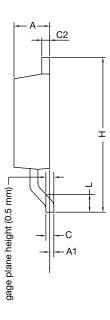
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg262778">www.vishay.com/ppg262778</a>.



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## **TO-252AA Case Outline**





	MILLIN	METERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090	BSC	
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0592-Rev. A, 02-Sep-13					

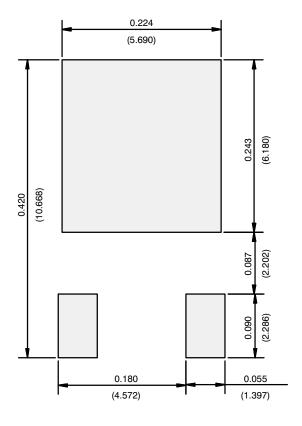
### DWG: 6019

Note

• Dimension L3 is for reference only.



### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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