Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)
- · Low thermal resistance
- · Low 0.8 mm profile

3. Applications

Active clamp circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	-100	V
V_{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-	-0.7	Α
Static chara	cteristics		·			·	
R _{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -0.7 A; T_j = 25 °C		-	930	1500	mΩ

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	1 2 3 4	D
2	S	source		
3	S	source		G (F) ¥)
4	G	gate		s
5	D	drain		017aaa094
6	D	drain		
7	D	drain	MLPAK33 (SOT8002-2)	
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package	ackage							
	Name	Description	Version						
PXP1500-100QS	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-2						

7. Marking

Table 4. Marking codes

Type number	Marking code
PXP1500-100QS	9AM

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-100	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-0.7	Α
		V _{GS} = -10 V; T _{amb} = 100 °C	[1]	-	-0.4	Α
		V _{GS} = -10 V; T _{sp} = 25 °C		-	-1.4	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-3	А
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	1.7	W
		T _{sp} = 25 °C		-	16.2	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	diode				•	•
Is	source current	T _{amb} = 25 °C	[1]	-	-0.66	А
Avalanche ru	ıggedness				•	•
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = -0.6 A; DUT in avalanche (unclamped)		-	7	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

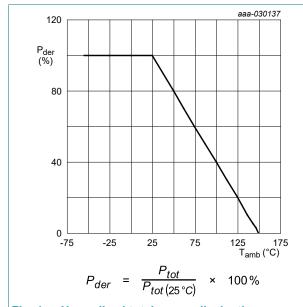


Fig. 1. Normalized total power dissipation as a function of ambient temperature

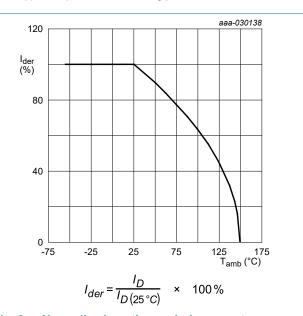


Fig. 2. Normalized continous drain current as a function of ambient temperature

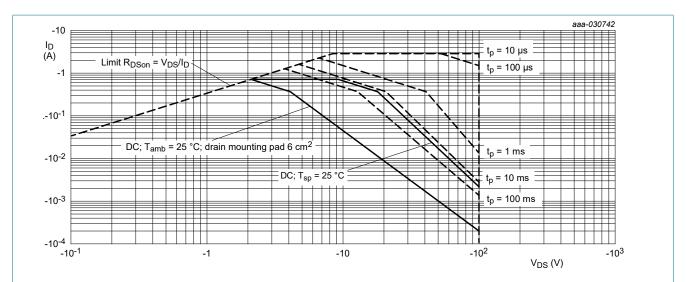


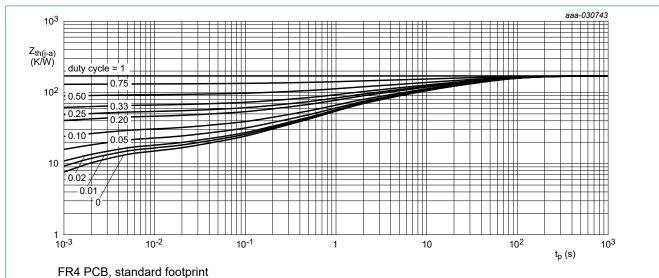
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

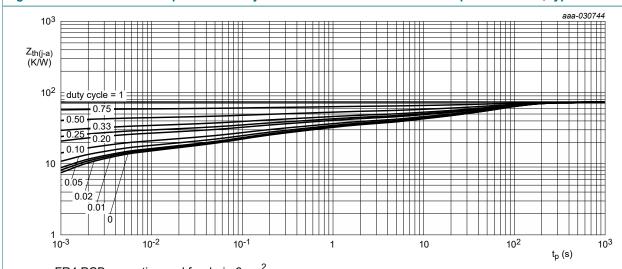
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from	in free air	[1]	-	170	205	K/W
junction to ambient	junction to ambient		[2]	-	75	90	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	17.2	20.5	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



1 14 1 GB, standard rootprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-100	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 ^{\circ}C$	-2	-3	-4	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = -100 V; T _j = 25 °C	-	-	-1	μΑ
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	V_{GS} = -10 V; I_D = -0.7 A; T_j = 25 °C	-	930	1500	mΩ
Doon	resistance	V _{GS} = -10 V; I _D = -0.7 A; T _j = 150 °C	-	2000	3165	mΩ
		$V_{GS} = -6 \text{ V}; I_D = -0.6 \text{ A}; T_j = 25 \text{ °C}$	-	1000	1700	mΩ
g _{fs}	forward transconductance	V_{DS} = -5 V; I_D = -0.7 A; T_j = 25 °C	-	1.6	-	S
R_G	gate resistance	f = 1 MHz	-	26	-	Ω
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	V_{DS} = -50 V; I_{D} = -0.6 A; V_{GS} = -10 V; T_{j} = 25 °C	-	3.1	4.5	nC
		$V_{DS} = -50 \text{ V}; I_D = -0.6 \text{ A}; V_{GS} = -6 \text{ V};$	-	2.1	3.1	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	0.6	-	nC
Q _{GD}	gate-drain charge	- 	-	0.9	-	nC
C _{iss}	input capacitance	V _{DS} = -50 V; f = 1 MHz; V _{GS} = 0 V;	-	159	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	8	-	pF
C _{rss}	reverse transfer capacitance		-	4.5	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = -50 \text{ V}; I_D = -0.6 \text{ A}; V_{GS} = -6 \text{ V};$	-	5	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	17	-	ns
t _{d(off)}	turn-off delay time]	-	5	-	ns
t _f	fall time]	-	12	-	ns
Source-drai	in diode		<u>'</u>	'		
V _{SD}	source-drain voltage	$I_S = -0.7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-0.8	-1.2	V
t _{rr}	reverse recovery time	I _S = -0.6 A; dI _S /dt = -100 A/μs;	-	24	-	ns
Q _r	recovered charge	$V_{GS} = -6 \text{ V}; V_{DS} = -40 \text{ V}; T_j = 25 \text{ °C}$	-	20	-	nC

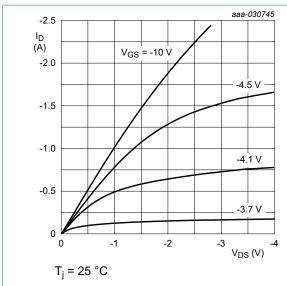


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

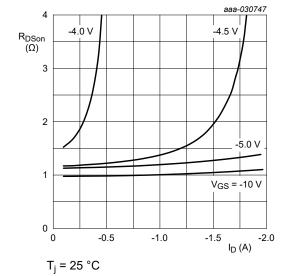


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

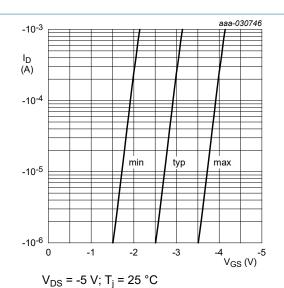


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

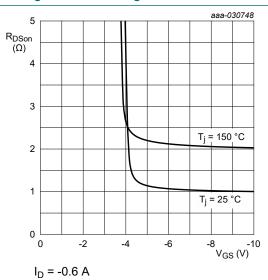


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

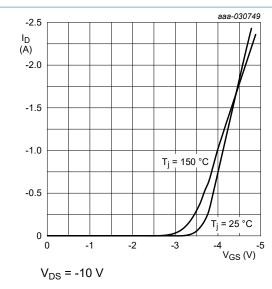


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

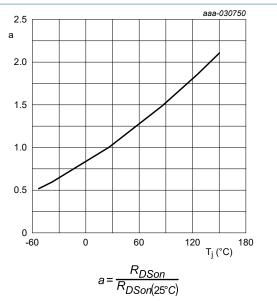


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

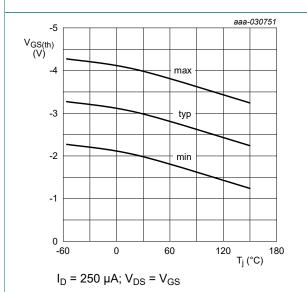


Fig. 12. Gate-source threshold voltage as a function of junction temperature

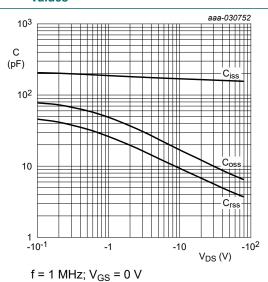


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

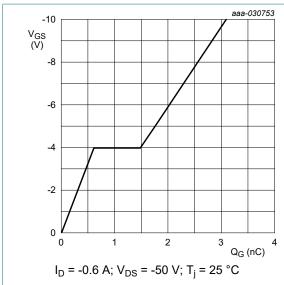


Fig. 14. Gate-source voltage as a function of gate charge; typical values

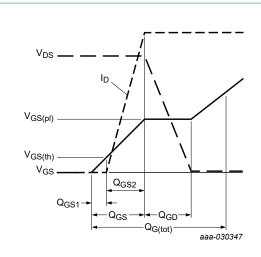


Fig. 15. Gate charge waveform definitions

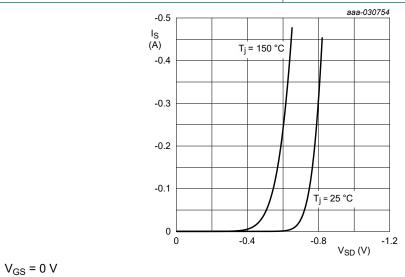
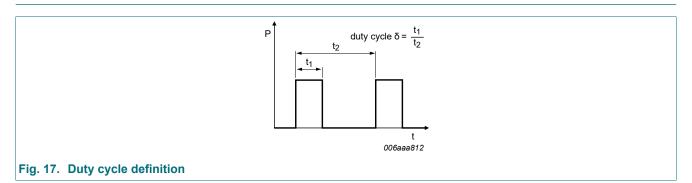
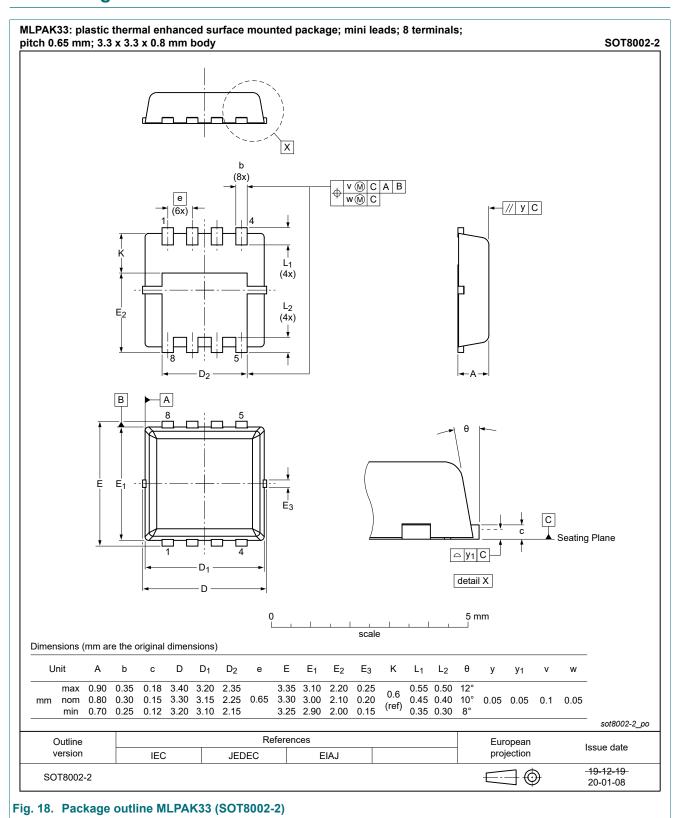


Fig. 16. Source current as a function of source-drain voltage; typical values

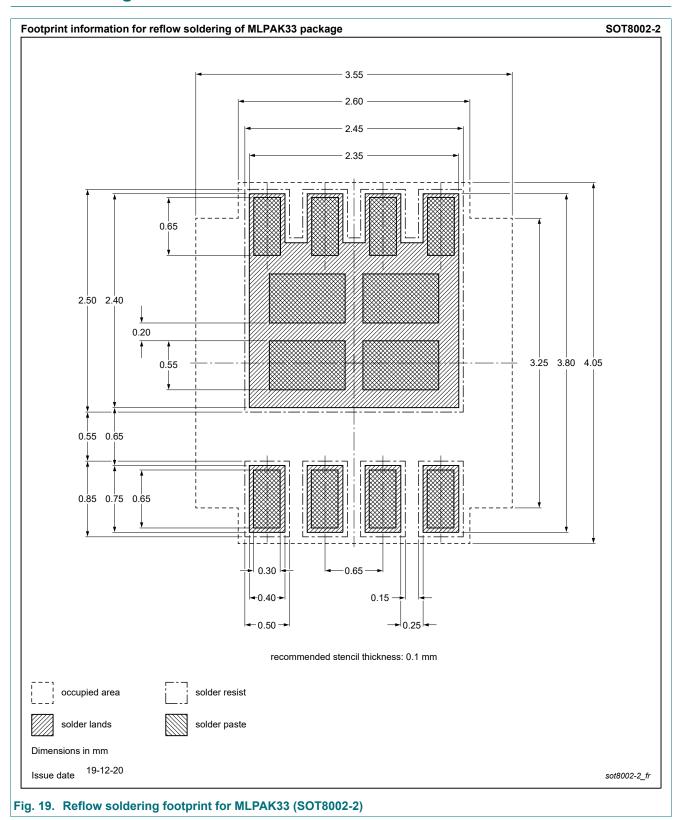
11. Test information



12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXP1500-100QS v.1	20200507	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 7 May 2020

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