FRDMKW38UG
FRDM-KW38 Freedom Development Board User's Guide

1 Introduction

This guide describes the hardware for the FRDM-KW38 Freedom development board. The FRDM-KW38 Freedom development board is highly configurable, low-power, and cost-effective evaluation and development board for application prototyping and demonstration of the *KW39A/38A/37A/38Z/37Z* family of devices. These evaluation boards offer easy-to-use mass-storage-device mode flash programmer, a virtual serial port, and standard programming and run-control capabilities.

The KW38 is an ultralow-power, highly integrated single-chip device that enables Bluetooth Low Energy (BLE 5.0) or Generic FSK (at 250, 500, 1000 and 2000 kbps) for portable, extremely low-power embedded systems.

The KW38 integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of GenFSK, an Arm$^®$ Cortex$^®$-M0+ CPU, up to 512 KB Flash and up to 64 KB SRAM, Bluetooth LE Link Layer hardware and peripherals optimized to meet the requirements of the target applications.

Contents

2 Overview and description

The FRDM-KW38 development board is an evaluation environment supporting NXP KW39A/38A/37A/38Z/37Z (KW38) Wireless Microcontrollers (MCU). The KW38 integrates a radio transceiver operating in the 2.4 GHz band (supporting a range of GFSK and Bluetooth LE 5.0) and an Arm$^®$ Cortex$^®$-M0+ MCU into a single package. NXP supports the KW38 with tools and software that include hardware evaluation and development boards, software development IDE, applications, drivers, and a custom PHY with a BLE Link Layer. The FRDM-KW38 development board consists of the KW38A device with a 32 MHz reference oscillator crystal, RF circuitry (including antenna), 4-Mbit external serial flash, CAN and LIN transceivers and supporting circuitry in the popular Freedom board form-factor. The board is a standalone PCB and supports application development with NXP's Bluetooth Low Energy and Generic FSK libraries.

2.1 Overview

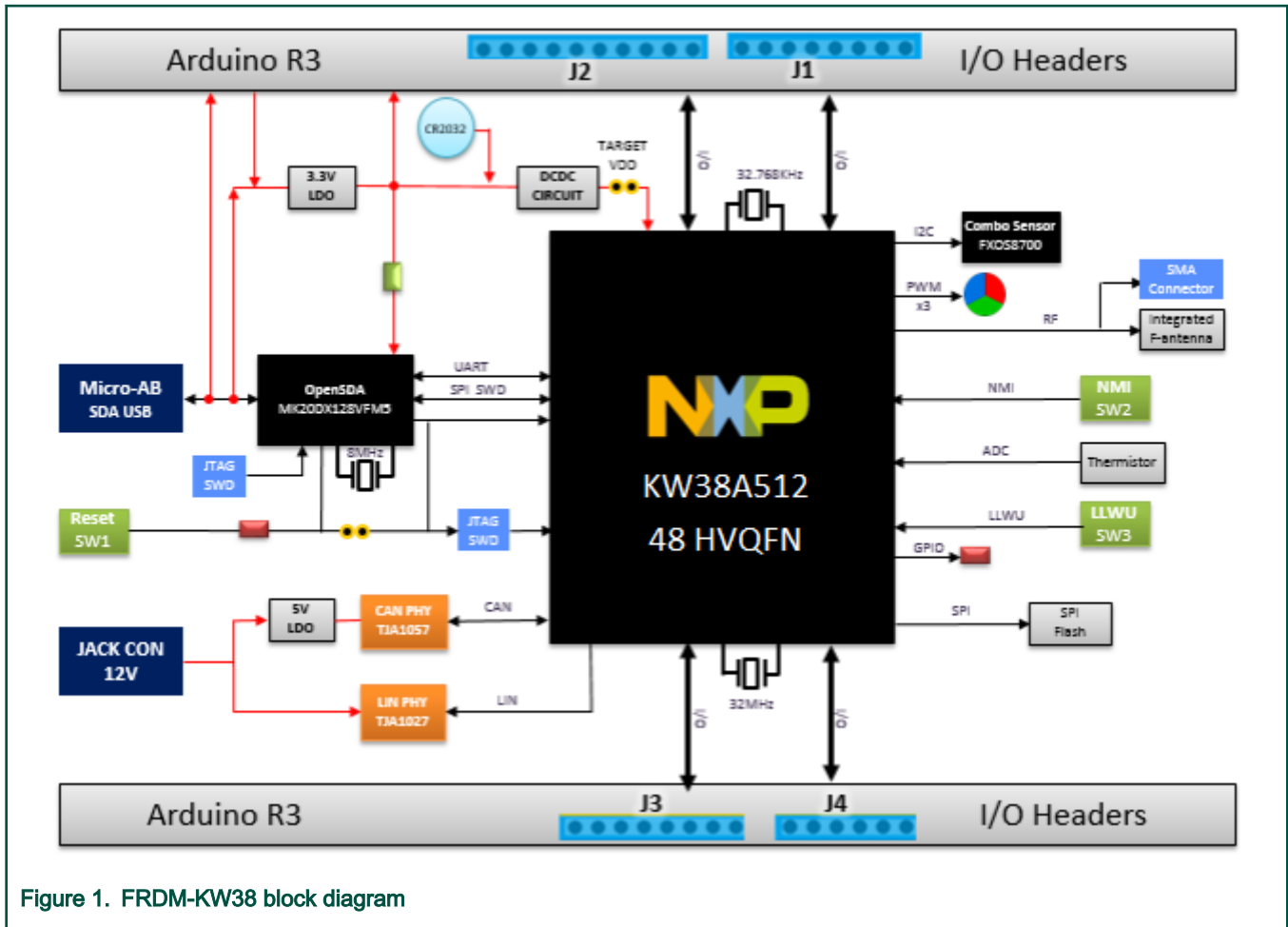Figure 1 shows a high-level block diagram of the FRDM-KW38 board features.

Figure 1. FRDM-KW38 block diagram

2.2 Feature description

The FRDM-KW38 development board is based on NXP Freedom development platform. It is the most diverse reference design containing the KW38A device and all necessary I/O connections for use as a stand-alone board, or connected in an application. Figure 2 shows the FRDM-KW38 development board.
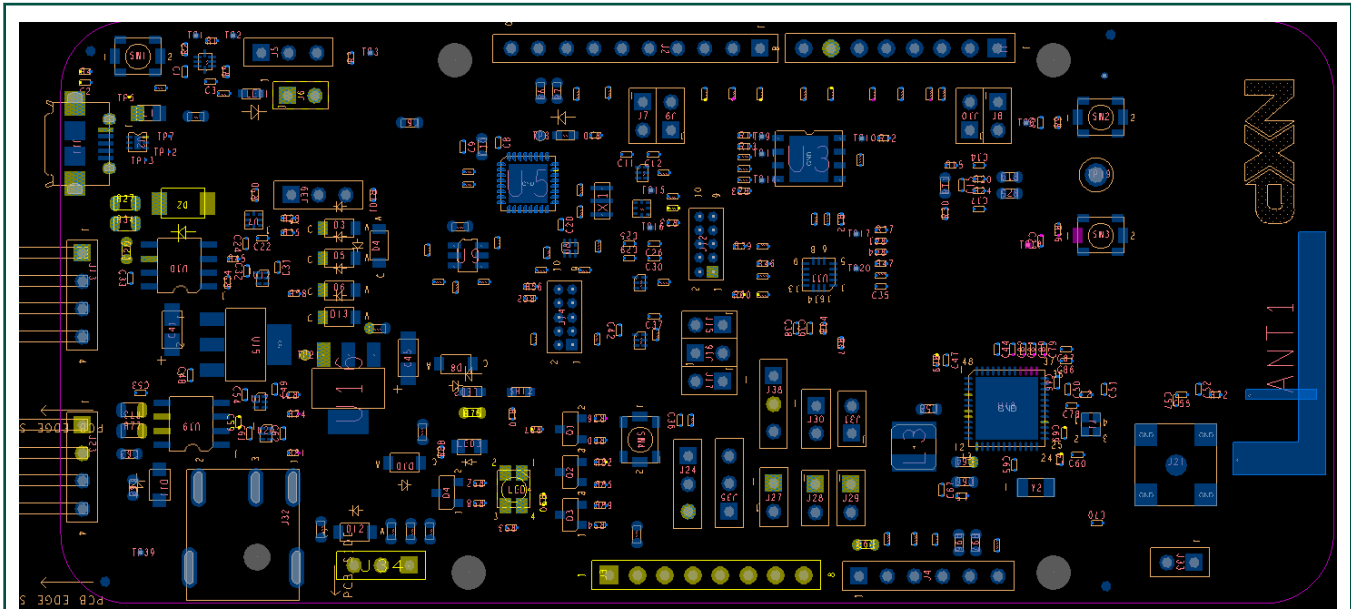
Figure 2. FRDM-KW38 Freedom development board

The FRDM KW38 development board includes these features:

- NXP's ultra-low-power KW38A Wireless MCU supporting Bluetooth LE and Generic FSK.

- Fully compliant Bluetooth v5.0 Low Energy (Bluetooth LE).

- Reference design area with small-footprint, low-cost RF node:

    — Single-ended input/output port

    — Low count of external components

    — Programmable output power from -30 dBm to +5 dBm at the SMA connector, when using DCDC Bypass or operating the DCDC in Buck mode

    — Receiver sensitivity is -98 dBm, typical (1Mbps@30.1% PER for 37 bytes payload packet) for GFSK applications (250 kbps, BT=0.5, h=0.5), at the SMA connector

    — Receiver sensitivity is -98 dBm (for 1 Mbps Bluetooth LE applications) at the SMA connector

- Integrated PCB inverted F-type antenna and SMA RF port (requires moving C7 to C8).

- Selectable power sources.

- DC-DC converter with Buck, and Bypass operation modes.

- 32 MHz reference oscillator for RF operation.

- 32.768 kHz reference oscillator mainly use for RTC operation and RF low power operation.

- 2.4 GHz frequency operation (ISM and MBAN).

- 4-Mbit (512 kB) external serial flash memory for Over-the-Air Programming (OTAP) support.

- NXP FXOS8700CQ Digital Sensor, 3D Accelerometer (±2g/±4g/±8g) + 3D Magnetometer.

- Thermistor circuit to test KW38 ADC module.

- Coin cell connector to be able to work using a CR2032 coin cell. CAN/LIN transceivers are not functional when using coin cell.

- Integrated Open-Standard Serial and Debug Adapter (OpenSDA).

- Cortex 10-pin (0.05") SWD debug port for target MCU.

- Cortex 10-pin (0.05") JTAG port for OpenSDA updates.

- One RGB LED indicator.

- One red LED indicator.

- Two push-button switches.

- NXP TJA1057 high-speed CAN transceiver.

- NXP TJA1027 LIN 2.2A/SAE J2602 transceiver.

Figure 3 shows the main board features and Input/Output headers for the FRDM-KW38 board.
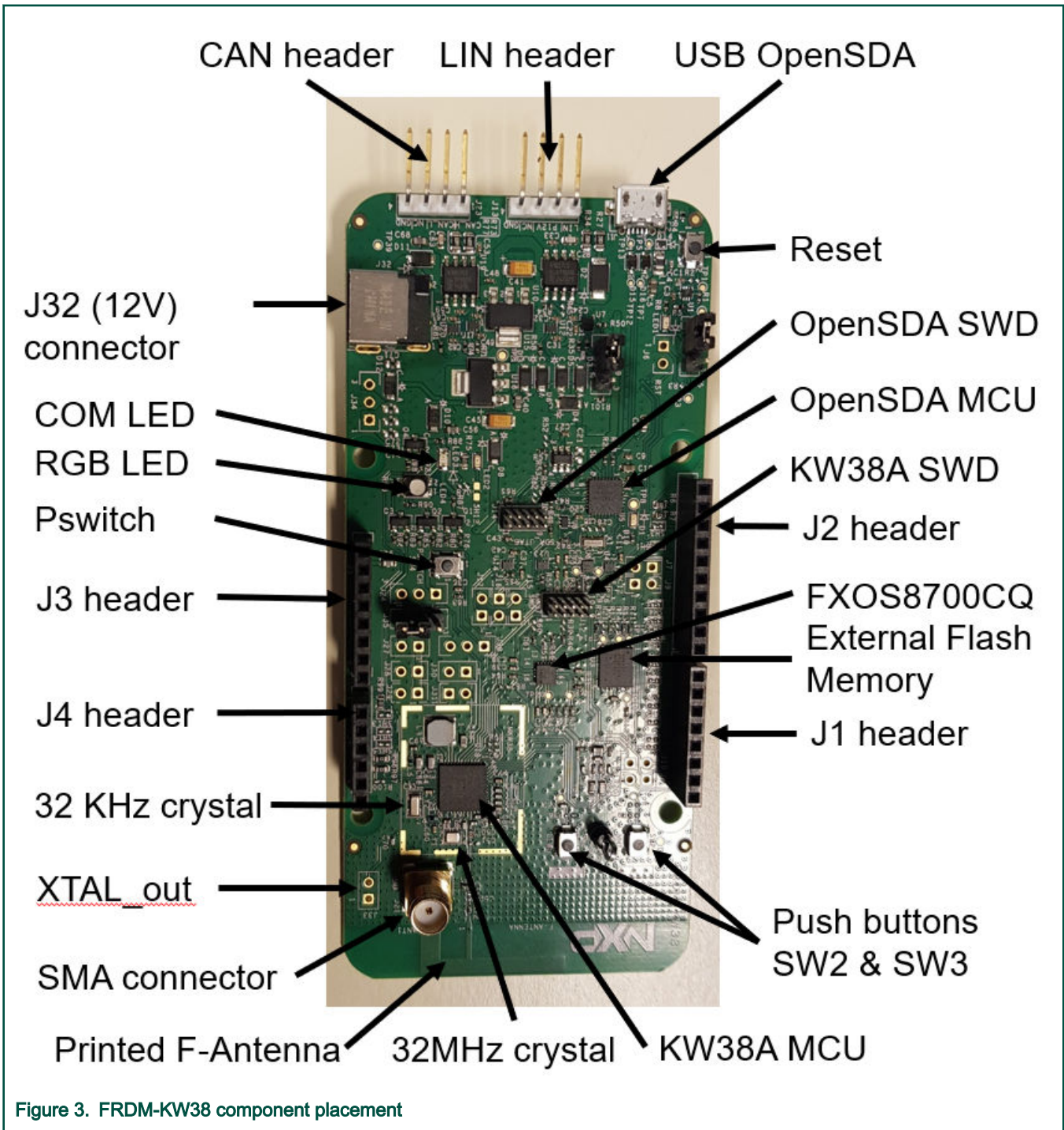

Figure 3. FRDM-KW38 component placement

2.3 OpenSDA serial and debug

The FRDM-KW38 development board includes OpenSDA v2.2- a serial and debug adapter circuit that includes an open-source hardware design, an open-source bootloader, and debug interface software. It bridges serial and debug communications between a USB host and an embedded target processor, as shown in Figure 4. The hardware circuit is based on an NXP Kinetis K20 family MCU (MK20DX128VFM5) with 128 KB of embedded flash and an integrated USB controller. OpenSDAv2.2 comes preloaded with the DAPLink bootloader - an open-source mass storage device (MSD) bootloader and the CMSIS-DAP Interface firmware, which provides a MSD flash programming interface, a virtual serial port interface, and a CMSIS-DAP debug protocol interface. For more information on the OpenSDAv2.2 software, see *mbed.org* (https://github.com/mbedmicro/DAPLink).
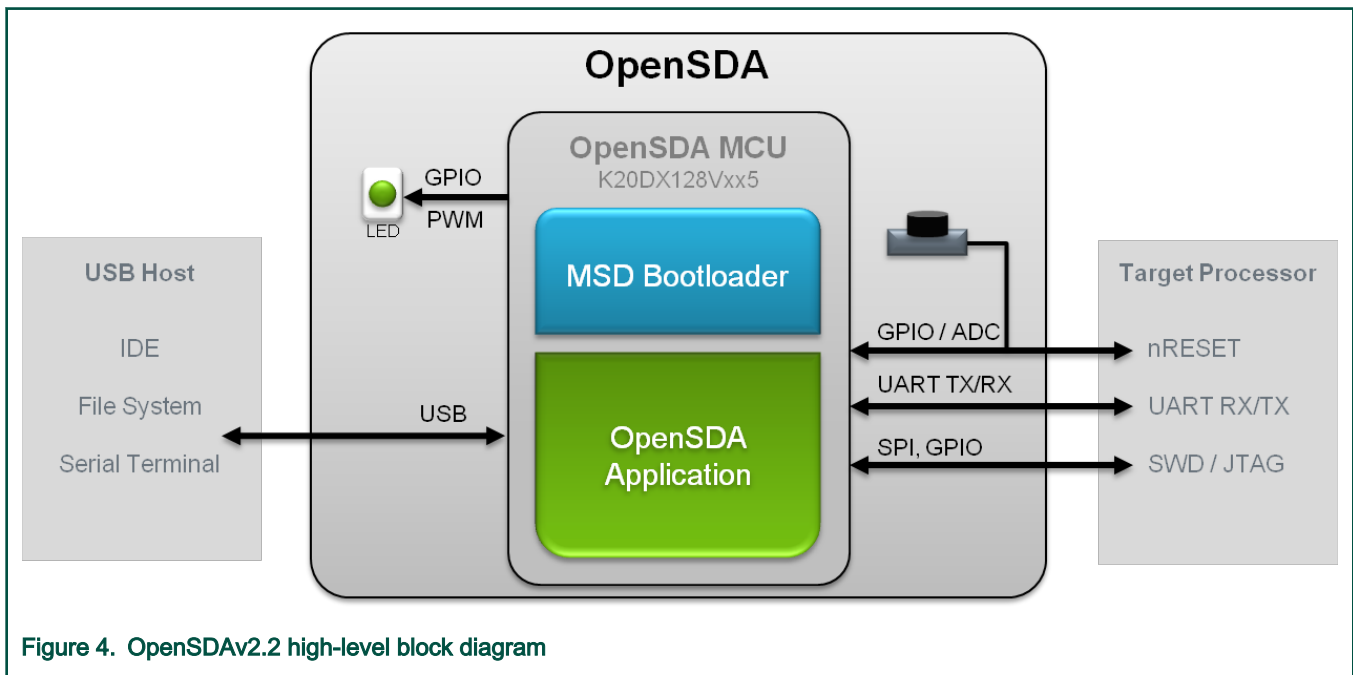

Figure 4. OpenSDAv2.2 high-level block diagram

OpenSDAv2.2 is managed by a Kinetis K20 MCU built on the ARM Cortex-M4 core. The OpenSDAv2.2 circuit includes a status LED (D1) and a pushbutton (SW1). The pushbutton asserts the Reset signal to the KW38 target MCU. It can also be used to place the OpenSDAv2.2 circuit into bootloader mode. UART and GPIO signals provide an interface to either the SWD debug port or the K20. The OpenSDAv2.2 circuit receives power when the USB connector J11 is plugged into a USB host.

2.3.1 Virtual serial port

A serial port connection is available between the OpenSDAv2.2 MCU and pins PTC6 and PTC7 of the KW38.

NOTE

To enable the Virtual COM, Debug, and MSD features, mbed drivers must be installed. Download the drivers at https://developer.mbed.org/handbook/Windows-serial-configuration.

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3 Functional description

The four-layer board provides the KW38 with its required RF circuitry, 32 MHz reference oscillator crystal, and power supply with a DC-DC converter including Bypass and Buck modes. The layout for this base-level functionality can be used as a reference layout for your target board.

3.1 RF circuit

The FRDM-KW38 RF circuit provides an RF interface for users to begin application development. A minimum matching network to the MCU antenna pin is provided through C50 and L2. An additional matching component, C51, is provided to match the printed F-antenna to a 50 ohms controlled line.

An optional SMA is located at J21. This is enabled by rotating the 10 pF capacitor in C55 to the location of C57. Figure 5 shows the RF circuit in detail.
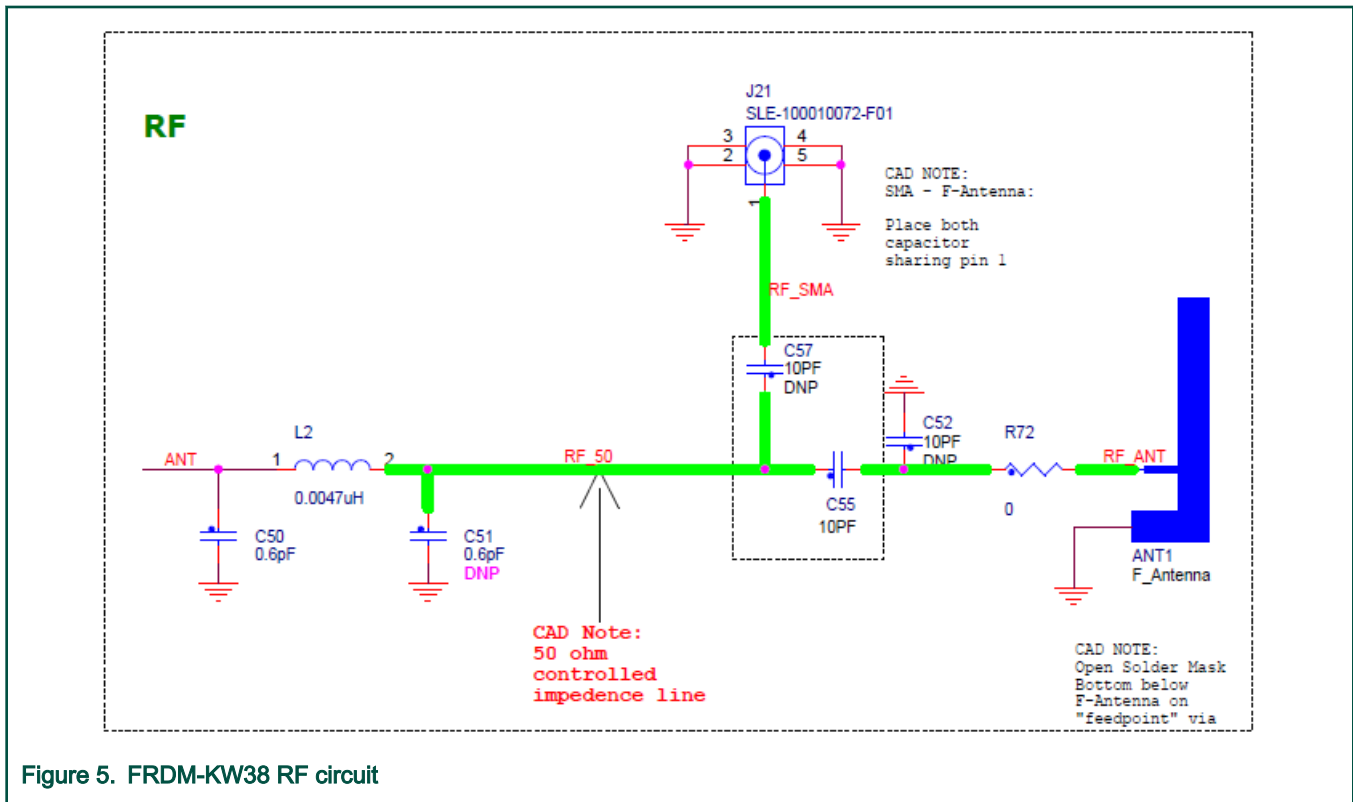

Figure 5. FRDM-KW38 RF circuit

3.2 Clocks

The FRDM-KW38 board provides two clocks. A 32 MHz for clocking MCU and Radio, and a 32.768 kHz to provide an accurate low power time base.

- 32 MHz reference oscillator
  - Figure 6 shows the 32 MHz external crystal Y1. The KW38A requires the frequency to be accurate less than ± 10 ppm. For more details, please refer to the device datasheet.
  - Internal load capacitors provide the crystal load capacitance. The internal load capacitor is adjustable which allows the center frequency of the crystal to be tuned.
  - To measure the 32 MHz oscillator frequency, program the CLKOUT (PTB0) signal to provide buffered output clock signal.

Figure 6. FRDM-KW38 32MHz oscillator circuit
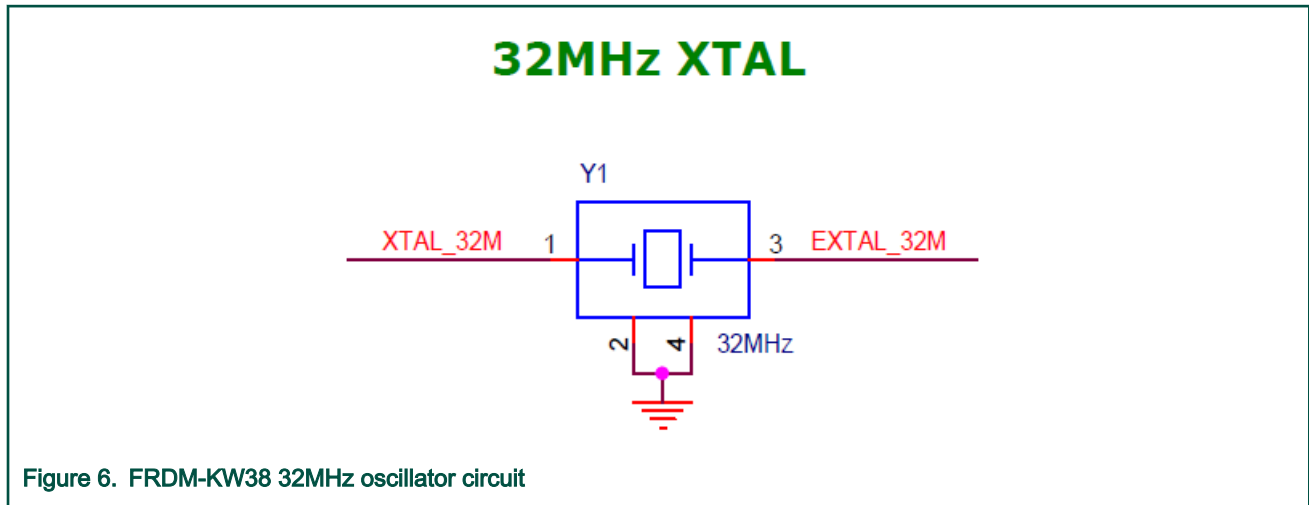
• 32.768 kHz Crystal Oscillator (for accurate low-power time base)

— A secondary 32.768 kHz crystal Y2 is provided (see Figure 7).

— Internal load capacitors provide the entire crystal load capacitance.

— Zero ohm resistors are supplied to bypass the Y2 crystal.

◦ This provides two extra GPIO to the I/O headers: PTB16 & PTB17.

Figure 7. FRDM-KW38 32.786 kHz oscillator circuit
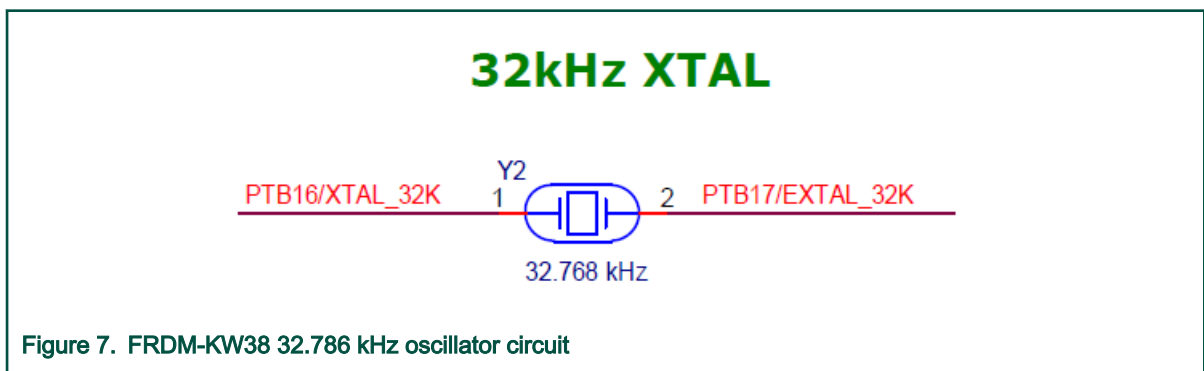
3.3 Power managemnt

There are several different ways to power and measure current on the FRDM-KW38 board. Figure 8 shows the FRDM-KW38 power-management circuit.
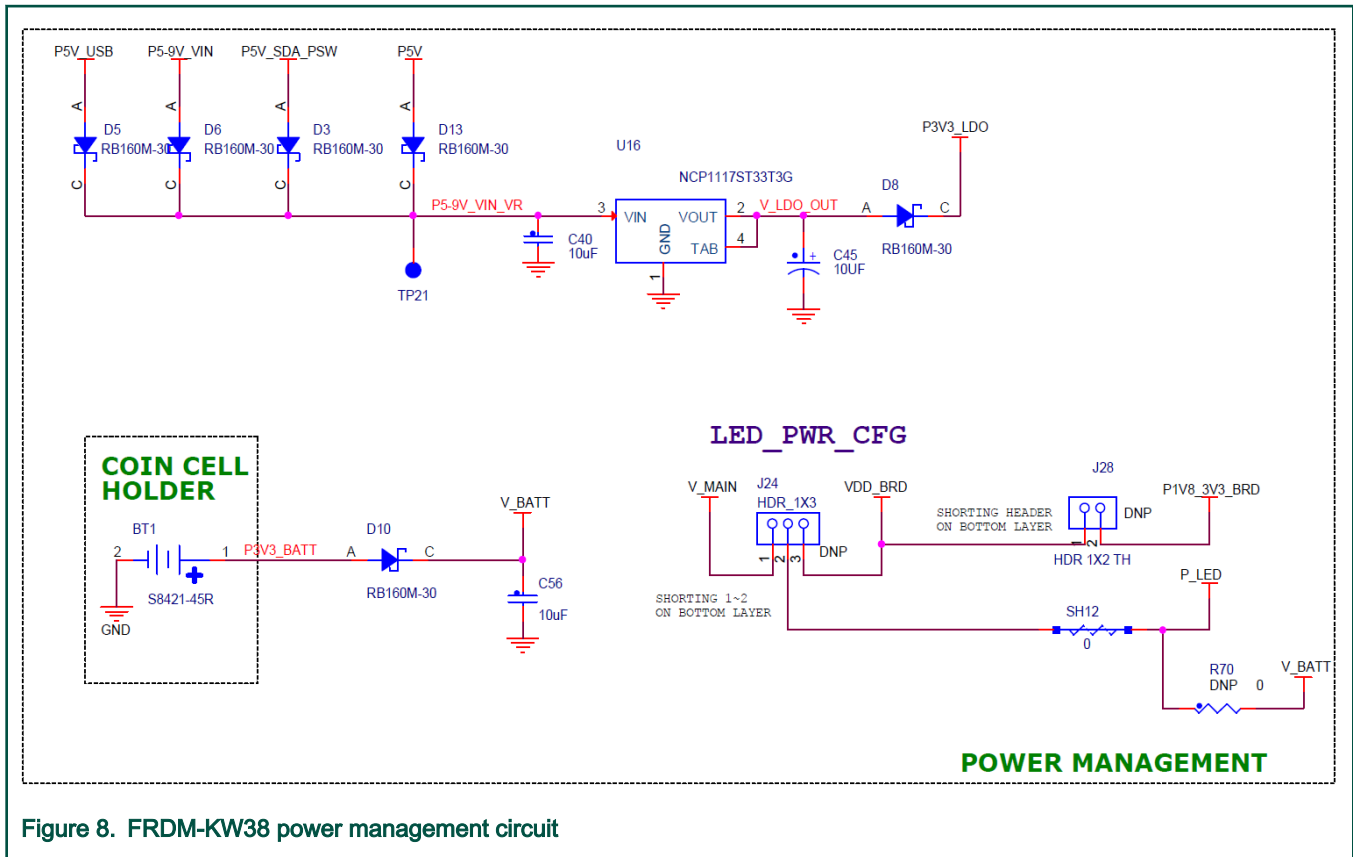
Figure 8. FRDM-KW38 power management circuit

The FRDM-KW38 can be powered by the following means:

- Through the micro USB type B connector (J11), which provides 5 V to the `P5V_SDA_PSW` signal into the 3V3 LDO (U16)

- Through the Freedom development board headers, which provide either P3.3 V or `P5-9V_VIN` on header J3 pin-8 to LDO 3V3 (U16)

- From an external battery (Coin-cell–CR2032). Use selector J35 pins 2-3.

- From an external DC supply in the following ways:

  — Connect an adapter that can supply 1.8 to 3.6 VDC to J35 pin 2. If the KW38 DC-DC is configured in buck mode, then, the voltage should be in the range of 2.1 V to 4.25 V.

  — Connect an adapter that can supply 12 V to the connector J32, J23 pin 3 or J13 pin 2. This option is to power CAN/LIN functionality in the board. At the same time, it also provides voltage to the regulator U15 which provides 5 V signal to P5V that also powers the KW38 through `P3V3_LDO` (U16). J35 needs to be in 1-2 position.

The jumper/headers J28 and J24 can supply current to various board components and can be used measure the current (if desired). Green LED marked as LED2 is available as a power indicator.

Power headers (J24, J28 and J35) can supply either the LED, MCU, or peripheral circuits. Measure the current by inserting a current meter in place of a designated jumper. See Table 5 for details on jumper descriptions.

The FRDM-KW38 can be configured to use either of the DCDC converter operating modes. These modes are Bypass, Buck (Manual-Start) and Buck (Auto-Start). Figure 9 to Figure 11 and Table 1 highlight the jumper settings for each of these modes. The board is configured in Buck (Auto-Start) by default. If different DCDC mode is desired, cut traces (bottom layer of the board) and jumpers (J27, J28, J29, J30, J31 and J38) should be populated in order to be able to configure the desired DCDC mode.
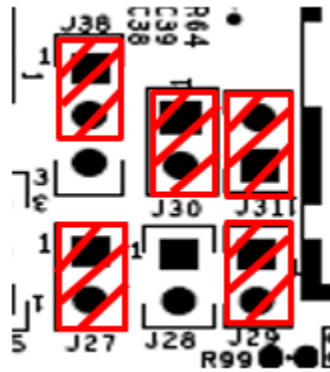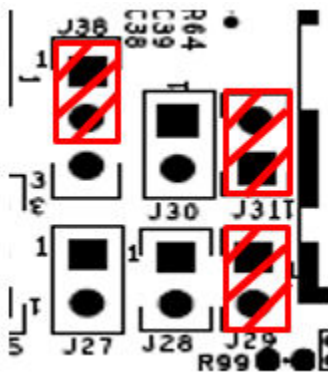
Figure 9. Jumper settings for Bypass mode

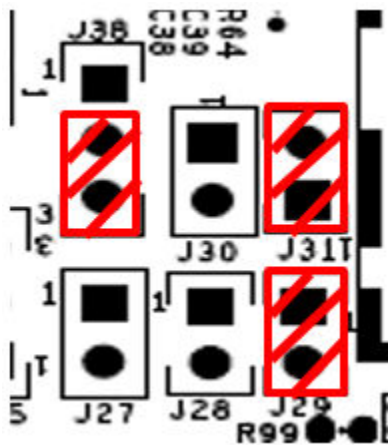Figure 10. Jumper settings for Buck mode (Manual-start)

Figure 11. Jumper settings for Buck mode (Auto-start)

Table 1 describs the DCDC mode jumper configurations.

Table 1. DCDC configurations

Mode	J38	J30	J27
Bypass Mode	1-2	ON	ON

Table continues on the next page...

Table 1. DCDC configurations (continued)

Mode	J38	J30	J27
Buck Mode (manual start)	1-2	OFF	OFF
Buck Mode (auto start)	2-3	OFF	OFF

3.3.1 Pswitch mode

This Pswitch mode allows the DCDC to be turned off **on the fly** while an application is running. When we turn the DCDC back on, it's just like doing a cold start on the KW3x. If the application demands, we can store some data in the NVM before turning off the DCDC.

Benefit of this power management is the device is Off, so very low power consumption (nA).

Example of Pswitch software modification in order to turn off DCDC by PSWITCH:

In the `board.c`, from line 297 (the function `BOARD_DCDCInit`):

```
void BOARD_DCDCInit(void)
{
#if gDCDC_Enabled_d == 1
    /* Initialize DCDC module */
    DCDC_Init(&mDcdcDefaultConfig);
    DCDC_InstallPSwitchCallback(pswitchCallback,gDCDC_PSwIntEdge_Rising_c);
#endif
}

void pswitchCallback(dcdcPSwStatus_t dcdcPSwStatus)
{
    for(int j=0; j<500000;j++); //A tempo is needed here for the Pswitch level to go low
    DCDC_ShutDown();
}
```

The line in green is the added line. Basically, a callback function is executed when an interruption on PSWITCH is triggered.

This interruption is triggered when there a transition from Low to High on PSWITCH, if it is triggered, the function pswitchCallback will be called. After a tempo, the DCDC will be turned OFF. The reason why this tempo is required is that we need to wait for the logic level on PSWITCH pin to return to Low.

Procedures:

- Poll on PSWITCH
- Start DCDC by getting PSWITCH high through switch SW4
- Measure usual power consumption
- When convenient (between two advertising), get PSWITCH low then write `0x3E77` in `DCDC_REG4`
- Measure DCDC OFF Power Consumption (~20 nA)
- Start DCDC by getting PSWITCH high through switch
- Measure usual power consumption

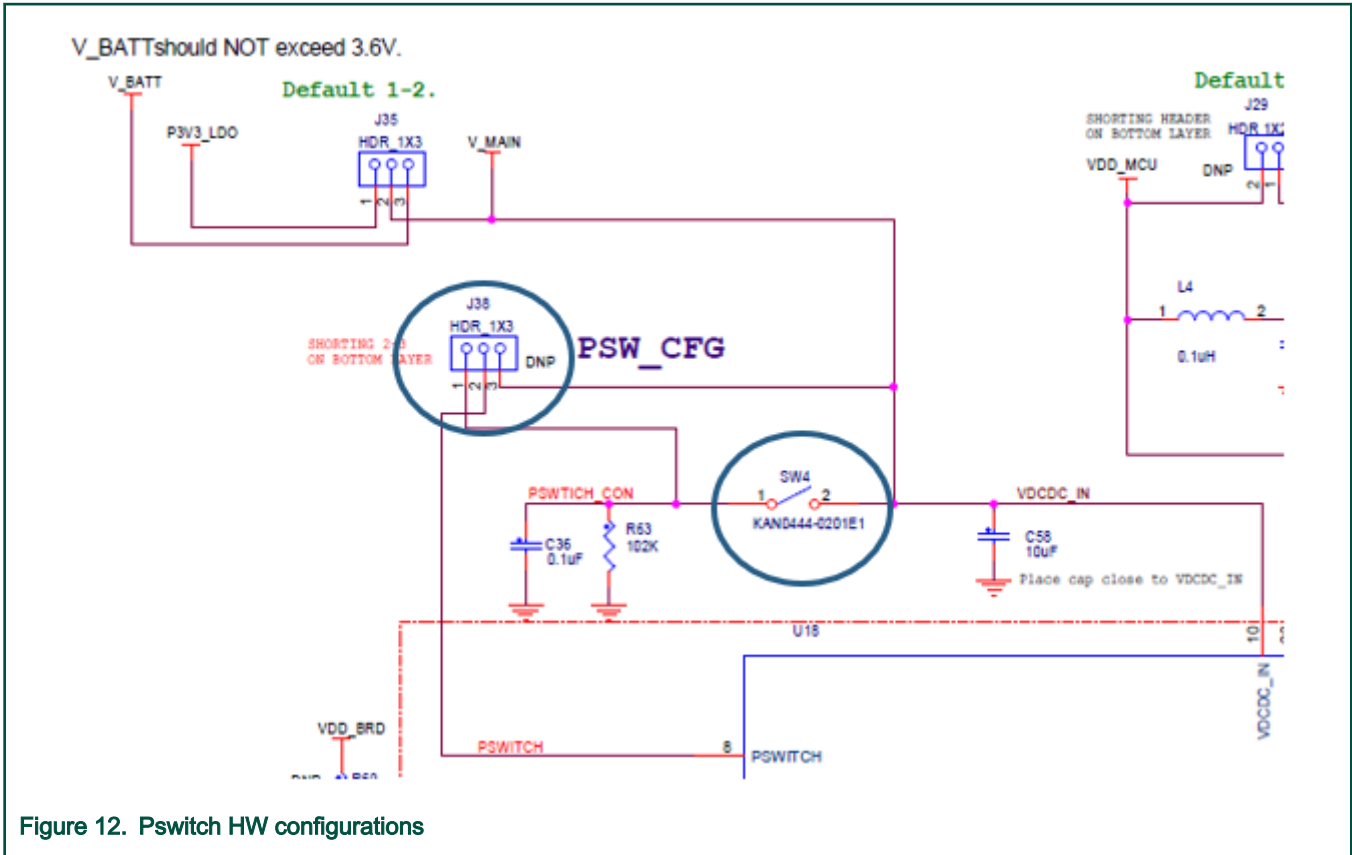Jumper J38 must be in position 1-2 (the default position is 2-3 in the FRDM-KW38 board).

Figure 12. Pswitch HW configurations

3.4 DCDC inductor (Buck mode)

For general application (car access for example), NXP recommends to use the 10 uH DCDC inductor from TDK (reference VLS4012CX-100M-1 serie): good performances (ESR, Isat) but quite **big** size.

It is indeed possible to use a smaller inductor size (WxLxH) but you need to be careful on the following items:

- ESR < 0.3 Ω
- Inductor value: 10 µH
- Saturation current > 300 mA

An alternative is the Wurth reference 744 025 100: Good performances (ESR, Isat), smaller than the TDK VLS reference but more expensive.

For keyfob application, NXP recommends to use the TDK MLZ2012N100LTD25 inductor: small size [SMD] for a better integration on small PCB with a thin design. It will prevent spurious from 100 KHz to 200 KHz which could interact with another reception device in the same board (for example, NXP LF device @125KHz).

Table 2. DCDC inductor selections

Inductor type	Value	Manufacturer	Reference	Automative qualified AEC-Q200	ESR (Ω)	Isat (mA)	Temperature range	Size (L × W × H) mm	Picture
Wound ferrite	10 uH	TDK	VLS4012CX-100M-1	Yes	0.19	890	-40 to +125 °C	4 × 4 × 1.2	

Table continues on the next page...

Table 2. DCDC inductor selections (continued)

Inductor type	Value	Manufacturer	Reference	Automative qualified AEC-Q200	ESR (Ω)	Isat (mA)	Temperature range	Size (L × W × H) mm	Picture
			iso VLS4012E						
SMD shielded multilayer ferrite	10 uH	TDK	MLZ2012N 100LTD25	Yes	0.3	110	-55 to +125 °C	2 × 1.25 × 0.85	
Wound shielded	10 uH	Wurth	744 025 100	Yes	0.19	1000	-40 to +125 °C	2.8 × 2.8 × 2.8	

3.5 Serial flash memory

Component U3 is the AT45DB041E 4-Mbit (512 KB) serial flash memory with SPI interface. It is intended for Over-the-Air Programming (OTAP) or for storing the non-volatile system data, or parameters.

Figure 13 shows the memory circuit:

- Memory power supply is `P1V8_3V3_BRD`.

- Discrete pull-up resistors pads for SPI port.

- You can share the SPI with other peripherals using the J1 I/O header.

- The SPI Write Protect and Reset has a discrete pull-up resistor.
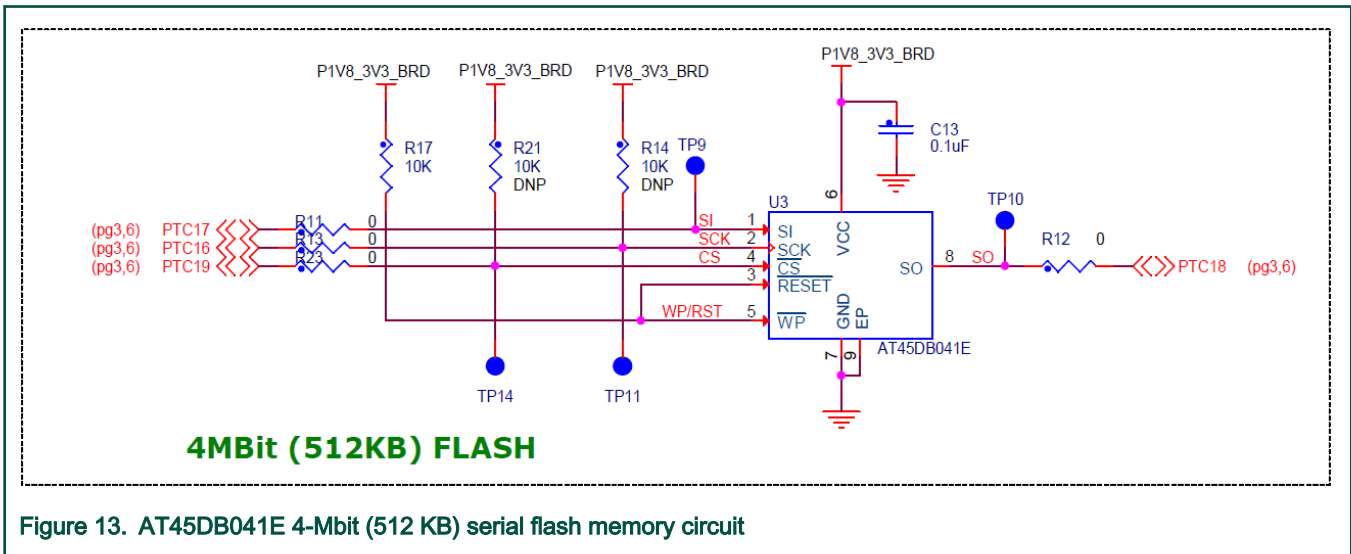
Figure 13. AT45DB041E 4-Mbit (512 KB) serial flash memory circuit

3.6 Accelerometer + Magnetometer combo sensor

Component U11 is NXP FXOS8700CQ sensor, a six-axis sensor with integrated linear accelerometer and magnetometer with very low power consumption, and selectable I^{2}C. Figure 14 shows the sensor circuit.

- The sensor powered by the P1V8_3V3_BRD rail.

- Discrete pull-up resistors for the I2 C bus lines are provided.

- Default address is configured as 0x1F:

— Address can be changed by pull-up/pull-down resistors on SA0 and SA1 lines.

- There is one interrupt signal routed.

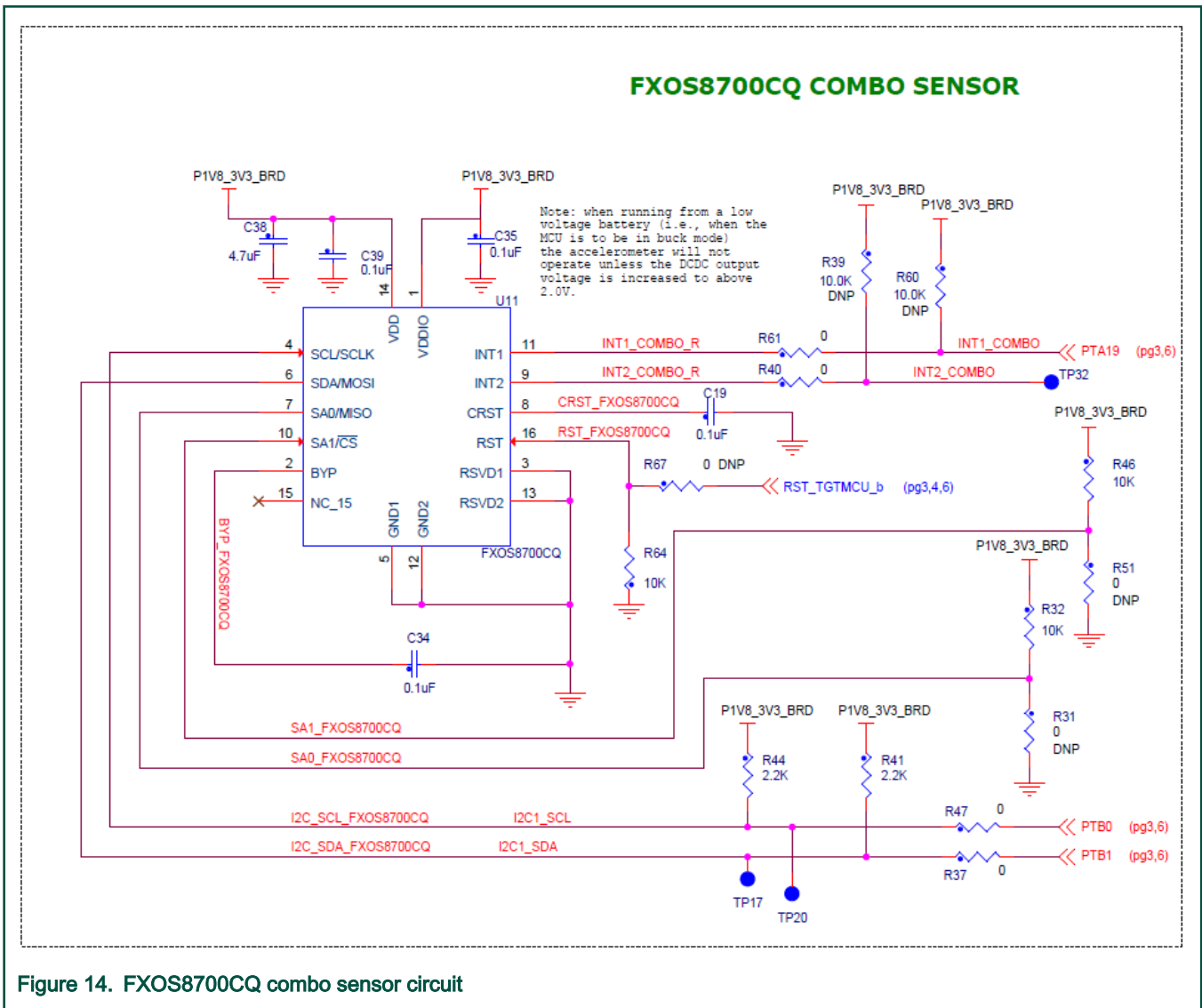- The I^{2}C can be shared with other peripherals through the J4 I/O header.

Figure 14. FXOS8700CQ combo sensor circuit

3.7 Thermistor

One thermistor (RT1) is connected to a differential ADC input (`ADC0_DP0` & `ADC_DM0`) of KW38A for evaluating the ADC module.
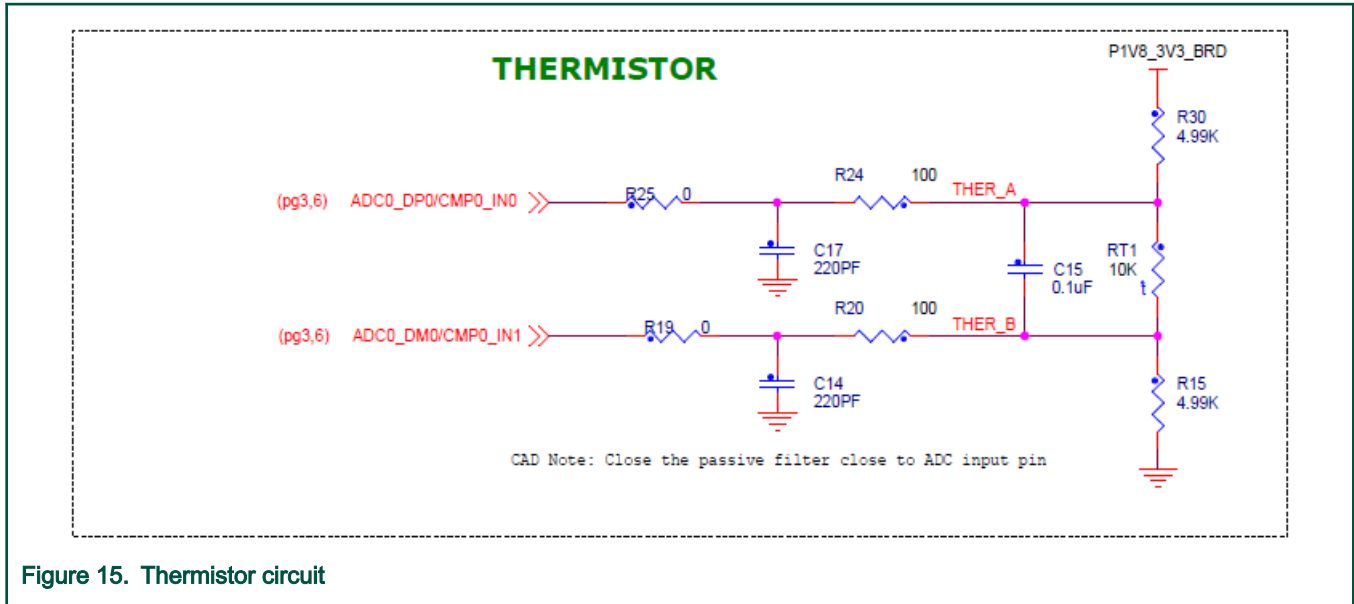
Figure 15. Thermistor circuit

3.8 User application LEDs

The FRDM-KW38 provides a RGB LED and a single Red LED for user applications. Figure 16 and Figure 17 show the circuitry for the application controlled LEDs.
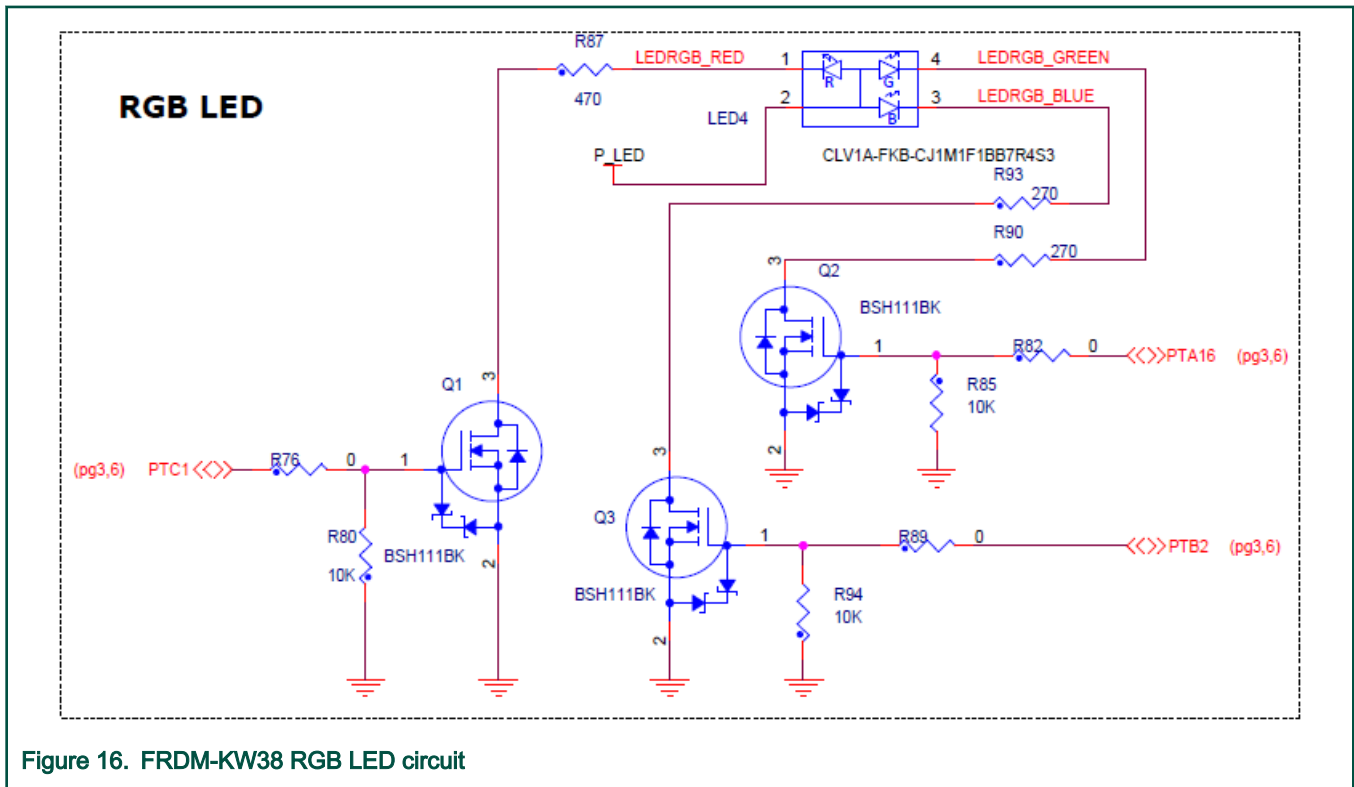
Figure 16. FRDM-KW38 RGB LED circuit
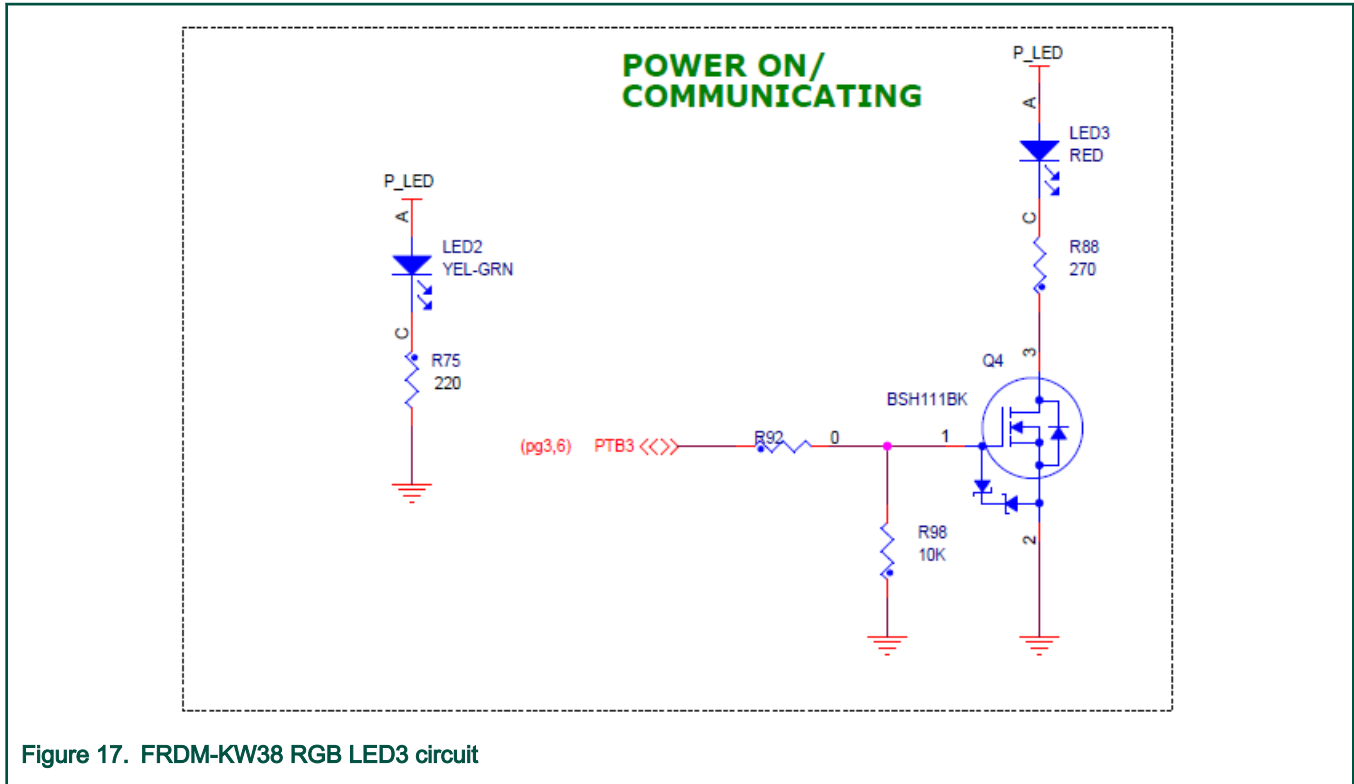
Figure 17. FRDM-KW38 RGB LED3 circuit

NOTE

When operating in default Buck configuration, the MCU would be operating at 1.8 V, which means that GPIO would be operating at 1.8 V. The LED circuitry allows proper behavior of the LEDs if `P_LED` is connected to `V_MAIN` with J24 in 1-2 position. The `V_MAIN` voltage should be at 3.3 V to work properly.

3.9 Interrupt pushbuttons

Two tactile buttons are populated on the FRDM-KW38 for Human Machine Interaction (HMI). Figure 18 shows the circuit for the tactile buttons.
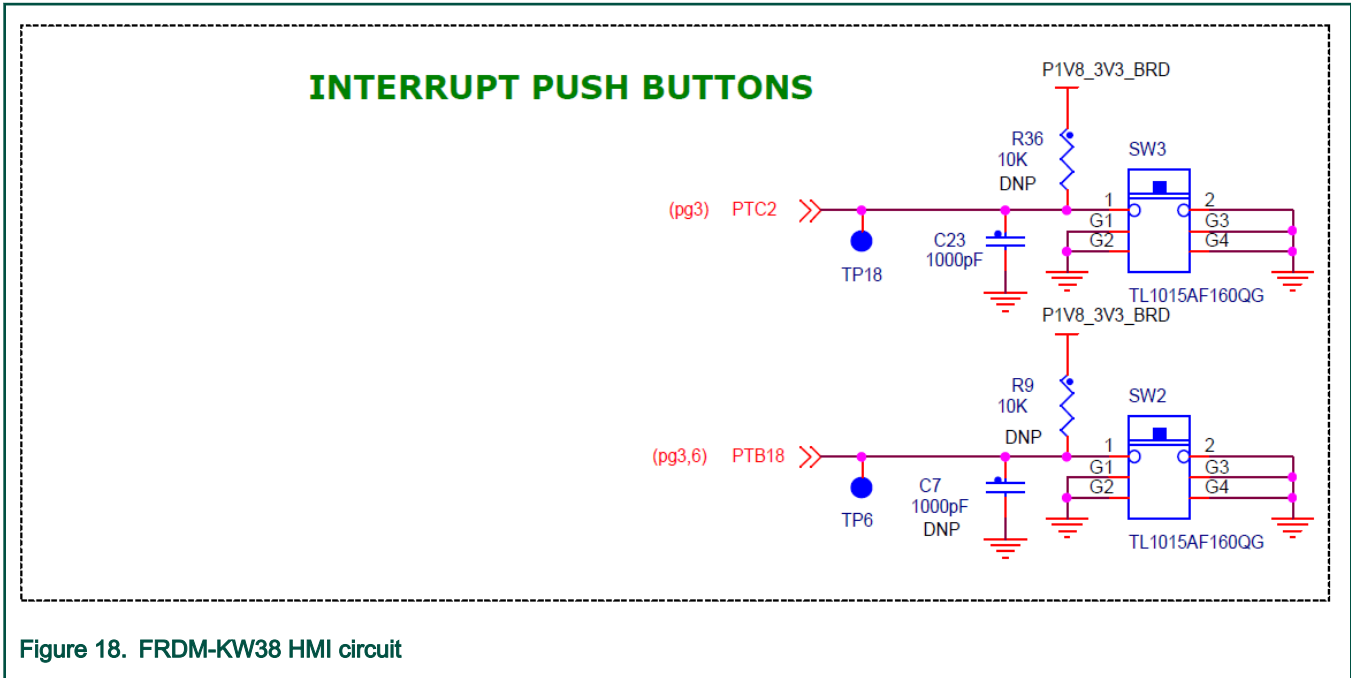
Figure 18. FRDM-KW38 HMI circuit

3.10 CAN/LIN power

As discussed in Power managemnt, the FRDM-KW38 can be powered through the J32, J23 pin 3 or J13 pin 2. The connector J32 is meant to be used as the power supply for the CAN and LIN interfaces. U15 is used to generates the P5V signal that CAN interface requires as per CAN physical requirements. P12V_BAT is used to supply the LIN transceiver as per LIN voltage domain. Figure 19 shows the CAN/LIN power circuit.

The P5V signal also goes to the regulator **U16** to generate P3V3_LDO to supply KW38 if J35 is set to 1-2 configuration.
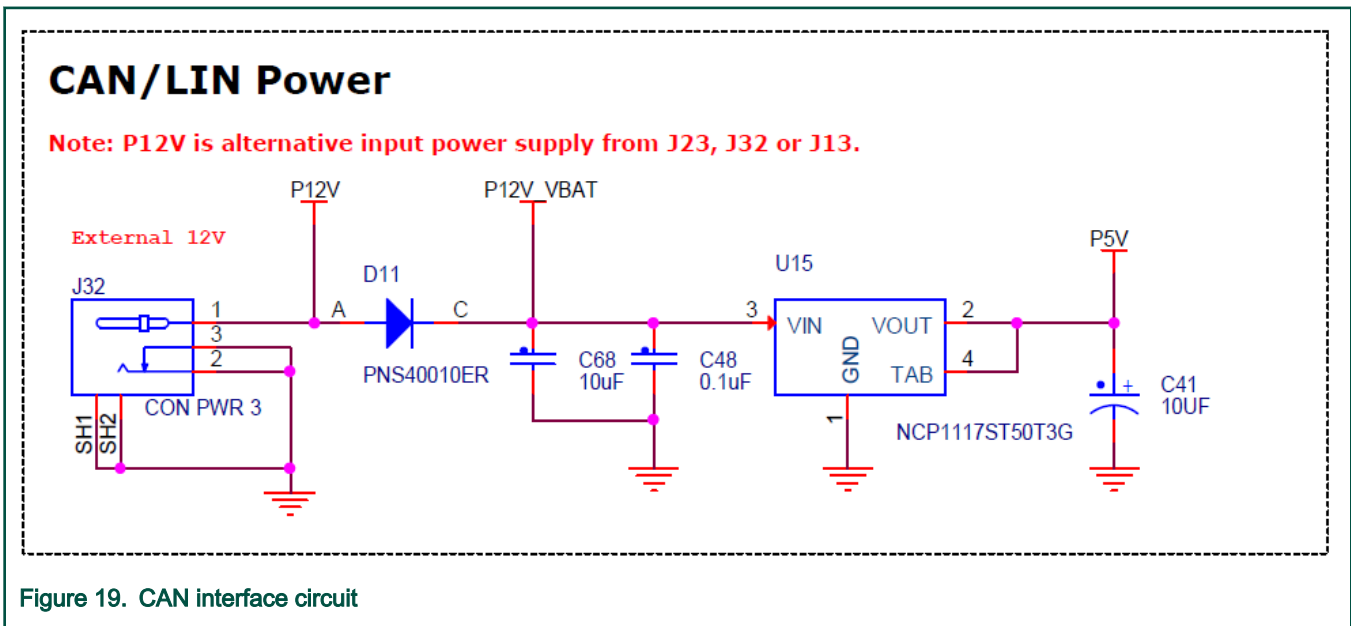
Figure 19. CAN interface circuit

NOTE

P12V signal can be also supplied through J23 pin 3 or J13 pin 2. Only one power input shall be chosen to supply P12V voltage (J32 or J23 or J13).

3.11 CAN interface

U19 is the NXP TJA1057 high speed CAN transceiver. It provides an interface between a Controller Area Network (CAN) protocol and the physical two-wire CAN bus. The transceiver is designated for high speed CAN applications in the automotive industry, providing the differential transmit and receive capability to a CAN protocol controller. shows the CAN Interface circuit.

- The TJA1057 power supply is P5V coming from the U15 (regulator) device.

- J23 provides pins to interface with a CAN bus.

- Pin 3 of the J23 can be used to power other FRDM-KW38 boards.

- Pin 3 of the J23 can be also used as an input to power the FRDM-KW38.

- CAN Interface is only functional if board is powered through the P12V signal which is supplied through J32, J23 or J13.
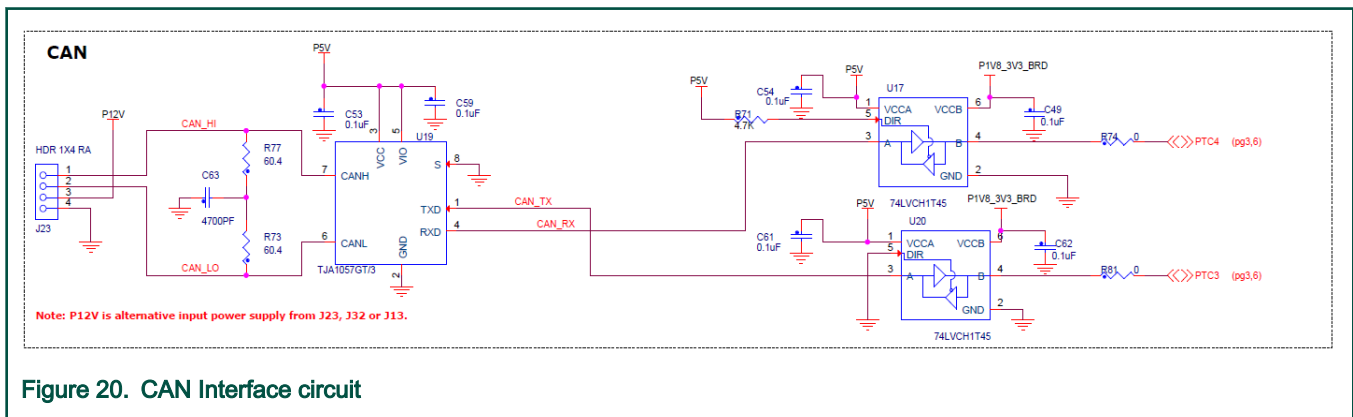
Figure 20. CAN Interface circuit

NOTE

Components U17 and U20 are level shifters to translate voltage level between KW38 and the NXP TJA1057 transceiver.

3.12 LIN interface

U10 is the NXP TJA1027 LIN 2.2A/SAE J2602 transceiver. It is the interface between the Local Interconnect Network (LIN) master/slave protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle sub-networks using baud rates up to 20kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602. Figure 21 shows the LIN Interface circuit.

- The TJA1027 power supply is P12V_VBAT coming from P12V.

- J13 provides pins to interface with a LIN network.

- J39 provides choice of the bidirectional RX LIN signal.

    — J39(1-2)(default): LIN J13-1 going to KW38 PTA17

    — J39(2-3): KW38 PTA17 going to LINJ13-1

- Pin 2 of the J13 can be used to power other FRDM-KW38 boards.

- Pin 2 of the J13 can be also used as an input to power the FRDM-KW38.

- LIN Interface is only functional if board is powered through the P12V signal which is supplied through J32, J23 or J13.

Figure 21. LIN Interface circuit
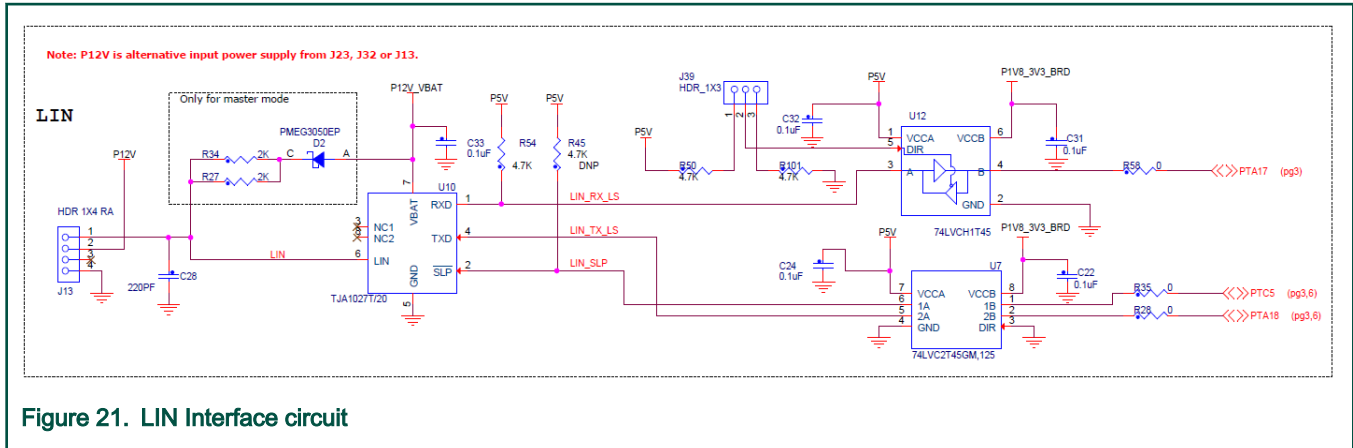
NOTE

Components U7 and U12 are level shifters to translate voltage level between KW38 and the NXP TJA1027 transceiver.

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4 Headers and jumpers

4.1 Arduino compatible I/O headers
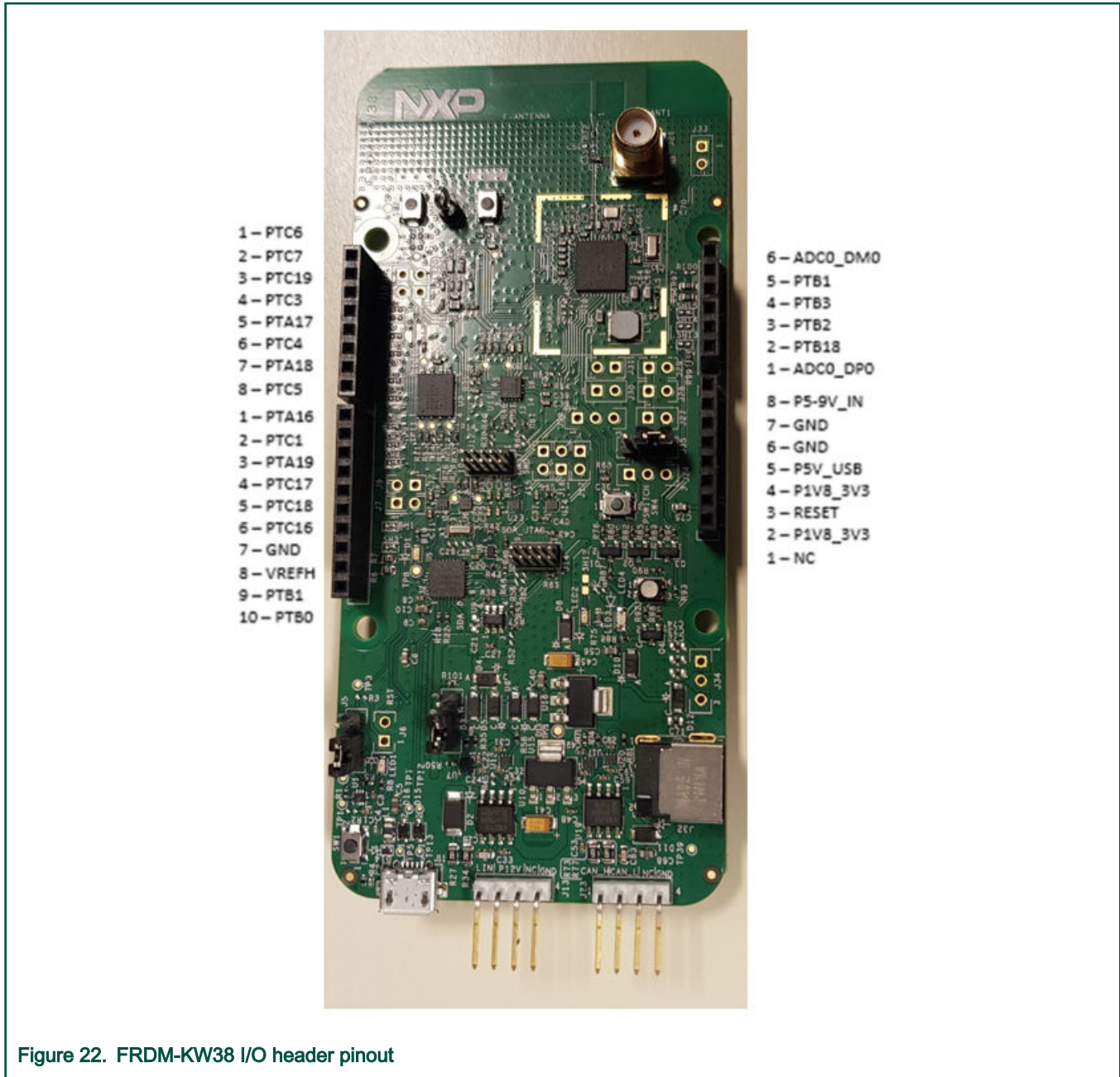
Figure 22 shows the I/O pinout.

Figure 22. FRDM-KW38 I/O header pinout

Table 3 and Table 4 show the signals that can be multiplexed to each pin.

Table 3. Arduino compatible header/connector pinout (J1 and J2)

HDR pin	1 × 10 connector (J2) - Description	IC pin
1	`PTA16/LLWU_P4/SPI1_SOUT/UART1_RTS_b/TPM0_CH0`	4
2	`PTC1/DIAG1/RF_EARLY_WARNING/ANT_B/I2C0_SDA/UART0_RTS_b/` `TPM0_CH2/SPI1_SCK/BSM_CLK`	37
3	`PTA19/ADC0_SE5/LLWU_P7/SPI1_PSC0/UART1_CTS_b/TMP2_CH1`	7

Table continues on the next page...

Table 3. Arduino compatible header/connector pinout (J1 and J2) (continued)

4	PTC17/LLWU_P1/RF_EXT_OSC_EN/SPI0_SOUT/I2C1_SCL/UART0_RX/ BSM_FRAME/DTM_RX/UART1_RX	46
5	PTC18/LLWU_P2/SPI0_IN/I2C1_SDA/UART0_TX/BSM_DATA/DTM_TX/ UART1_TX	47
6	PTC16/LLWU_P0/SPI0_SCK/I2C0_SDA/UART0_RTS_b/TPM0_CH3/ UART1_RTS_b	45
7	GND	—
8	VREFH/VREF_OUT	27
9	ADC0_SE1/CMP0_IN5/PTB1/RF_PRIORITY/DTM_RX/I2C0_SDA/ LPTMR0_ALT1/TPM0_CH2/CMT_IRO/CAN0_RX	17
10	PTB0/LLWU_P8/RF_RFOSC_EN/RF_DFT_RESET/I2C0_SCL/CMP0_OUT/ TPM0_CH1/CLKOUT/CAN0_TX	16
HDR pin	**1 × 10 connector (J2) - Description**	**IC pin**
1	PTC6/LLWU_14/RF_RFOSC_EN /I2C1_SCL/UART0_RX/TPM2_CH0/ BSM_FRAME	42
2	PTC7/LLWU_P15/SPI0_PCS2/I2C1_SDA/UART0_TX/TPM2_CH1/BSM_DATA	43
3	PTC19/LLWU_P3/RF_EARLY_WARNING/SPI0_PCS0/I2C0_SCL/ UART0_CTS_b/BSM_CLK/UART1_CTS_b	48
4	PTC3/DIAG3/LLWU_P11/RX_SWITCH/I2C1_SDA/UART0_TX/TPM0_CH1/ DTM_TX/SPI1_SIN/CAN0_TX	39
5	PTA17/LLWU_P5/RF_DFT_RESET/SPI1_SIN/UART1_RX/CAN0_TX/ TPM_CLKIN1	5
6	PTC4/DIAG4/RF_ACTIVE/LLWU_P12/ANT_A/EXTRG_IN/UART0_CTS_b/ TPM1_CH0/BSM_DATA/SPI1_PCS0/CAN0_RX	40
7	PTA18/LLWU_P6/SPI1_SCK/ UART1_TX/CAN0_RX/TPM2_CH0	6
8	PTC5/LLWU_P13/RF_RF_OFF/ LPTMR0_ALT2/UART0_RTS_b/TPM1_CH1/ BSM_CLK	41

Table 4. Arduino compatible header/connector pinout (J3 and J4)

HDR pin	1 × 8 connector (J2) - Description	IC pin
1	NC	—
2	IOREF(1V8_3V3)	—
3	PTA2/TPM0_CH3/RESET_b	3
4	1V8_3V3	—
5	5 V	—
6	GND	—
7	GND	—

Table continues on the next page...

Table 4. Arduino compatible header/connector pinout (J3 and J4) (continued)

HDR pin	1 × 10 connector (J2) - Description	IC pin
8	5-9 V IN	—
HDR pin	1 × 10 connector (J2) - Description	IC pin
1	`ADC0_DP0/CMP0_IN0`	24
2	`NMI_b/ADC0_SE4/CMP0_IN2/PTB18/UART1_CTS_b/I2C1_SCL/` `TPM_CLKIN0/TPM0_CH0`	23
3	`ADC0_SE3/CMP0_IN3/PTB2/RF_RF_OFF/ DTM_TX/TPM1_CH0`	18
4	`ADC0_SE2/CMP0_IN4/PTB3/UART1_RTS_b/CLKOUT/TPM1_CH1/RTC_CLKOUT`	19
5	`ADC0_SE1/CMP0_IN5/PTB1/RF_PRIORITY/DTM_RX/I2C0_SDA/` `LPTMR0_ALT1/TPM0_CH2/CMT_IRO/CAN0_RX`	17
6A	`ADC0_DM0/CMP0_IN1`	25
6B	`PTB0/LLWU_P8/RF_RFOSC_EN/RF_DFT_RESET/I2C0_SCL/CMP0_OUT/` `TPM0_CH1/CLKOUT/CAN0_TX`	16

NOTE

If the I^{2}C functionality is desired in J4 (pin 5 and pin 6). 6B needs to be routed to this pin, thus, resistor R97 should be removed and R100 shall be populated.

4.2 Jumper table

Table 5 describes the jumper settings on the FRDM-KW38. * denote jumper selection is shorted on board by default. Bold text indicates default selection.

Table 5. FRDM-KW38 jumper table

Jumper	Option	Setting	Description
J5	RST Button Bypass	**1-2** 2-3	**Reset button connected to OpenSDA** Reset button connected to Target MCU
J6	SDA_RST_TGTMCU	1-2*	Isolate OpenSDA MCU from target MCU reset signal
J15	SWD_CLK_TGTMCU	1-2*	Isolate SWD_CLK from SWD header
J16	SWD_DIO	1-2*	OpenSDA SWD_DIO isolation jumper
J17	SWD_CLK	1-2*	OpenSDA SWD_CLK isolation jumper
J24	`LED_PWR_CFG`	**1-2*** 2-3	**V_MAIN as a power supply for** `P_LED` **(LEDs on board).** `P_LED` is supplied from `VDD_BRD` (`VDD_1PV8OUT` pin) if

Table continues on the next page...

Table 5. FRDM-KW38 jumper table (continued)

Jumper	Option	Setting	Description
			DCDC is in buck mode. `V_MAIN` if in bypass.
J27	VDCDC_IN/VDD_MCU	1-2	Isolate `VDCDC_IN` from `VDD_1P8OUT` pin and `VDD_0/ VDD_1`.
J28	`VDD_BRD/P1V8_3V3`	**1-2***	**Isolate board supply from board peripherals**
J29	VDD_MCU	**1-2***	**Isolate `VDD_MCU`. It is also to measure `VDD_0` and `VDD_1` power consumption.**
J30	`VDCDC_IN/VDD_RFx`	1-2	Isolate `VDCDC_IN` from `VDD_RF1/RF2/RF3`.
J31	`VDD_RF`	**1-2***	**Isolate VDD_RF from `VDD_1P45OUT_PMCIN`.**
J35	`V_MAIN` selection	1-2 2-3	`P3V3_LDO` **as a power supply for `V_MAIN`. It can be also used to measure power consumption.** `V_BATT` as a power supply for `V_MAIN`. It can be also used to measure power consumption.
J7/J9	SPI IN/OUT	**J7-1 J7-2 / J9-1 J9-2*** J7-1 J9-2 / J7-2 J9-1	**SOUT to J2-4 / SIN to J2-5** SOUT to J2-5 / SIN to J2-4
J8/J10	UART RX/TX	**J8-1 J8-2 / J10-1 J10-2*** J8-1 J10-2 / J8-2 J10-1	**RX to J1-1 / TX to J1-2** RX to J1-2 / TX to J1-1

5 References

The following references are available on www.nxp.com/FRDM-KW38.

- FRDM-KW38 Design Package
- *Tuning I2C Timing In Slave Mode* (document AN12377)