



Product Change Notification - SYST-31DPZZ651

Date:

01 Apr 2020

Product Category:

8-bit Microcontrollers

Affected CPNs:



Notification subject:

ERRATA - ATtiny87/167 Silicon Errata and Data Sheet Clarification Errata Document Revision

Notification text:

SYST-31DPZZ651

Microchip has released a new Product Documents for the ATtiny87/167 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [ATtiny87/167 Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change: Updated the data sheet link in the Data Sheet Clarifications section

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 01 April 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[ATtiny87/167 Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

ATTINY167-A15MD
ATTINY167-A15MZ
ATTINY167-A15MZ-V01
ATTINY167-A15MZ-V02
ATTINY167-A15SZ
ATTINY167-A15XD
ATTINY167-A15XZ
ATTINY167-MMU
ATTINY167-MMUR
ATTINY167-MMURB20
ATTINY167-MU
ATTINY167-MUR
ATTINY167-SU
ATTINY167-SUR
ATTINY167-W-NG
ATTINY167-XU
ATTINY167-XUR
ATTINY87-A15MD
ATTINY87-A15MZ
ATTINY87-A15SZ
ATTINY87-A15XD
ATTINY87-A15XZ
ATTINY87-MU
ATTINY87-MUR
ATTINY87-SU
ATTINY87-SUR
ATTINY87-XU
ATTINY87-XUR



ATtiny87/167

ATtiny87/167 Silicon Errata and Data Sheet Clarification

Introduction

The ATtiny87/167 devices you have received conform functionally to the current device data sheet (<http://microchip.com/DS40002167>), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the ATtiny87/167 devices.

Note:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current.

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1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- X** Erratum is applicable.
- * This silicon revision was never released to production.

Peripheral	Short Description	Valid for Silicon Revision					
		ATtiny87			ATtiny167		
		Rev. A	Rev. B	Rev. C	Rev. A	Rev. B	Rev. C
System Clock and Clock Options	2.2.1 Gain Control of the Crystal Oscillator	*	*	X	*	*	X
	2.2.2 "Disable Clock Source" Command Remains Enabled	*	*	X	*	*	X

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- X** Erratum is applicable.
- * This silicon revision was never released to production.

2.2 System Clock and Clock Options

2.2.1 Gain Control of the Crystal Oscillator

The crystal oscillator (0.4 → 16 MHz) does not latch its gain control (CKSEL/CSEL[2:0] bits):

1. The “Recover System Clock Source” command does not return the CSEL[2:0] bits.
2. The gain control can be modified on the fly if CLKSELR changes.

Work around:

1. No work around.
2. As soon as possible, after any CLKSELR modification, rewrite the appropriate crystal oscillator setting (CSEL[3]=1 and CSEL[2:0] / CSUT[1:0] bits) in CLKSELR.

Example 2-1.

```
; Select crystal oscillator ( 16MHz crystal, fast rising power)
ldi temp1, ((0x0F<<CSEL0) | (0x02<<CSUT0))
sts CLKSELR, temp1
; Enable clock source (crystal oscillator)
ldi temp2, (1<<CLKCCE)
ldi temp3, (0x02<<CLKC0) ; CSEL = "0010"
sts CLKCSR, temp2 ; Enable CLKCSR register access
sts CLKCSR, temp3 ; Enable crystal oscillator clock
; Clock source switch
ldi temp3, (0x04<<CLKC0) ; CSEL = "0100"
sts CLKCSR, temp2 ; Enable CLKCSR register access
sts CLKCSR, temp3 ; Clock source switch
; Select watchdog clock ( 128KHz, fast rising power)
ldi temp3, ((0x03<<CSEL0) | (0x02<<CSUT0))
sts CLKSELR, temp3 ; (*)
; (*) !!! Loose gain control of crystal oscillator !!!
; ==> WORKAROUND ...
sts CLKSELR, temp1
; ...
```

Affected Silicon Revisions

ATtiny87							
Rev. A	Rev. B	Rev. C					
*	*	X					

ATtiny167							
Rev. A	Rev. B	Rev. C					

.....continued

ATtiny167							
*	*	X					

2.2.2 “Disable Clock Source” Command Remains Enabled

In the Dynamic Clock Switch module, the “Disable Clock Source” command remains running after disabling the targeted clock source (the clock source is set in the CLKSELR register).

Work around:

After a “Disable Clock Source” command, reset the CLKCSR register by writing 0x80.

Example 2-2.

```

; Select crystal oscillator
ldi temp1, (0x0F<<CSEL0)
sts CLKSELR, temp1
; Disable clock source (crystal oscillator)
ldi temp2, (1<<CLKCCE)
ldi temp3, (0x01<<CLKC0) ; CSEL = "0001"
sts CLKCSR,temp2 ; Enable CLKCSR register access
sts CLKCSR,temp3 ; (*) Disable crystal oscillator clock
; (*) !!! At this moment, if any other clock source is selected by CLKSELR,
; this clock source will also stop !!!
; ==> WORKAROUND ...
sts CLKCSR,temp2

```

Affected Silicon Revisions

ATtiny87							
Rev. A	Rev. B	Rev. C					
*	*	X					

ATtiny167							
Rev. A	Rev. B	Rev. C					
*	*	X					

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (<http://microchip.com/DS40002167>).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc Rev.	Date	Comments
B	03/2020	<ul style="list-style-type: none">Updated the data sheet link in the Data Sheet Clarifications section
A	01/2020	Initial release of this document. <ul style="list-style-type: none">Content moved from the data sheet and restructured to the new document templateUpdated the die revision list to reflect die revisions in production

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