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Lucent Technologies
Bell Labs Innovations

Field-Programmable Gate Arrays (FPGA) Qualification Manual

Lucent Technologies' Quality Policy

Lucent Technologies is committed to achieving sustained business excellence by integrating quality principles and methods into all we do at every level of our company to:

- **Anticipate and** meet customer needs and exceed their expectations, every time.
- **Relentlessly improve** how we work—to deliver the world's best and most innovative communications solutions—faster and more cost-effectively than our competitors.

Quality Principles

- **Customer Value—**Drive actions from a desire to serve customers. Know current and emerging needs. Understand why customers buy from us and why they don't, and act on that knowledge to deliver superior value.
- **Partnership—**Build long-term relationships with customers and strategic suppliers based on shared objectives.
- **Leadership—**Develop leaders who set high expectations, live by our Lucent Values, and create an environment for serving customers and achieving business excellence.
- **Ownership—**Become personally involved in the success of the business. Turn good ideas into better ways of doing business—working together, taking prudent risks, learning from mistakes, and implementing improvements based on what we learn.
- **Process—**Manage work with a focus on results—improving efficiency and productivity, delivering value to customers, and creating financial rewards for shareowners.
- **Improvement—**Make the plan-do-check cycle the way we operate—to achieve both continuous and breakthrough improvements in cost, cycle time, and quality.
- **Management by Fact—**Know what you want. Measure what you get. Act on the difference.
- **Results Orientation—**Establish and meet both short- and long-term commitments to all key stakeholders—customers, employees, shareholders, suppliers, partners, and society.

Shared Methods

- **Policy Deployment—**To set, deploy, and reach goals and align efforts company wide.
- **Process Management—**To manage, improve, and streamline how we work to deliver greater value to customers.
- **Problem-solving—**To close the gaps that separate us from our goal to be the industry leader.
- **Benchmarking—**To set meaningful standards and learn from the successful practices of best-in-class companies.
- **Management System Assessment—**To improve the way we manage the business through systematic evaluation, feedback, and action.

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Lucent Technologies' Quality Plan

The IC Division is committed to the ISO 9000-series quality system standards as a key element in attracting and retaining satisfied customers. Initially, we focused our efforts throughout the manufacturing locations, which were registered in 1993. In 1994 and 1995, we expanded our scope to include several of our worldwide design centers. These registrations and expansion plans are summarized in Table 1. We have also begun a two-year program to further expand our scope by registering additional worldwide design centers and our worldwide sales offices. These will be completed in 1997.

Table 1. ISO Registration Summary. (All of our manufacturing (mfg) facilities are ISO registered.)

Mfg Facilities	Yr.	Design Centers	Yr.	Sales Offices	Yr.
Madrid	93	Reading	93	Framingham	95
Singapore	93	Allentown	93	Santa Clara	96
Bangkok	93	Bracknell	94	Bracknell	96
Reading	93	Madrid	94	Munich	96
Orlando	93	Munich	94	Tokyo	97
Allentown	93	Santa Clara	95	Singapore	97
		Singapore	95	Berkeley Heights	97
		Taiwan	95	Allentown	97
		Framingham	96		
		Tokyo	97		

Lucent Technologies' Product Qualification Process

The process of qualifying a new product at Lucent Technologies is divided into two major efforts: qualification of a new technology and qualification of new device types or designs in the new technology.

Both of these qualifications are described in detail in this section.

Technology Qualification Plan

Lucent Technologies' Process Qualification Plan for both new wafer fabrication and package technologies involves rigorous environmental, mechanical, and electrical testing to confirm technology robustness. Industry-standard tests are applied to test devices. Specialized tests to examine electrostatic discharge and latch-up parameters are also incorporated.

Prior to qualification and manufacture of devices using a new process technology, thousands of ICs from different device types involving multiple wafer lots are subjected to extended reliability tests, and extensive generic reliability tests are conducted.

After the technology is introduced into manufacture, a continuous quality improvement program is begun. Improvements are introduced into the technology, with new issues of the technology put into effect at a rate of about one per year.

Reliability and yield studies are performed on a standard evaluation circuit (SEC).

Testing

Much of the evaluation of a new technology is done with an SEC. The SEC is tested with a very rigorous methodology, intended to ensure the device functions well beyond its intended operating range.

A voltage stress test is included to detect breakdown of any weak oxides. The device is required to be operational during this stress test. Functional testing is done before and after stress testing. Other tests are performed to detect low-level transistor leakage; these include a variety of hold time tests with various patterns. The same test routine is performed in at least three manufacturing stages: at wafer probe, after packaging, and at the end of reliability testing. Hold time and voltage guard band limits are built into the testing.

Lucent Technologies' Product Qualification Process (continued)

Intrinsic Reliability Data

Electromigration

Electromigration is a well-known failure mechanism that affects continuity or isolation of interconnections. Interconnections are allowed a maximum failure budget of 10 FITS at a junction temperature of 85 °C over 40 years.

This failure mechanism follows a log-normal distribution. Activation energies, standard deviations, and median times to failure are measured separately for each level in the interconnect structure. For failure rate calculations, the die dissipates about 2 W of power. Measurements are made with current levels 10 to 20 times higher than the maximum allowed by the current density design rules.

Hot Electron Effects

Device aging typically shows greater than 10 years to 10% Gm degradation under worst-case substrate current conditions. Actual devices should not be affected by charge injection mechanisms.

Mobile Ion Contamination

Mobile ion contamination is checked at wafer level using a triangular voltage sweep (TVS) procedure.

Time-Dependent Dielectric Breakdown (TDDB)

Extensive time-dependent dielectric breakdown measurements are made on specially designed large area test structures taken from the line monitor circuit. These devices are packed and put under test at electric fields as high as 6 mV/cm and temperatures as high as 150 °C. Both the thermal and voltage characteristics of the oxide failures are studied. The thermal activation energy is shown to be approximately 0.6 eV at an electric field of 6 mV/cm and a linear electric field acceleration parameter of three decades/(mV/cm). Correlations have been made with wafer-level tests using a gate oxide zone tester. This tester is used to routinely monitor oxide quality.

Lucent Technologies' Product Qualification Plan

Lucent Technologies' product qualification plan involves rigorous environmental, mechanical, and electrical testing to confirm product soundness.

Industry-standard tests, generally derived from military methods, are applied to test devices; additional specialized tests are administered to determine electrostatic discharge and latch-up sensitivity.

Table 2 presents a menu of tests from which a qualification plan for a new device is developed. It gives the sample size and lot tolerance percent defective (LTPD) for each test. The qualification process is administered by the Qualification Review Board (QRB) described in this section.

Depending upon whether the qualification is for a package, die, or process change—or for a change in fabrication facilities—the QRB determines the tests from Table 2 to be administered. Tests normally required for a new qualification can be satisfied by a reference to recent successful testing on a similar product under appropriate conditions. The QRB maintains a database called the Qualification Testing Results System (QTRS) that contains accurate records of each qualification.

The QRB is also responsible for the requalification of any changes in design, fabrication, or packaging of integrated circuit products. The requalification process implemented by the QRB is shown in Figure 1. Note that the QRB determines the seriousness of the change and supervises the requalification. Note also that the customer is involved in the requalification process.

Lucent Technologies' Product Qualification Process (continued)

Table 2. IC Qualification Tests

Test No./ Symbol	Test Description	Method	Sample Size	LTPD (%)
1. LT–1 or LT–2	High-Temperature Operating Bias, 125 °C High-Temperature Operating Bias, 150 °C	M-1005 M-1005	195 100	2 4
2. CL	CLASS (Component Lead Assembly Simulation)	A88AL1005	77	5
2a. C*n*PRE	Moisture Sensitivity Level	A88AL1005	77	5
3. BH	Temperature-Humidity Bias	A89AL0135	77	5
4. SB	Steam Bomb	A89AL0111	77	5
5. TC	Temperature Cycling	M-1010	77	5
6. TS	Thermal Shock	M-1011	25	15
7. MR	Moisture Resistance	M-1004	38	10
8. LK	Gross/Fine Leak	M-1014	38	10
9. SA	Salt Atmosphere	M-1009	15	15
10. WV	Internal Water Vapor	M-1018	5	50
11. RT	Low-Temperature Aging	A88AL1007	77	5
12. SE	Soft Error Rate	M-1032	10	—
13. PS	Photo Sensitivity	—	10	22
14. FL	Flammability and O_2 Index	*UL** 94 and ASTM 2863-77	—	—
15. SR	Solvent Resistance	M-2015	15	15
16. IV	Internal Visual	M-2014	5	50
17. PD	Physical Dimensions	M-2016	15	15
18. SD	Solderability	M-2003/ A89AL0006	4	—
19. MS	Mechanical Shock	M-2002	38	10
20. VF	Variable Frequency Vibration	M-2007	38	10
21. CA	Constant Acceleration	M-2001	38	10
22. SQ	Mechanical Sequence	—	38	10
23. LI	Lead Integrity	M-2004	15	15
24. BS	Bond Strength	M-2011	15	15
25. DS	Die Shear Strength	M-2019	5	50
26. XR	X-Ray	M-2012	5	50
27. TQ	End Torque	M-2024	15	15
28. ES	Electrostatic Discharge (ESD)	A91AL015/ X-19435	18	—
29. LU	Latch-up	A88AL1006	6	—

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

Qualification Review Board

All new IC devices fabricated in any manufacturing process technology, as well as any changes in a process technology, must be qualified under the administration of the Qualification Review Board (QRB).

The QRB is a committee of Lucent Technologies Bell Labs Innovations and Lucent Technologies representatives who deal with the procedures and issues related to qualification or requalification of silicon integrated circuit devices or processing technologies. Such a qualification must take place before the device or processing technology can be shipped.

A QRB is formed each time a new device type or process change is to be qualified. Each QRB consists of a core group, which defines the qualification needs, plus several additional members who act as auditors of the qualification and provide further expertise. The QRB may ask any member of Lucent Technologies to participate in a qualification review, should the need arise.

Every QRB includes experts in reliability engineering, design, or processing. It may also include specialists in packing, quality assurance, product engineering, processing, and electrostatic discharge phenomenon. All members must be satisfied with the completion of a qualification plan before they sign the completed plan. Control of product shipment prior to qualification, usually in the form of models, is the responsibility of the quality assurance representative of the QRB.

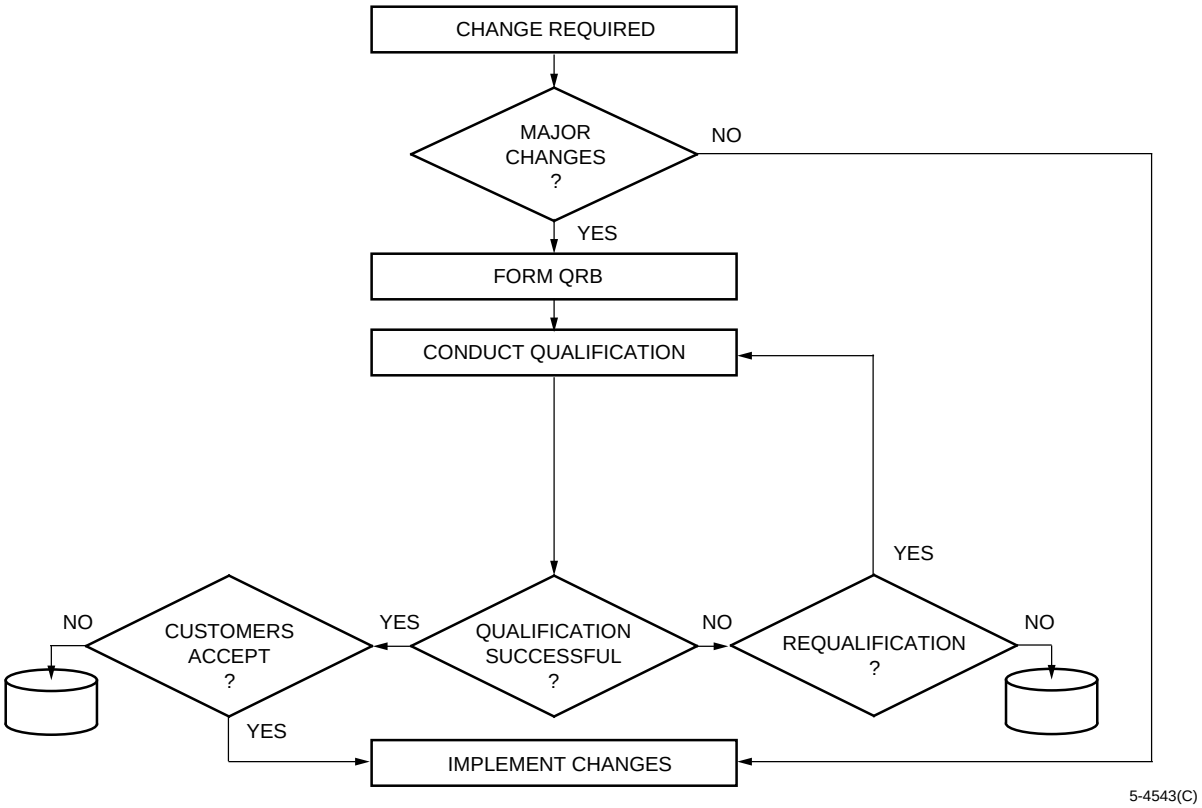

Figure 1. Requalification Process Flow

FPGA Product Qualification Plan

Lucent Technologies' product qualification plan for *ORCA*® and ATT3000 Series FPGAs involves rigorous environmental, mechanical, and electrical testing to confirm product soundness.

Industry-standard tests are applied to test devices. Specialized tests to examine electrostatic discharge and latch-up parameters are also incorporated.

Lucent Technologies' FPGAs are qualified by a four-phase process: Lucent Technologies' 0.6 µm/0.55 µm/0.5 µm/0.35 µm CMOS processes, the design of the device itself, and the performance of a given die in a given package.

Since all Lucent Technologies FPGAs are manufactured using the Lucent Technologies 0.6 µm, 0.55 µm, 0.5 µm, or 0.35 µm CMOS processes, they are carefully monitored and tested. Regarding device design, since each of the devices in each series of FPGAs (ATT3000, ATT1Cxx, ATT2Cxx, ATT2Txx, OR2CxxA, or OR2TxxA) is a matrix of repetitive elements, the QRB determined that qualifying one of the six dies would qualify the design for the product family.

Finally, the QRB determined the qualification testing necessary to qualify each die in a given package. Industry-standard tests were chosen, based on prior qualifications with the given package for prior CMOS designs in the same technology.

For example, if a prior qualification of a 0.6 µm CMOS design had been performed with a larger die than the one in question, the only new tests needed would be electrostatic discharge (ESD) and latch-up.

However, if the die to be qualified was the largest 0.6 µm CMOS design to be put in that package, more extensive testing would be required. A table of the tests performed is included in the section on package qualification.

0.35 µm, 0.5 µm, 0.55 µm, and 0.6 µm CMOS Process Qualifications

Introduction

This section presents quality and reliability information for Lucent Technologies' 0.35 µm, 0.5 µm, 0.55 µm, and 0.6 µm advanced CMOS processes. These processes employ N- and P-channel LDD MOS transistors. The 0.35 µm and 0.5 µm processes also use three levels of metal, and the 0.55 µm and 0.6 µm processes use two levels of metal.

These technologies have been rigorously tested for reliability and manufacturability. Prior to qualification and manufacture of devices using these process technologies, approximately 10,000 devices were subjected to extended reliability tests and extensive generic reliability tests.

After introduction into manufacture, a continuous quality improvement program was begun. This report concentrates on the latest version of the technologies. New improvements are introduced into the technologies, with new issues put into effect at a rate of about one per year.

As part of the processes' qualification, the following tests are performed.

High-Temperature Operating Bias (HTOB)

The main vehicle for studying HTOB is the standard evaluation circuit (SEC). After testing, the failed parts were examined with physical FMA techniques. On the SEC, electrical failure modes are easily correlated with failure locations. The failing parts were taken through electrical and physical FMA. Gate-level defects are caused by silicon particles at the gate level. Several programs are now in place to attack gate-level defects.

Temperature Humidity Bias (THB)

Temperature humidity bias testing was performed on the SEC per Lucent Technologies' requirements of static bias at 85 °C and 85% relative humidity. THB is known to induce mechanical stress effects due to expansion of the plastic due to water absorption.

Temperature Cycling (TC)

Temperature cycling was performed per MIL-STD-883C, Method 1010, Condition C.

Thermal Shock (TS)

Thermal shock was performed per MIL-STD-883, Method-1011, which requires –65 °C to +125 °C, liquid to liquid, for 100 cycles.

Steam Bomb (SB)

Steam bomb testing was run on the SEC test chips.

Bond Strength (BS) and Die Shear (DS)

Bond strength was tested per the usual procedure in the models packaging shop at Allentown, PA. All packages for reliability evaluation were packaged at this shop. Die shear strength was also measured on these devices.

Summary

The latest issues of the 0.35 µm, 0.5 µm, 0.55 µm, and 0.6 µm CMOS technologies meet or exceed requirements for qualification in all critical areas.

Infant mortality and long-term failure rates have decreased significantly with the lots processed with this log, and it is expected that further improvements will be made as part of a continuous quality improvement program.

1.2 µm EEPROM CMOS Process Qualification

Introduction

This section presents quality and reliability information for the 1.2 µm EEPROM CMOS process used to fabricate the ATT1700A family of serial PROMs. As part of process qualification, the following tests are performed.

High-Temperature Operating Bias (HTOB)

The main vehicle for studying HTOB is the standard evaluation circuit (SEC). After testing, the failed parts were examined with physical FMA techniques. On the SEC, electrical failure modes are easily correlated with failure locations. The failing parts were taken through electrical and physical FMA. Gate-level defects are caused by silicon particles at the gate level. Several programs are now in place to attack gate-level defects.

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Temperature Cycling (TC)

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Thermal Shock (TS)

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Steam bomb testing was run on the SEC test chips.

Bond Strength (BS) and Die Shear (DS)

Bond strength was tested per the usual procedure in the models packaging shop at Allentown, PA. All packages for reliability evaluation were packaged at this shop. Die shear strength was also measured on these devices.

Summary

This latest issue of the 1.2 µm CMOS technology meets or exceeds requirements for qualification in all critical areas.

Device Qualification Testing

Overview

Lucent Technologies' product quality program for the ATT3000 and *ORCA* Series FPGAs requires that the devices undergo a rigorous testing program prior to introduction. The program includes a series of life and environmental tests designed to accelerate failure probabilities in the die and package. As part of device qualification, the following tests are performed:

Environmental Tests

- High-Temperature Operating Bias (HTOB) 150 °C, 4.1 V (3.3 V devices) or 150 °C, 6.2 V (5.0 V devices)
- Component Lead Assembly Simulation Sequence or CLASS (CL)
- Moisture Sensitivity Level (C*n*PRE) 30 °C to 85 °C/ 60% RH to 85% RH/6 hrs. to 168 hrs.
- Temperature Humidity Bias (THB) 85 °C/85% RH
- Autoclave (SB) 121 °C, 2 ATM
- Temperature Cycling (TC) –65 °C to +150 °C (air to air)
- Thermal Shock (TS) –55 °C to +125 °C (liquid to liquid)
- Moisture Resistance (MR)
- Salt Atmosphere or Corrosion (SA)

Mechanical Tests

- Flammability and O2 Index (FL)
- Solvent Resistance (SR)
- Physical Dimensions (PD)
- Solderability (SD)
- Bond Strength (BS)
- Die Shear Strength (DS)
- X-Ray (XR)

Electrical Tests

- Electrostatic Discharge (ESD) for Each Pin
- Latch-up (LU)

The specific tests used to qualify devices such as the Lucent Technologies' FPGA product family are described below. Test characteristics, parameters, allowed failure rates, and other details are included.

Failure mode analysis (FMA) is used as an integral part of quality testing and surveillance to assess any performance flaw, determine corrective measures, and implement these measures to eliminate recurrence.

Test results are presented in the following section.

Environmental Tests

High-Temperature Operating Bias (HTOB)

HTOB testing, also called dynamic life testing, is performed at 150 °C/4.1 V (3.3 V devices) and 150 °C/ 6.2 V (5.0 V devices) to provide acceleration over the condition of use.

Dynamic operating life stress is considered to be more representative than static stress because the continual switching of internal circuit nodes more closely approximates the operation of the device in an actual system.

Component and Lead Assembly Simulation Sequence or CLASS (CL)

This test involves heating, infrared solder simulation, and lead bending. It is a preconditioning test for THB.

Moisture Sensitivity Level (C*n*PRE)

Moisture sensitivity level of a part is evaluated during the CLASS testing using JEDEC method A-113. This is summarized in Table 3.

Table 3. Moisture Sensitivity Levels

Moisture Sensitivity Level	Allowable Exposure to Moisture at Customer's Assembly Site	Moisture Exposure During Qualification Testing
1	Unlimited storage at up to 90% RH and 30 °C	168 hrs. at 85% RH and 85 °C
2	One year storage at up to 60% RH and 30 °C	168 hrs. at 60% RH and 85 °C
3	Up to 1 week storage at up to 60% RH and 30 °C	192 hrs. at 60% RH and 30 °C
4	Up to 3 days storage at up to 60% RH and 30 °C	78 hrs. at 60% RH and 30 °C
5	Up to 1 day storage at up to 60% RH and 30 °C	48 hrs. at 60% RH and 30 °C
6	Up to 6 hrs. storage at up to 60% RH and 30 °C	6 hrs. at 60% RH and 30 °C

Device Qualification Testing (continued)

Temperature Humidity Bias (THB)

Because a plastic package is inherently nonhermetic, the penetration of ambient moisture could damage the device due to galvanic action. Thus, temperature humidity bias and autoclave (steam bomb) tests are used to accelerate moisture ingression in order to determine the tolerance of the die to its presence.

THB testing is performed at an ambient temperature of 85 °C and a relative humidity of 85%. The sample devices are tested for 1,000 hours at 5 V, and go through presoak at 85 units/85 units for 96 hours.

Autoclave (SB)

Autoclave, also known as steam bomb, is a storage test employing the environmental conditions of T_A = 121 °C, 100% relative humidity, and 15 psig. This test is used as an additional stringent test to measure the moisture resistance of the packaging system and the susceptibility of the die to corrosion. As with THB testing, both package integrity and actual die construction play major roles in the results.

Temperature Cycle (TC)

The compatibility of materials used in the fabrication of any device is essential to that device's reliability. Any appreciable mismatch in physical properties, such as thermal expansion coefficients, can cause long-term device failures.

In the temperature cycle test, devices are subjected to temperature extremes of –65 °C to +150 °C in nitrogen-filled chambers. One test cycle consists of a 10-minute dwell at each temperature extreme plus a transition time of approximately five minutes.

The gradual change of temperature and relatively long dwell times in an air ambient tend to uncover problems related to expansion rate differentials. Devices are electrically tested after 100 cycles.

Thermal Shock (TS)

Just as with the temperature cycle test, the thermal shock test is designed to reveal differences in expansion coefficients for components of the packaging system. However, thermal shock creates a more severe stress in that the device is exposed to a sudden change in temperature due to the high thermal conductivity and capacity of the liquid ambient.

Devices are placed in a fluorocarbon bath cooled to –65 °C. After remaining in the cold chamber for at least five minutes, the sample is transferred to an adjacent chamber filled with fluorocarbon at 125 °C and is held for an equivalent time. After 100 cycles, thermal shock end-point testing is performed.

Moisture Resistance (MR)

This test evaluates, on an accelerated schedule, how well component parts and constituent materials resist deterioration from the high temperature and humidity that is typical of tropical environments. The test differs from the steady-state humidity test and derives its added effectiveness by employing temperature cycling, which alternates periods of condensation and drying. This is essential to developing the corrosion process and, in addition, produces a breathing action of moisture into partially sealed containers. The test is carried out per MIL-STD-883C (method 1004).

Salt Atmosphere or Corrosion (SA)

This test is an accelerated laboratory corrosion test. It simulates the effects of seacoast atmosphere on devices and package elements. The test is carried out per MIL-STD-883C (method 1009).

Low-Temperature Aging (RT)

This test studies device aging due to hot carrier effects. Since it is well known that hot carrier effects are more pronounced at lower temperatures, the devices are aged at –10 °C for 1,000 hours.

Mechanical Tests

Flammability and O2 Index (FL)

This test follows *UL* 94 and ASTM 2863-77 methods.

Solvent Resistance (SR)

This test is performed per MIL-STD-883C (method 2015). Its purpose is to verify that the marking on the component parts will not become illegible when the parts are subjected to solvents. It also seeks to ensure the solvents will not cause deleterious mechanical or electrical damage, or deterioration of the materials or finishes used in the part.

Device Qualification Testing (continued)

Physical Dimensions (PD)

This test is performed to verify that the external physical dimensions of the device are in accordance with the applicable procurement document. The test is carried out per MIL-STD-883C (method 2016).

Solderability Test (SD)

This test is conducted to determine the solderability of all terminations normally joined by soldering. The determination is made on the basis of the ability of these terminations to be wetted or coated by solder.

Test procedures verify whether treatment during the manufacturing process to facilitate soldering is satisfactory, and that such treatment has been applied to the required portion of the part which is designed to accommodate a solder connection.

The test includes an accelerated aging test which simulates at least six months' natural aging under a combination of storage conditions, each designed to produce particular deleterious effects. This test is carried out per MIL-STD-883C (method 2003).

Bond Strength (BS)

This test measures bond strength and evaluates bond strength distributions, and can therefore be used to determine compliance with specified bond strength requirements of the product's acquisition document. The test is carried out per MIL-STD-883C (method 2011).

Die Shear Strength (DS)

This test determines the integrity of materials and procedures used to attach semiconductor die or surface-mounted passive elements to package headers or other substrates. It is carried out per MIL-STD-883C (method 2019).

X-Ray (XR)

This examination is performed to nondestructively detect defects within the sealed case, especially those resulting from the sealing process. It is also performed to discover internal defects such as foreign objects, improper interconnecting wires, and voids in the die attach material or in the glass when glass seals are used. The test is carried out per MIL-STD-883C (method 2012).

Electrical Tests

ESD Human-Body Model as per Lucent Technologies Method A97AL1494

Described later in this section, this qualification requires that each pin in the package be protected up to 1000 V from electrostatic discharge caused by human contact.

ESD Charged-Body Model as per Lucent Technologies Method A97AL1494

Described later in this section, this qualification requires that each pin in the package be protected up to 1000 V from electrostatic discharge from any charged surface.

Latch-Up as per Lucent Technologies Method A88AL1006

Described in detail later in this section, latch-up stressing includes three components:

- dc stressing of all inputs, outputs, and I/O pins
- Power supply overvoltage stressing
- Poststress ATE testing

Three unstressed, fully functional devices are used for each of the first two tests. A device is considered latched up if, due to the application of stress, the I_{CC} current exceeds the manufacturer's maximum I_{CC} current and remains at that level after the stress is removed. After three devices each are stressed using Test 1 and Test 2, all six devices must be functionally and parametrically retested per Test 3.

Table 4. Latch-Up Qualification Summary

Test	Test Type	Stress Limits*	
1	I/O Stress	200 mA	≤1.5 Vmax
2	Power Supply Overvoltage	1.5 Vmax	≤300 mA
3	Poststress ATE	Must Pass	

* Refer to the Latch-Up Test Details section on page 16.

Details of Electrostatic Discharge (ESD) Tests

ESD Test Methods and Requirements

Source: Lucent Technologies Bell Laboratories Specification A97AL1494

Purpose

This specification describes a uniform method for establishing electrostatic discharge (ESD) withstand thresholds. It also includes threshold requirements and reporting procedures. A97AL1494 includes pertinent graphics.

Scope

All packaged semiconductor devices, thin-film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, and hybrid integrated circuits (HICs) containing any of these devices are to be evaluated according to this specification. The device thresholds are to be reported in the product design information (PDI) document. Device thresholds and corner pin thresholds are to be reported in the appropriate qualification documents.

Product Design Information (PDI)

The PDI is the official Lucent Technologies document in which the responsible design and manufacturing organizations agree that the product information contained therein satisfies manufacturing, legal, and regulatory requirements; it also places certain manufacturing documents under formal change order control.

ESD testing is conducted before transmitting new PDIs and when existing PDIs are reissued due to process, design, packaging, or specification changes. Tests are conducted on the device and package that represent the product in all details presented in the PDI.

Types of Testing

Two types of testing are required:

- Human-body model (HBM)
- Charged-device model (CDM)

Pin Combinations to Be Tested

For the human-body model, ESD stressing is performed according to the pin combinations outlined in accordance with Mil-Std-883, method 3015, EOS/ESD Association S6.1, and EIA/JESD22-A114:

- Stress each input (or output) pin while grounding all power supply pins
- Stress each power supply pin while grounding each differently named supply pin (or group of pins)
- Stress each input (or output) pin while grounding all output (or input) pins.

The power supply pins include V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, and V_{REF}. Pins such as offset adjust, compensation, clocks, controls, address, data, and input are considered input pins. Output and input/output pins are considered output pins. In addition, do not test no connects (NCs). For the charged-device model (CDM), test each pin.

Voltage levels for HBM ESD testing include:

100 V	500 V	2000 V
200 V	1000 V	4000 V

Voltage levels for CDM ESD testing include:

100 V	500 V	2000 V
200 V	1000 V	

Any devices that fail at 500 V are tested further at 100 mV increments to determine threshold value.

Test Procedure Overview

At least six devices are needed to obtain the HBM and CDM thresholds; prepare at least three of these for HBM testing and at least three more for the CDM tests. Carry out all testing at room temperature. Circuit schematics for HBM and CDM testing are shown in Figure 2 and Figure 3, respectively.

Details of Electrostatic Discharge (ESD) Tests (continued)

Specific Test Procedure: HBM

Insert the first device under test (DUT) into the socket as shown in Figure 2. Start with the recommended voltage or with any desired level, as discussed above. At each voltage level, stress all pin combinations as described earlier in this section.

At each voltage level, apply one pulse of each polarity with a minimum 0.3 s interval between pulses to the DUT. Test the device, using the failure criteria specified later in this section. Record the PASS/FAIL results for each device. Use the device result for the next step, described below.

If the result is PASS, stress the same device or a new device at the next higher level as shown in the tables earlier in this section (when you reach the highest level, stop testing). If the result is FAIL, decrease the voltage to the next lower level, select a new device, and stress the new devices if step stress procedure is used. If there is no lower level, stop testing. Repeat these steps until the highest passing voltage for the device and the corner pins is determined.

During device testing procedures, it is allowable to separate polarity; in other words, to stress a device with one polarity and a new device with the opposite polarity. First, determine the threshold for each polarity, as described above. Then, report the threshold value with the lower magnitude.

These test procedures can be modified to fit special circumstances. For example, the withstand threshold is the highest level at which three out of three stressed devices pass. If the device does not pass any level, its threshold is 0 V.

Specific Test Procedure: CDM

Prepare at least three samples. Place the first device onto the CDM testers. Start with the recommended (or any desired) voltage level, as discussed earlier in the section. All pins will be tested.

To perform CDM, charge the device with a positive potential by charging the package and discharging each pin. Repeat this procedure three times consecutively with a >0.1 s interval between discharges. Repeat the procedure for the negative polarity.

Follow the procedure detailed earlier in this section to determine the CDM threshold. This completes the CDM testing procedure.

Summary of Pass Criteria

Dependent upon device technology and customer requirements, devices shall meet 1000 V or 2000 V for HBM and 500 V CDM for all pins, 1000 V CDM for corner pins.

Failure Criteria

Parameters identified in the device specification are monitored for ESD testing. If a device cannot pass its own specifications, it is considered to have failed.

Other Information

The devices used for each of the above tests will not be used for any prior or future qualification tests. In addition, the test devices are handled with extreme care, using ESD preventative measures so as not to influence the test results. All operators wear grounding straps when handling the devices. The devices are transported in appropriate ESD protective packaging.

Details of Electrostatic Discharge (ESD) Tests (continued)

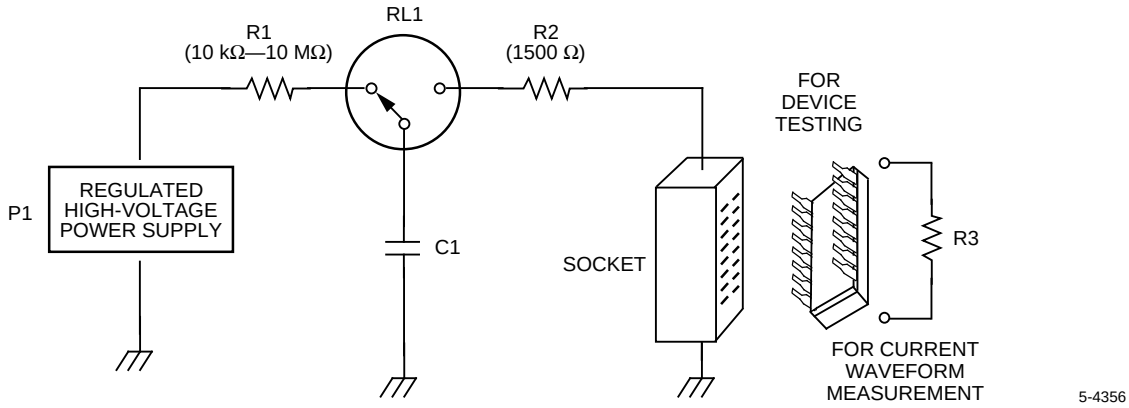

Figure 2. Circuit Schematic of Human-Body ESD Simulator

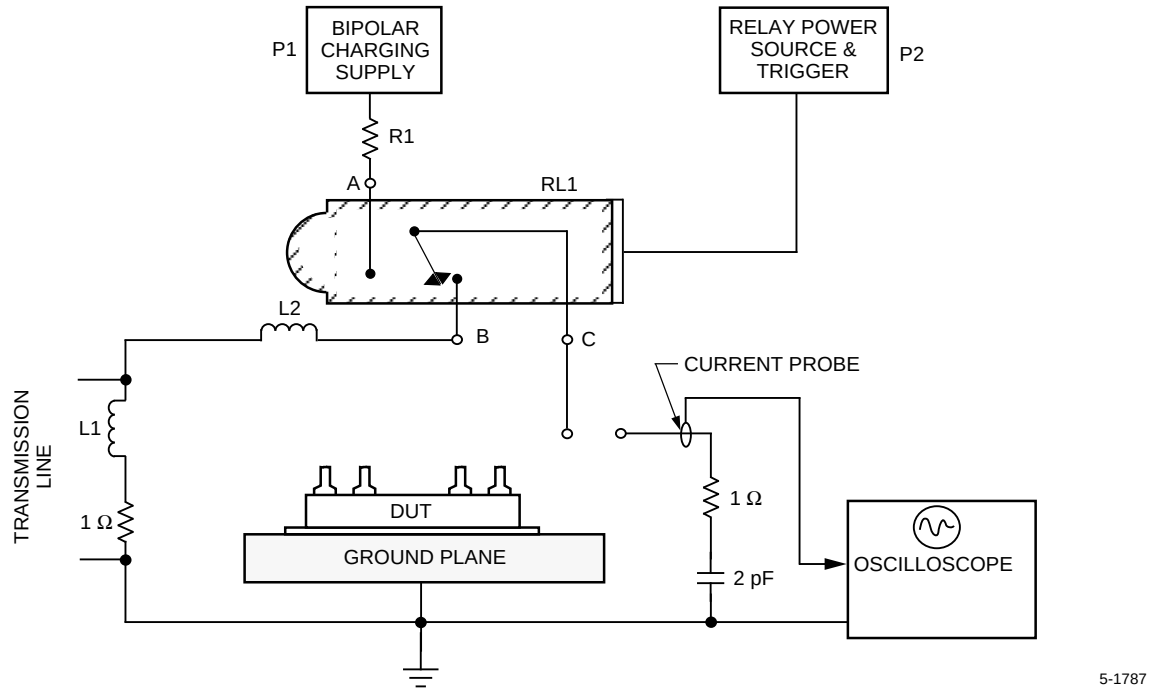

Figure 3. Circuit Schematic for CDM Simulator and Waveform Measurement (Ref. EOS/ESD Association-DS 5.3)

Details of Latch-Up Tests

Integrated Circuit Latch-Up Test Procedure per Lucent Technologies Method A88AL1006

Purpose

This section describes the latch-up stressing method Lucent Technologies uses to screen product for adequate latch-up immunity. This method was last revised 10/97 to align its procedure with JEDEC 17 and meet or exceed the pass/fail requirements of EIA/JESD78.

Test Procedure

The latch-up testing procedure includes three tests:

- dc stressing of all inputs, outputs, and I/O pins
- Power supply overvoltage stressing
- Poststress ATE testing

Three unstressed, fully functional devices are used for each of the first two tests. Each DUT is stressed at 25 ± 10 °C ambient temperature. The duration of the dc stimulus applied to the DUT is less than two seconds, and power supply levels are set to the manufacturer's maximum recommended operating level (Vmax). All six stressed devices must also pass all functional and parametric tests in order to be qualified.

Biasing

Input pins not under test are biased initially high and alternately biased low. Output and I/O pins are left floating. This pin configuration applies, as long as it does not cause the DUT to malfunction.

If the DUT does malfunction due to this pin configuration, an alternate pin configuration more consistent with the intended device function may be determined by the responsible device qualification engineer. The engineer will record the alternate configuration in the comments section of the results report form.

Latch-Up Test Details

Test 1: Stressing of Input, Output and I/O Pins

The I/O stress limits, detailed in Table 4, state a current and voltage limit. Current is forced into a pin under test via latch-up stress hardware, until either 200 mA or 1.5 Vmax is attained or latch-up occurs as defined above. For negative polarity I/O stress, current is extracted from the pin under test until either 200 mA or –0.5 Vmax is attained.

With the power supply current clamped to 300 mA, the DUT is placed in the test socket, and the V_{CC} and V_{SS} pins are connected to their respective potentials (Vmax). Then, the input pins not under test are biased high (repeated later, biased low) and the pin under test is current stressed first positively and then negatively.

After each stress, the dc stimulus is removed from the pin under test, and the I_{CC} is observed to determine whether latch-up has occurred. V_{CC} and V_{SS} are removed and reapplied before stressing the next pin in order to prevent possible high current damage to the DUT. This procedure is repeated until all inputs, outputs, and I/O pins are current stressed for both polarities and with inputs initially biased high and alternately biased low. The results are recorded on the results report form. Figure 4 illustrates equipment hookup.

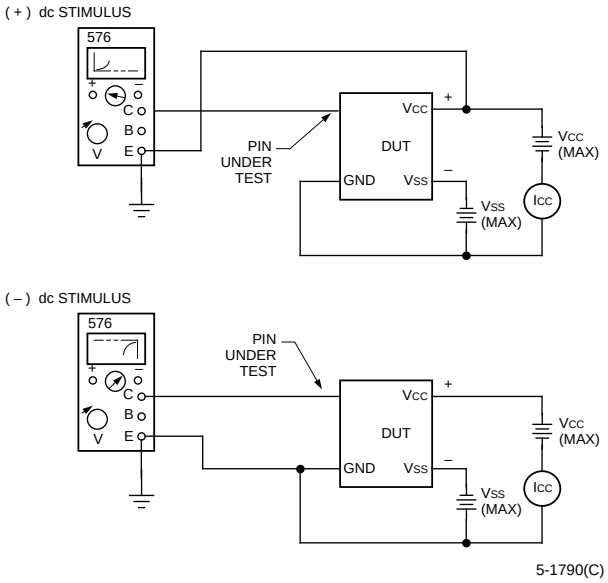

Figure 4. Test 1: Equipment Hookup: I/O Stress

Details of Latch-Up Tests (continued)

Test 2: Power Supply Overvoltage Test

If the DUT has multiple power supplies, each power supply pin is stressed separately. The power supply pin(s) not under test are set to the manufacturer's recommended nominal voltage (Vnom) before the power supply pin under test is stressed.

The input and I/O pin configuration during this test is the same as for the tests detailed earlier in this section. See Figure 5 for equipment hookup. The DUT is placed in the test socket, and the voltage is raised on all power supply pins to Vnom. The voltage on the power supply pin under test is then raised to the power supply overvoltage limit (1.5 Vmax).

The voltage on the power supply pin under test is returned to Vnom, and the I_{CC} is observed to determine whether latch-up has occurred. This procedure is repeated for each power supply pin. The results are recorded on the results report form.

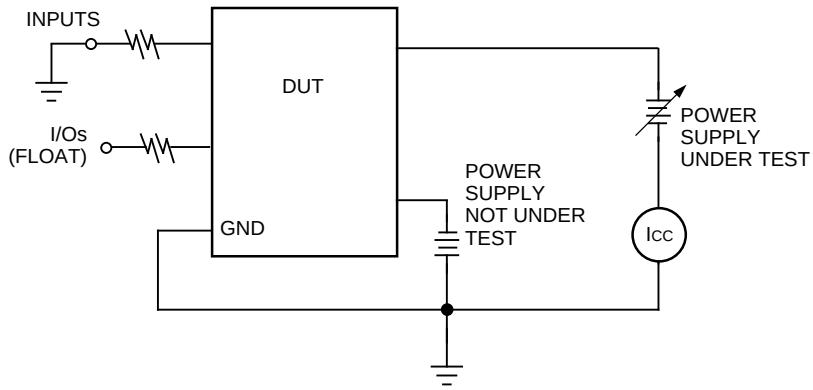

Figure 5. Test 2: Power Supply Overvoltage Stress Equipment Hookup

Test 3 and Pass/Fail Criteria

A device is considered latched up if, due to the application of a stress, the I_{CC} current exceeds the manufacturer's maximum I_{CC} current and remains at that level after the stress is removed. Quantitatively, the allowed current increase cannot exceed 140% of the typical current at Vmax or 10 mA, whichever is greater. For both Test 1 and Test 2, all six devices must not exhibit latch-up when stressed at the levels shown in Table 4. In addition, all six devices must pass functional and parametric testing after latch-up stressing to ensure adequate immunity to moderate electrical overstress conditions.

Package Qualification

Introduction

This section will document the qualification test procedures and results for the devices in the Lucent Technologies FPGA product family. The QRB determined the qualification requirements of each die in a given package. Test results are presented in Table 5 for the ATT3000 Series (0.6 µm), in Table 6 for the ATT3000 Series (0.55 µm), in Table 7 for the *ORCA* 1C Series, in Table 8 for the *ORCA* 2C Series of FPGAs, in Table 9 for the *ORCA* 2CxxA (5.0 V) Series, in Table 10 for the *ORCA* 2TxxA (3.3 V) Series, and in Table 11 for the ATT1700A series of EEPROMs. **For more detailed qualification information, please see the qualification test procedures and results at the end of this section**.

ESD and latch-up tests have been done on all of the FPGA families, with varying results for each device in each package. For the ATT3000 Series, the ESD results for the human-body model (ESD-HBM) varied from >2000 V to >3500 V, and the ESD results for the charged-device model (ESD-CDM) varied from >2500 V to >3000 V. Most devices passed LU Class IV, with a few passing only LU Class III. For the 1C Series of FPGAs, both ESD-HBM and ESD-CDM passed for >2000 V, which was the highest value tested. These devices also passed LU Class IV. For the 2C Series of devices, ESD-HBM passed for >2000 V and ESD-CDM passed for >1000 V, which, again, were the highest values tested. These devices also passed LU Class IV. For the 2CxxA (5.0 V) Series of devices, ESD-HBM passed for >2000 V and ESD-CDM varied from >1000 V to >2000 V. These devices passed LU Class II. For the 2TxxA (3.3 V) Series of devices, ESD-HBM passed for >2000 V and ESD-CDM passed for >1000 V. These devices passed LU Class II with a few passing Class III.

Qualification Status

Table 5. Qualification Status of ATT3000 Series FPGAs (0.6 µm)

Device	Qual No.	References	Tests Performed	Status
3020-68PLCC	—	Q92055, Q89166	—	Fully Qualified
3020-84PLCC	—	Q92055, Q89166	—	Fully Qualified
3020-100QFP	—	Q90001 or Q90111	—	Fully Qualified
3030-44PLCC	—	Q92055, Q89166	—	Fully Qualified
3030-68PLCC	—	Q92055, Q89166	—	Fully Qualified
3030-84PLCC	—	Q92055, Q89166	—	Fully Qualified
3030-100QFP	—	Q90001 or Q90111	—	Fully Qualified
3030-100TQFP	—	Q92055	—	Fully Qualified
3042-84PLCC	—	Q92055, Q89166	—	Fully Qualified
3042-100TQFP	QRB92.51	Q92055	ESD, LU	Fully Qualified
3042-100QFP	QRB93.2	Q90001 or Q90111	ESD, LU	Fully Qualified
3042-132PPGA	—	Q90137	—	Fully Qualified
3064-84PLCC	—	Q92055, Q89027	—	Fully Qualified
3064-132PPGA	—	Q90137	—	Fully Qualified
3064-160QFP	—	Q89129.1, Q90140	—	Fully Qualified
3090-84PLCC	Q92055	Q90148, Q89027	LT, ESD, LU	Fully Qualified
3090-160QFP	—	Q89129.1, Q90140	—	Fully Qualified
3090-175PPGA	Q92054	Q90137	LT, ESD, LU	Fully Qualified
3090-208SQFP	—	MR120, Q92055	—	Fully Qualified

Note: Status as of 2Q96.

Package Qualification (continued)

Table 6. Qualification Status of ATT3000 Series FPGAs (0.55 μm)

Device	Qual No.	References	Tests Performed	Status
3020-68PLCC	—	Q95273, Q89166	—	Fully Qualified
3020-84PLCC	—	Q95273, Q89166	—	Fully Qualified
3020-100QFP	—	Q95273, Q90111	—	Fully Qualified
3030-44PLCC	—	Q95273, Q89166	—	Fully Qualified
3030-68PLCC	—	Q95273, Q89166	—	Fully Qualified
3030-84PLCC	—	Q95273, Q89166	—	Fully Qualified
3030-100QFP	—	Q95273, Q90111	—	Fully Qualified
3030-100TQFP	—	Q95273, Q92055	—	Fully Qualified
3042-84PLCC	Q95273	MR109, Q89166	LT, ESD, LU	Fully Qualified
3042-100QFP	—	Q95273, Q90111	—	Fully Qualified
3042-100TQFP	—	Q95273, Q92055	—	Fully Qualified
3042-132PPGA	—	Q95273, Q90137	—	Fully Qualified
3064-84PLCC	—	Q95273, Q89027	—	Fully Qualified
3064-132PPGA	—	Q95273, Q90137	—	Fully Qualified
3064-160QFP	—	Q95273, Q90140	—	Fully Qualified
3090-84PLCC	Q96098	Q95273, Q89027	ESD, LU	Fully Qualified
3090-160QFP	—	Q95273, Q90140	—	Fully Qualified
3090-175PPGA	—	Q95273, Q90137	—	Fully Qualified
3090-208SQFP	Q96099	Q95273, MR120	ESD, LU	Fully Qualified

Note: Status as of 2Q96.

Package Qualification (continued)

Table 7. Qualification Status of *ORCA* 1C Series FPGAs

Device	Qual No.	References	Tests Performed	Status
ATT1C03-84PLCC	—	Q92167, Q92168	—	Fully Qualified
ATT1C03-100TQFP	—	Q92167, QRB92.51	—	Fully Qualified
ATT1C03-132BQFP	—	Q92167, Q92168	—	Fully Qualified
ATT1C03-208SQFP	—	Q92167, Q92168	—	Fully Qualified
ATT1C03-225CPGA	—	Q92167, Q92161	—	Fully Qualified
ATT1C03-225PPGA	—	Q92054, Q92167	—	Fully Qualified
ATT1C05-84PLCC	—	Q92167, Q92168	—	Fully Qualified
ATT1C05-100TQFP	—	Q92167, QRB92.51	—	Fully Qualified
ATT1C05-132BQFP	—	Q92167, Q92168	—	Fully Qualified
ATT1C05-208SQFP	—	Q92167, Q92168	—	Fully Qualified
ATT1C05-225PPGA	—	Q92054, Q92167	—	Fully Qualified
ATT1C05-225CPGA	—	Q92167, Q92161	—	Fully Qualified
ATT1C05-240SQFP	Q92167	—	All major tests	Fully Qualified
ATT1C07-208SQFP	—	Q92167, Q92168	—	Fully Qualified
ATT1C07-240SQFP	—	Q92167, Q92168	—	Fully Qualified
ATT1C07-280CPGA	—	Q92167, Q92161	—	Fully Qualified
ATT1C07-304SQFP	Q94044	Q92167, Q92168	ESD	Fully Qualified
ATT1C09-208SQFP	—	Q92167, MR120	—	Fully Qualified
ATT1C09-240SQFP	—	Q92167, MR141	—	Fully Qualified
ATT1C09-304SQFP	—	Q94044	—	Fully Qualified

Note: Status as of 2Q96.

Package Qualification (continued)

Table 8. Qualification Status of *ORCA* 2C Series FPGAs

Device	Qual No.	References	Tests Performed	Status
ATT2C04-84PLCC	Q94291	Q93234, T92222, MR109	None	Fully Qualified
ATT2C04-144TQFP	—	Q93234, Q93181	None	Fully Qualified
ATT2C04-160QFP	Q95319	Q93234, MR119	ESD, LU	Fully Qualified
ATT2C04-208SQFP	—	Q93234, Q94124	None	Fully Qualified
ATT2C06-84PLCC	—	Q93234, T92222	None	Fully Qualified
ATT2C06-144TQFP	—	Q93234, Q93181	None	Fully Qualified
ATT2C06-160QFP	—	Q93234, MR119, Q95319	None	Fully Qualified
ATT2C06-208SQFP	—	Q93234, Q94124	None	Fully Qualified
ATT2C06-240SQFP	—	Q93234	None	Fully Qualified
ATT2C08-160QFP	—	Q93234, MR119, Q95319	None	Fully Qualified
ATT2C08-208SQFP	—	Q93234, Q94124	None	Fully Qualified
ATT2C08-240SQFP	—	Q93234	None	Fully Qualified
ATT2C08-256PBGA	—	Q96068, Q95013	None	Fully Qualified
ATT2C08-304SQFP	—	Q93234, Q94046	None	Fully Qualified
ATT2C10-160QFP	—	Q93234, MR119, Q95319	None	Fully Qualified
ATT2C10-208SQFP	—	Q93234, Q94124	None	Fully Qualified
ATT2C10-240SQFP	—	Q93234	None	Fully Qualified
ATT2C10-256PBGA	Q96068	Q95013	TC, SB, TS, PD, ESD, LU	Fully Qualified
ATT2C10-304SQFP	Q95041	Q94046	SB, X-ray	Fully Qualified
ATT2C12-208SQFP	—	Q93234, Q94124	None	Fully Qualified
ATT2C12-240SQFP	—	Q93234	None	Fully Qualified
ATT2C12-256PBGA	—	Q96068, Q95013	None	Fully Qualified
ATT2C12-304SQFP	—	Q95041	None	Fully Qualified
ATT2C12-364CPGA	—	Q93231	None	Fully Qualified
ATT2C15-208SQFP	Q94290	Q93234, Q94124	ESD, LU	Fully Qualified
ATT2C15-240SQFP	Q93234	Q94046	LT, CL, BH, SB, TC, TS, ESD, LU	Fully Qualified
ATT2C15-304SQFP	Q94046	—	CL, BH, SB, TC, ESD, LU	Fully Qualified
ATT2C15-364CPGA	Q93231	Q94046, Q94290	LT, TC, TS, SQ, ESD, LU	Fully Qualified
ATT2C26-208SQFP-PQ2	—	Q94227	None	Fully Qualified
ATT2C26-240SQFP-PQ2	—	Q94227, Q95007	None	Fully Qualified
ATT2C26-304SQFP-PQ2	Q94227	—	LT, CL, BH, SB, TC, TS, ESD, LU, PD	Fully Qualified
ATT2C40-208SQFP-PQ2	QRB95.17	Q95007	PD	Fully Qualified
ATT2C40-240SQFP-PQ2	Q95007	Q94227	CL, BH, TC, PD, ESD, LU	Fully Qualified
ATT2C40-304SQFP-PQ2	—	Q95007, Q94227	None	Fully Qualified

Note: Status as of 2Q96.

Package Qualification (continued)

Table 9. Qualification Status of *ORCA* 2CxxA (5.0 V) Series FPGAs

Device	Qual No.	References	Tests Performed	Status
OR2C04A–84PLCC	Q96235.2	Q97176, EE97260, Q91016.3	ESD, LU	Fully Qualified
OR2C04A–100TQFP	Q96236.1	T96005, MR221	ESD, LU	Fully Qualified
OR2C04A–144TQFP	—	Q96365.1, MR225	None	Fully Qualified
OR2C04A–160QFP	—	T96005, MR217	None	Fully Qualified
OR2C04A–208SQFP	—	T96005, MR229	None	Fully Qualified
OR2C06A–84PLCC	—	Q97176, EE97260, Q91016.3, Q96235.2	None	Fully Qualified
OR2C06A–100TQFP	—	T96005, MR221	None	Fully Qualified
OR2C06A–144TQFP	—	Q96365.1, MR225	None	Fully Qualified
OR2C06A–160QFP	—	T96005, MR217	None	Fully Qualified
OR2C06A–208SQFP	—	T96005, MR229	None	Fully Qualified
OR2C06A–240SQFP	—	EE95210.1, MR232	None	Fully Qualified
OR2C06A–256PBGA	—	T95276.1, Q96068.1	None	Fully Qualified
OR2C08A–84PLCC	—	Q97176, EE97260, Q91016.3, Q96235.2	None	Fully Qualified
OR2C08A–160QFP	—	T96005, MR217	None	Fully Qualified
OR2C08A–208SQFP	—	T96005, MR229	None	Fully Qualified
OR2C08A–240SQFP	—	EE95210.1, MR232	None	Fully Qualified
OR2C08A–256PBGA	—	T95276.1, Q96068.1	None	Fully Qualified
OR2C10A–84PLCC	—	Q97176, EE97260, Q91016.3, Q96235.2	None	Fully Qualified
OR2C10A–160QFP	—	T96005, MR217	None	Fully Qualified
OR2C10A–208SQFP	—	T96005, MR229	None	Fully Qualified
OR2C10A–240SQFP	—	EE95210.1, MR232	None	Fully Qualified
OR2C10A–256PBGA	—	T95276.1, Q96068.1	None	Fully Qualified
OR2C10A–352PBGA	—	T95276.1	None	Fully Qualified
OR2C12A–84PLCC	—	Q97176, EE97260, Q91016.3, Q96235.2	None	Fully Qualified
OR2C12A–208SQFP	—	T96005, MR229	None	Fully Qualified
OR2C12A–240SQFP	—	EE95210.1, MR232	None	Fully Qualified
OR2C12A–256PBGA	—	T95276.1, Q96068.1	None	Fully Qualified
OR2C12A–304SQFP	—	EE95210.1, MR233	None	Fully Qualified
OR2C12A–352PBGA	—	T95276.1	None	Fully Qualified
OR2C15A–84PLCC	—	Q97176, EE97260, Q91016.3, Q96235.2	None	Fully Qualified
OR2C15A–208SQFP	T96005.1[1]	T96005, MR229	LT, CL, BH, SB, TC, TS, XR, ESD, LU	Fully Qualified
OR2C15A–208SQFP2	—	EE95210.1, Q96406, MR243	None	Fully Qualified
OR2C15A–240SQFP	—	EE95210.1, MR232	None	Fully Qualified
OR2C15A–240SQFP2	—	EE95210.1, MR244	None	Fully Qualified
OR2C15A–256PBGA	—	T95276.1, Q96068.1	None	Fully Qualified
OR2C15A–304SQFP	Q97037[2]	EE95210.1, T96005, MR233	LT, CL, BH, C8PRE, SB, TC, TS, XR, ESD	Fully Qualified

1. Qual No. T96005.1 was created to conform with the package's code marking; therefore, tests performed are referenced from Qual No. T96005.
2. Qual No. Q97037 was created to conform with the package's code marking; therefore, tests performed are referenced from Qual No. EE95210.1.

Note: Status as of 3Q97.

Package Qualification (continued)

Table 9. Qualification Status of *ORCA* 2CxxA (5.0 V) Series FPGAs (continued)

Device	Qual No.	References	Tests Performed	Status
OR2C15A–352PBGA	T95276.2[3]	T95276.1, Q95013, T96005	LT, CL, BH, C6PRE, SB, TC, TS, PD, XR, ESD	Fully Qualified
OR2C15A–432EBGA	—	Q96284.2, T95276.1	None	Fully Qualified
OR2C26A–208SQFP2	—	EE95210.1, MR243	None	Fully Qualified
OR2C26A–240SQFP2	—	EE95210.1, MR244	None	Fully Qualified
OR2C26A–304SQFP2	—	EE95210.1, MR245	None	Fully Qualified
OR2C26A–352PBGA	—	T95276.1	None	Fully Qualified
OR2C26A–432EBGA	—	Q96284.2, T95276.1	None	Fully Qualified
OR2C40A–208SQFP2	—	EE95210.1, Q95007, Q95204, MR243	None	Fully Qualified
OR2C40A–240SQFP2	—	EE95210.1, Q95007, MR244	None	Fully Qualified
OR2C40A–304SQFP2	—	EE95210.1, Q95007, Q94227.1, MR245	None	Fully Qualified
OR2C40A–432EBGA	—	Q96284.2, T95276.1	None	Fully Qualified
OR2C40A–600EBGA	—	Q97048.1, Q96284.2	None	In Process

1. Qual No. T96005.1 was created to conform with the package's code marking; therefore, tests performed are referenced from Qual No. T96005.
2. Qual No. Q97037 was created to conform with the package's code marking; therefore, tests performed are referenced from Qual No. EE95210.1.
3. Qual No. T95276.2 was created to conform with the package's code marking; therefore, tests performed are referenced from Qual No. T95276.1.

Note: Status as of 3Q97.

Package Qualification (continued)

Table 10. Qualification Status of *ORCA* 2TxxA (3.3 V) Series FPGAs

Device	Qual No.	References	Tests Performed	Status
OR2T04A–84PLCC	Q96298.2	Q91016.3, EE97260	ESD, LU	Fully Qualified
OR2T04A–100TQFP	Q96299.2	Q96120, EE97260, MR221	ESD, LU	Fully Qualified
OR2T04A–144TQFP	—	Q96365.1, EE97260, MR225	None	Fully Qualified
OR2T04A–160QFP	—	T96005, Q96270, MR217	None	Fully Qualified
OR2T04A–208SQFP	—	T96005, Q97193, Q97102.1, Q97053.1, MR229	None	Fully Qualified
OR2T06A–84PLCC	—	Q91016.3, EE97260, Q96298.2	None	Fully Qualified
OR2T06A–100TQFP	—	Q96120, EE97260, Q96299.2, MR221	None	Fully Qualified
OR2T06A–144TQFP	—	Q96365.1, EE97260, MR225	None	Fully Qualified
OR2T06A–160QFP	—	T96005, Q96270, MR217	None	Fully Qualified
OR2T06A–208SQFP	—	T96005, Q97193, Q97102.1, Q97053.1, MR229	None	Fully Qualified
OR2T06A–240SQFP	—	EE95210.1, EE97260, MR232	None	Fully Qualified
OR2T06A–256PBGA	—	T95276.1, EE97260, Q97100, Q96068.1	None	Fully Qualified
OR2T08A–84PLCC	—	Q91016.3, EE97260, Q96298.2	None	Fully Qualified
OR2T08A–160QFP	—	T96005, Q96270, MR217	None	Fully Qualified
OR2T08A–208SQFP	—	T96005, Q97193, Q97102.1, Q97053.1, MR229	None	Fully Qualified
OR2T08A–240SQFP	—	EE95210.1, EE97260, MR232	None	Fully Qualified
OR2T08A–256PBGA	—	T95276.1, EE97260, Q97100, Q96068.1	None	Fully Qualified
OR2T10A–84PLCC	—	Q91016.3, EE97260, Q96298.2	None	Fully Qualified
OR2T10A–160QFP	—	T96005, Q96270, MR217	None	Fully Qualified
OR2T10A–208SQFP	—	T96005, Q97193, Q97102.1, Q97053.1, MR229	None	Fully Qualified
OR2T10A–240SQFP	—	EE95210.1, EE97260, MR232	None	Fully Qualified
OR2T10A–256PBGA	—	T95276.1, EE97260, Q97100, Q96068.1	None	Fully Qualified
OR2T10A–352PBGA	—	T95276.1, EE97260	None	Fully Qualified
OR2T12A–84PLCC	—	Q91016.3, EE97260, Q96298.2	None	Fully Qualified
OR2T12A–208SQFP	—	T96005, Q97193, Q97102.1, Q97053.1, MR229	None	Fully Qualified
OR2T12A–240SQFP	—	EE95210.1, EE97260, MR232	None	Fully Qualified
OR2T12A–256PBGA	—	T95276.1, EE97260, Q97100, Q96068.1	None	Fully Qualified
OR2T12A–352PBGA	—	T95276.1, EE97260	None	Fully Qualified
OR2T15A–84PLCC	—	Q91016.3, EE97260, Q96298.2	None	Fully Qualified
OR2T15A–208SQFP	—	T96005, Q97193, Q97102.1, Q97053.1, MR229	None	Fully Qualified
OR2T15A–240SQFP	—	EE95210.1, EE97260, MR232	None	Fully Qualified
OR2T15A–256PBGA	—	T95276.1, EE97260, Q97100, Q96068.1	None	Fully Qualified
OR2T15A–352PBGA	—	T95276.1, EE97260	None	Fully Qualified
OR2T15A–432EBGA	—	Q96284.2, EE97260	None	Fully Qualified

Note: Status as of 3Q97.

Package Qualification (continued)

Table 10. Qualification Status of *ORCA* 2TxxA (3.3 V) Series FPGAs (continued)

Device	Qual No.	References	Tests Performed	Status
OR2T26A–208SQFP2	—	EE95210.1, EE97260, Q96380, MR243	None	Fully Qualified
OR2T26A–240SQFP2	—	EE95210.1, EE97260, MR244	None	Fully Qualified
OR2T26A–352PBGA	—	T95276.1, EE97260	None	Fully Qualified
OR2T26A–432EBGA	—	Q96284.2, EE97260	None	Fully Qualified
OR2T40A–208SQFP2	—	EE95210.1, EE97260, Q95007, Q95204, MR243	None	Fully Qualified
OR2T40A–240SQFP2	—	EE95210.1, EE97260, Q95007, MR244	None	Fully Qualified
OR2T40A–352PBGA	—	T95276.1, EE97260	None	Fully Qualified
OR2T40A–432EBGA	—	Q96284.2, EE97260	None	Fully Qualified
OR2T40A–600EBGA	Q97048.1	None	LT, CL, BH, C6PRE, SB, TC, TS, MR, SA, SR, PD, SD, XR, ESD, LU	In Process

Note: Status as of 3Q97.

Table 11. Qualification Status of ATT1700A Series EEPROMS

Device	Qual No.	References	Tests Performed	Status
ATT1700A-8DIP	Q94362	—	LT, BK, BH, HAST, SB, TC, TS, MR, SA, RT, SR, PD, SD, LI, HBM, CDM, LU	Fully Qualified
ATT1700A-8SONB	Q94363	Q94362	BH, HAST, SB, TC0, TC, TS, MR, SA, RT, SR, PD, SD, LI, HBM, CDM, LU	Fully Qualified
ATT1700A-20PLCC	Q94364	Q94362	BH, HAST, SB, TC, TS, MR, SA, RT, SR, PD, SD, LI, HBM, CDM, LU	Fully Qualified

Note: Status as of 2Q96.

Vendor Quality Monitoring

Overview

Quality of all purchased raw material, parts, and components used in IC manufacture is monitored by the Purchased Material Inspection Section. Partnerships are formed with suppliers of critical materials.

Inspection

A flow chart of the incoming inspection process is shown in Figure 6. Purchase orders for materials prescribe complete and precise specifications. Inspection and testing requirements are included and, where required, requests are made for evidence of chemical, physical, and electrical tests in the form of certificates. Quality Control produces monthly summaries of the results of all inspections, including established and new suppliers. The individual inspections involve various personnel:

- Silicon and Wafers—performed by resident Quality Assurance (QA) inspectors.
- Piece Parts—performed by the inspectors of the Purchased Material Inspection Section.
- Chemicals—incoming chemicals are sampled and inspected by the Analytical Lab.
- Gases—a certificate of inspection and analysis is required with each shipment of compressed gases. Each certificate is reviewed by the Purchased Materials Inspector for completeness and compliance with specifications.

Vendor Qualification

New vendors are qualified by a team that includes representatives from product engineering, quality control, and purchasing. The qualification process may include evaluation of product samples and an audit of the supplier's facility to assess quality programs, practices, and manufacturing capabilities. Approved vendors and products are listed on the Approved Vendors List maintained by Quality Control.

Vendor Commodity Teams

Vendor partnerships are created with the intent of establishing and maintaining close working relationships with key suppliers. This formal program is administered by Vendor Commodity Teams composed of members from Purchasing, Materials Management, Quality, Bell Laboratories, and Product Engineering.

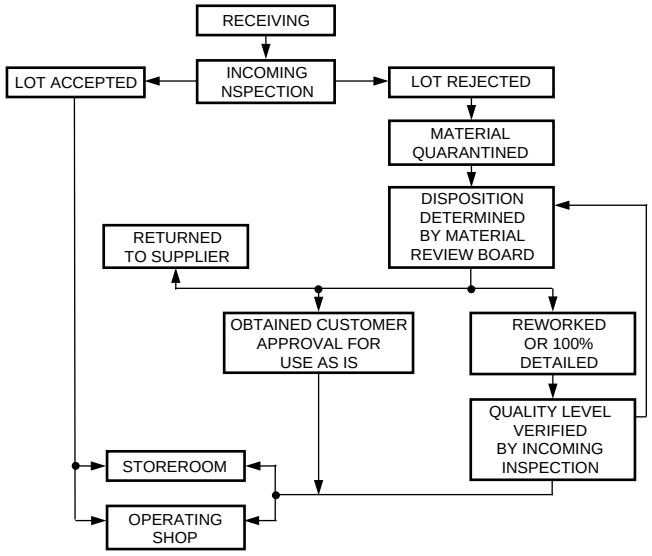

Figure 6. Flow Diagram for Purchased Material

Manufacturing Control and Improvement

Wafer level and quality improvement is an aggressive, proactive program aimed at improving the quality and reliability of the MOS manufacturing product lines.

An example of this process is the use of a line monitor to enhance the control of CMOS fabrication lines. While all IC fabrication lines use zone monitors and process monitors, the CMOS fabrication lines also employ a line monitor that is used to achieve tighter process control for newer technologies.

This program, called the Yield Enhancement System (YES), involves measuring and modeling yield in order to provide process engineers with the tools to efficiently collect data at significant points of the manufacturing process, and guiding quality improvement activities. Lucent Technologies' 1.2 μm and 0.9 μm CMOS technologies benefit from the YES program.

Key tools designed for the YES program include a line monitor, zone monitors, a data management system, and a yield model. A key part of the data management system is a rigorous statistical process control program. Each is described below.

Line Monitor

The primary element of the YES program is the line monitor, a device which receives and evaluates the full integrated circuit process from design through packaging.

The line monitor has three components: a Standard Evaluation Circuit (SEC), a Tester for Reliability and Yield Components (TRYC), and a Process Monitor (PM).

Lucent Technologies' SEC is a specially designed, highly diagnosable memory with DRAM and SRAM arrays whose yield can be monitored. The SEC is also run with monitored burn-in and extended life tests for periodic reliability evaluation of MOS product lines.

The TRYC contains patterns for measuring defect densities to arrive at a correlation between direct measurement of defect density and SEC yield. It also contains structures for evaluating intrinsic reliability. These structures provide for the characterization of electromigration of Metal 1 and Metal 2 runners and contacts, time-dependent dielectric breakdown of gate oxides, hot carrier aging, and mobile ion contamination.

The PM consists of structures in the kerf or grid that measure electrical parameters such as threshold voltage, linear gain, and leakage current.

Zone Monitors

Although the line monitor provides an excellent evaluation of the complete fabrication process, often faster feedback is required. This is achieved by the zone monitors, test structures fabricated in parts (zones) of the process to measure the defect density of a particular processing segment.

Each zone monitor measures the defect density for particular failure modes. Since it addresses specific performance, isolated defects are identified, and the overall sensitivity of the measurement is enhanced. All YES tools permit fast turnaround, and are used for defect density reduction experiments plus routine monitoring of portions of the process.

Yield Model

A yield model has been developed to analyze the effects of defect densities on product yields. The results provided by this model also help to prioritize defect reduction projects.

Statistical Process Control (SPC)

Statistical Process Control is a key component of Lucent Technologies' quality program.

As the flow chart in Figure 7 illustrates, the SPC plan progresses in three phases: data collection (Monitoring), process control (Performance Studies), and process improvement (Process Capability). Typical areas under SPC monitoring during wafer fabrication and package assembly are illustrated in Table 12 and Table 13. Quality Improvement Teams (QITs), composed of the process engineers, shop supervisors, and quality control engineers, identify the critical nodes (processes). The quality control engineer is responsible for completing performance studies on all nodes, and calculating Process Capability (Cp) indices for each.

The QIT seeks to reduce variation at all critical nodes beginning with those having process capability indices of less than 1.33. Critical nodes are identified by engineering judgment and customer feedback. The team then applies its energies to reducing variation at nodes having values of less than 2.0.

Lucent Technologies' goal is to become a 6 sigma manufacturer. To accomplish this goal, the team uses experimental design techniques, Pareto analyses, distributions, correlation studies, control chart patterns, and process capability studies, as detailed in the Lucent Technologies Statistical Quality Control Handbook.

In addition to driving process improvements, the team has procedures for corrective action on all quality-related problems within its area of responsibility. It evaluates the potential impact of each problem in terms of customer satisfaction, performance, reliability, safety, and cost. Cause and effect are determined, and significant variables are identified.

The team's control extends to remedial action both on work in progress and on devices already shipped. If indicated, recall procedures and decision processes are implemented without delay, in order to preserve customer confidence.

Based on its findings, the team recommends and implements changes to manufacturing, packing, shipping, and storage processes, or revises specifications or the quality system itself. The team then tracks the successful implementation of its recommendations, and monitors the results.

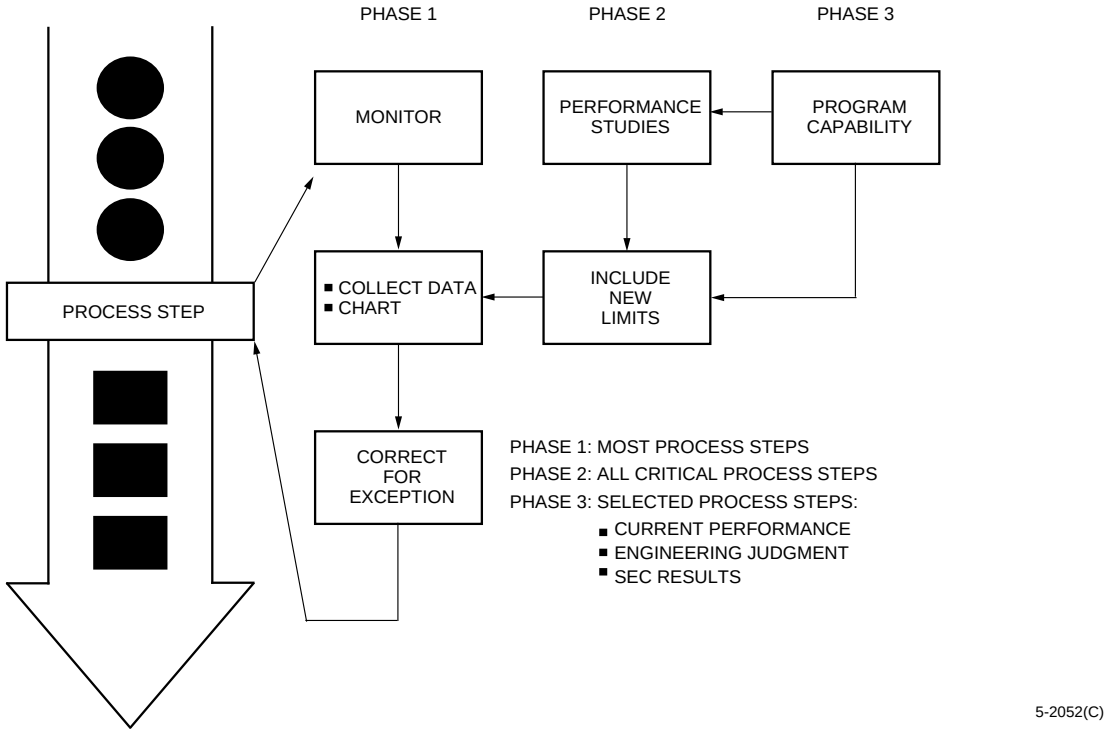

Figure 7. The SPC Process Flow

Statistical Process Control (continued)

Table 12. 0.35 μm MOS Fabrication Area Statistical Process Control Monitor Examples

Operation	Characteristic	Frequency	Sample Size
Pad 1 Oxidation	Oxide Thickness	Each Run	2/4 Wafers
Nitride 1 Deposition	Nitride Thickness	Each Run	2/4 Wafers
NTub Photoresist	Line Size	Each Lot	2 Wafers
Tub Oxidation	Oxide Thickness	Each Run	2/4 Wafers
Pad Oxidation	Oxide Thickness	Each Run	2/4 Wafers
Undoped Silicon Deposition	Silicon Thickness	Each Run	4 Wafers
Nitride Deposition	Nitride Thickness	Each Run	4 Wafers
GASAD Photoresist	Line Size	Each Lot	2 Wafers
GASAD Bioradiation	Misalignment	Each Lot	1 Wafer
GASAD Final Measurement	Etched Line Size	Each Lot	2 Wafers
Chan-Stop Photoresist	Line Size	Each Lot	2 Wafers
Field Oxidation	Oxide Thickness	Each Lot	2/4 Wafers
Screen Oxidation	Oxide Thickness	Each Lot	2/4 Wafers
V_T Adjust Photoresist	Line Size	Each Lot	2 Wafers
Gate Oxidation	Oxide Thickness	Each Lot	2/4 Wafers
Polysilicon Deposition	Polysilicon Thickness	Each Run	4 Wafers
Phosphorous Diffusion	Sheet Resistance	Each Run	2 Wafers
AMI BPTEOS Hard Mask	Film Thickness	Each Lot	1 Wafer/1 Chamber
Polysilicon Photoresist	Line Size	Each Lot	2 Wafers
Polysilicon Bioradiation	Misalignment	Each Lot	1 Wafer
Polysilicon Final Measurement	Etched Line Size	Each Lot	2 Wafers
N-L_{DD} Photoresist	Line Size	Each Lot	2 Wafers
TEOS Deposition	TEOS Thickness	Each Lot	5 Wafers
PLOD Photoresist	Line Size	Each Lot	2 Wafers
TEOS Deposition	TEOS Thickness	Each Lot	5 Wafers
Spacer Etch	Final Field Oxidation Thickness	Each Lot	1 Wafer/Chamber
P-Drain Photoresist	Line Size	Each Lot	2 Wafers
N-Drain Photoresist	Line Size	Each Lot	2 Wafers
AMI BPTEOS Tri-Layer	Composite Thickness	Each Lot	1 Wafer/Chamber
Window 1 Photoresist	Line Size	Each Lot	2 Wafers
Window 1 Bioradiation	Misalignment	Each Lot	1 Wafer
Window 1 Final Measurement	Etched Line Size	Each Lot	2 Wafers
Sputter Metal 1 Stack	Ti + TiN + Alum + Ti Thickness + R_S of Each Film	1/Day	1 Control/Film
Metal 1 Photoresist	Line Size	Each Lot	2 Wafers
Metal 1 Bioradiation	Misalignment	Each Lot	1 Wafer
Metal 1 Final Measurement	Etched Line Size	Each Lot	2 Wafers
Deposition Plasma TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Etch TEOS	Final TEOS Thickness	Each Lot	3 Wafers
Deposition Plasma TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Etch TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Window 2 Photoresist	Line Size	Each Lot	2 Wafers

Statistical Process Control (continued)

Table 12. 0.35 µm MOS Fabrication Area Statistical Process Control Monitor Examples (continued)

Operation	Characteristic	Frequency	Sample Size
Window 2 Bioradiation	Misalignment	Each Lot	1 Wafer
Etch Window 2	PETEOS Thickness	Each Lot	1 Wafer/Chamber
Window 2 Final Measurement	Line Size	Each Lot	2 Wafers
Sputter Metal 2 Stack	Ti + TiN + Alum + Ti Thickness + Rs of Each Film	1/Day	1 Control/Film
Metal 2 Photoresist	Line Size	Each Lot	2 Wafers
Metal 2 Bioradiation	Misalignment	Each Lot	1 Wafer
Metal 2 Final Measurement	Etched Line Size	Each Lot	2 Wafers
Deposition Plasma TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Etch TEOS	Final TEOS Thickness	Each Lot	3 Wafers
Deposition Plasma TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Etch TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Window 3 Photoresist	Line Size	Each Lot	2 Wafers
Window 3 Bioradiation	Misalignment	Each Lot	1 Wafer
Etch Window 3	PETEOS Thickness	Each Lot	1 Wafer/Chamber
Window 3 Final Measurement	Line Size	Each Lot	2 Wafers
Sputter Metal 3 Stack	Ti + TiN + Alum + Ti Thickness + Rs of Each Film	1/Day	1 Control/Film
Metal 3 Photoresist	Line Size	Each Lot	2 Wafers
Metal 3 Bioradiation	Misalignment	Each Lot	1 Wafer
Metal 3 Final Measurement	Etched Line Size	Each Lot	2 Wafers
Deposition Plasma TEOS	TEOS Thickness	Each Lot	1 Wafer/Chamber
Sincaps Deposition	Sincaps Thickness	Each Lot	2 Wafers
Visual Inspection	Visual Defects	Each Lot	12% of lot

Statistical Process Control (continued)

Table 13. Assembly Area Statistical Process Control Monitor Examples

Operation	Inspection	Frequency	Sample Size
Wafer Saw	Visual Inspection	Twice Per Machine Per Shift	20 Units
	Machine Inspection	Once Per Machine Per Shift	Each Machine
Die Attach	Visual Inspection	Every Magazine	Three Strips
	Epoxy Resistivity	Once Per Month	Two Glass Slides
	Die Shear	Once Per Machine Per Shift	Three Units
	Epoxy Void	Once Per Machine Per Shift	10 Units
	Machine Inspection	Once Per Machine Per Shift	Each Machine
	Oven Cure	Once Per Machine Per Shift	Each Machine
Wire Bond	Visual Inspection	Every 10 Strips	One Strip
	Bond Pull Strength	Once Per Machine Per Shift	Five Wires Per Unit
	Ball Shear Strength	Twice Per Machine Per Shift	Five Wires Per Unit
	Machine Inspection	Once Per Machine Per Shift	Each Machine
Mold	Visual Inspection	Every 20 Mold Runs	One Mold Run
	X-Ray	Twice Per Machine Per Shift	12 Units
	Machine Inspection	Once Per Machine Per Shift	Each Machine
Code Mark	Visual Inspection	Every 120 Strips	Three Strips
	Permanency	One Out of Five Lots	Four Units
	Machine Inspection	Once Per Day	Each Machine
Trim and Form	Visual Inspection	Every 20 Tubes	20 Units
	Lead Spread	Twice Per Machine Per Shift	Five Units
	Coplanarity	Twice Per Machine Per Shift	Two Units
Solder	Visual Inspection	One Lot Per Package Type Per Shipment	22 Units
	Ionic Contamination	Each Shipment	Two Strips
	Solderability (Incoming from Plater)	Twice Per Week	12 Units
	Thickness (COFC)	Each Shipment	One in Three Lots
	Outgoing Solderability	Once Per Week	Four Units

Document Control

The overall procedures and standards by which Lucent Technologies exercises its control of the manufacture, quality, and reliability of ICs are depicted in a series of A-drawings. A-drawings are interpreted and implemented by engineering organizations using shop instructions (SIs), inspection layouts (ILs), training documents (TDs), and test equipment requirements (TERs). Each of these secondary documents has a provision for adding information via supplementary information forms (SIFs). SIFs must be referenced to the interpretive drawing (for example, SIF-IL5349-009).

The document control group's responsibility is to maintain the current issues of each of these documents and to control the procedures for document changes. The current issue of each document is kept in the Manufacture Information Distribution System (MIDS) database. The document control group places paper copies of current documents applicable to the efforts of a given work area in manufacturing information books, and maintains these books. For example, all drawings applicable to reliability monitoring are contained in a book (MI-098-RI) kept in the reliability laboratory.

Changes in any document are made by engineering staff responsible for the specific process. Revisions must be approved by the appropriate members of the engineering staff and by Quality Control before being implemented.

QC confirms that appropriate qualification of changes has been conducted and, when required, notifies the customer and obtains approval.

Quality Conformance Inspection

This section summarizes the completed product audit for MOS products and describes final inspection procedures used by Quality Assurance (QA). When manufacturing is completed and product is presented for shipment, QA selects samples and confirms that they meet specifications. Sampling procedures apply to electrical and mechanical inspection.

Electrical sampling is performed on a device type basis, using a two-tier sampling plan as shown in Figure 8. Normal inspection is performed lot by lot at 0.1% Acceptable Quality Level (AQL). For example, in 1990, QA measured fewer than 25 parts per million (ppm) defective during electrical audit. Devices with exceptional quality (no defects found in the last 10 lots sampled) receive skip lot inspection, performed on one of every four lots received by Quality Assurance using the same 0.1% AQL plan.

Mechanical/visual inspection uses the same process, but lots may be grouped by package type as well as by device type.

Sampling procedures specify that sticks (or tubes) of devices are randomly selected until the required sample size is reached. To avoid mixing of products in final inspection, only samples from one lot are inspected at a time, and are then returned to the parent lot before choosing samples from the next lot.

Devices may move to skip-lot inspection after 10 consecutive lots pass the procedure lot by lot. Any rejected lot causes the device or package type to return (or remain) on the lot-by-lot sampling approach.

Specific procedures exist for tighter sampling and inspection procedures when QA determines them to be necessary.

Final inspection electrical tests are made in accordance with the latest issue of the device specification. Mechanical/visual requirements are obtained from package drawings and internal workmanship standards. Nonacceptable production lots are returned to the operating ship for corrective action.

QA reports the results of the electrical and mechanical/visual inspections as measures of outgoing quality expressed in ppm. These reports are generated from a computerized database which gathers information entered by inspectors on each lot as inspection is performed. MOS quality performance has shown a 35% improvement rate per year, as illustrated in Figure 9.

Quality Conformance Inspection (continued)

Specific procedures exist for tighter sampling and inspection procedures when QA determines them to be necessary. Final inspection electrical tests are made in accordance with the latest issue of the device specification. Mechanical/visual requirements are obtained from package drawings and internal workmanship standards. Nonacceptable production lots are returned to the operating shop for corrective action.

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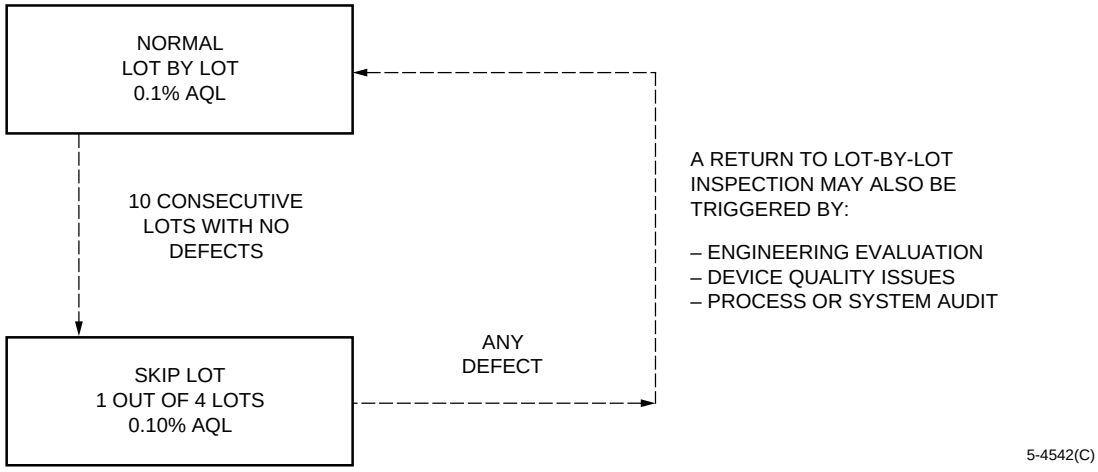

Figure 8. Electrical Test Sampling Level and Flow (Device Code Basis)

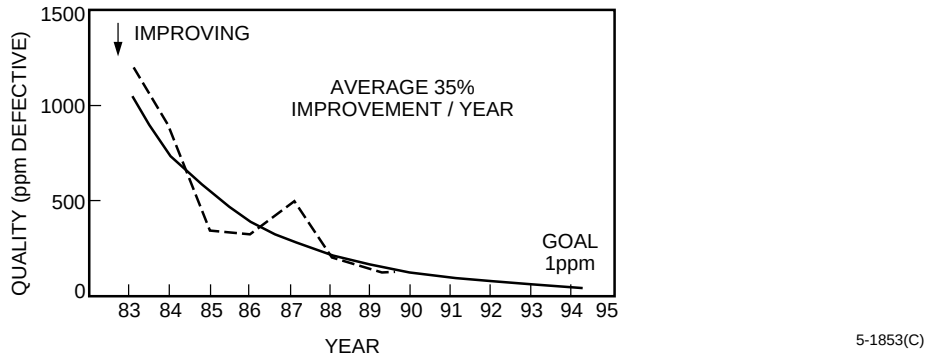

Figure 9. Product Quality Improvement Rate

Reliability Monitoring Program

Introduction

In this section, we present the Lucent Technologies Reliability Model and the Lucent Technologies Reliability Monitoring Program. The section begins with a review of reliability concepts, followed by the device failure model, concepts of accelerated testing, and the Lucent Technologies Reliability Monitoring Program as administered by the Reliability Review Board.

Reliability is the ability of an electronic system to operate satisfactorily over a period of time. Since electronic systems consist of electronic components (devices), system reliability depends on the reliability of each component in the application environment.

A generally accepted definition of reliability is the probability that an item will perform a required function under stated conditions for a stated period of time.

The required function includes both a definition of satisfactory and unsatisfactory operation (failure). The stated conditions are the total physical environment, including mechanical, thermal, and electrical conditions. The stated period of time is the time during which satisfactory operation is desired.

Device Failure Model

The Lucent Technologies Reliability Model is presented in terms of the failure rate, λ (t). Historically, failure rates have been modeled in the bathtub curve shown in Figure 10.

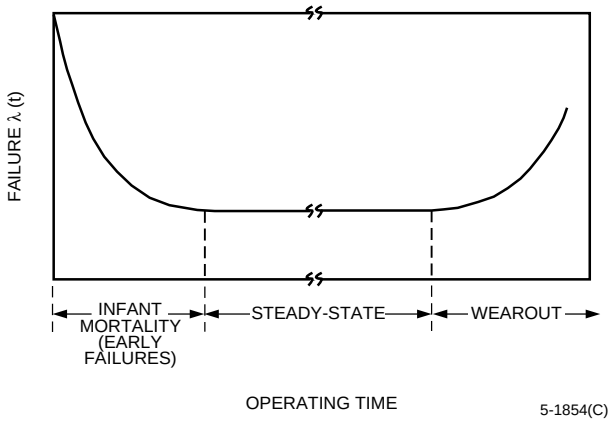

Figure 10. Reliability Bathtub Curve

This curve has three regions with distinct characteristics. The regions are associated with infant mortality, steady-state operation, and wear-out.

In most cases, the bathtub curve model is only partly appropriate for electronic devices. Although such devices exhibit infant mortality and steady-state periods, generally those supplied by reputable suppliers exhibit no wear-out during intended device life.

The failure rate in the infant mortality region of the bathtub curve is modeled by a Weibull distribution. The Weibull failure rate can be expressed as:

$$\lambda\,(t) = \lambda(1)t^{-a}$$

One feature of this distribution is that the failure rate is a straight line when plotted on log-log paper. In such a plot, the slope is –a and the intercept at t = 1 hour is l1. Beyond the infant mortality period, the failure rate is assumed to be determined by the exponential distribution.

Two distinct sources of information exist on device reliability: accelerated life tests and performance actually monitored in the factory or field. These sources provide two quite different measures of reliability. Accelerated life tests provide information about expected reliability in the very long term (decades). Factory or field data gives a real measure of actual device reliability in the short term (less than a few years).

Measures of Reliability

Reliability is usually measured in number of defects or percentage of defects per unit of time. This definition relates more to the unit's failure rate than to its reliability function. A common unit for describing failure rate behavior is the FIT: failures in 109 device hours of operation.

Accelerated Stress Testing

Because devices are so reliable, failure-accelerating stresses are needed to observe failure distributions within a reasonable time period. The accelerating effect of the stress must be well understood to interpret the results of accelerated stress testing.

The relationship between stress and time to failure for a given product is determined by the activation energies of the failure mechanisms which are dominant in that product. The activation energies are determined from extensive accelerated stress testing, usually done at the time the failure mechanism is first discovered.

Reliability Monitoring Program

(continued)

When evaluating the impact of specific problems on device life expectancy, it is important to treat the different failure mechanisms that may occur within a sample independently; they may be accelerated differently, and extrapolations from combined data can be very misleading. (This emphasizes the need for failure analysis to identify the failure mechanism.)

Effects of Operating Voltage on Failure Rates

The dielectric breakdown of oxide film can be accelerated by applied field, particularly for MOS devices. Extensive investigations have established a voltage-dependent acceleration factor that could be applied to MOS devices in which a voltage stress in excess of nominal voltages is applied. This research has led to the relationship

$$A_V = \mathrm{EXP}\left[\frac{C}{t_{ox}}\,(V_1 - V_2)\right]$$

where:

C = voltage acceleration constant in A/V

t_{OX} = oxide thickness in Å

V_1 = stress voltage in V

V_2 = operating voltage in V

For Lucent Technologies MOS products, these values are shown in the table below:

Table 14. Voltage-Dependent Acceleration Values

Technology	C/tox
0.35 µm	3.0 $(V)^{-1}$
0.5 µm	3.0 $(V)^{-1}$
0.55 µm	3.4 $(V)^{-1}$
0.6 µm	3.4 $(V)^{-1}$
0.9 µm	3.4 $(V)^{-1}$
1.25 µm	2.3 $(V)^{-1}$
>2.0 µm	2.3 $(V)^{-1}$

Time-Temperature Relationship (Arrhenius Equation)

Many of the chemical and physical processes leading to failure are accelerated by temperature in a way that can be readily modeled and reproduced. This makes temperature a very useful accelerating stress.

The equation describing the temperature acceleration factor, A_T, is found from the Arrhenius relationship. It is written as:

$$A_T = \mathrm{EXP}\,\frac{Ea}{ko}\left[\frac{1}{T_0} - \frac{1}{T_1}\right]$$

where:

Ea = activation energy (in eV)

k_0 = Boltzman constant

$$8.6 \times 10^{-5}\ \frac{eV}{°K}$$

T_1 = stress ambient temperature in °K, and

T_0 = operating ambient temperature in °K

Assumed Activation Energies

In many cases, device reliability can be approximated by using a composite activation energy. Studies of the infant mortality period indicate a very low activation energy for these failure mechanisms. Recent data suggests that a 0.55 eV activation energy is the most appropriate for establishing this time-temperature trade-off in screening for infant mortality. An activation energy of 0.7 eV is generally assumed as an average activation energy for times beyond the infant mortality period. Lucent Technologies often uses 0.7 eV and 55 °C operating temperature for steady-state reliability calculations. With these assumptions, temperature acceleration factors become:

A_T = 78—for 125 °C stress temperature

A_T = 260—for 150 °C stress temperature

Product Reliability Monitoring Plan

Lucent Technologies' product reliability monitoring plan is based on our fundamental pursuit of quality in every device within each product family we offer. Thus, we monitor our devices constantly, examining their performance over time as we search for and identify opportunities to further increase their reliability.

Reliability Monitoring Program

(continued)

Three-Tier Testing Program

A keystone of Lucent Technologies' reliability plan is its three-tier program of stress testing. Level 1 represents Lucent Technologies' extended life testing program, in which samples of devices are taken for initial qualification—and on a regular monthly schedule thereafter—from each reliability testing group and stressed for periods simulating up to 40 years of product life.

Level 2 is Lucent Technologies' normal production monitoring program in which a sample of devices is chosen from each testing group and stressed for a period approximating 10 years of product life. Level 2 samples are normally taken biweekly. Level 2 HTOB testing includes a test point at 24 hours which is intended as an infant mortality measurement.

Level 0 (HTOB testing) represents a test point of 24 hours, and is intended as an infant mortality measurement. It should be noted that some product families (particularly memory) omit Level 0 testing for HTOB.

Reliability Testing Procedures

Specific Procedures for HTOB Testing

Sample devices, chosen according to the protocol in Table 15, are loaded into boards and placed into the HTOB oven set for 150 °C (if not otherwise specified).

After testing, samples are cooled to 30 °C oven ambient temperature while under bias for a minimum of 30 minutes. They are then removed from the oven and electrically tested. Samples designated for Level 1 testing are then returned to the oven for an additional 840 hours: a total of 1,000 hours.

Specific Procedures for Temperature-Humidity Bias (THB) Testing

THB is designed to test the integrity of the package-chip interface, as well as chip metallization. THB samples are selected monthly from the testing universes shown in Table 16 in this section. Device selection is rotated within the testing group to give a representation of the different pinouts for different package sizes.

Samples are loaded into prescribed load boards, placed in the THB chamber for 240 hours (Level 2), and then electrically tested. Units which pass are reloaded and returned to the stressing chamber to complete 1,000 hours of testing.

Within one hour after this phase, the sample is placed in a moisture chamber, and posttesting is performed. Devices which fail in posttest are returned to the THB testing board for a 48-hour presoak (no bias), followed by a minimum of 48 hours with bias, and then retested.

Specific Procedures for Temperature Cycling (TC)

TC stressing is designed to detect thermal mismatches of materials. Devices are cycled through temperature extremes to accelerate such failure mechanisms.

TC samples are selected monthly from the testing universes depicted in Table 17. Device selection is rotated to ensure a distribution of different package types.

Samples are placed in the TC chamber with no bias for 100 cycles at the conditions listed in the accompanying tables. They are then tested electrically, and the data is entered into the database. Good devices are then returned to TC stressing to complete 300 cycle stressing.

Level 1 temperature cycling is considered destructive, and test devices are not shipped as normal products.

Failure recording is conducted as in the other stress testing routines.

Reliability Monitoring Program (continued)

Table 15. Sampling Plan: High-Temperature Operating Bias (HTOB)

Test Level	Test Hours	Sampling Frequency	Stress Conditions	Sample Size	LTPD (%)
0	48	Biweekly	125 °C	116	2.0
2	160	Biweekly	125 °C	116	2.0
1	1,000	Monthly	125 °C	116	2.0
0	24	Biweekly	150 °C	100	4.0
2	160	Biweekly	150 °C	100	4.0
1	1,000	Monthly	150 °C	58	4.0

Table 16. Sampling Plan: Temperature-Humidity Bias (THB)

Test Level	Test Hours	Sampling Frequency	Stress Conditions	Sample Size	LTPD (%)
2	240	Monthly	85 °C/85% RH	76	3.0
1	1,000	Monthly	85 °C/85% RH	76	3.0

Table 17. Sampling Plan: Temperature Cycle (TC)

Test Level	Test Cycles	Sampling Frequency	Stress Conditions	Sample Size	LTPD (%)
2	100	Monthly	–65 °C/+150 °	45	5.0
1	300	Monthly	–65 °C/+150 °	45	5.0

Product Families and Sampling Coverage

To facilitate product sampling and ensure complete coverage of our reliability program, all Lucent Technologies IC products are grouped into families according to their basic design and manufacturing process. The resulting product families are shown here.

- ASIC (including FPGAs)
- HPIC
- Microprocessors (including digital signal processors)
- Communication

Sample Selection and Sampling Universes

Level 2 samples are selected from the testing universes shown in Table 18 and Table 19. For HTOB, when several clean rooms are represented in the same testing universe, samples are taken from each combination of clean room and assembly location. Successive samples are taken from different wafer lots to ensure the reliability data represents a continuous flow of product from each clean room.

160-hour samples are extended 24-hour samples. Every other 160-hour sample is extended to 1,000 hours.

If a sample has more failures than permitted by the LTPD standards shown in Table 15, Table 16, and Table 17, a special RRB meeting is called to address the issue.

Reliability Monitoring Program (continued)

Table 18. Sampling Universes by Technology: HTOB

Super Family	Process Technology	Layout Style
CMOS		
A	3.5/5.0 LC	Analog
	3.5/5.0 C	Analog
	3.5/5.0 C	Custom Digital
	3.5/5.0 C	Standard Cell Digital
B	2.5 C	Custom Digital
	2.5 C	Standard Cell Digital
C	1.75 CT	Standard Cell Digital
	1.75 C	Analog/Custom Digital
	1.75 C	Standard Cell (1P 1M)
C.1	1.75 LC	Analog/Standard Cell (2P 1M)
D	1.25 C	Custom Digital
	1.25 C	Standard Cell Digital
	1.25 C	Memory
D.1	1.25 CT (2-level metal)	Standard Cell Digital
E	0.9 LC	Analog
	0.6 LC	Analog
F	0.9 CT	Standard Cell Digital
	0.6 CT	Standard Cell Digital
G	0.6 HD	High-Density CMOS
G.1	0.55 HD	High-Density CMOS
H	0.5 CT	Standard Cell Digital
I	0.35 CT	Standard Cell Digital
HPIC		
—	Linear Bipolar CBIC-M CBIC-L CBIC-R CBIC-S	—
—	Digital Bipolar SFOXL OXL SBC BEST	—
—	High-Voltage IC	—
—	Solid-State Relays	—
—	GaAs	—
NMOS		
J	3.5 N	Standard Cell Digital
	5.0/7.5 N	Analog
	5.0/7.5 N	Standard Cell Digital
K	1.7/1.9/2.8 N	Custom Digital

Table 19. Sampling Universes by Technology: THC and TC

Package Universe	Package Type	Package Variation
A	Ceramic DIP	300 MIL
		600 MIL
B	Plastic DIP	300 MIL
		600 MIL
C	Ceramic Chip Carrier	<40 Pins
		>40 Pins
D	Plastic Chip Carrier	<40 Pins
		>40 and <100 Pins
		≥100 Pins
E	Plastic Quad, Fine Pitch	≥100 Pins
F	Pin Grid Array	All
	Multiple In Line	All
G	Small Outline	SOJ
		SOG
H	Ceramic Leadless CC	All
I	Plastic Leadless CC	All
J	Ball Grid Array	All

Reliability Monitoring Program

(continued)

Calculating Failure Rates

Infant Mortality

Lucent Technologies measures devices after 24 hours of stress at 150 °C. With the following assumptions, 24-hour failure rates approximate the percentage of ICs that could be expected to fail in the first month of continuous use:

Ea = 0.4 eV
To = 55 °C

Early Life

With the same assumptions as for infant mortality, Lucent Technologies' 160-hour failure rate approximates the percentages of failures that could be expected to fail in the first half-year of continuous use.

Steady-State Life

IC instantaneous failure rates rapidly decrease to a low, relatively constant level. Steady-state instantaneous failure rates are often expressed in units of FITs, failures in 1 billion hours of operation. The FIT rate can be calculated from the equation:

$$\frac{X^2 (10)^9}{2 \times \text{sample size} \times \text{hours of stress} \times \text{acceleration factor}}$$

X^2 can be found from the probability table using (2f+2) degrees of freedom. For example, if two ICs in a sample of 500 fail after 1000 hours of life testing at 150 °C:

Instantaneous failure rate =

$$\frac{6.212 (10)^9}{2 \times 500 \times 1000 \times 260} = 24 \text{ FITs}$$

Assumptions:

Ea = 0.7 eV

To = 55 °C

X^2 @ 60% probability

Failure Mode Analysis (FMA)

Failure mode analysis (FMA) is a comprehensive procedure that determines the cause of IC failures that occur during manufacturing, qualification, or reliability monitoring. Special attention and high priority is assigned to customer returns.

Lucent Technologies' FMA laboratory is responsible for conducting FMA analysis. The laboratory is staffed by highly trained personnel who, through training and experience, have distinguished themselves as specialists.

Devices sent to the FMA lab are initially tested to confirm failure and determine test failure signature. The FMA engineer analyzes the results and determines the nature of the failure (opens or shorts, parametric, or functional).

The engineer may elect to perform full characterization and schmoo plots as well. When test results are complete, the engineer proceeds with the FMA.

Parametric failures and opens, shorts, or leakage are verified by a curve tracer or parametric analyzer.

Reliability Monitoring Program

(continued)

Functional failures of operating devices include pattern sensitivity, loss of voltage range, and timing failures. Bit maps are used to pinpoint these failures.

Functional failures are subjected to analysis of the die surface. The die is exposed using a decapsulation technique known not to compromise the bond pad or wire bond integrity.

After decapsulation, inspections are performed in the suspected areas. Layout and circuit schematics are used to confirm defects. If further analysis is needed, a systematic removal of the device layers is done, with a detailed inspection performed after each etch.

Analytical Lab

When more sophisticated analytical techniques are needed, the Lucent Technologies-Bell Labs Innovations analytical lab is used to conduct further FMA.

The analytical lab's facilities span the fields of optical and electron microscopy, ion beam techniques, and traditional analytical chemistry. Its staff is eminently qualified and equipped to perform any of a battery of more than 50 complex tests under controlled conditions.

Corrective Action

In cases in which a reliability sample has a significant number of failures (exceeding the allowed sample limit) such that the lot fails, corrective action of some form is necessary. Corrective action is also necessary when there are customer returns having unique failure mechanisms or when shop yield loss becomes excessive.

Corrective action in these cases is carried out by a Reliability Review Board (RRB). A Reliability Review Board may be convened by anyone with a device issue. The membership of an RRB is composed of those technical experts needed to determine the nature of the device issue. RRB membership is flexible but usually consists of product engineers, reliability engineers, process engineers, and customer technical support engineers. Other people with technical expertise are added to RRB membership as the need arises.

The first obligation of an RRB is to protect the customer. To this end, every effort is made to confine the device issue to a wafer lot or an assembly lot and isolate the offending material. If material has escaped and represents a threat to the customer, the RRB is obligated to notify all customers receiving the affected product. Secondly, the RRB is responsible for obtaining careful failure analysis to determine the root cause of failure. With an accurate determination of root cause in hand, the RRB determines the corrective action to be implemented. The ownership of the corrective action is assigned, and implementation is carried out under the direction of the process owner.

The RRB must then determine if the corrective action has been effective. Only after sufficient data are gathered to verify the effectiveness of the corrective action is the work of the RRB completed and the RRB disbanded.

Corrective action is documented in several different ways. The RRB may keep minutes of their meetings. If minutes are not kept, the reliability engineer (who is a member of the RRB) is obligated to maintain a running summary of the activities of the RRB. This summary is reviewed periodically for progress toward stated goals. In addition, a RRB Corrective Action report is made to management when the RRB is formed. It is updated periodically and reissued when the RRB disbands.

INQUIRE Database

INQUIRE Database and Its Role in Quality Assurance

Lucent Technologies maintains a number of databases as part of its Quality Information Systems Architecture, organized into a system called INQUIRE. Figure 11 shows the INQUIRE system architecture.

INQUIRE is an on-line system which provides access to component quality information. It provides access to data produced as a result of qualification, reliability, and final inspection testing performed throughout Lucent Technologies. INQUIRE also features access to an index of documents available on manufactured devices, and documents can be easily ordered via an on-line request feature.

INQUIRE collects information from several internal Lucent Technologies databases used to manage and track the quality of manufactured product. Its menu-driven system offers query functions, help options, report and graphics generation, and a bulletin board. It also features a single point of contact for user questions, and the on-line documentation ordering function.

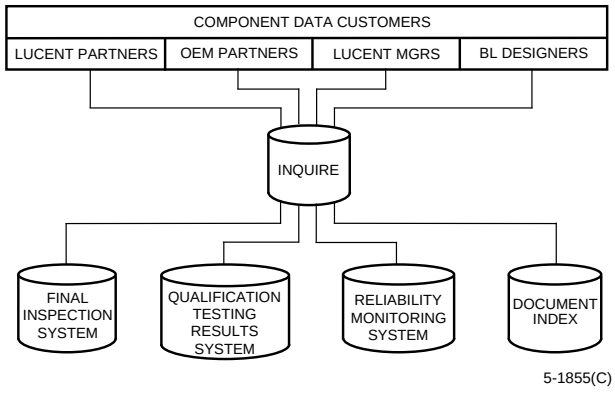

Figure 11. INQUIRE System Architecture

Qualification Test Data

Lucent Technologies performs qualification testing on devices in many product families. The testing is performed to demonstrate the reliability of both new technologies and changes to existing technologies.

Product qualification results are tracked throughout Lucent Technologies' production facilities by the Qualification Testing Results Systems (QTRS) and fed to INQUIRE in twice-weekly consolidated updates. The qualification information available from INQUIRE can be displayed in query or report format and includes qualification test results by device type.

Historical bases for the individual qualifications such as new process qualifications and new code qualifications are also available. As the qualification process of a product evolves, its status can be tracked. Available reports include a qualification device summary list.

Reliability Monitoring Data

Lucent Technologies also performs reliability testing on devices in most product families, in order to ensure that reliability objectives are met on an ongoing basis. These results are tracked by the Reliability Monitoring System (RELMS) and fed to INQUIRE in weekly updates.

INQUIRE can display this data in query, report, or graphic format. Data includes reliability test results summarized by device code, test universe, or technology family. All Failure Mode Analysis (FMA) data and related corrective actions are also available.

Available reports include a reliability test summary report, a test universe summary, and a reliability device level summary report. Graphic output includes charts summarizing percent defective per technology family and percent defective per test universe.

Lucent Technologies product quality data is collected on a lot-by-lot basis for all manufactured device codes and used to calculate and report the performance of product families.

INQUIRE Database (continued)

Final inspection test results are tracked throughout Lucent Technologies by the Final Inspection System (FIS) and fed to INQUIRE in monthly consolidated updates. Product performance is reported in ppm defective, and represents the Average Outgoing Quality (AOQ) of the product.

Report data is available through INQUIRE in query, report, or graphic format. Final inspection test results can by summarized by Strategic Business Unit, such as MOS; by product family, such as ASICs, or by individual device type. Results can also be organized by current month, three-month interval, and 12-month interval.

Document Availability Information

Lucent Technologies provides documents for most of its devices. These documents take the form of data sheets, user manuals, application notes, and product briefs, for example.

Document availability is tracked by INQUIRE's Document Index Database. Users can order documents on-line and can query document availability on-line as well as obtain printed reports.

Applications

System designers and component selection engineers can use INQUIRE to choose components for their specific application. Users can input a specific device type into INQUIRE, and extract the information they need to make a choice.

After they identify components for specific applications, users can confirm that the components have been appropriately qualified by accessing the Qualification Data Query screen, which displays the qualification document number plus qualification results.

As these users continue the component selection process, they can access the Reliability Data Query Screen and the Final Inspection Data Query Screen to identify ongoing reliability data, as well as the quality performance of each device in order to make an informed decision. System designers who need more information can order data sheets electronically from INQUIRE as well.

Customer Support

Customer Service and the Device Quality Issue (DQI) Process

Customer satisfaction is a top priority in the Lucent Technologies quality effort. Lucent Technologies utilizes a philosophy of having a central point of contact for customers to obtain information, gain access to additional resources, and log complaints. The Customer Technical Support Center (CTSC) is the central point of contact for quality issues, and is responsible for receiving and resolving formal and informal complaints of a technical nature. All of our customer contact employees (salespersons, engineers, managers, etc.) are instructed to direct informal complaints to the CTSC to ensure that all complaints are aggregated into quality issues.

Formal quality complaints are generally received and managed via our Device Quality Issue (DQI) process shown in Figure 12. The process incorporates documentation of the pertinent facts surrounding the issue and the provision of samples for analysis. Complaints originating from customers unfamiliar with our DQI system are converted to DQIs to provide a common internal path for all quality complaint management. These customers also receive information about our DQI system to aid any future complaint resolution. A comprehensive database is maintained to aggregate and track DQI issues.

All pertinent facts related to the issue are identified, including the source of the issue (incoming inspection, factory failure, and field failure), the generic type of issue (conformance with specifications, performance of existing specifications, customer-induced failure, and no trouble found), and a brief description of the mode of failure and corrective action.

In addition, the CTSC maintains a telephone log of customer comments and general issues. A routine report analyzes the DQI database to identify trends. The report is distributed to all responsible management.

Customer Support (continued)

In addition to the DQI system, a Return Material Approval (RMA) system, managed by the Customer Service Organization, is monitored by CTSC personnel. The RMAs are reviewed to determine if a quality-related problem caused the return. If so, a DQI is issued to investigate and report on the issue.

The customer is provided with an initial response within 48 hours of the receipt of a quality issue. When appropriate, the response reports on the results of the initial retest of the product. In any case, the 48-hour response notifies the customer that the quality issue has been received and is being addressed.

The goal is to provide a final, written report within ten working days of initiation of the issue. The report provides the initial retest results, the failure-mode analysis findings, and the corrective action to be implemented. When more than ten days are required to complete the investigation and the report, a written report of the proposed procedure necessary to complete the investigation is provided within ten days. The customer is the final arbiter in any investigation regarding the satisfactory nature of the investigation of the report.

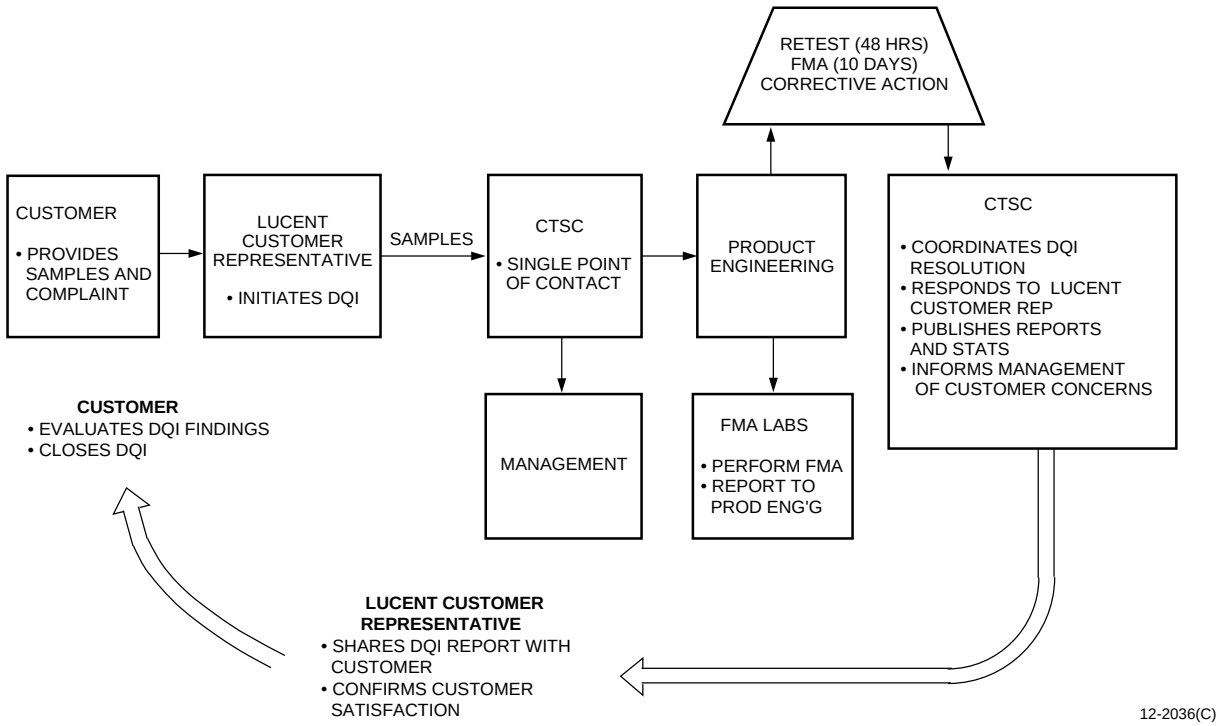

Figure 12. DQI Full-Circle Process Flow

Device Qualification Test Procedures and Results

The purpose of this section is to document the qualification test procedures and results of the ATT3000 and *ORCA* Series FPGA product families. The qualification plan for these FPGA product families involves rigorous environmental, mechanical, and electrical testing to confirm product soundness. Industry-standard tests are applied to test devices, as well as additional specialized tests to examine electrostatic discharge and latch-up parameters.

Failure mode analysis (FMA) is a comprehensive procedure which determines the cause of any failure encountered during the qualification testing. FMA is used as an integral part of quality testing and surveillance to assess any performance flaw, determine corrective measures, and implement these measures to eliminate recurrence.

ATT3000 Series Qualification

There are five arrays in the ATT3000 Series FPGA product family: ATT3020, ATT3030, ATT3042, ATT3064, and ATT3090. These arrays are then assembled in a number of different plastic packages. These packages are plastic-leaded chip carrier (PLCC), plastic-pin grid array (PPGA), metric-quad flat pack (MQFP), thin-quad flat pack (TQFP), and shrink-quad flat pack (SQFP).

Qualification Strategy

The qualification of ATT3000 Series FPGAs can be broken into three specific groups: process technology, silicon design, and package.

Process Technology: These arrays are processed using the 0.6 µm and 0.55 µm CMOS technologies. Lucent Technologies' 0.6 µm and 0.55 µm CMOS processes employ N- and P-channel LDD MOS transistors. They also use two levels of metal and one level of polycide. Source and drain regions are silicided for low resistance. These technologies have been rigorously tested for reliability and manufacturability and are fully qualified.

Silicon Design: Since the five arrays in the ATT3000 Series FPGAs are a matrix of repetitive elements, the Qualification Review Board (QRB) decided to qualify one die which would qualify the silicon design methodology of all five arrays. Therefore, needed tests were performed on the ATT3090 die in the 84-pin PLCC package for 0.6 µm and on the ATT3042 die in the 84-pin PLCC package for 0.55 µm.

Package: The QRB determined the qualification requirements of each die in a given package. The results are given in Table 20 (0.6 µm) and Table 21 (0.55 µm).

ATT3000 Series Qualification (continued)

Table 20. ATT3000 Series (0.6 μm)

Qualification Information	Device						
	3090-84PLCC (Q92055)	3090-175PPGA (Q92054)	3042-100TQFP (QRB92.51)	3042-100QFP (QRB93.2)	3090-84PLCC (0.9 μm) (Q90148)	3090-160QFP (0.9 μm) (Q90140)	3090-175PPGA (0.9 μm) (Q90137)
ESD-HBM[1]	>2000 V	>2500 V	>2000 V	>1500 V	>3500 V	>2000 V	>3000 V
ESD-CDM[1]	>2000 V	>3000 V	>3000 V	>3000 V	>3000 V	>2000 V	>2500 V
1000 hrs. HTOB	1/105[2] Pass	1/105[3] Pass	—	—	—	—	0/98 Pass
1000 hrs. THB	—	—	—	—	0/133 Pass	1/134[4] Pass	1/135[6] Pass
CLASS	—	—	—	—	0/134 Pass	0/134 Pass	0/135 Pass
Autoclave (96 hrs. SB)	—	—	—	—	0/105 Pass	2/105 Pass	—
100 c/s TC	—	—	—	—	0/105 Pass	2/105[5] Pass	0/105 Pass
15 c/s TS	—	—	—	—	0/25 Pass	0/25 Pass	0/125 Pass
Moisture Resistance	—	—	—	—	—	—	0/38 Pass
Corrosion	—	—	—	—	—	—	0/15 Pass
Solvent Resistance	—	—	—	—	—	—	0/8 Pass
Physical Dimensions	—	—	—	—	—	Pass	0/15 Pass
Solderability	—	—	—	—	—	—	Note 7
Bond Strength	—	—	—	—	—	—	Pass
Die Shear Strength	—	—	—	—	—	—	Pass
X-Ray	—	—	—	—	—	—	0/5 Pass
LU Class	IV	IV	IV	IV	IV	IV	IV
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. FMA reported a gate-level defect.
3. Defective package. 5 Ω short from V_{SS} to V_{DD}.
4. FMA reported gate-level defect found and isolated. Changes in the silicide process have been made to address this failure mechanism.
5. FMA reported lifted ball bond and package stress crack.
6. Defective package.
7. Leads to be solder dipped before shipment.

ATT3000 Series Qualification (continued)

Table 20. ATT3000 Series (0.6 μm) (continued)

Qualification Information	Device			
	1042L.BR (Q89166)	**409AT (Q89027)**	***WE*®-DSP32CF32 (Q89129.1)**	**409ATX (Q90001)**
Chip Size (μm)	7410 x 7710	7040 x 6830	8210 x 10960	6830 x 7040
Package	68-pin PLCC	100-pin PLCC	164-pin PQFP	100-pin MQFP
Steam Bomb	0/105 Pass	—	1/105 Pass	1/105 Pass
1000 hrs. HTOB	0/135 Pass	1/142 Pass	0/105 Pass	2/168 Pass
Class	2/135 Pass	1/134 Pass	1/137 Pass	0/132 Pass
1000 hrs. THB	0/132 Pass	1/133 Pass	0/135 Pass	0/132 Pass
100 c/s TC or 300 c/s TC	1/105 Pass	1/105 Pass	0/105 Pass	0/105 Pass
15 c/s TS or 100 c/s TS	0/24 Pass	0/25 Pass	0/25 Pass	0/25 Pass
Moisture Resistance	—	—	—	0/38 Pass
Corrosion	—	—	—	0/15 Pass
Solvent Resistance	—	—	—	0/8 Pass
Physical Dimension	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Solderability	—	—	—	0/22 (3 devices) Pass
LI	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Bond Strength	—	0/15 Pass	—	—
Die Shear Strength	—	0/5 Pass	—	—
X-Ray	0/5 Pass	0/5 Pass	0/5 Pass	0/5 Pass
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

ATT3000 Series Qualification (continued)

Table 20. ATT3000 Series (0.6 μm) (continued)

Qualification Information	Device	
	S1116X (Q90111)	**MR120 (Q92055)**
Chip Size (μm)	6830 x 7040	8130 x 8130
Package	100-pin MQFP	208-pin SQFP
Steam Bomb	0/105 Pass	0/105 Pass
1000 hrs. HTOB	1/105 Pass	0/105 Pass
Class	2/132 Pass	0/132 Pass
1000 hrs. THB	0/129 Pass	0/129 Pass
100 c/s TC or 300 c/s TC	1/105 Pass	1/105 Pass
15 c/s TS or 100 c/s TS	0/25 Pass	1/25 Pass
Moisture Resistance	0/38 Pass	—
Corrosion	0/15 Pass	—
Solvent Resistance	0/8 Pass	—
Physical Dimension	0/15 Pass	0/15 Pass
Solderability	0/22 (3 devices) Pass	—
LI	0/15 Pass	—
Bond Strength	—	—
Die Shear Strength	—	—
X-Ray	0/5 Pass	—
Status	Fully Qualified	Fully Qualified

ATT3000 Series Qualification (continued)

Table 21. ATT3000 Series (0.55 μm)

Qualification Information	Device		
	3042-84PLCC (Q95273)	**3090-84PLCC (Q96098)**	**3090-208SQFP (Q96099)**
ESD-HBM[1]	>1000 V	>1000 V	>2000 V
ESD-CDM[1]	>1000 V	>500 V[2]	>1000 V
1000 hrs. HTOB	0/105 Pass	—	—
1000 hrs. THB	—	—	—
CLASS	—	—	—
Autoclave (96 hrs. SB)	—	—	—
100 c/s TC	—	—	—
15 c/s TS	—	—	—
Moisture Resistance	—	—	—
Corrosion	—	—	—
Solvent Resistance	—	—	—
Physical Dimensions	—	—	—
Solderability	—	—	—
Bond Strength	—	—	—
Die Shear Strength	—	—	—
X-Ray	—	—	—
LU Class	II	III	II
Status	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. The corner pins pass >1000 V.

ATT3000 Series Qualification (continued)

Table 21. ATT3000 Series (0.55 μm) (continued)

Qualification Information	Device	
	MR109 (MR109)	**MR120 (MR120)**
Chip Size (μm)	10280 x 10120	8130 x 8130
Package	84-pin PLCC	208-pin SQFP
Steam Bomb	0/45 Pass	0/105 Pass
1000 hrs. HTOB	0/135 Pass	0/105 Pass
Class	0/132 Pass	0/132 Pass
1000 hrs. THB	0/132 Pass	0/129 Pass
100 c/s TC or 300 c/s TC	1/105[3] Pass	1/105 Pass
15 c/s TS or 100 c/s TS	0/25 Pass	1/25 Pass
Moisture Resistance	0/38 Pass	—
Corrosion	0/15 Pass	—
Solvent Resistance	0/8 Pass	—
Physical Dimension	0/15 Pass	0/15 Pass
Solderability	0/22 Pass	—
LI	0/15 Pass	—
Bond Strength	0/15 Pass	—
Die Shear Strength	0/5 Pass	—
X-Ray	0/5 Pass	—
Status	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. The corner pins pass >1000 V.
3. Aluminum short caused by collet damage.

ORCA 1C Series Qualification

There are four arrays in the *ORCA* 1C Series FPGA product family: ATT1C03, ATT1C05, ATT1C07, and ATT1C09. These arrays are then assembled in a number of different packages. These packages are plastic-leaded chip carrier (PLCC), metric-quad flat pack (MQFP), thin-quad flat pack (TQFP), shrink-quad flat pack (SQFP), and ceramic-pin grid array (CPGA).

Qualification Strategy

The qualification of *ORCA* 1C Series FPGAs can be broken into three specific groups: process technology, silicon design, and package.

Process Technology: These arrays are processed using the 0.6 µm CMOS technology. Lucent Technologies' 0.6 µm CMOS process employs N- and P-channel LDD MOS transistors. The process also uses two levels of metal and one level of polycide. Source and drain regions are silicided for low resistance. This technology has been rigorously tested for reliability and manufacturability and is fully qualified.

Silicon Design: Since the four arrays in the *ORCA* 1C Series FPGAs are a matrix of repetitive elements, the qualification review board (QRB) decided to qualify one die which would qualify the silicon design methodology of all four arrays. Therefore, needed tests were performed on the ATT1C05 die in the 240-pin SQFP package.

Package: The QRB determined the qualification requirements of each die in a given package. The results are given in Table 22.

ORCA 1C Series Qualification (continued)

Table 22. *ORCA* 1C Series (0.6 μm)

Qualification Information	Device				
	ATT1C05-240SQFP (Q92167)	ATT3090-175PPGA (Q92054)	ATT1C07-304SQFP (Q94044)	ATT3090-175CPGA (Q92161)	1051CN (Q92168)
ESD—HBM[1]	>2000 V	>2500 V	>2000 V	>1000 V	>1000 V
ESD—CDM[1]	>3000 V	>3000 V	>2000 V	>2000 V	>2000 V
1000 hrs. HTOB	0/109 Pass	1/105 Pass[3]	—	0/133 Pass	1/105 Pass[7]
1000 hrs. THB	1/132 Pass[2]	—	—	—	—
Class	0/132 Pass	—	—	—	—
Steam Bomb	1/105 Pass[4]	—	—	—	—
100 c/s TC or 300 c/s TC	1/105 Pass[5]	—	—	0/105 Pass	—
15 c/s TS or 100 c/s TS	1/15 Pass[6]	—	—	—	—
Moisture Resistance	0/38 Pass	—	—	—	—
Corrosion	—	—	—	—	—
Solvent Resistance	—	—	—	—	—
Physical Dimension	0/15 Pass	—	—	—	—
Solderability	0/22 Pass	—	—	0/3 Pass	—
Bond Strength	—	—	—	—	—
Die Shear Strength	—	—	—	—	—
X-Ray	0/5 Pass	—	—	—	—
Latch-Up	IV	IV	III	IV	IV
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. One marginal functional failure after 432 hours (acceptable). No other devices failed after 1000 hours.
3. Defective package. 5 Ω short from V_{SS} to V_{DD}.
4. No defect found.
5. One open via found.
6. One mechanically broken wire found.
7. Particles at polysilicon along edge of gate due to poor spacer.

ORCA 1C Series Qualification (continued)

Table 22. *ORCA* 1C Series (0.6 µm) (continued)

Qualification Information	Device		
	3042-100TQFP (QRB92.51)	**MR120 (Q92055)**	**MR141**[8]
ESD—HBM[1]	>2000 V	>1000 V	—
ESD—CDM[1]	>3000 V	>1000 V	—
1000 hrs. HTOB	—	0/105 Pass	0/105 Pass
1000 hrs. THB	—	0/129 Pass	0/131 Pass
Class	—	0/132 Pass	—
Steam Bomb	—	0/105 Pass	0/105 Pass
100 c/s TC or 300 c/s TC	—	0/105 Pass	0/105 Pass
15 c/s TS or 100 c/s TS	—	1/25 Pass[9]	0/25 Pass
Moisture Resistance	—	—	0/38 Pass
Corrosion	—	—	0/15 Pass
Solvent Resistance	—	—	0/8 Pass
Physical Dimension	—	0/15 Pass	—
Solderability	—	—	0/22 Pass
Bond Strength	—	—	0/15 Pass
Die Shear Strength	—	—	0/15 Pass
X-Ray	—	—	0/5 Pass
Latch-Up	IV	II	—
Status	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. One marginal functional failure after 432 hours (acceptable). No other devices failed after 1000 hours.
3. Defective package. 5 Ω short from V_{SS} to V_{DD}.
4. No defect found.
5. One open via found.
6. One mechanically broken wire found.
7. Particles at polysilicon along edge of gate due to poor spacer.
8. Also passed lead integrity (0/15).
9. Gate-level defect found under polysilicon gate.

ORCA 2C Series Qualification

There are eight arrays in the *ORCA* 2C Series FPGA product family: ATT2C04, ATT2C06, ATT2C08, ATT2C10, ATT2C12, ATT2C15, ATT2C26, and ATT2C40. These arrays are then assembled in a number of different packages. These packages are plastic-leaded chip carrier (PLCC), metric-quad flat pack (MQFP), plastic-quad flat pack (QFP), plastic-ball grid array (PBGA), thin-quad flat pack (TQFP), shrink-quad flat pack (SQFP), and ceramic-pin grid array (CPGA).

Qualification Strategy

The qualification of *ORCA* 2C Series FPGAs can be broken into three specific groups: process technology, silicon design, and package.

Process Technology: These arrays are processed using the 0.5 µm CMOS technology. Lucent Technologies' 0.5 µm CMOS process employs N- and P-channel LDD MOS transistors. The process also uses three levels of metal. This technology has been rigorously tested for reliability and manufacturability and is fully qualified.

Silicon Design: Since the eight arrays in the *ORCA* 2C Series FPGAs are a matrix of repetitive elements, the Qualification Review Board (QRB) decided to qualify one die which would qualify the silicon design methodology of all eight arrays. Therefore, needed tests were performed on the ATT2C15 die in the 304-pin SQFP package.

Package: The QRB determined the qualification requirements of each die in a given package. The results are given in Table 24.

ORCA 2C Series Qualification (continued)

Table 23. *ORCA* 2C Series (0.5 μm)

Qualification Information	Device					
	ATT2C04-160QFP (Q95319)	ATT2C10-256BGA (Q96068)	ATT2C10-304SQFP (Q95041)	ATT2C15-208SQFP (Q94290)	ATT2C15-240SQFP (Q93234)	ATT2C15-304SQFP (Q94046)
ESD—HBM[1]	>2000 V	>2000 V	>2000 V	>2000 V	>2000 V	>2000 V
ESD—CDM[1]	>1000 V	>1000 V	>1000 V	>1000 V	>1000 V	>1000 V
1000 hrs. HTOB	—	—	—	—	1/60 Pass[2]	1/60 Pass[2]
1000 hrs. THB	—	—	—	—	1/120 Pass[3]	1/132 Pass[4]
Class	—	—	—	—	0/133 Pass	0/133 Pass
Steam Bomb	—	0/46 Pass	0/45 Pass	—	0/105 Pass	0/105 Pass
100 c/s TC or 300 c/s TC	—	0/47 Pass	—	—	0/105 Pass	0/105 Pass
15 c/s TS or 100 c/s TS	—	0/16 Pass	—	—	0/16 Pass	0/15 Pass
Moisture Resistance	—	—	—	—	—	—
Corrosion	—	—	—	—	—	—
Solvent Resistance	—	—	—	—	—	—
Physical Dimension	—	0/15 Pass	—	—	—	—
Solderability	—	—	—	—	—	—
Bond Strength	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—
X-Ray	—	—	0/5 Pass	—	—	—
Latch-Up	II	II	II	II	II	II
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model; see page 13 for test descriptions.
2. Electrical overstress.
3. Metal 1 short.
4. FMA found failure due to horizontal crack, which created EOS damage.

ORCA 2C Series Qualification (continued)

Table 23. *ORCA* 2C Series (0.5 μm) (continued)

Qualification Information	Device						
	ATT2C26-304SQFP-PQ2 (Q94227)	ATT2C15-364CPGA (Q93231)[5]	ATT2C40-208SQFP-PQ2 (QRB95.17)	ATT2C40-240SQFP-PQ2 (Q95007)	1159J (Q94124)	T92020S (Q93181)	1042BG (T92222)
ESD—HBM[1]	>2000 V	—	—	>2000 V	>2000 V	>2000 V	>2000 V
ESD—CDM[1]	>1000 V	>1000 V	—	>1000 V	>1500 V	>1000 V	>2000 V
1000 hrs. HTOB	0/65 Pass	1/60 Pass[6]	—	—	0/97 Pass	1/105[7] Pass	0/105 Pass
1000 hrs. THB	0/100 Pass	—	—	0/77 Pass	0/132 Pass	0/130 Pass	0/132 Pass
Class	0/100 Pass	—	—	0/80 Pass	0/132 Pass	0/132 Pass	0/132 Pass
Steam Bomb	0/45 Pass	—	—	—	0/105 Pass	0/105 Pass	0/105 Pass
100 c/s TC or 300 c/s TC	0/50 Pass	0/45 Pass	—	0/46 Pass	0/105 Pass	0/105 Pass	0/105 Pass
15 c/s TS or 100 c/s TS	0/15 Pass	0/15 Pass	—	—	0/25 Pass	0/25 Pass	0/25 Pass
Moisture Resistance	—	—	—	—	—	—	—
Corrosion	—	—	—	—	—	—	—
Solvent Resistance	—	—	—	—	—	—	—
Physical Dimension	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass	—	0/15 Pass	—
Solderability	—	—	—	—	—	—	—
Bond Strength	—	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—	—
X-Ray	—	—	—	—	—	—	—
Latch-Up	II	—	—	II	IV	II	IV
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model; see page 13 for test descriptions.
2. Electrical overstress.
3. Metal 1 short.
4. FMA found failure due to horizontal crack, which created EOS damage.
5. Mechanical sequence test was also passed (0/38).
6. Conductive particle in interlevel dielectric.
7. No failure found in FMA.

ORCA 2C Series Qualification (continued)

Table 23. *ORCA* 2C Series (0.5 μm) (continued)

Qualification Information	Device		
	MR109 (MR109) 84-PLCC	**MR119 (MR119)**	**ATT2C26-388BGA (Q95013)**[12]
ESD—HBM[1]	>3000 V	—	>2000 V
ESD—CDM[1]	>1000 V	—	>500 V[13]
1000 hrs. HTOB	0/135 Pass	1/103[9] Pass	0/59 Pass
1000 hrs. THB	0/132 Pass	0/130 Pass	0/48 Pass
Class	0/132 Pass	—	0/89 Pass
Steam Bomb	0/45 Pass	0/105 Pass	0/50 Pass
100 c/s TC or 300 c/s TC	1/105[8] Pass	2/105[10] Pass	0/50 Pass
15 c/s TS or 100 c/s TS	0/25 Pass	0/25 Pass	0/15 Pass
Moisture Resistance	0/38 Pass	1/38[11] Pass	0/38 Pass
Corrosion	0/15 Pass	0/15 Pass	0/15 Pass
Solvent Resistance	0/8 Pass	0/8 Pass	0/15 Pass
Physical Dimension	0/15 Pass	—	0/15 Pass
Solderability	0/22 Pass	0/22 Pass	—
Bond Strength	0/15 Pass	—	—
Die Shear Strength	0/5 Pass	—	—
X-Ray	0/5 Pass	0/5 Pass	0/5 Pass
Latch-Up	IV	—	II
Status	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model; see page 13 for test descriptions.
2. Electrical overstress.
3. Metal 1 short.
4. FMA found failure due to horizontal crack, which created EOS damage.
5. Mechanical sequence test was also passed (0/38).
6. Conductive particle in interlevel dielectric.
7. No failure found in FMA.
8. Aluminum short caused by collet damage.
9. No defect found.
10. FMA found failure was due to ball bond pullout.
11. EOS damage.
12. Ball integrity test was also passed (0/15).
13. Corner pins pass >1000 V.

ORCA 2CxxA (5.0 V) Series Qualification

There are eight arrays in the *ORCA* 2CxxA Series FPGA product family: OR2C04A, OR2C06A, OR2C08A, OR2C10A, OR2C12A, OR2C15A, OR2C26A, and OR2C40A. These arrays are then assembled in a number of different packages. These packages are plastic-leaded chip carrier (PLCC), plastic-quad flat pack (QFP), thin-quad flat pack (TQFP), shrink-quad flat pack (SQFP), shrink-quad flat pack—powerquad 2 option (SQFP2), plastic-ball grid array (PBGA), and enhanced-ball grid array (EBGA).

Qualification Strategy

The qualification of *ORCA* 2CxxA Series FPGAs can be broken into three specific groups: process technology, silicon design, and package.

Process Technology: These arrays are processed using the 0.35 µm CMOS technology. Lucent Technologies' 0.35 µm CMOS process employs N- and P-channel LDD MOS transistors. The process also uses three levels of metal. This technology has been rigorously tested for reliability and manufacturability and is fully qualified.

Silicon Design: Since the eight arrays in the *ORCA* 2CxxA Series FPGAs are a matrix of repetitive elements, the Qualification Review Board (QRB) decided to qualify one die which would qualify the silicon design methodology of all eight arrays. Therefore, needed tests were performed on the OR2C15A die in the 208-pin SQFP package.

Package: The QRB determined the qualification requirements of each die in a given package. The results are given in Table 24.

ORCA 2CxxA (5.0 V) Series Qualification (continued)

Table 24. OR2CxxA Series (0.35 μm)

Qualification Information	Device					
	OR2C04A 84 PLCC (Q96235.2)	OR2C04A 100 TQFP (Q96236.1)	OR2C15A 208 SQFP (T96005.1)[2]	ATT2C15AE 208 SQFP (T96005)	OR2C15A 304 SQFP (Q97037)[3]	ATT2C15AE 304 SQFP (EE95210.1)
ESD—HBM[1]	>2500 V	>2500 V	Ref.	>2000 V	—	—
ESD—CDM[1]	>2000 V	>2000 V	Ref.	>1000 V	Ref.	>1000 V
1000 hrs. HTOB	—	—	Ref.	0/64 Pass	Ref.	0/62 Pass
1000 hrs. THB	—	—	Ref.	0/80 Pass	Ref.	0/104 Pass
Class	—	—	Ref.	0/85 Pass	Ref.	0/108 Pass
Moisture Sensitivity Level	—	—	—	—	Ref.	3
Steam Bomb	—	—	Ref.	0/80 Pass	Ref.	0/105 Pass
100 c/s TC or 300 c/s TC	—	—	Ref.	0/80 Pass	Ref.	0/50 Pass
15 c/s TS or 100 c/s TS	—	—	Ref.	0/26 Pass	Ref.	0/25 Pass
Moisture Resistance	—	—	—	—	—	—
Corrosion	—	—	—	—	—	—
Solvent Resistance	—	—	—	—	—	—
Physical Dimension	—	—	—	—	—	—
Solderability	—	—	—	—	—	—
Bond Strength	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—
X-Ray	—	—	Ref.	0/5 Pass	Ref.	0/5 Pass
Latch-Up	II	II	Ref.	II	—	—
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qual No. T96005.1 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T96005.
3. Qual No. T97037 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. EE95210.1.

ORCA 2CxxA (5.0 V) Series Qualification (continued)

Table 24. OR2CxxA Series (0.35 μm) (continued)

Qualification Information	Device				
	OR2C15A 352 PBGA (T95276.2)[4]	ATT2C15AE 352 PBGA (T95276.1)	OR2T40A 600 EBGA (Q97048.1)	160 MQFP (MR217)[6,8]	100 TQFP (MR221)[6,7]
ESD—HBM[1]	—	—	—	—	—
ESD—CDM[1]	Ref.	>1000 V	—	—	—
1000 hrs. HTOB	Ref.	0/105 Pass	—	0/64 Pass	0/105 Pass
1000 hrs. THB	Ref.	0/74 Pass	—	0/132 Pass	0/80 Pass
Class	Ref.	3/75[5] Pass	—	0/132 Pass	0/133 Pass
Moisture Sensitivity Level	Ref.	4	—	—	—
Steam Bomb	Ref.	0/80 Pass	—	0/105 Pass	0/47 Pass
100 c/s TC or 300 c/s TC	Ref.	0/80 Pass	—	0/105 Pass	0/47 Pass
15 c/s TS or 100 c/s TS	Ref.	0/26 Pass	—	0/25 Pass	0/25 Pass
Moisture Resistance	—	—	—	0/37 Pass	0/38 Pass
Corrosion	—	—	—	0/15 Pass	0/15 Pass
Solvent Resistance	—	—	—	0/8 Pass	0/8 Pass
Physical Dimension	Ref.	0/15 Pass	—	0/15 Pass	0/15 Pass
Solderability	—	—	—	0/22 Pass	0/22 Pass
Bond Strength	—	—	—	—	—
Die Shear Strength	—	—	—	—	—
X-Ray	Ref.	0/5 Pass	—	0/5 Pass	0/5
Latch-Up	—	—	—	—	—
Status	Fully Qualified	Fully Qualified	In Process	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qual No. T96005.1 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T96005.
3. Qual No. T97037 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. EE95210.1.
4. Qual No. T95276.2 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T95276.1.
5. Codemarking lifted off of three devices, but they passed electrically and a second THB run.
6. Qualification Information may be referenced from multiple Qualification Numbers.
7. Also passed lead integrity (0/15).
8. Also passed lead integrity (0/5).

ORCA 2CxxA (5.0 V) Series Qualification (continued)

Table 24. OR2CxxA Series (0.35 μm) (continued)

Qualification Information	Device						
	144 TQFP (MR225)[6,7]	208 SQFP (MR229)[6,8]	240 SQFP (MR232)[6,7]	304 SQFP (MR233)[6,7]	208 SQFP2 (MR243)[6,7]	240 SQFP2 (MR244)[6,7]	304 SQFP2 (MR245)[6,7]
ESD—HBM[1]	—	—	—	—	—	—	—
ESD—CDM[1]	—	—	—	—	—	—	—
1000 hrs. HTOB	0/105 Pass	0/64 Pass	0/62 Pass	0/62 Pass	0/62 Pass	0/62 Pass	0/62 Pass
1000 hrs. THB	0/130 Pass	0/80 Pass	1/120[10] Pass	1/120[10] Pass	0/100 Pass	0/100 Pass	0/100 Pass
Class	0/132 Pass	0/85 Pass	0/148 Pass	0/148 Pass	0/101 Pass	0/101 Pass	0/101 Pass
Moisture Sensitivity Level	—	—	—	—	—	—	—
Steam Bomb	0/105 Pass	0/80 Pass	0/48 Pass	0/48 Pass	0/45 Pass	0/45 Pass	0/45 Pass
100 c/s TC or 300 c/s TC	1/105[9] Pass	0/80 Pass	0/80 Pass	0/80 Pass	0/50 Pass	0/50 Pass	0/50 Pass
15 c/s TS or 100 c/s TS	0/45 Pass	0/26 Pass	0/16 Pass	0/16 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Moisture Resistance	0/38 Pass	0/37 Pass	0/38 Pass	0/38 Pass	0/38 Pass	0/38 Pass	0/38 Pass
Corrosion	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Solvent Resistance	0/8 Pass	0/8 Pass	0/8 Pass	0/8 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Physical Dimension	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass	0/12 Pass	0/15 Pass	0/15 Pass
Solderability	0/22 Pass	0/22 Pass	0/22 Pass	0/22 Pass	—	—	—
Bond Strength	—	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—	—
X-Ray	0/5 Pass	0/5 Pass	0/5 Pass	0/5 Pass	0/5 Pass	0/5 Pass	0/5 Pass
Latch-Up	—	—	—	—	—	—	—
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qual No. T96005.1 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T96005.
3. Qual No. T97037 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. EE95210.1.
4. Qual No. T95276.2 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T95276.1.
5. Codemarking lifted off of three devices, but they passed electrically and a second THB run.
6. Qualification Information may be referenced from multiple Qualification Numbers.
7. Also passed lead integrity (0/15).
8. Also passed lead integrity (0/5).
9. FMA results: The one failure passed 300 cycles after retest.
10. FMA results: METAL1 short.

ORCA 2CxxA (5.0 V) Series Qualification (continued)

Table 24. OR2CxxA Series (0.35 μm) (continued)

Qualification Information	Device						
	ATT2C26 388 BGA (Q95013)[11]	**ATT2C10 256 BGA (Q96068.1)**[6]	**1286B 432 EBGA (Q96284.2)**[6,11]	**1219L 240 SQFP (Q96406)**[6]	**1174J2 144 TQFP (Q96365.1)**	**OR2T15A 84 PLCC (EE97260)**	**OR2C15A 240 CSM (Q97176)**[6]
ESD—HBM[1]	>2000 V	>2000 V	>2500 V	>2000 V	>2500 V	—	>2000 V
ESD—CDM[1]	>500 V[12]	>1000 V	>1000 V	>500 V[12]	>1000 V	—	>2000 V
1000 hrs. HTOB	0/59 Pass	—	0/105 Pass	0/62 Pass	0/105 Pass	0/105 Pass	0/105 Pass
1000 hrs. THB	0/48 Pass	—	0/49 Pass	—	0/45 Pass	—	0/48 Pass
Class	0/89 Pass	0/35 Pass	0/50 Pass	—	—	—	0/80 Pass
Moisture Sensitivity Level	—	3	4	3	3	3	3
Steam Bomb	0/50 Pass	0/46 Pass	0/50 Pass	—	0/45 Pass	—	0/48 Pass
100 c/s TC or 300 c/s TC	0/45 Pass	0/47 Pass	0/50 Pass	0/48 Pass	0/46 Pass	0/48 Pass	0/48 Pass
15 c/s TS or 100 c/s TS	0/15 Pass	0/16 Pass	0/16 Pass	—	0/45 Pass	—	0/16 Pass
Moisture Resistance	0/38 Pass	—	0/38 Pass	—	—	—	—
Corrosion	0/15 Pass	—	0/15 Pass	—	—	—	—
Solvent Resistance	0/15 Pass	—	0/15 Pass	—	—	—	—
Physical Dimension	0/15 Pass	0/15 Pass	0/15 Pass	—	—	—	—
Solderability	—	—	—	—	—	—	—
Bond Strength	—	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—	—
X-Ray	0/5 Pass	—	0/5 Pass	—	—	—	—
Latch-Up	II	II	—	II	III	—	II
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qual No. T96005.1 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T96005.
3. Qual No. T97037 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. EE95210.1.
4. Qual No. T95276.2 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T95276.1.
5. Codemarking lifted off of three devices, but they passed electrically and a second THB run.
6. Qualification Information may be referenced from multiple Qualification Numbers.
7. Also passed lead integrity (0/15).
8. Also passed lead integrity (0/5).
9. FMA results: The one failure passed 300 cycles after retest.
10. FMA results: METAL1 short.
11. Ball integrity test was also passed (0/15).
12. Corner pins pass >1000 V.

ORCA 2CxxA (5.0 V) Series Qualification (continued)

Table 24. OR2CxxA Series (0.35 μm) (continued)

Qualification Information	Device			
	ATT2C40 240 PQ2 (Q95007)	**ATT7C157M 52 PLCC (Q91016.3)[7]**	**1232C 208 PQ2 (Q95204)**	**ATT2C26 304 PQ2 (Q94227.1)**
ESD—HBM[1]	>2000 V	>2000 V	>1000 V	>2000 V
ESD—CDM[1]	>1000 V	>2000 V	>1000 V	>1000 V
1000 hrs. HTOB	—	0/164 Pass	—	0/65 Pass
1000 hrs. THB	0/77 Pass	1/131[13] Pass	—	0/100 Pass
Class	0/80 Pass	1/132[14] Pass	—	0/101 Pass
Moisture Sensitivity Level	—	—	—	3
Steam Bomb	—	1/105[15] Pass	—	0/45 Pass
100 c/s TC or 300 c/s TC	0/46 Pass	0/105 Pass	—	0/50 Pass
15 c/s TS or 100 c/s TS	—	0/25 Pass	—	0/15 Pass
Moisture Resistance	—	0/38 Pass	—	—
Corrosion	—	0/15 Pass	—	0/15 Pass
Solvent Resistance	—	0/8 Pass	—	0/15 Pass
Physical Dimension	0/15 Pass	0/15 Pass	0/12 Pass	0/15 Pass
Solderability	—	0/22 Pass	—	—
Bond Strength	—	—	—	—
Die Shear Strength	—	—	—	—
X-Ray	—	0/5 Pass	—	—
Latch-Up	II	II	II	II
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qual No. T96005.1 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T96005.
3. Qual No. T97037 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. EE95210.1.
4. Qual No. T95276.2 was created to conform with package codemarking; therefore, the Qualification Information is referenced from Qual No. T95276.1.
5. Codemarking lifted off of three devices, but they passed electrically and a second THB run.
6. Qualification Information may be referenced from multiple Qualification Numbers.
7. Also passed lead integrity (0/15).
8. Also passed lead integrity (0/5).
9. FMA results: The one failure passed 300 cycles after retest.
10. FMA results: METAL1 short.
11. Ball integrity test was also passed (0/15).
12. Corner pins pass >1000 V.
13. FMA result: No defect found.
14. FMA result: Lifted ball bond.
15. FMA result: Thin oxide defect.

ORCA 2TxxA (3.3 V) Series Qualification

There are eight arrays in the *ORCA* 2TxxA Series FPGA product family: ORTC04A, OR2T06A, OR2T08A, OR2T10A, OR2T12A, OR2T15A, OR2T26A, and OR2T40A. These arrays are then assembled in a number of different packages. These packages are plastic-leaded chip carrier (PLCC), plastic-quad flat pack (QFP), thin-quad flat pack (TQFP), shrink-quad flat pack (SQFP), shrink-quad flat pack—powerquad 2 option (SQFP2), plastic-ball grid array (PBGA), and enhanced-ball grid array (EBGA).

Qualification Strategy

The qualification of *ORCA* 2TxxA Series FPGAs can be broken into three specific groups: process technology, silicon design, and package.

Process Technology: These arrays are processed using the 0.35 µm CMOS technology. Lucent Technologies' 0.35 µm CMOS process employs N- and P-channel LDD MOS transistors. The process also uses three levels of metal. This technology has been rigorously tested for reliability and manufacturability and is fully qualified.

Silicon Design: Since the eight arrays in the *ORCA* 2TxxA Series FPGAs are a matrix of repetitive elements, the Qualification Review Board (QRB) decided to qualify one die which would qualify the silicon design methodology of all eight arrays. Therefore, needed tests were performed on the OR2T40A die in the 600-pin EBGA package.

Package: The QRB determined the qualification requirements of each die in a given package. The results are given in Table 25.

ORCA 2TxxA (3.3 V) Series Qualification (continued)

Table 25. OR2TxxA Series (0.35 μm)

Qualification Information	Device							
	OR2T04A 84 PLCC (Q96298.2)	OR2T04A 100 TQFP (Q96299.2)	OR2T15A 84 PLCC (EE97260)	OR2T40A 600 EBGA (Q97048.1)	160 MQFP (MR217)[2,4]	100 TQFP (MR221)[2,3]	144 TQFP (MR225)[2,3]	208 SQFP (MR229)[2,4]
ESD—HBM[1]	>2000 V	>2000 V	—	—	—	—	—	—
ESD—CDM[1]	>1000 V	>1000 V	—	—	—	—	—	—
1000 hrs. HTOB	—	—	0/105 Pass	—	0/97 Pass	0/97 Pass	0/97 Pass	0/97 Pass
1000 hrs. THB	—	—	—	—	0/132 Pass	0/80 Pass	0/130 Pass	0/80 Pass
Class	—	—	—	—	0/132 Pass	0/133 Pass	0/132 Pass	0/85 Pass
Moisture Sensitivity Level	—	—	3	—	—	—	—	—
Steam Bomb	—	—	—	—	0/105 Pass	0/47 Pass	0/105 Pass	0/80 Pass
100 c/s TC or 300 c/s TC	—	—	0/48 Pass	—	0/105 Pass	0/47 Pass	1/105[5] Pass	0/80 Pass
15 c/s TS or 100 c/s TS	—	—	—	—	0/25 Pass	0/25 Pass	0/45 Pass	0/26 Pass
Moisture Resistance	—	—	—	—	0/37 Pass	0/38 Pass	0/38 Pass	0/37 Pass
Corrosion	—	—	—	—	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Solvent Resistance	—	—	—	—	0/8 Pass	0/8 Pass	0/8 Pass	0/8 Pass
Physical Dimension	—	—	—	—	0/15 Pass	0/15 Pass	0/15 Pass	0/15 Pass
Solderability	—	—	—	—	0/22 Pass	0/22 Pass	0/22 Pass	0/22 Pass
Bond Strength	—	—	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—	—	—
X-Ray	—	—	—	—	0/5 Pass	0/5	0/5 Pass	0/5 Pass
Latch-Up	II	III	—	—	—	—	—	—
Status	Fully Qualified	Fully Qualified	Fully Qualified	In Process	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qualification Information may be referenced from multiple Qualification Numbers.
3. Also passed lead integrity (0/15).
4. Also passed lead integrity (0/5).
5. FMA results: The one failure passed 300 cycles after retest.

ORCA 2TxxA (3.3 V) Series Qualification (continued)

Table 25. OR2TxxA Series (0.35 μm) (continued)

Qualification Information	Device						
	240 SQFP (MR232)[2,3]	208 SQFP2 (MR243)[2,3]	240 SQFP2 (MR244)[2,3]	ATT2C10 256 PBGA (Q96068.1)[2]	1159AE 160 MQFP (Q96270)	1627T 100 TQFP (Q96120)	1286B 432 EBGA (Q96284.2)[2,7]
ESD—HBM[1]	—	—	—	>2000 V	>2500 V	>2000 V	>2500 V
ESD—CDM[1]	—	—	—	>1000 V	>1000 V	>2000 V	>1000 V
1000 hrs. HTOB	0/97 Pass	0/97 Pass	0/97 Pass	—	0/60 Pass	0/105 Pass	0/60 Pass
1000 hrs. THB	1/120[6] Pass	0/100 Pass	0/100 Pass	—	—	0/135 Pass	0/49 Pass
Class	0/148 Pass	0/101 Pass	0/101 Pass	0/35 Pass	—	0/135 Pass	0/50 Pass
Moisture Sensitivity Level	—	—	—	3	3	—	4
Steam Bomb	0/48 Pass	0/45 Pass	0/45 Pass	0/46 Pass	—	0/77 Pass	0/50 Pass
100 c/s TC or 300 c/s TC	0/80 Pass	0/50 Pass	0/50 Pass	0/47 Pass	0/48 Pass	0/77 Pass	0/50 Pass
15 c/s TS or 100 c/s TS	0/16 Pass	0/15 Pass	0/15 Pass	0/16 Pass	—	0/25 Pass	0/16 Pass
Moisture Resistance	0/38 Pass	0/38 Pass	0/38 Pass	—	—	—	0/38 Pass
Corrosion	0/15 Pass	0/15 Pass	0/15 Pass	—	—	—	0/15 Pass
Solvent Resistance	0/8 Pass	0/15 Pass	0/15 Pass	—	—	—	0/15 Pass
Physical Dimension	0/15 Pass	0/12 Pass	0/15 Pass	0/15 Pass	—	—	0/15 Pass
Solderability	0/22 Pass	—	—	—	—	—	—
Bond Strength	—	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—	—
X-Ray	0/5 Pass	0/5 Pass	0/5 Pass	—	—	—	0/5 Pass
Latch-Up	—	—	—	II	III	II	—
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qualification Information may be referenced from multiple Qualification Numbers.
3. Also passed lead integrity (0/15).
4. Also passed lead integrity (0/5).
5. FMA results: The one failure passed 300 cycles after retest.
6. FMA results: METAL1 short.
7. Also passed ball integrity (0/15).

ORCA 2TxxA (3.3 V) Series Qualification (continued)

Table 25. OR2TxxA Series (0.35 μm) (continued)

Qualification Information	Device						
	ATT2C15AE 208 SQFP (T96005)	**ATT2C15AE 304 SQFP (EE95210.1)**	**ATT2C15AE 352 PBGA (T95276.1)**	**ATT2C40 240 PQ2 (Q95007)**	**ATT7C157M 52 PLCC (Q91016.3)[3]**	**1232C 208 PQ2 (Q95204)**	**1174J2 144 TQFP (Q96365.1)**
ESD—HBM[1]	>2000 V	—	—	>2000 V	>2000 V	>1000 V	>2500 V
ESD—CDM[1]	>1000 V	>1000 V	>1000 V	>1000 V	>2000 V	>1000 V	>1000 V
1000 hrs. HTOB	0/64 Pass	0/62 Pass	0/105 Pass	—	0/164 Pass	—	0/105 Pass
1000 hrs. THB	0/80 Pass	0/104 Pass	0/74 Pass	0/77 Pass	1/131[9] Pass	—	0/45 Pass
Class	0/85 Pass	0/108 Pass	3/75[8] Pass	0/80 Pass	1/132[10] Pass	—	—
Moisture Sensitivity Level	—	3	4	—	—	—	3
Steam Bomb	0/80 Pass	0/105 Pass	0/80 Pass	—	1/105[11] Pass	—	0/45 Pass
100 c/s TC or 300 c/s TC	0/80 Pass	0/50 Pass	0/80 Pass	0/46 Pass	0/105 Pass	—	0/46 Pass
15 c/s TS or 100 c/s TS	0/26 Pass	0/25 Pass	0/26 Pass	—	0/25 Pass	—	0/45 Pass
Moisture Resistance	—	—	—	—	0/38 Pass	—	—
Corrosion	—	—	—	—	0/15 Pass	—	—
Solvent Resistance	—	—	—	—	0/8 Pass	—	—
Physical Dimension	—	—	0/15 Pass	0/15 Pass	0/15 Pass	0/12 Pass	—
Solderability	—	—	—	—	0/22 Pass	—	—
Bond Strength	—	—	—	—	—	—	—
Die Shear Strength	—	—	—	—	—	—	—
X-Ray	0/5 Pass	0/5 Pass	0/5 Pass	—	0/5 Pass	—	—
Latch-Up	II	—	—	II	II	II	III
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qualification Information may be referenced from multiple Qualification Numbers.
3. Also passed lead integrity (0/15).
4. Also passed lead integrity (0/5).
5. FMA results: The one failure passed 300 cycles after retest.
6. FMA results: METAL1 short.
7. Also passed ball integrity (0/15).
8. Code marking lifted off of three devices, but they passed electrically and a second THB run.
9. FMA result: No defect found.
10. FMA result: Lifted ball bond.
11. FMA result: Thin oxide defect.

ORCA 2TxxA (3.3 V) Series Qualification (continued)

Table 25. OR2TxxA Series (0.35 μm) (continued)

Qualification Information	Device				
	1242AM 208 SQFP (Q97053.1)[2]	**1218H 128 SQFP (Q97193)**	**TMPR28051 208 SQFP (Q97102.1)**	**1235C 304 SQFP2 (Q96380)**	**1292B 272 PBGA (Q97100)[2]**
ESD—HBM[1]	>2000 V	>2500 V	>2000 V	>2000 V	>2000 V
ESD—CDM[1]	>500 V[12]	>2000 V	>1000 V	>500 V[12]	>1000 V
1000 hrs. HTOB	0/105 Pass	0/105 Pass	—	—	1/189[14] Pass
1000 hrs. THB	—	0/48 Pass	—	—	0/74 Pass
Class	—	0/48 Pass	—	—	—
Moisture Sensitivity Level	3	3	3[13]	3	4
Steam Bomb	—	0/48 Pass	—	—	0/80 Pass
100 c/s TC or 300 c/s TC	0/48 Pass	0/48 Pass	1/79[13] Pass	0/48 Pass	0/48 Pass
15 c/s TS or 100 c/s TS	—	0/48 Pass	—	—	0/26 Pass
Moisture Resistance	—	—	—	—	—
Corrosion	—	—	—	—	—
Solvent Resistance	—	—	—	—	—
Physical Dimension	—	—	—	—	0/15 Pass
Solderability	—	—	—	—	—
Bond Strength	—	—	—	—	—
Die Shear Strength	—	—	—	—	—
X-Ray	—	—	—	—	—
Latch-Up	III	II	III	III	III
Status	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model.
2. Qualification Information may be referenced from multiple Qualification Numbers.
3. Also passed lead integrity (0/15).
4. Also passed lead integrity (0/5).
5. FMA results: The one failure passed 300 cycles after retest.
6. FMA results: METAL1 short.
7. Also passed ball integrity (0/15).
8. Code marking lifted off of three devices, but they passed electrically and a second THB run.
9. FMA result: No defect found.
10. FMA result: Lifted ball bond.
11. FMA result: Thin oxide defect.
12. All corner pins passed 1000 V.
13. Lifted ball bonds/sheared ball bonds.
14. FMA unable to duplicate 3-state leakage occurrence.

ATT1700A Series Qualification

The ATT1700A Series of EEPROMs are assembled in three different packages. These packages are plastic-leaded chip carrier (PLCC), plastic dual-in-line package (DIP), and small-outline narrow body (SONB).

Qualification Strategy

The qualification of the ATT1700A Series EEPROMs was done by performing a full set of tests on the device in each package, with one exception: the HTOB and Bake device tests were only performed on the 8-pin DIP.

Table 26. ATT1700A Series EEPROMs (1.2 μm)

Qualification Information	Device		
	ATT1700A-8DIP (Q94362)	**ATT1700A-8SONB (Q94363)**	**ATT1700A-20PLCC (Q94364)**
ESD—HBM[1]	>2000 V	>2000 V	>2000 V
ESD—CDM[1]	>2000 V	>2000 V	>2000 V
1000 hrs. HTOB	6/768 Pass[2]	—	—
1000 hrs. THB	2/3564 Pass[3]	0/2865 Pass	5/2443 Pass[4]
150 °C Bake	0/899 Pass	—	—
Steam Bomb	0/46 Pass	0/46 Pass	0/3322 Pass
100 c/s TC or 300 c/s TC	0/644 Pass	0/1012 Pass	1/907 Pass[5]
15 c/s TS or 100 c/s TS	0/46 Pass	0/46 Pass	6/878 Pass[6]
Moisture Resistance	0/46 Pass	0/46 Pass	0/46 Pass
Corrosion	0/15 Pass	0/15 Pass	0/15 Pass
Solvent Resistance	0/15 Pass	0/15 Pass	0/15 Pass
Physical Dimension	0/2 Pass	0/2 Pass	0/2 Pass
Solderability	0/22 Pass	0/22 Pass	0/22 Pass
Lead Integrity	0/15 Pass	0/15 Pass	0/15 Pass
HAST	0/122 Pass	0/122 Pass	0/281 Pass
Latch-Up	II	II	II
Status	Fully Qualified	Fully Qualified	Fully Qualified

1. HBM = human-body model, and CDM = charged-device model; see page 13 for test descriptions.
2. Bad column in EEPROM array.
3. I_{DD} standby.
4. Three failed from single bit charge loss, one from leakage, one from extended V_{DD} range.
5. Double row failure.
6. Single/multiple bit charge loss.

Notes

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