# SEMiX®

## IGBT Modules & Bridge Rectifier Family

Technical Explanations

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## Content

# 1 Introduction

SEMiX was introduced as part of SEMIKRON's new line of IGBT modules at PCIM 2003. SEMiX modules are now available as a complete module family featuring different housing sizes and adapted bridge rectifiers (Fig. 1-1). Thanks to its features, this product line has become a standard for new developments.

## 1.1 Features

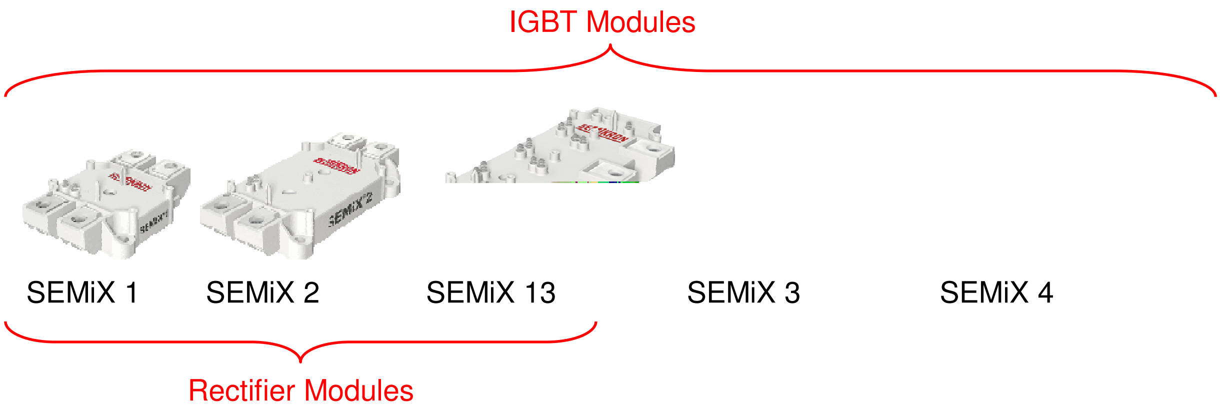



Fig. 1-1 SEMiX family concept: IGBT modules and matching input rectifiers

The low-profile housing design of SEMiX modules offers several advantageous features:

- Solder-free mounting for the driver with no additional wiring or connectors (Fig. 1-2)
- Spring contacts for the auxiliary contacts
- Family concept, meaning a similar package design for both input rectifiers and IGBT modules
- Complete product line from $I_{C,\,max}$ = 100 A to 900 A in 600 V, 1200 V and 1700 V
- Separate AC, DC terminals and control unit
- 17-mm-high main terminals

Fig. 1-2 SEMiX housing size 3 with SKYPER driver core and adapter board

## 1.2 Advantages and Benefits

The above-mentioned features allow for a compact, flat and low-inductance inverter design (see Fig. 1-3 and Fig. 1-4). The DC-link connections can be short and very low inductive, resulting in reduced voltage overshoots. In the case of paralleled IGBT modules, even and balanced current sharing can be achieved.
Thanks to the directly mounted driver (see Fig. 1-2) optimum IGBT control can be achieved and noise on gate wires or loose connectors can be ruled out.

With SEMiX modules, the entire inverter design can be simplified. Furthermore, the assembly processes involved in inverter production for the units are less complex (e.g. no manual or additional wave soldering). As a result, quality is boosted, while the overall system costs decrease.

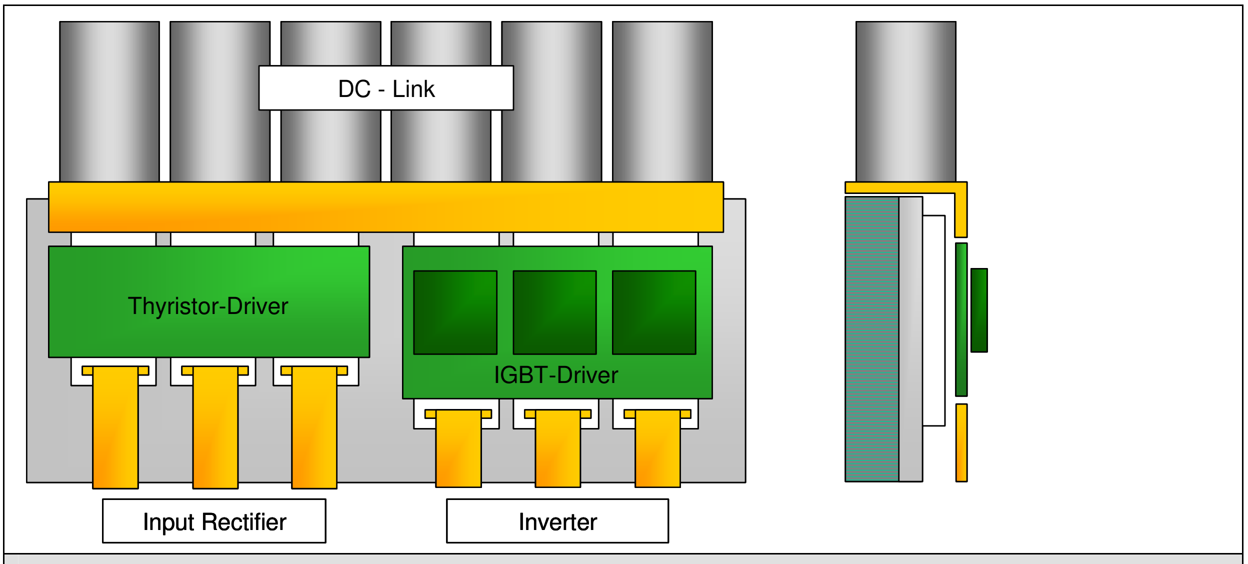



Fig. 1-3 Possible inverter design with SEMiX for input rectifier and inverter (conceptual study)

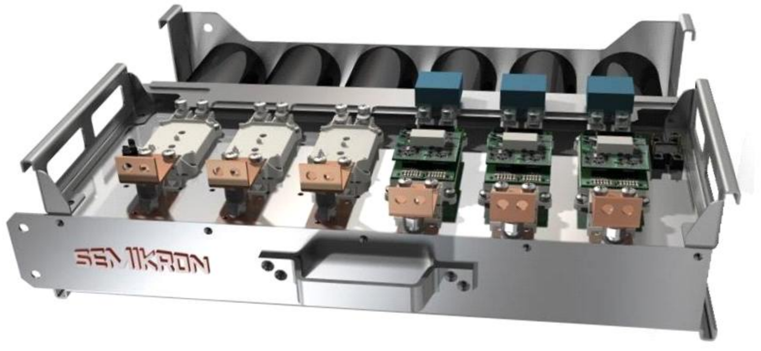



Fig. 1-4 Possible inverter design with SEMiX for input rectifier and inverter (conceptual study)

# 2 Technical Details of SEMiX

The SEMiX range is available in two product lines: one IGBT module line and one rectifier module line. The whole module family is based on the same design principles, a fact that also boasts advantages in terms of quality and production logistics at SEMIKRON.

## 2.1 Mechanical Design

One of the basic principles behind SEMiX is the platform principle: with a few basic parts (Fig. 2-1) a variety of modules can be produced. All SEMiX IGBT modules use the same substrates, main terminals, springs etc. The only parts that are different are the base plates and the plastic housings (Fig. 2-3).

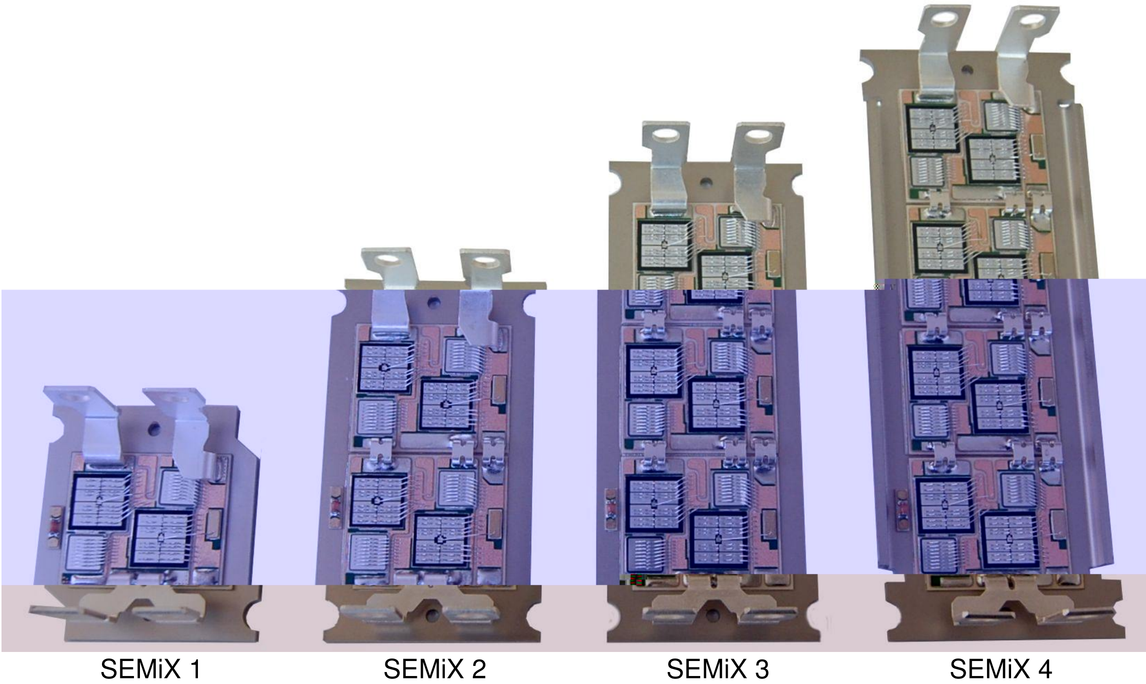



Fig. 2-3 SEMiX platform principle: housing sizes 2, 3 and 4 based on the same basic parts

## 2.2 Housing Sizes and Available Topologies

**SEMiX 1**

84 x 62 x 17 mm³

## 2.3 The “GND” Contact Spring

All SEMiX modules contain a ground “GND” contact spring. This spring is connected to the base plate of the module, as shown in Fig. 2-4. This means that it is usually on the same electrical potential as the heat sink (in most cases ground).
This connection is useful for bypassing the displacement currents which occur from the potential shift across the parasitic coupling capacitor formed by the DBC substrate between chip and heat sink.

Since the spring contacts are limited in their current capabilities, the “GND” spring must not be part of any protection circuit.

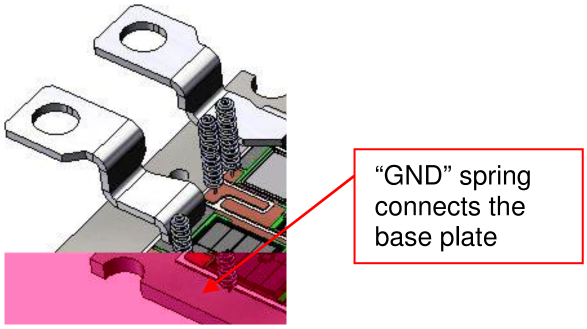



Fig. 2-4 SEMiX detail with “GND” spring contact (3D CAD sketch)

## 2.4 Different Spring Heights

SEMiX springs appear as if they have different lengths, where in fact they are all identical in length. What makes them appear different in length is the fact that their landing points are on three different levels, meaning that they protrude out of the plastic housing differently.
When the springs are designed the different heights are taken into regard. This means that a guarantee is provided that even with the lowest spring sufficient spring force is reached, so that the contacts achieve long-term reliability.
The minimum spring height is 18 mm over the heat sink - after mounting the module (please refer to the data sheet drawings for details).

The 3D CAD sketch in Fig. 2-5 shows the different possibilities:

- The “GND” spring lands on the base plate and appears to be the shortest spring.
- The gate springs G21, G22, G23 and G24 land on additional DCB substrates on top of the standard substrates, which is why these springs appear to be the longest ones.
- All other springs land on the substrates and appear to be of a similar height.

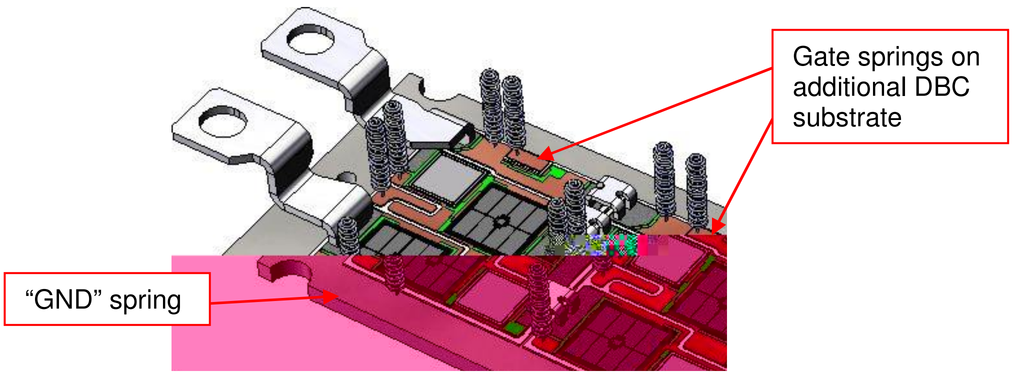



Fig. 2-5 SEMiX detail with spring contacts on different landing points (3D CAD sketch)

## 2.5 Creepage and Clearance Distances

All SEMiX IGBT and rectifier modules comply with the required creepage and clearance distances in accordance with EN 50178 for

- Nominal voltage = 1700 V (DC-link voltage = 1400 V)
- Basic isolation
- Pollution degree 2
- Comparative Tracking Index "CTI" value of the case = 175

The following values are complied with:

| | |
|---|---|
| Creepage distance on top of the housing from terminal to terminal | ≥ 14.0 mm |
| Clearance distance on top of the housing from terminal to terminal | ≥ 4.4 mm |
| Creepage distance from any terminal to heat sink potential | ≥ 14.0 mm |
| Clearance distance from any terminal to heat sink potential (screw head) | ≥ 5.5 mm |
| Creepage distance on the PCB from landing pad to landing pad | ≥ 7.1 mm |

Tab. 2-2 Creepage and clearance distances for SEMiX

"From terminal to terminal" means for main and auxiliary terminals between high-voltage potentials, not between terminals on same voltage potential, e.g. gate and emitter contacts (± 20 V) or contacts for the temperature sensor contacts.

Inside its housing, SEMiX is filled with a silicone gel for electrical isolation. The gel has an isolation capability of > 20 kV/mm.

## 2.6 Isolation Measurement

As stated in the data sheets, all SEMiX modules are specified for an isolation voltage $V_{isol}$ = 4 kV, AC sinus 50 Hz for 1 minute. In the course of production, this isolation voltage is guaranteed with a 100% measurement. The measurement is done with $V_{measurement}$ = 4.8 kV DC for 3 seconds. This value is in accordance with the DIN EN 50178 standard (VDE 0160).

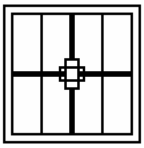
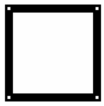
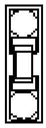
The measurement is performed in two steps:
During the first measurement all main and auxiliary terminals (including main, auxiliary emitter, gate and temperature sensor contacts) are short circuited and measured against the base plate.
In the second measurement stage the main and auxiliary terminals (including main, auxiliary emitter, gate contacts) are short circuited, as are the base plate and the temperature sensor contacts. The voltage $V_{measurement}$ is then applied between these two circuits.

## 2.7 Chip Locations

For detailed temperature measurements the exact positions of the chips have to be known. Inside SEMiX the chips are always located in the same positions, regardless of the chip size. The drawings Fig. 2-9 to Fig. 2-18 show the chip positions measured from the centre of the bottom left screw hole.

### 2.7.1 IGBT Modules

|  |  |  |
|---|---|---|
| Fig. 2-6 IGBT Chip | Fig. 2-7 CAL Diode Chip | Fig. 2-8 Temperature Sensor |

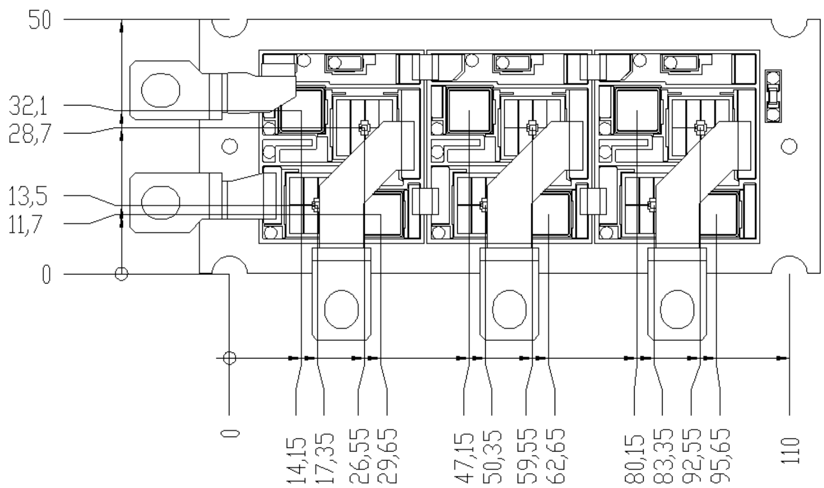



Fig. 2-9 Chip positions in SEMiX 13

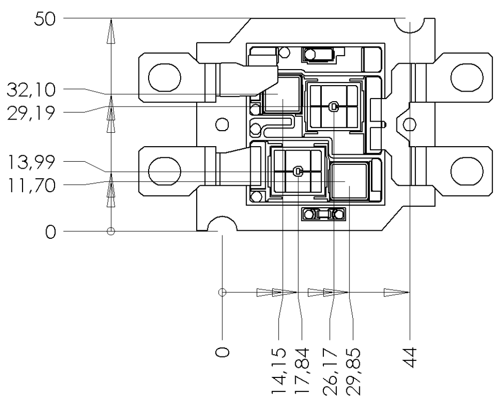



Fig. 2-10 Chip positions in SEMiX 1

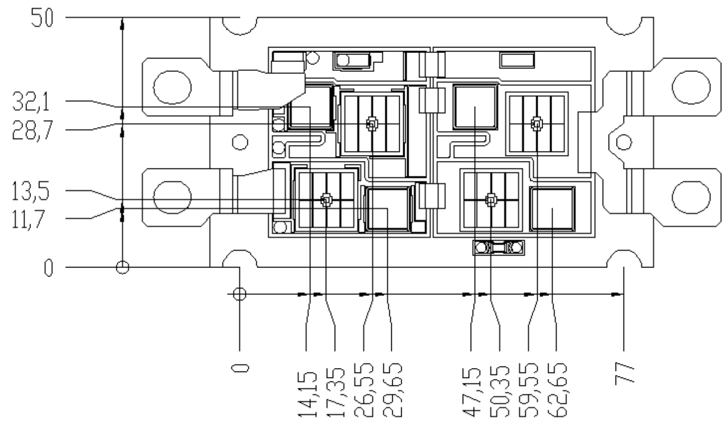



Fig. 2-11 Chip positions in SEMiX 2

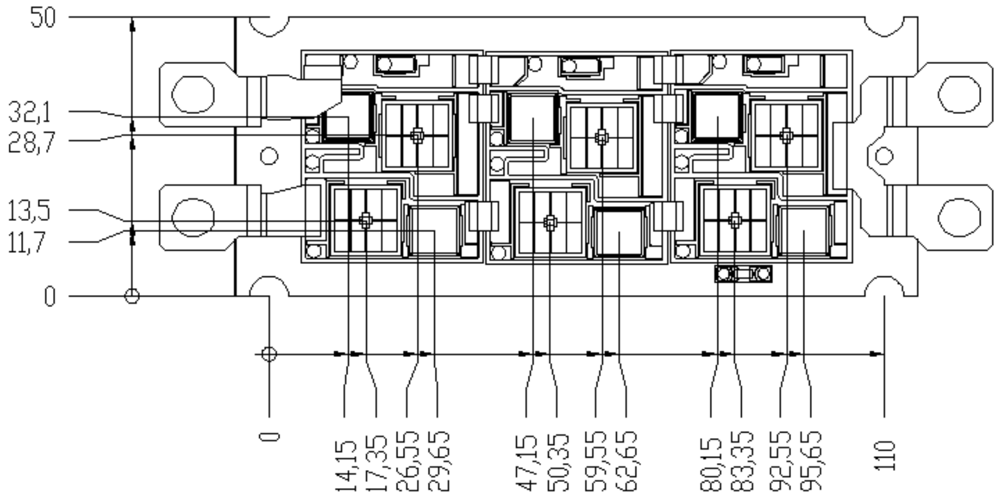



Fig. 2-12 Chip positions in SEMiX 3 (Also applicable to SEMiX 33c)

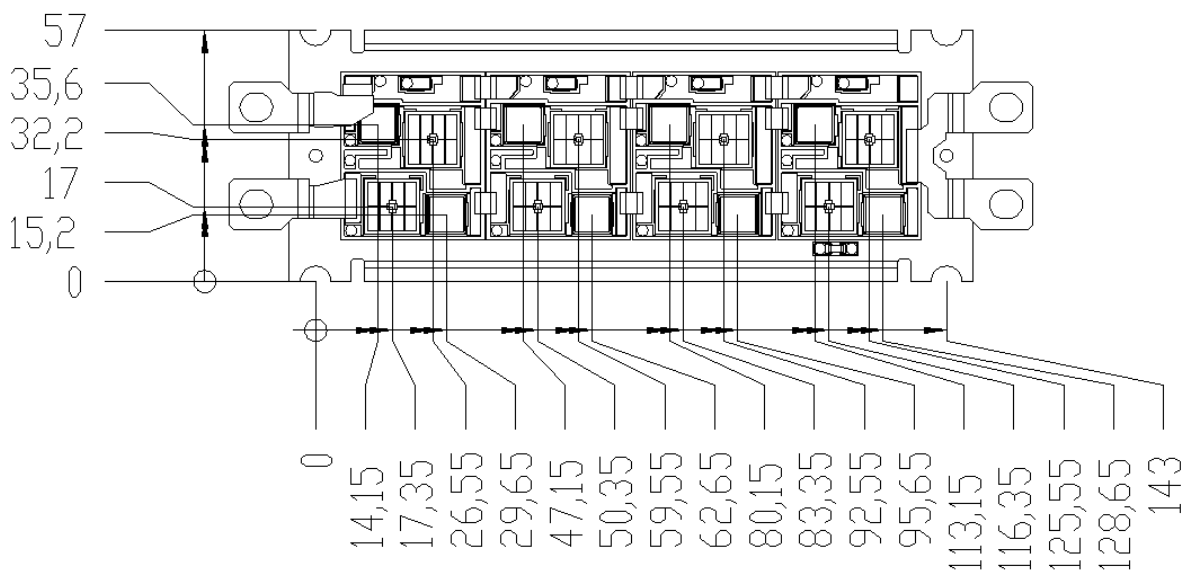



Fig. 2-13 Chip positions in SEMiX 4

### 2.7.2 Rectifier Modules

Rectifier modules are available as “KD”, “KH” and “KT” modules. The chip positions are always the same; only the type of chip (thyristor or diode) changes accordingly. Since the “KD” and “KT” modules include two diodes or two thyristors, Fig. 2-16 to Fig. 2-18 show the position of the thyristors and diodes in the half controlled KH rectifier modules.

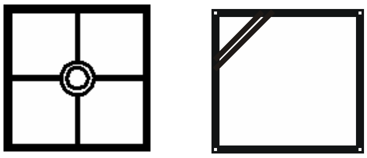


Fig. 2-14 Thyristor Chips

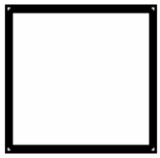


Fig. 2-15 Rectifier Diode Chip

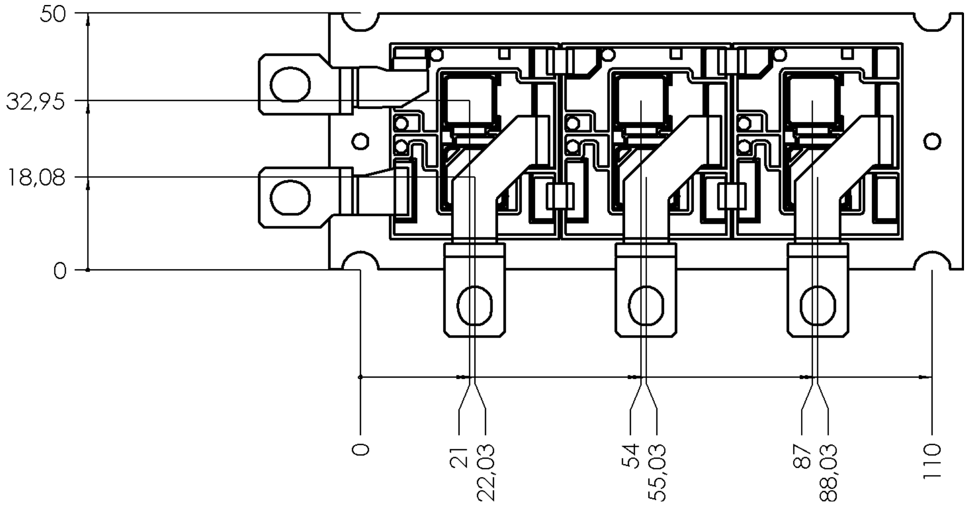



Fig. 2-16 Chip positions in SEMiX 13 “DH”

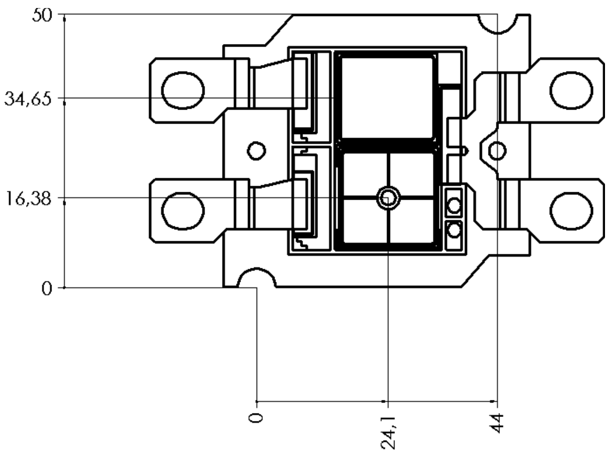



Fig. 2-17 Chip positions in SEMiX 1 “KH”

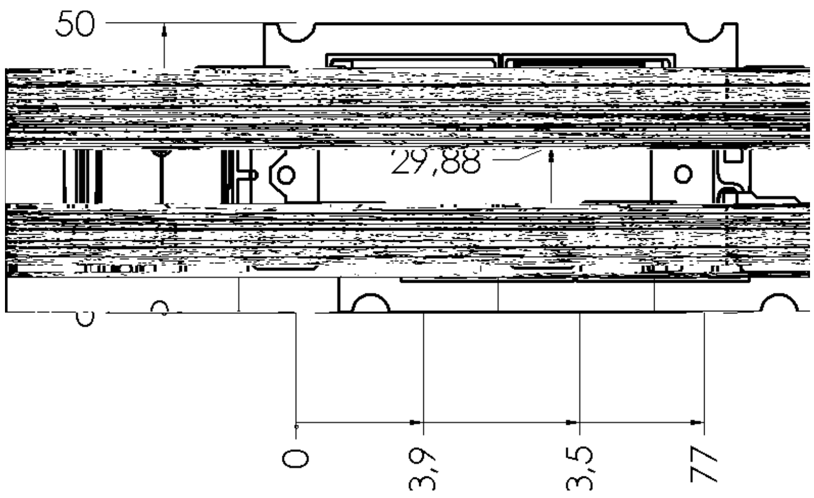



Fig. 2-18 Chip positions in SEMiX 2 “KH”

## 2.8 Thermal Material Data

For thermal simulations it is necessary to have the thermal material parameters as well as the typical thickness of the different layers in the package. In Tab. 2-3 this data is given. For better understanding, the sketch in Fig. 2-19 shows the different layers of the package.

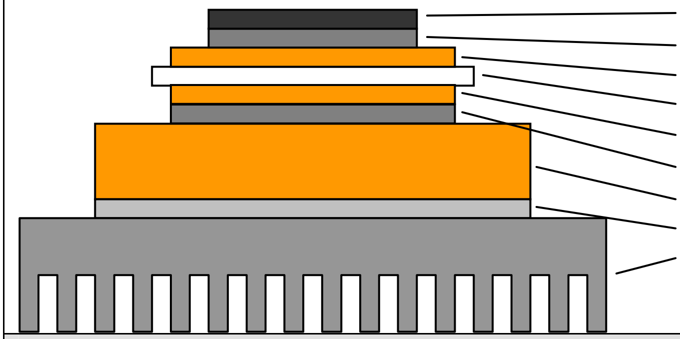



Fig. 2-19 Sketch of SEMiX package (cross sectional view)

| Layer | Material | Layer thickness [mm] | Spec. thermal conductivity [W/m/K] | Spec. thermal capacity [kJ/m³/K] | Density [g/cm³] |
|---|---|---|---|---|---|
| IGBT chip ("066") | Si | 0.07 | 106 | 1650 | 2.33 |
| IGBT chip ("126") | Si | 0.14 | 106 | 1650 | 2.33 |
| IGBT chip ("128") | Si | 0.13 | 106 | 1650 | 2.33 |
| IGBT chip ("12T4") | Si | 0.12 | 106 | 1650 | 2.33 |
| IGBT chip ("176") | Si | 0.19 | 106 | 1650 | 2.33 |
| Diode chip | Si | 0.24 | 106 | 1650 | 2.33 |
| Chip solder | SnAg alloy | ~ 0.07 | 83 | 1670 | 7.40 |
| DBC copper | Cu | 0.30 | 394 | 3400 | 8.96 |
| DBC ceramic | $Al_2O_3$ | 0.38 | 24 | 3024 | 3.78 |
| DBC copper | Cu | 0.30 | 394 | 3400 | 8.96 |
| Base plate solder | SnAgCu alloy | ~ 0.07 | 60 | 1670 | 7.40 |
| Base plate | Cu | 3 | 394 | 3400 | 8.96 |
| Thermal paste | Customer specific | | | | |
| Heat sink | Customer specific | | | | |

Tab. 2-3 Material data for thermal simulations

# 3 Chip Technologies and Product Ranges

## 3.1 IGBT Chip Technologies: Product Range

SEMiX IGBT modules are available with 600 V, 1200 V and 1700 V IGBTs. Two different IGBT technologies are in use: Field-Stop Trench-Gate IGBTs and Soft Punch Through Planar-Gate IGBTs.

### Design Principles

IGBT chips are based on two different main design principles. The first is related to the gate structure: trench or planar gate, while the second relates to the IGBT technology used: punch through ("PT") or non-punch through ("NPT").

The planar gate is a cost-effective structure based on doping processes and produces a horizontal gate structure (Fig. 3-3). The sophisticated trench gate, in comparison, is based on a combination of doping, etching and filling processes. The trench process leads to a very efficient, vertical gate structure and allows for small chip sizes (Fig. 3-4), which in turn allow for compact module design. But still, the smaller chip sizes lead to higher thermal resistance at the same time.

The term "Punch-Through" describes the behaviour of the electric field inside the IGBT during blocking state. As shown in Fig. 3-1, the electric filed punches through the $n^-$ layer into the $n^+$ layer. Inside the $n^+$ layer the field is steeper than in the $n^-$ layer. Thanks to this, the PT-IGBT can be thinner than an NPT-IGBT (Fig. 3-2) and the overall losses are lower.
In the past PT-IGBTs were made with what is called "epitaxial" material and had a negative temperature coefficient for the forward voltage drop $V_{CE(sat)}$, making paralleling very difficult. State-of-the-art "Soft-Punch Through" and "Field Stop" PT-IGBTs, however, have a positive temperature coefficient and allow for parallel use.

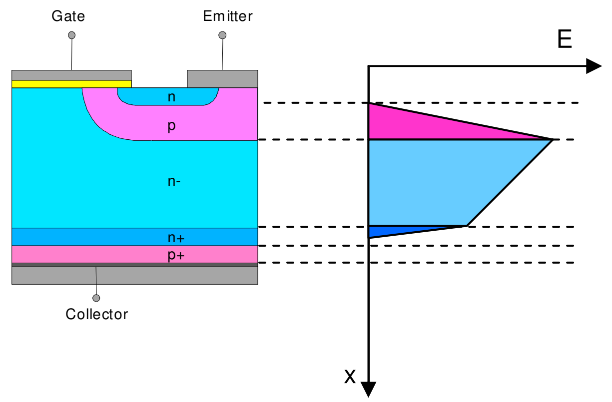



Fig. 3-1 Punch-Through IGBT (with planar gate)

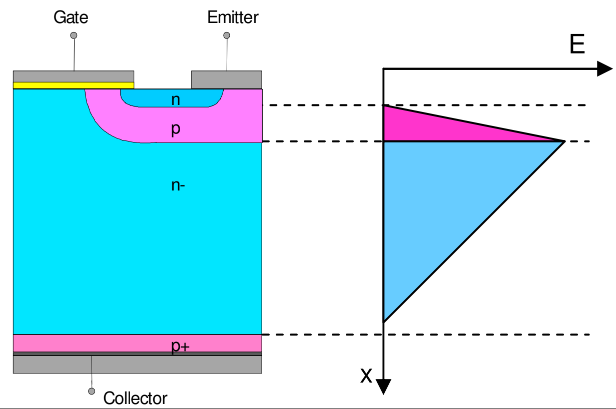



Fig. 3-2 Non-Punch Through IGBT (with planar gate)

### SPT-IGBT

SEMIKRON type designation: "128" for 1200 V SPT and "S2" for 1200 V $SPT^+$.

The Soft-Punch-Through (SPT) IGBT chip design is based on a planar-gate structure combined with a "Soft-Punch-Through" $n^+$ buffer layer (Fig. 3-3). In the majority of applications it provides important benefits compared to other technologies, i.e. lower switching losses, low thermal resistance and a positive temperature coefficient. SEMIKRON has successfully introduced this type of chip and has been using it in its standard IGBT module range since 2003.

### Trench-IGBT

SEMIKRON type designation: "066" for 600 V, "126" for 1200 V, "176" for 1700 V $3^{rd}$-generation "IGBT3", and "12T4" for the 1200 V $4^{th}$-generation "IGBT4".

The "Trench IGBT" chip design is based on a trench-gate structure combined with a "Field Stop" $n^+$ buffer layer for punch through feature, as shown in Fig. 3-4. With the introduction of the $4^{th}$ generation, this general design was not changed, but the trade-off between the on-state losses $V_{CE(sat)}$ and the switching losses $E_{on}+E_{off}$ was optimised for operation with switching frequencies above 4 kHz. Furthermore, the “IGBT4” is able to operate with a maximum junction temperature $T_{j,max}$ = 175 °C. The increased $T_{j,max}$ offers more flexibility in overload conditions or for applications with few temperature cycles (e.g. pumps or fans) where the junction temperature might now exceed the former limits.

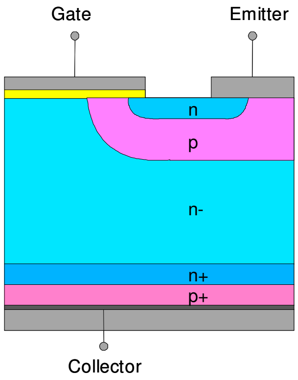



Fig. 3-3 IGBT with planar gate and “Soft Punch Through” technology

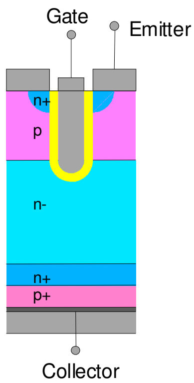



Fig. 3-4 IGBT with trench gate and “Field Stop” technology

For further information on “IGBT4” please refer to:
- R. Annacker, R. Herzer, “*IGBT4 Technology Improves Application Performance*”, Bodo´s Power Systems, Issue June 2007
- A. Wintrich, “*IGBT4 and Freewheeling Diode CAL4 in IGBT Modules*”, SEMIKRON Application Note 7005, 2008

## Inverse and Freewheeling Diodes

The free-wheeling diodes used in SEMiX IGBT modules are specially optimized CAL (**C**ontrolled **A**xial **L**ifetime) diodes, or HD CAL (**H**igh **D**ensity CAL) diodes. These fast, "super soft" planar diodes are characterised by the optimal axial profile of the charge carrier life-time, which was achieved in an implantation process using helium ions and a basic carrier life-time setting.
This leads to:
- Low peak reverse current and thus a lower inrush load on the IGBTs in bridge circuits.
- "Soft" decrease of the reverse current throughout the entire operating temperature range, which minimizes switching surges and interference.
- Robust performance when switching high di/dt.
- Paralleling capability thanks to the negligible negative temperature coefficient and the small forward voltage $V_F$ spread.

Compared with CAL diodes, HD CAL diodes display reduced forward voltages at negligible higher switching losses and an almost indifferent forward voltage temperature coefficient.

SEMIKRON’s newly developed “CAL4” diode is designed specifically for use with the “IGBT4”. This new device boasts low thermal losses and outstanding soft switching behaviour even at extreme commutation speeds. Further, the newly developed junction termination ensures safe operation up to 175 °C.

For further information on CAL4 please refer to:
- V. Demuth et al., “*CAL 4: The Next-Generation 1200V Freewheeling Diode*”, Proceedings PCIM China, 2007

### Comparison

The following table provides a brief overview of the chip technologies described before and the available current ranges in SEMiX modules. For details on type designations, electrical values etc. please refer to the SEMIKRON homepage or catalogues.

| Parameter | | SEMiX IGBT | | | | |
|---|---|---|---|---|---|---|
| | | **“066”** | **“126”** | **“128”** | **“12T4”** | **“176”** |
| IGBT Technology | | Trench | Trench | SPT | Trench | Trench |
| $V_{CES}$ | [V] | 600 | 1200 | 1200 | 1200 | 1700 |
| From $I_{C.\,max,}$ $T_C$ = 25 °C ($I_{C,nom}$) | [A] | 130 (100) | 130 (75) | 150 (75) | 310 (75) | 260 (150) |
| To $I_{C.\,max,,}$ $T_C$ = 25 °C ($I_{C,nom}$) | [A] | 800 (600) | 910 (600) | 750 (400) | 910 (600) | 830 (600) |
| $V_{CE,sat}$, $T_j$ = 25 °C | [V] | 1,45 | 1,7 | 1,9 | 1,8 | 2,0 |
| $E_{on}$ + $E_{off}$ $T_j$ = 125 °C / 100 A | [mJ] | 7 | 25 | 22 | 20 | 100 |
| $Q_{Gate}$ $V_{GE}$ = -8 …+15 V | [µC] | 0,8 | 0,9 | 1,2 | 0,57 | 0,93 |
| $T_{j,max}$ | [°C] | 150 | 150 | 150 | 175 | 150 |
| 100 A chip size | [mm²] | 54 | 109 | 158 | 96 | 128 |

Tab. 3-1 Comparison of IGBT chip parameters

## 3.2 Safe Operating Area for IGBTs

Safe Operating Areas are not included in the datasheets. They are given as standardized figures. These figures apply to 600 V, 1200 V and 1700 V.

### Safe Operating Area

IGBT modules must not be used in linear mode.

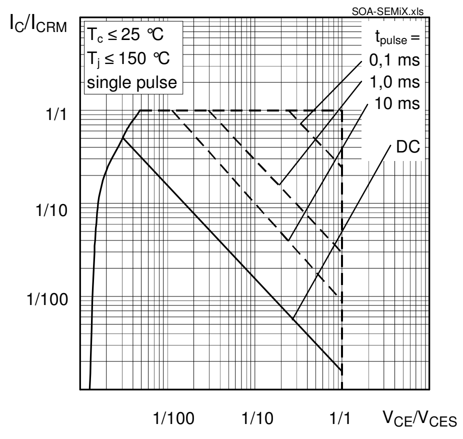



Fig. 3-5 Safe Operating Area (SOA)

## Reverse Bias Safe Operating Area

The maximum $V_{CES}$ value must never be exceeded. Due to the internal stray inductance of the module, a small voltage will be induced during switching. The maximum voltage at the terminals $V_{CE\,max,\,T}$ must therefore be smaller than $V_{CE\,max}$ (see dotted line in Fig. 3-6). This value can be calculated using the formula (3-1) given below. The value for $t_f(I_C)$ can be taken from figure 7 of the data sheets.

$$V_{CEmax,T} = V_{CES} - L_{CE} \times \left[ \frac{I_C \times 0.8}{t_f(I_C)} \right] \qquad (3\text{-}1)$$

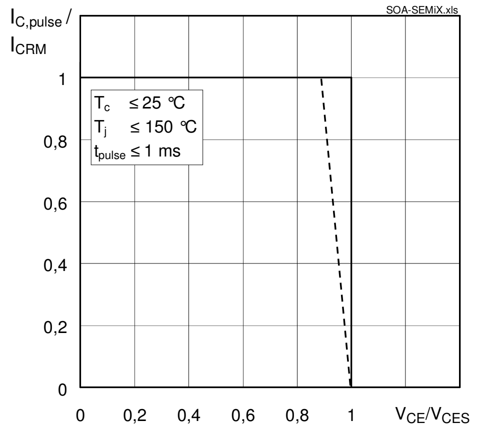



Fig. 3-6 Reverse Bias Safe Operating Area (RBSOA)

## Short Circuit Safe Operating Area

The number of short circuits must not exceed 1000. The time between short circuits must be > 1 s. The duration time of the short circuit pulse $t_{psc}$ is limited. Please refer to the maximum values for $t_{psc}$ given in the data sheet.

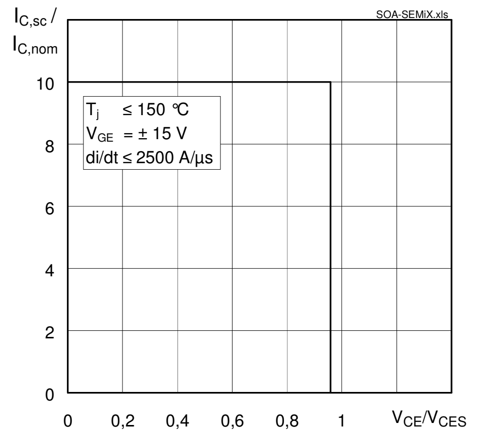



Fig. 3-7 Short Circuit Safe Operating Area (SCSOA)

## 3.3 Surge Current Characteristics of CAL Diodes

When the CAL diode operates as a rectifier diode in an “IV-Q” application, it is necessary to know the ratio of the permissible overload on-state current $I_{F(OV)}$ to the surge on-state current $I_{FSM}$ as a function of the load period t and the ratio of $V_R$ / $V_{RRM}$. $V_R$ denotes the reverse voltage applied between the sinusoidal half waves. $V_{RRM}$ is the peak reverse voltage.

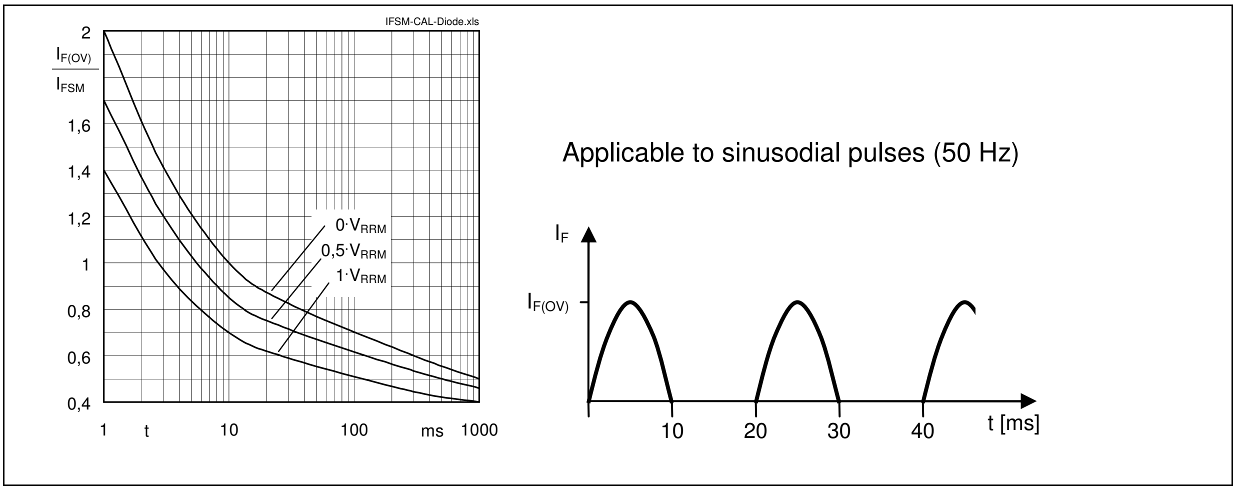



Fig. 3-8 Surge overload current vs. time

## 3.4 Rectifier Modules: Product Range

SEMiX rectifier modules are based on the same chip technology as the proven SEMIPACK product line by SEMIKRON. SEMiX rectifiers are available as controlled, half controlled and uncontrolled circuits (refer also to Tab. 2-1). For details on type designations, electrical values etc. please refer to the SEMIKRON homepage or catalogues.

The internal concept behind the rectifiers varies slightly from that of the IGBT modules, as demonstrated in chapter 2.1. Inside the rectifier modules, chips are not paralleled. SEMiX 1 contains one substrate with 2 chips (“top” and “bottom”), while SEMiX 2 contains two substrates with one chip for “top” and “bottom” each. The strongest rectifier is integrated into a SEMiX 2 case with $I_{FAV}$ = 300 A ($T_C$ = 85 °C). A stronger SEMiX rectifier module, e.g. in a SEMiX 3 case, is technically not feasible, since rectifier chips should not be paralleled due to their negative temperature coefficient.

For higher currents, the use of SEMIPACK rectifier modules is recommended.

## 3.5 Selection Guide

Selecting the right IGBT modules depends very much on the application itself. A lot of different parameters and conditions have to be taken into account: $V_{in}$, $I_{in}$, $V_{out}$, $I_{out}$, $f_{switch}$, $f_{out}$, overload, load cycles, cooling conditions, etc. Given this huge variety of parameters, providing a simplified selection guide is hardly feasible.

For this reason SEMIKRON’s SEMISEL calculation and simulation tool (http://semisel.semikron.com) can be used to make the right choices for specific applications. With SEMISEL virtually any design parameter can be modified for various input or output conditions, and different cooling conditions can be chosen and specific design needs determined effectively.

# 4 Thermal Resista[redacted]ces

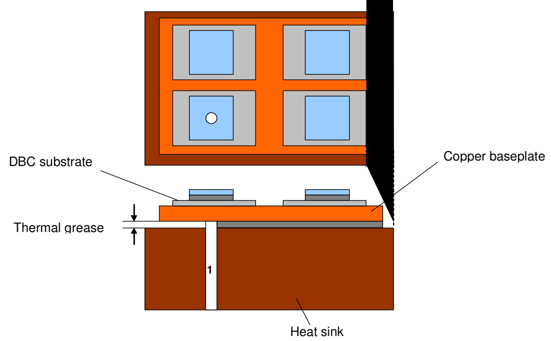
## 4.1 Measuring Therm[redacted]l Resistance $R_{th(j-c)}$ and $R_{th(c-s)}$

The thermal resistance is define[redacted]as given in the following equation (4-1)

$$R_{th(1-2)} = \frac{\Delta T}{P_V} = \frac{T_1 - T_2}{P_V}$$ ([redacted]-1)

The data sheet values for the th[redacted]rmal resistances are based on measured values. As can be seen in equation (4-1), the temperature [redacted]fference ΔT has a major influence on the $R_{th}$ value. As a result, the reference points and the measu[redacted]ment methods will have a major influence, too.
SEMIKRON measures the $R_{th(j-c}$[redacted]nd $R_{th(c-s)}$ in SEMiX modules using method A shown in Fig. 4-1. This means the reference points are [redacted] follows:

- For $R_{th(j-c)}$ they are the junct[redacted]n of the chip ($T_j$) and the bottom side of the module ($T_c$), measured directly beneath the chip via[redacted]drill hole in the heat sink. Reference point 1 in Fig. 4-1.
- For $R_{th(c-s)}$ once again the bo[redacted]om side of the module ($T_c$), measured as described above. The heat sink temperature $T_s$ is mea[redacted]ured on the top of the heat sink surface as close to the chip as possible. See reference poin[redacted]2 in Fig. 4-1.



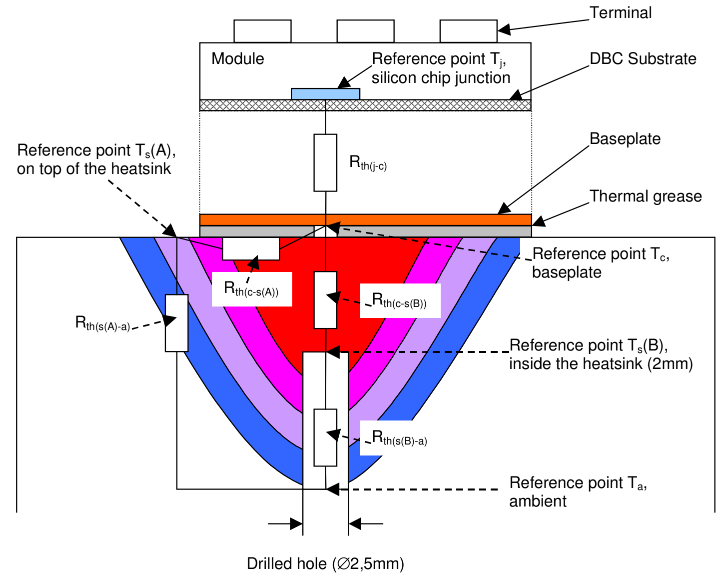



Fig. 4-3 Thermal distribution and positions of different reference points for $T_j$, $T_c$, $T_s$ and $T_a$ for the methods A and B

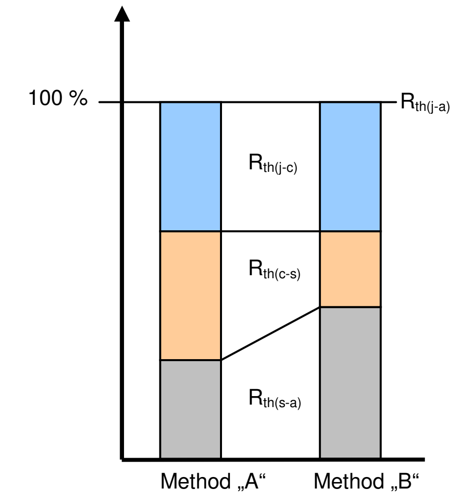



Fig. 4-4 Comparison of the resulting $R_{th}$ values for the different methods

For further information on the measurement of thermal resistances please refer to:

- M. Freyberg, U. Scheuermann, "*Measuring Thermal Resistance of Power Modules*"; PCIM Europe, May, 2003

## 4.2 Transient Thermal Impedance

When switching on a "cold" module, the thermal resistance $R_{th}$ appears smaller than the static value as given in the data sheets. This phenomenon occurs due to the internal thermal capacities of the package (refer also to Fig. 2-19). These thermal capacities are "uncharged" and will be charged with the heating energy resulting from the losses during operation. In the course of this charging process the $R_{th}$ value seems to increase. During this time it is therefore called transient thermal impedance $Z_{th}$. When all thermal capacities are charged and the heating energy has to be emitted to the ambience, the transient thermal resistance $Z_{th}$ will has reached static data sheet value $R_{th}$.
The advantage of this behaviour is the short-term overload capability of the power module.

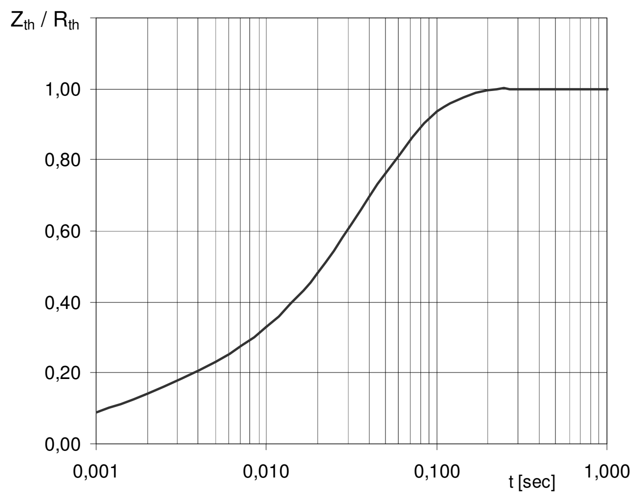



Fig. 4-5 Transient Thermal Impedance

During SEMIKRON's module approval process the transient thermal behaviour is measured. On the basis of this measurement mathematical model is derived, resulting in the following equation (4-2):

$$Z_{th}(t) = R_1\left(1 - e^{-\frac{t}{\tau_1}}\right) + R_2\left(1 - e^{-\frac{t}{\tau_2}}\right) \quad (4\text{-}2)$$

For SEMiX modules, the coefficients $R_1$, $\tau_1$, and $R_2$, $\tau_2$ can be determined using the data sheet values as given in Tab. 4-1.

| | | **IGBT, CAL diode** | **Thyristor, rectifier diode** |
|---|---|---|---|
| $R_1$ | [K/W] | 0.85 x $R_{th(j-c)}$ | 0.85 x $R_{th(j-c)}$ |
| $R_2$ | [K/W] | 0.15 x $R_{th(j-c)}$ | 0.15 x $R_{th(j-c)}$ |
| $\tau_1$ | [sec] | 0.035 | 0.055 |
| $\tau_2$ | [sec] | 0.002 | 0.0035 |

Tab. 4-1 Parameters for $Z_{th(j-c)}$ calculation using equation (4-2)

# 5 Integrated Temperature Sensor Specifications

All SEMiX IGBT modules feature a temperature-dependent resistor for temperature measurement. The resistor is soldered onto a separate DBC ceramic substrate close to the IGBT and diode chips and reflects the actual case temperature.
Since the cooling conditions have a significant influence on the temperature distribution inside the SEMiX module, it is necessary to evaluate the dependency between the temperatures of interest (e.g. chip temperature) and the signal from the integrated temperature sensor.

Rectifier modules do not include temperature sensors, because rectifiers are usually chosen with regard to pulse currents, meaning that they do not reach critical temperatures during normal operation. A sensor would be too slow in detecting short-term overloads.

## 5.1 Electrical Characteristic

The temperature sensor has a nominal resistance of 5 kΩ at 25 °C and 0.493 kΩ at 100 °C. The sensor is most accurate at 100 °C with a tolerance of ± 5 %. The measuring current should be 1 mA; the maximum value is 3 mA.

The built-in temperature sensor in SEMiX modules is a resistor with a negative temperature coefficient (NTC). Its characteristic is given in Fig. 5-1 and Fig. 5-2. The ohmic resistance values (min., type, max.) of the sensor as a function of temperature are given in Tab. 5-1.

A mathematical expression for the sensor resistance as a function of temperature R(T) is given by:

$$R(T) = R_{100} \times \exp[B_{100/125} \times (1/T - 1/T_{100})]$$

With $R_{100} = 0.493\ k\Omega$ (± 5 %)
$B_{100/125} = 3550\ K$ (± 2 %)
$T_{100} = 100\ °C = 373.15\ K$

$$R(T) = 0.493\ k\Omega \times \exp[3550 \times (1/T - 1/373.15\ K)]$$

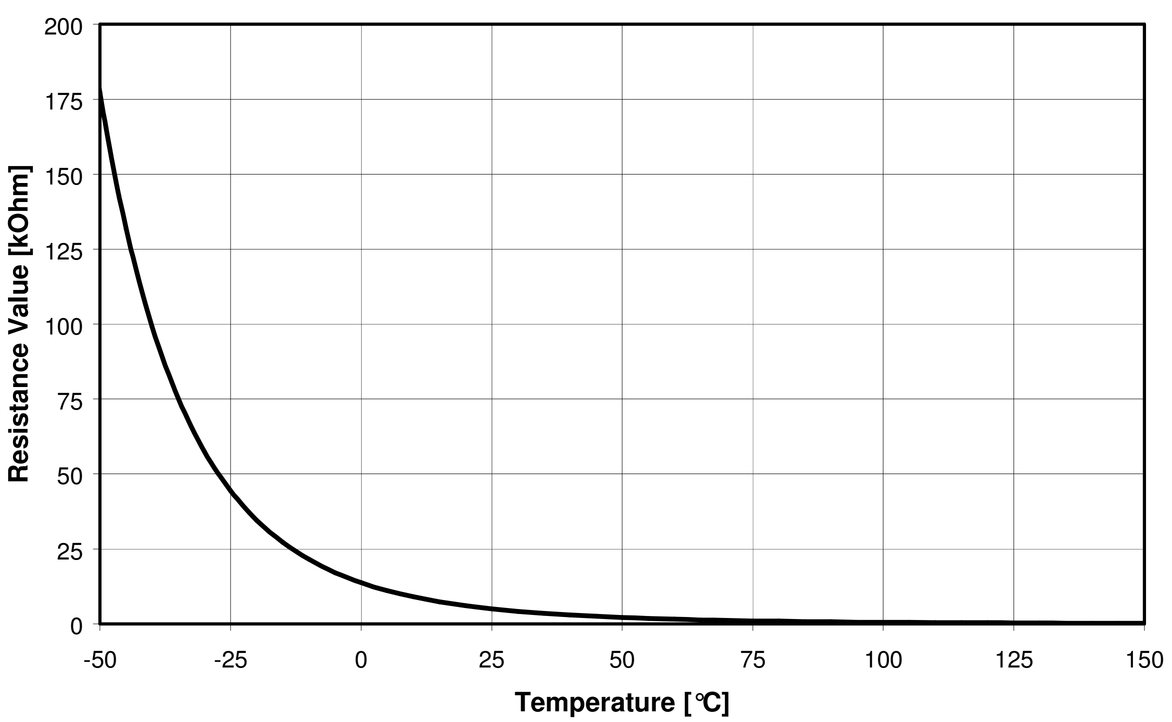



Fig. 5-1 Typical characteristic of the NTC temperature sensor included in SEMiX modules

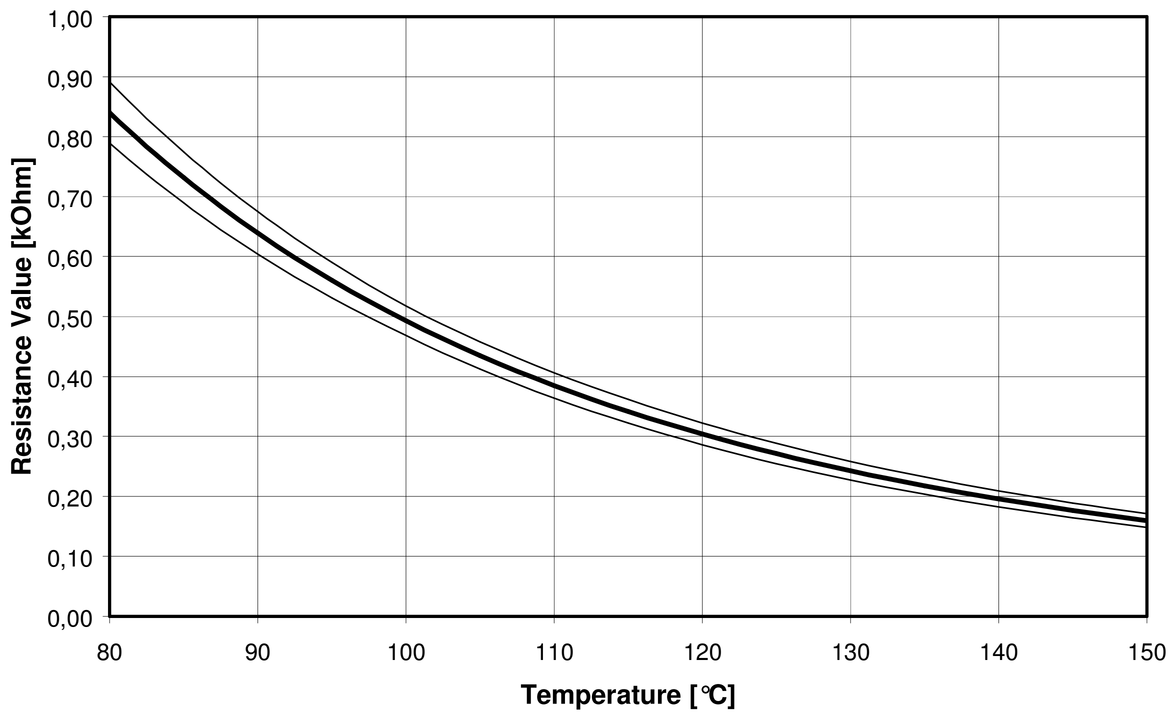



Fig. 5-2 NTC temperature sensor characteristic incl. tolerances

| Temperature | Resistance Value | | | Tolerance |
|---|---|---|---|---|
| [°C] | minimum [kΩ] | standard [kΩ] | maximum [kΩ] | maximum deviation [%] |
| -50 | 148.183 | 177.265 | 211.525 | 20.2 |
| -40 | 83.924 | 99.034 | 116.572 | 18.5 |
| -30 | 49.348 | 57.508 | 66.850 | 16.2 |
| -20 | 30.019 | 34.582 | 39.738 | 14.9 |
| -10 | 18.832 | 21.465 | 24.404 | 13.7 |
| 0 | 12.151 | 13.713 | 15.438 | 12.6 |
| 10 | 8.044 | 8.995 | 10.034 | 11.6 |
| 20 | 5.452 | 6.045 | 6.685 | 10.6 |
| 30 | 3.776 | 4.153 | 4.557 | 9.7 |
| 40 | 2.668 | 2.913 | 3.172 | 8.9 |
| 50 | 1.920 | 2.082 | 2.251 | 8.1 |
| 60 | 1.406 | 1.514 | 1.626 | 7.4 |
| 70 | 1.046 | 1.119 | 1.195 | 6.8 |
| 80 | 0.789 | 0.840 | 0.891 | 6.1 |
| 90 | 0.604 | 0.639 | 0.675 | 5.6 |
| 100 | 0.468 | 0.493 | 0.518 | 5.0 |
| 110 | 0.364 | 0.385 | 0.406 | 5.5 |
| 120 | 0.286 | 0.304 | 0.322 | 6.0 |
| 130 | 0.227 | 0.243 | 0.258 | 6.5 |
| 140 | 0.183 | 0.196 | 0.209 | 7.0 |
| 150 | 0.148 | 0.159 | 0.171 | 7.4 |

Tab. 5-1 Resistance values and tolerance as given by the supplier

## 5.2 Electrical Isolation

Inside SEMiX modules the temperature sensor is mounted onto a separate substrate close to the IGBT and diode dice. The minimum distance between the copper conductors is ≥ 0.71 mm. (Fig. 5-3)

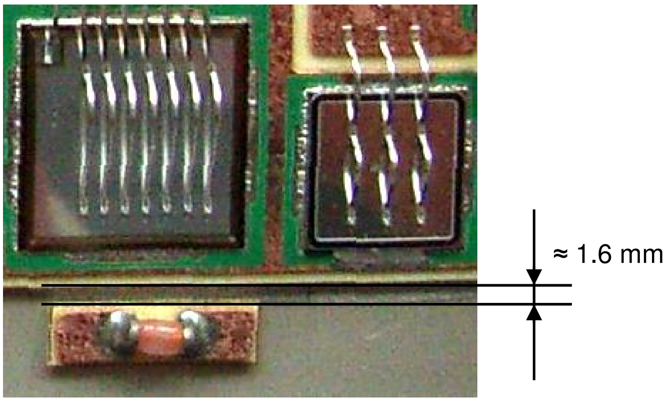



Fig. 5-3 Detail: Temperature sensor inside SEMiX

According to EN 50178 (VDE 0160), this design does not provide "Safe Electrical Insulation", because the temperature sensor inside the SEMiX module might be exposed to high voltages during semiconductor short circuit failure mode. After electrical overstress the bond wires could melt off, producing an arc with high-energy plasma in the process (as shown in Fig. 5-4). In this case the direction of plasma expansion is unpredictable and the temperature sensor might come into contact with the plasma.

The safety grade "Safe Electrical Insulation" in accordance with EN 50178 can be achieved by different additional means, which are described in this standard in more detail.

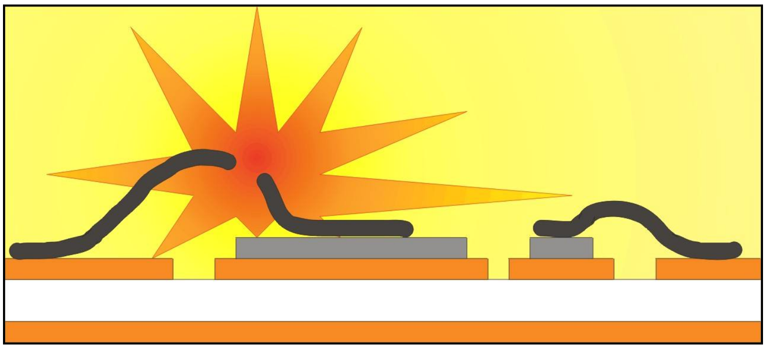


Fig. 5-4 Sketch of high energy plasma caused by bond wire melting

Please note: To ensure that electrical isolation $V_{isol}$ as stated in the data sheets is provided, suitable measurements are performed during the production process, as described in chapter 2.6.

# 6 Spring Contact System Specifications

## 6.1 Spring and Contact Specifications

| | Rating / Specification | Comment |
|---|---|---|
| Material | Copper: DIN 2076-CuSn6<br>With silver surface: Abrasiveness 75 to 95 HV, thickness 3 to 5 µm, tarnish protection 'silverbrite W ATPS'– thickness < 0.1 µm | |
| Contact force | 3 to 5 N | |
| Maximum contact resistance including ageing | - 200 mΩ (current ≤ 1A)<br>- 25 mΩ (current > 1A) | For one spring, tested according to IEC 600068-2-43 (10 days, 10 ppm H2S, 75 % RH, 25°C) |

Tab. 6-1 SEMiX contact springs specifications

## 6.2 PCB Specifications (Landing Pads for Springs)

| | Rating / Specification | Comment |
|---|---|---|
| Chem. Sn<br>(Chemically applied) | No min. thickness | Intermetallic phases may be contacted |
| HAL Sn<br>(Hot Air Levelling) | No min. thickness | Intermetallic phases may be contacted |
| NiAu | Ni ≥ 3µm, Au ≥ 20nm<br>(Electro-less nickel, immersion gold) | Tight Ni diffusion barrier required |
| SnPb | No min. thickness | Intermetallic phases may be contacted |

Tab. 6-2 Specifications for the surface metallization of landing pads for SEMiX contact springs

## 6.3 Storage Conditions

| | Rating / Specification | Comment |
|---|---|---|
| Unassembled | 20 000 h / 60 °C 95% RH | After extreme humidity the reverse current limits may be exceeded but do not degrade the performance of the SEMiX |
| Assembled | 20 000 h / 60 °C 95% RH | |

Tab. 6-3 Storage conditions for SEMiX modules with silver-plated contact springs

## 6.4 Stray Inductance of Contact Springs

The spiral springs look like the coils of an inductor. This would seem to contradict one of the main requirements in power electronics: “low inductance”. In measurements, however, these springs have not been shown to have any influence on switching behaviour. The following calculations verify the results obtained in practice.

In this respect, the SEMiX module, which features springs and PCB tracks between the driver and the springs, is comparable with a SEMITRANS module, which has internal wiring and wiring between driver and module.

### 6.4.1 Self Inductance of the Spring Connection

Fig. 6-1 Principle sketch of springs and PCB conductors

Fig. 6-2 SEMiX with directly mounted driver

Inductance spiral spring $L_{Sp}$ (with l = 5…10 D)

$$L_{Sp} = \mu \cdot n^2 \cdot \frac{\pi \cdot D^2}{4 \cdot \sqrt{l^2 + D^2}}$$

$$L_{SP} = 112\,\text{nH}$$

| | |
|---|---|
| μ | = $\mu_0$ = 1,26 µH/m |
| l | = 10 mm (length, spring under pressure) |
| D | = 2 mm (inner diameter) |
| n | = 17 (number of coils) |

Inductance PCB tracks $L_{PCB}$

$$L_{PCB} = \frac{l \cdot 2 \cdot \mu}{\pi} \cdot \ln\left(1 + \frac{a}{d+b}\right)$$

$$L_{PCB} = 31\,\text{nH}$$

| | |
|---|---|
| μ | = $\mu_0$ = 1,26 µH/m |
| l | = 100 mm (length of spring pad to driver output stage) |
| a | = 0.5 mm (distance between conductors on PCB) |
| d | = 50 µm (thickness of copper layer) |
| b | = 1 mm (width of the copper track) |

Total: $\mathbf{L_{Sp+PCB} = 143\ nH}$

### 6.4.2 Self-Inductance of a SEMITRANS Module

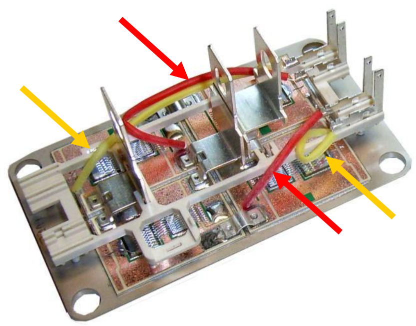


Fig. 6-3 Open SEMITRANS 3 module. Yellow and red wires are gate and emitter wires

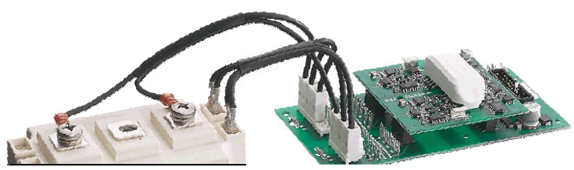


Fig. 6-4 SEMITRANS 3 module with wire connections to driver

Inductance inside of the module $L_{W1}$

$$L_{W1} = \frac{l_1 \cdot \mu}{\pi} \cdot \ln\left(\frac{2 \cdot a}{d}\right)$$

$$L_{W1} = 50nH$$

μ = $\mu_0$ = 1,26 μH/m
$l_1$ = 50 mm (wire length inside the module)
a = 3 mm (distance between wires)
d = 0.5 mm (wire diameter)

Inductance outside of the module $L_{W2}$

$$L_{W1} = \frac{l_2 \cdot \mu}{\pi} \cdot \ln\left(\frac{2 \cdot a}{d}\right)$$

$$L_{W1} = 100nH$$

μ = $\mu_0$ = 1,26 μH/m
$l_2$ = 100 mm (wire length outside the module)
a = 3 mm (distance between wires)
d = 0.5 mm (wire diameter)

Total: **$L_{W1+W2}$ = 150 nH**

This inductance lies in the same range as that of a solution with spring contacts and a PCB track.

### 6.4.3 Conclusion and Discussion

Since the values for the parasitic inductances of SEMiX and SEMITRANS modules are in the same range, a comparison would not prove particularly useful. Instead, the influence of the stray inductance on the gate voltage is generally looked at for comparison. Fig. 6-5 shows that self-inductance in wires has virtually no effect on the switching behaviour of the power semiconductor (neither in theory nor in the measurements performed).

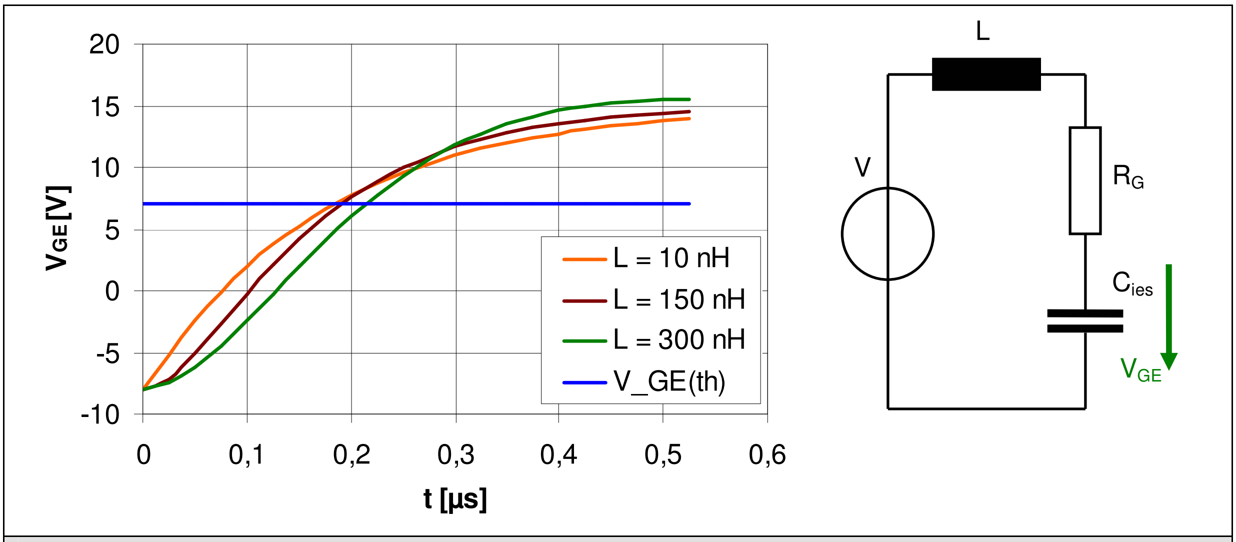



Fig. 6-5 Influence of stray inductance on the gate voltage (model: voltage rise $V_{GE}$ at a capacitor $C_G$ for different circuit inductances L) ($C_{ies} \approx Q_G / V_G$ = 1 μC / 23 V = 43 nF, $R_G$ = 4 Ω, $dV_{GE}$ = 23 V)

A voltage across the gate wire inductance is induced only at the beginning when the gate voltage is applied. This voltage is far below the threshold voltage $V_{GE(th)}$. When the voltages rise into within the range of the threshold voltage where the switching event starts, the voltages are similar for all inductances. A small effect on the delay time during switching can be seen; in the example given in Fig. 6-5 this delay is around 20 ns for the highest assumed value of 300 nH. For higher gate resistor values this small difference disappears entirely.

# 7 Reliability

## 7.1 Standard Tests for Qualification

The objectives of the test programme (refer to Tab. 7-1) are:
1. To ensure general product quality and reliability.
2. To evaluate design limits by performing stress tests under a variety of test conditions.
3. To ensure the consistency and predictability of the production processes.
4. To appraise process and design changes with regard to their impact on reliability.

| Reliability Test | Standard Test Conditions for | |
|---|---|---|
| | **MOS / IGBT Products:** | **Diode / Thyristor Products:** |
| High Temperature Reverse Bias (HTRB) *IEC 60747* | 1000 h, 95% $V_{DSmax}/V_{CEmax}$, 125°C ≤ $T_c$ ≤ 145°C | 1000 h, DC, 66% of voltage class, 105°C ≤ $T_c$ ≤ 120°C |
| High Temperature Gate Bias (HTGB) *IEC 60747* | 1000 h, ± $V_{GSmax}/V_{GEmax}$, $T_{vjmax}$ | not applicable |
| High Humidity High Temperature Reverse Bias (THB) *IEC 60068-2-67* | 1000 h, 85°C, 85% RH, $V_{DS}/V_{CE}$ = 80%, $V_{DSmax}/V_{CEmax}$, max. 80V, $V_{GE}$ = 0V | 1000 h, 85°C, 85% RH, $V_D/V_R$ = 80% $V_{Dmax}/V_{Rmax}$, max. 80V |
| High Temperature Storage (HTS) *IEC 60068-2-2* | 1000 h, $T_{stg\ max}$ | 1000 h, $T_{stg\ max}$ |
| Low Temperature Storage (LTS) *IEC 60068-2-1* | 1000 h, $T_{stg\ min}$ | 1000 h, $T_{stg\ min}$ |
| Thermal Cycling (TC) *IEC 60068-2-14 Test Na* | 100 cycles, $T_{stg\ max}$ – $T_{stg\ min}$ | 25 cycles $T_{stg\ max}$ – $T_{stg\ min}$ |
| Power Cycling (PC) *IEC 60749-34* | 20.000 load cycles, $\Delta T_j$ = 100 K | 10.000 load cycles $\Delta T_j$ = 100 K |
| Vibration *IEC 60068-2-6 Test Fc* | Sinusoidal sweep, 5g, 2 h per axis (x, y, z) | Sinusoidal sweep, 5g, 2 h per axis (x, y, z) |
| Mechanical Shock *IEC 60068-2-27 Test Ea* | Half sine pulse, 30g, 3 times each direction (±x, ±y, ±z) | Half sine pulse, 30g, 3 times each direction (±x, ±y, ±z) |

Tab. 7-1 SEMIKRON standard tests for product qualification

## 7.2 Reliability of Spring Contacts

The SEMiX spring contact for the auxiliaries is a solder-free contact. It can therefore be compared with other solder-free contacts such as screw terminals or plug connectors. Fig. 7-1 shows these "connections" for comparison.

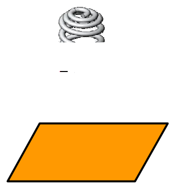
| Screwed main terminals | Plug connectors | Spring contacts |
|---|---|---|
| | |  |
| pressure force<br>typically 50 N/mm² | pressure force<br>typically 10 N/mm² | pressure force<br>typically 20 - 100 N/mm² |

Fig. 7-1 Comparison of non-soldered electrical connections

The surface materials used for the spring contacts as given in Tab. 6-1 and Tab. 6-2 (silver-plated spring and, for example, tin surface for PCB landing pads) are based on "state of the art" knowledge as gained from long-term experience with plug connectors and SEMIKRON's long-term experience with spring connections. Compared to a plug connector, the spring contact has a much higher pressure and contact force, which accounts for the even better reliability of this connection.

To verify this reliability, several harsh tests were performed on the spring contacts: "Temperature Cycling", "Temperature Shock", "Fretting Corrosion" (= "Micro Vibration"), "Electromigration", and a corrosive atmosphere test in accordance with IEC 60068-2-43:

- Atmosphere: 10 ppm $H_2S$
- Temperature: 25 °C
- Relative humidity: 75 %
- Volume flow: > volume x 3 per hour
- Duration: 10 days
- No current load during storage

All of these tests were passed successfully and demonstrated the outstanding reliability of SEMIKRON's spring contacts.

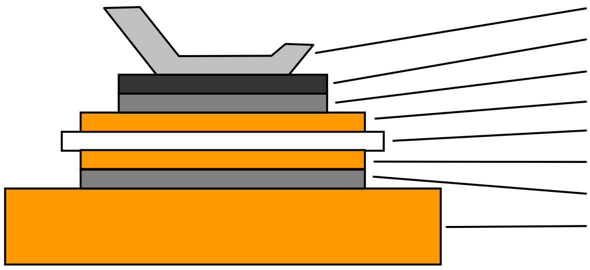
It goes without saying that SEMiX modules passed all SEMIKRON standard reliability tests as given in Tab. 7-1.

For further information on the reliability of spring contacts please refer to:


- F. Lang, Dr. U. Scheuermann, "*Reliability of spring pressure contacts under environmental stress*", Proc. Microelectronics Reliability Volume 47, Issues 9-11, September-November 2007, (18th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis)

## 7.3 Lifetime Calculations

The lifetime of a power module is limited by mechanical fatigue of the package. This fatigue is caused by thermally induced mechanical stress caused by different coefficients of thermal expansion (CTE). This means that in the course of heating (power on) and cooling (power off) = temperature swing (power cycle), the materials try to expand differently on account of their different CTEs. Since the materials are joined, however, they are unable to expand freely, leading to the aforementioned thermally induced mechanical stress. (Refer also to Fig. 7-2)



| Component | CTE |
|---|---|
| Wire bond | ~ 24 x $10^{-6}$/K |
| Chip | ~ 3 x $10^{-6}$/K |
| Chip solder | ~ 25 x $10^{-6}$/K |
| DBC copper | ~ 17 x $10^{-6}$/K |
| DBC ceramic | ~ 7 x $10^{-6}$/K |
| DBC copper | ~ 17 x $10^{-6}$/K |
| Base plate solder | ~ 25 x $10^{-6}$/K |
| Base plate | ~ 17 x $10^{-6}$/K |

Fig. 7-2 Cross sectional view of SEMiX package, including the coefficients of thermal expansion (at 20 °C)

When temperature changes, the mechanical stresses, that occur inside the different material layers, lead to material fatigue. The bigger the temperature difference ($\Delta T$), the more stress is induced. With every temperature cycle aging takes place. Wire bonding and solder layers are particularly affected by this. In time aging results in small cracks which start at the edges and increase in the direction of the centre of the material with every power cycle that occurs. The higher the medium temperature $T_j m$, the faster the cracks grow, because the activating energy is higher.
The typical resulting failure picture from field returns is “lift off” of the wire bonds. This means that the cracks meet in the centre and open the connection such that the wire bond is loose.

This shows that the lifetime is determined by the number of temperature cycles which can be withstood by the module. In the 90’s intensive investigations were carried in this area, including a research project known as the “LESIT study”. One of the main findings of this study was the equation given below (7-1), which shows relationship between the number of cycles Nf and the junction temperature difference $\Delta T_j$ and the medium temperature $T_j m$. (For better understanding see also to Fig. 7-3)

SEMiX modules are based on the same design principles as the modules which were investigated in the course of the LESIT study. For this reason the LESIT results may be used for life time estimations. That said, the reliability of power modules has improved since the LESIT study was concluded, which is why the results of equation (7-1) can be seen as a worst-case scenario.

$$Nf = A \times \Delta T_j^{\alpha} \times \exp\left(\frac{Q}{R \times T_j m}\right) \qquad (7\text{-}1)$$

With A = 640, $\alpha$ = -5, Q = 7.8 $10^{-4}$ J/mol and R = 8.314 J/mol K; $\Delta T_j$ and $T_j m$ in [K]

Fig. 7-4 shows the experimental results of the LESIT study (as bullet points) as well as the results of equation (7-1) as drawn lines.

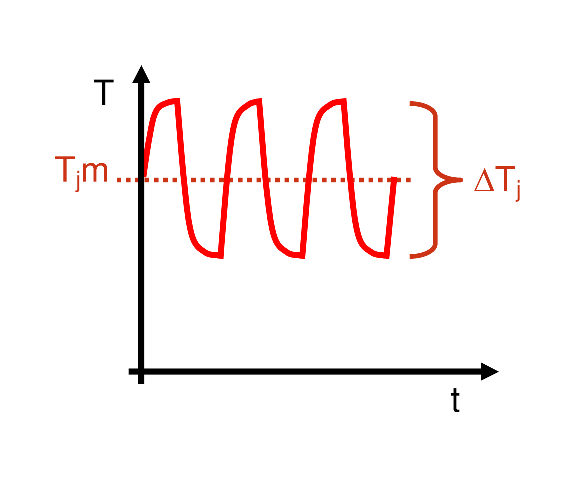



Fig. 7-3 Example of $T_jm$ and $\Delta T_j$

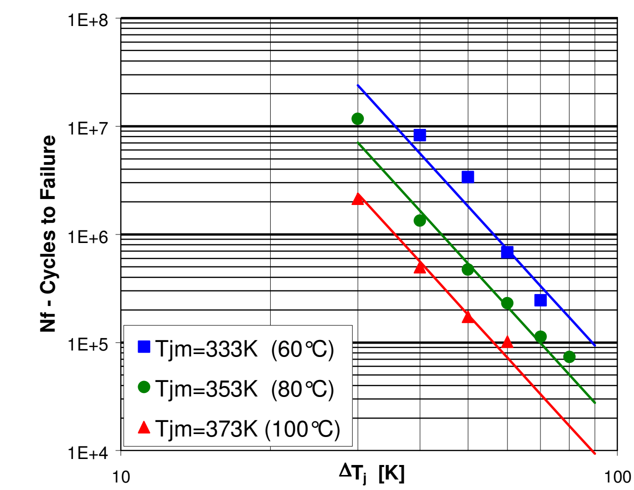



Fig. 7-4 "LESIT" curves, based on experimental results

For further information on the lifetime calculations for power modules please refer to:

- M. Held et.al., "*Fast Power Cycling Tests for IGBT Modules in Traction Application*"; Proceedings PEDS, pp 425 – 430, 1997

# 8 Design Recommendations for SEMiX

The following recommendations are tips only and do not constitute a complete set of design rules. The responsibility for proper design remains with the user of the SEMiX modules.

SEMIKRON recommends using SKYPER® or SKYPER® PRO drivers. Detailed information on this state-of-the-art driver core can be found on the SEMIKRON website at http://www.semikron.com/.

## 8.1 Printed Circuit Board Design

### 8.1.1 PCB Specifications

Recommendations for the printed circuit board:

- "FR 4" material can be used as a material for the printed circuit board.
- The thickness of copper layers should be compliant with IEC 326-3.
- The landing pads must not contain plated-through holes ("VIAs") to prevent any deterioration in contact. In the remaining area VIAs can be used as desired.
- The landing pads for the auxiliary contacts must have a diameter of Ø = 3.5 mm ± 0.2 mm.
- As stated in chapter 6.2, pure tin (Sn) is an approved interface for use with SEMiX spring contacts. Sufficient plating thickness must be guaranteed in accordance with the PCB manufacturing process. The tin surface is normally applied to the PCB chemically or in a hot-air levelling process.

  A second approved surface for the landing pads is electro-less nickel with a final immersion gold layer (Ni + Au).

  Not recommended for use are boards with "organic solder ability preservative" (OSP) passivation, because OSP is not suitable for guaranteeing long-term corrosion-free contact. The OSP passivation disappears during soldering or after approximately 6 months of storage.
- During the solder processes the landing pads for SEMiX spring contacts need to be covered and protected from contamination. This is particularly crucial for wave soldering. No residue of the cover material must be left on the landing pads, as this could lead to deterioration of the electrical contact in the long term.
- If SEMiX 13 (Fig. 1-1) is also used with a PCB for the main DC and AC currents, i.e. a PCB will be screwed to the main terminals, it is necessary to use "press-in bushes" here (in accordance with EN 50178 - A7.1.8.5). These "press-in bushes" must be able to permanently withstand the forces that occur from mounting, as described in chapter 9.2.3.

### 8.1.2 Gate and Emitter Connections

Inside a SEMiX module, substrates with IGBT dice are paralleled as shown in Fig. 2-1. The main terminals are already connected and paralleled inside the module. The auxiliary terminals for gate and emitter are freely accessible for every single IGBT. On account of this feature, every single chip can be controlled and the switching behaviour of the entire module can be optimised. This is advantageous in individual use as well as in parallel use of SEMiX IGBT modules.
Examples of PCB layouts can be found on the SEMIKRON website at http://www.semikron.com/. Please refer to: "Products" → "Electronics" → "Evaluations Boards".

The gate contacts are not connected internally in any of the SEMiX modules. For this reason, all of the gates have to be connected via the control board.
To achieve optimum and smooth switching behaviour for all paralleled IGBT chips, it is necessary to ensure gate signals decoupling. To achieve this, every single gate needs its own gate resistor $R_{G,x}$ (≥ 2 Ω), as shown in Fig. 8-1.
The integrated gate resistors on the IGBT chips of the "126" and "128" product lines are able to perform acceptable decoupling. Even in these cases, the circuit shown in Fig. 8-1 offers advantages.

The different SEMiX IGBT modules display different spring pin layouts. For the different SEMiX product lines not all possible emitter spring positions are equipped with springs. (Please refer to the Pin Out drawings in the data sheet for details). Inside, the emitters are connected and coupling inside the module via the main connections influences the switching behaviour of the individual paralleled chips. All emitter springs must be connected via the control board, because only then can good switching behaviour be ensured.

In the “12T4” product line all emitter positions are equipped with springs. In Fig. 8-1 resistors $R_{E,x}$ (≥ 0.5 Ω) at every emitter contact can be seen. These resistors are necessary to ensure homogeneous switching of the paralleled IGBTs inside the module. Additionally, these resistors dampen cross currents in the network resulting from the main and the auxiliary emitter paralleling.

The additional Shottky diode (100 V, 1 A) parallel to $R_{E,x}$ ensures safe turn-off of high currents (e.g. in the event of a short-circuit).

To achieve similar parasitic inductances and homogeneous switching behaviour, the conductor lengths form the supply point to the individual gate and emitter connections should be identical for all paralleled IGBTs.

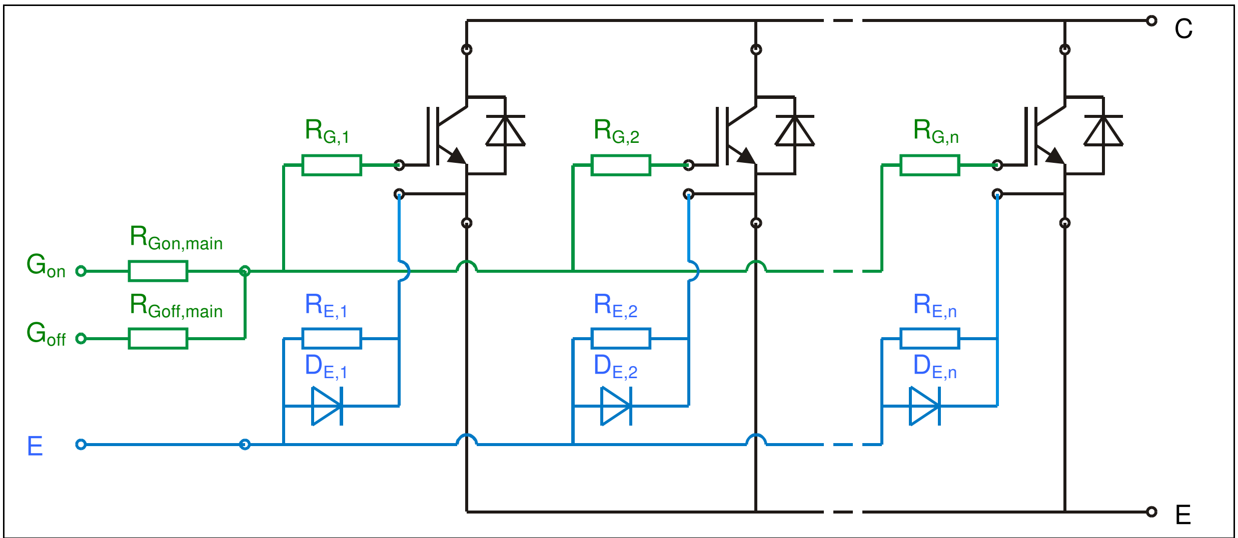



Fig. 8-1 Circuit with $R_{G,x}$ and $R_{E,x}$ for signal decoupling.

Should the data sheet values be measured with the circuit shown in Fig. 8-1, the values for $R_{Gon,main}$, $R_{Goff,main}$, $R_{G,x}$ and $R_{E,x}$ are given under “Remarks”.

### 8.1.3 Data Sheet Values for $R_G$

The data sheet value for the gate resistors $R_{G,on}$ and $R_{G,off}$ refers to a resistor between the driver and the module, as shown in Fig. 8-2. With regard to Fig. 8-1, $R_{G,on}$ and $R_{G,off}$ are each the sum of all parallel and serially connected resistors given in the equations (8-1) and (8-2).

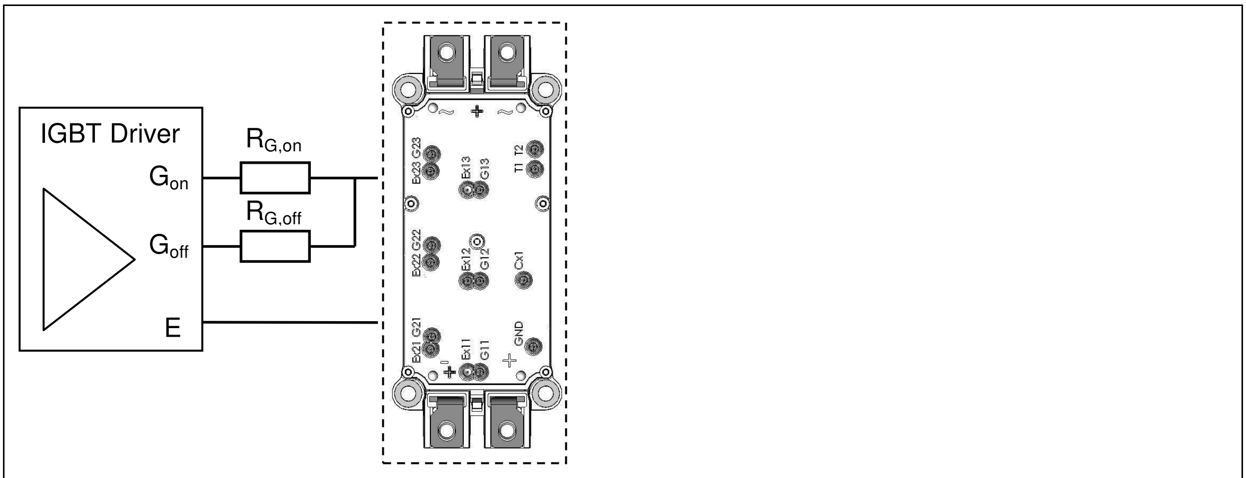



Fig. 8-2 How to understand the value for $R_G$ as given in the data sheets

$$R_{G,on} = R_{Gon,main} + \frac{1}{\frac{1}{R_{G,1} + R_{E,1}} + \frac{1}{R_{G,2} + R_{E,2}} + \ldots + \frac{1}{R_{G,n} + R_{E,n}}} \quad (8\text{-}1)$$

$$R_{G,off} = R_{Goff,main} + \frac{1}{\frac{1}{R_{G,1} + R_{E,1}} + \frac{1}{R_{G,2} + R_{E,2}} + \ldots + \frac{1}{R_{G,n} + R_{E,n}}} \quad (8\text{-}2)$$

The $R_G$ value given in the data sheet is determined under laboratory conditions, taking into account optimum losses and short-circuit capabilities without any snubber circuit. In the final application fine tuning of the resistor network and further optimisation is possible and recommended. This might include the introduction of different $R_{G,on}$ and $R_{G,off}$. A further possible optimisation possibility is the use of an additional resistor for short-circuit turn-off.

Nowadays, most IGBT chips have an integrated gate resistor (refer to Fig. 8-3). Since this resistor, and hence its influence on the switching behaviour, cannot be modified, it is not taken into regard when determining the values for $R_{G,on}$ and $R_{G,off}$. To calculate the necessary driver output power this value is necessary, which is why $R_{G,int}$ is given in the data sheet as a separate value. The $R_{G,int}$ given in the data sheet is already the sum of the paralleled $R_{Gint,x}$ inside the SEMiX module.

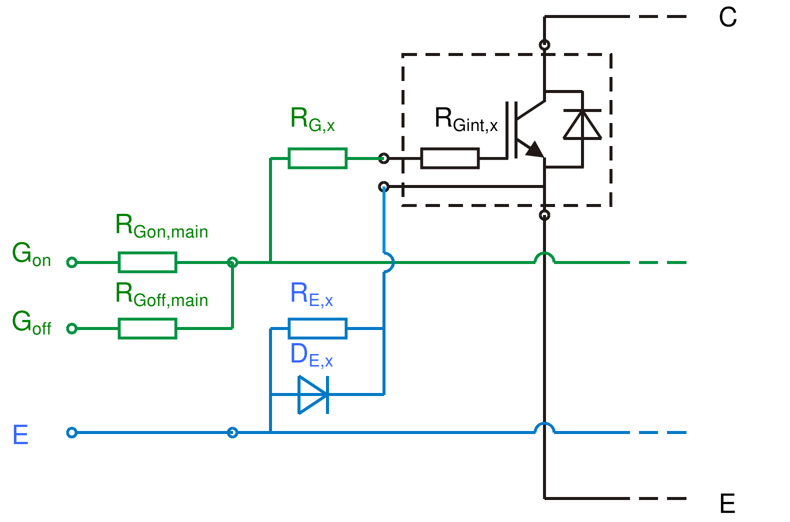



Fig. 8-3 How to understand the value for $R_{G,int}$ given in the data sheets

## 8.1.4 Gate Clamping

To ensure that the gate voltage $V_{GE}$ does not exceed the maximum value as stated in the data sheet, the use of an appropriate gate clamping circuit (e.g. two anti-serial Z-diodes $D_{GE}$, $V_Z$ = 16 V, as shown in Fig. 8-4) is recommended. This circuit has to be placed as close to the auxiliary contacts as possible.

It is necessary to ensure that the IGBT is always in a defined state, especially in cases where the driver is not able to deliver a defined gate voltage $V_{GE}$. A suitable solution to this problem is to use a resistor between gate and emitter $R_{GE}$ (≈ 20 kΩ).

This circuit is meant as an addition to the circuit shown in Fig. 8-1

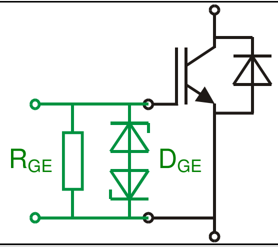



Fig. 8-4 Gate clamping circuit

### 8.1.5 General Design Rules

The following general design rules should be taken into account when developing an IGBT driver circuit:

- To suppress interference in the gate signals, magnetic coupling of any kind between the main current and the gate circuits has to be avoided. This can be achieved, for example, by using short gate and emitter connections, whose tracks should be led parallel and very close to each other, i.e. "no open loops". Furthermore, the tracks should be in line with the main magnetic field = 90° to the main current flow $I_C$.
- IGBT modules need to be turned off by a negative gate voltage $V_{GEoff}$. Otherwise unwanted switch-on via Miller capacitance $C_{res}$ may occur.
- For short-circuit switch-off, a soft-switch-off circuit in the gate drive circuit (e.g. increased $R_{Goff}$) is recommended to decrease the voltage overshoots in this particular case. SEMIKRON's SKYPER® PRO offers this feature.

## 8.2 Paralleling SEMiX IGBT Modules

When paralleling SEMiX IGBT modules it is necessary to ensure a gate signal decoupling as well as homogeneous and low inductance AC and DC connections.

To get the maximum power out of the modules thermal management should be optimised. For more details on this please refer to chapter 8.4.

### 8.2.1 Paralleling Gate and Emitter Connections

If paralleled IGBT modules are used, it follows that the IGBT chips are also paralleled. Consequently, control signal decoupling (as described in chapter 8.1.2) is needed and the circuit as given in Fig. 8-1should be continued. This leads to a circuit as shown in Fig. 8-5.

Paralleled IGBT modules must be controlled by one driver, also shown in Fig. 8-5. If a separate driver is used for every paralleled module it is not possible to ensure that all of the IGBTs switch simultaneously, meaning that the current sharing between these modules will not be even.

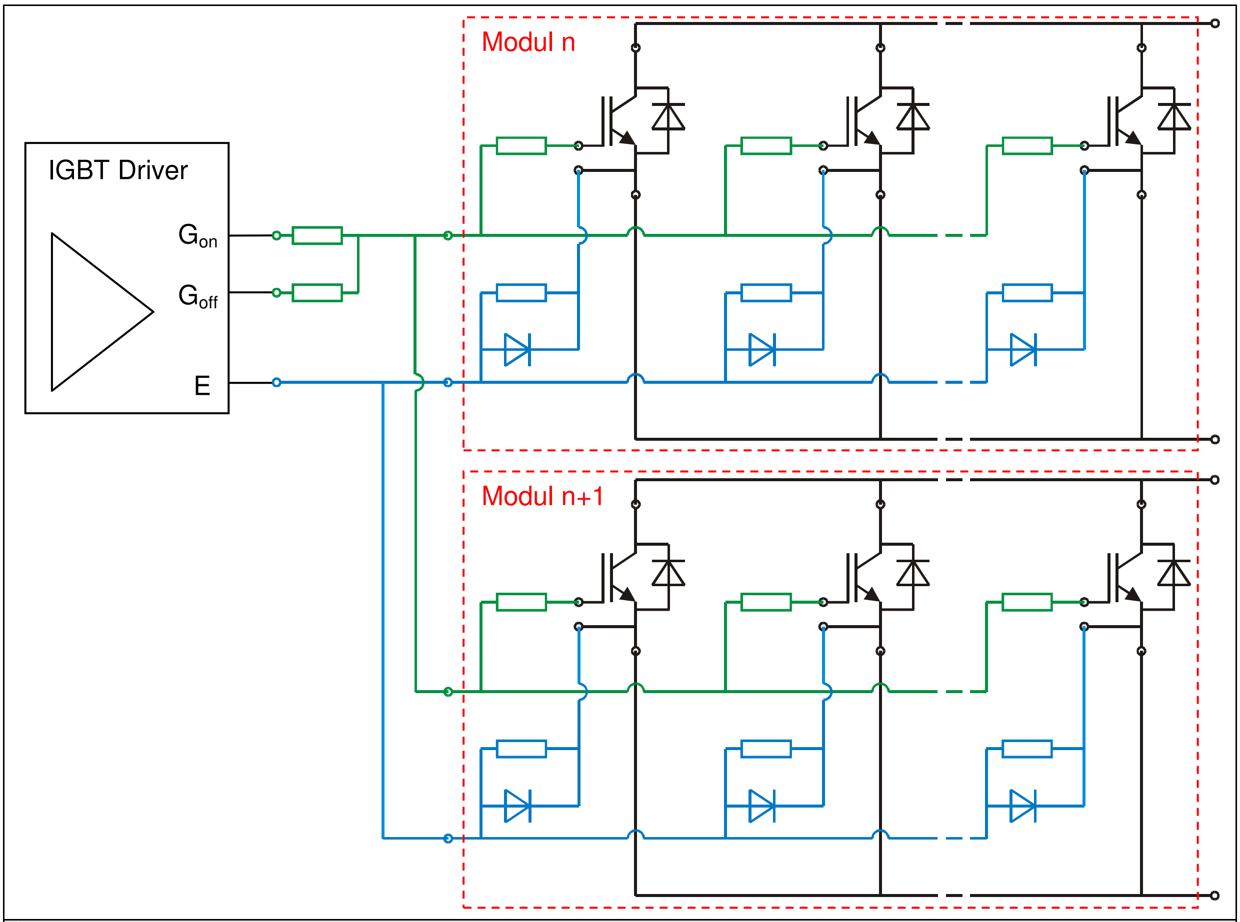



Fig. 8-5 Principle gate-control circuit for paralleled SEMiX IGBT modules

### 8.2.2 Paralleling Main Terminals

For optimum current sharing all parasitic stray inductances have to be the same for every module. The same loop length for all connections is a good indicator of the same inductance. Fig. 8-6 shows an optimised AC connection: the length from all module terminals to the output is identical and all terminals are shorted very close to the module, keeping them on the same voltage potential.

The same rules apply to the DC connection. In this case, a further important point is that the point of supply from the rectifier should be central and not from one side. This ensures very similar stray inductances at the DC terminals, too.

Note: an additional mechanical support is recommended to prevent mechanical overloading of the terminals – also refer to chapter 9.2.3

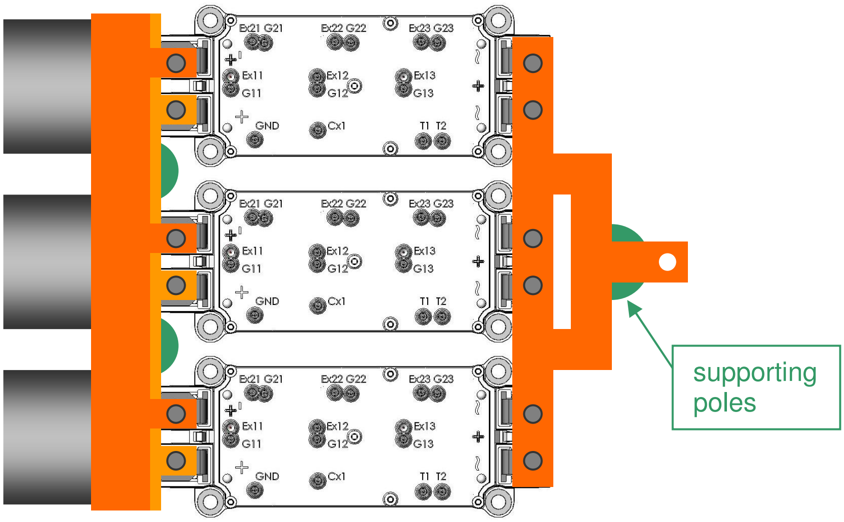
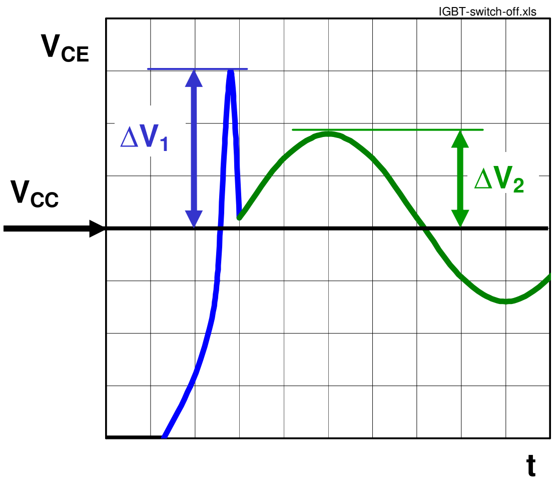



Fig. 8-6 Paralleled SEMiX with low-inductance DC-link and symmetric AC-link for optimised current sharing

## 8.3 DC-Link Bus Bars, Snubber Capacitors

Due to stray inductances in the DC link, voltage overshoots as shown in Fig. 8-7 occur during IGBT switch-off (caused by the energy which is stored in the stray inductances). These voltage overshoots may destroy the IGBT module because they are added to the DC-link voltage and may lead to $V_{CE} > V_{CES}$.

First of all, the stray inductances have to be reduced to the lowest possible limit. This includes low-inductance DC-link design as well as the use of low-inductance DC-link capacitors. The use of snubber capacitors with a very low stray inductance, low Equivalent Series Resistance (ESR) and a high “IR” Ripple Current Capability is recommended.




$$\Delta V_1 = L_{stray-snubber} \times di_C/dt$$

$$\Delta V_2^2 = \frac{L_{stray-DC-bus} \times i_C^2}{C_{snubber}}$$

$i_C$ = operating current
$di_C/dt$ = during switch-off

$V_{CC}$ = DC-link voltage

Fig. 8-7 Voltage overshoots caused by parasitic inductances

Furthermore, a pulse capacitor (see Fig. 8-8 and Fig. 8-9) should be placed between the +/- DC terminals of the SEMiX as a snubber. This snubber works as a low-pass filter and “absorbs” the voltage overshoot.
Typical values for these capacitors are from 0.1 µF to 1.0 µF. The choice of the right snubber should be determined by proper measurements.

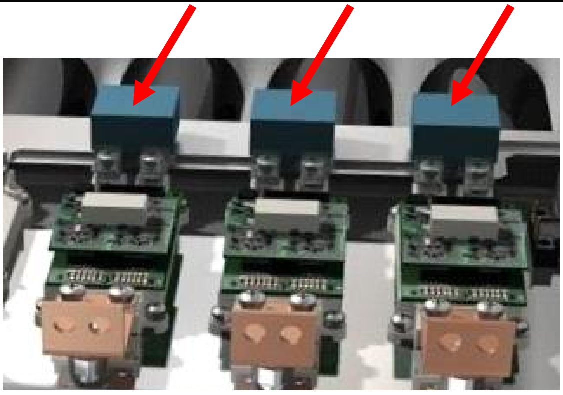
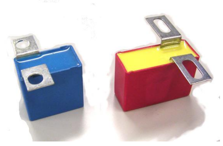


Fig. 8-8 SEMiX inverter with snubber capacitors mounted directly at the +/- DC main terminals

Recommended snubber capacitor



Non-recommended snubber capacitor, due to too high stray inductance

Fig. 8-9 Different snubber capacitors

## 8.4 Thermal Management

Optimum positioning of SEMiX modules on the heat sink can help improve thermal management significantly. Using three SEMiX half bridges with between 20 mm and 30 mm clearance between the modules (Fig. 8-11) reduces the thermal resistance by approximately 15 % compared to the $R_{th}$ of a six-pack in a SEMiX 33c case (Fig. 8-10).

This decrease in thermal resistance results directly in a higher maximum output current $I_C$.

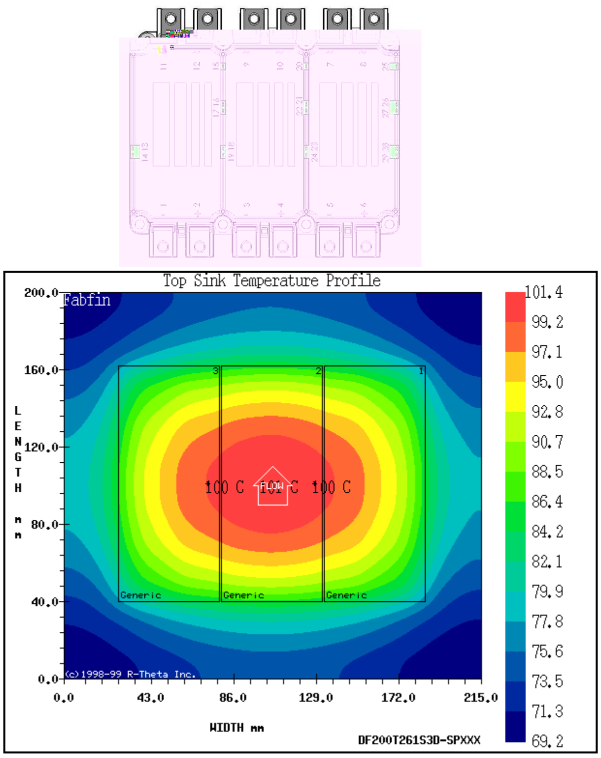



Fig. 8-10 SEMiX "33c" six-pack module

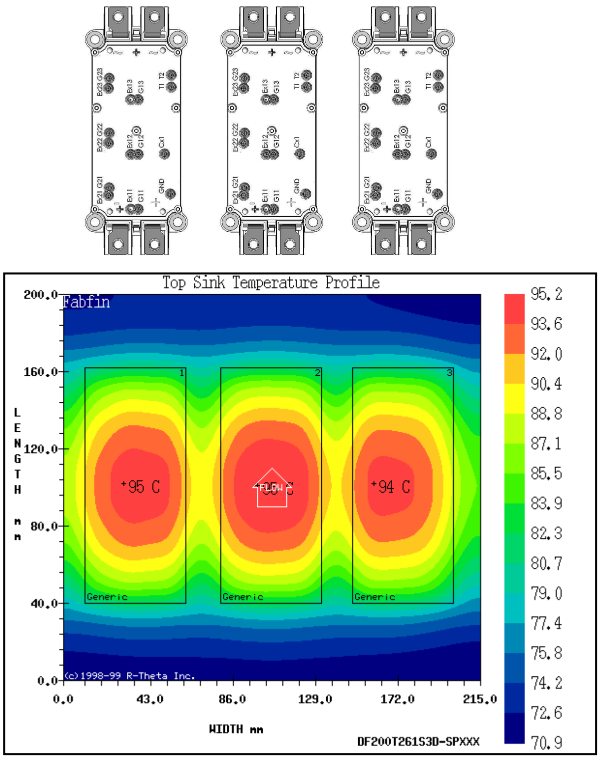



Fig. 8-11 3 x SEMiX "3" module for optimised thermal management

# 9 Mounting Instructions

## 9.1 Preparation, Surface Specifications

To obtain maximum thermal conductivity the underside of the module must be free from grease and particles. Furthermore, to ensure long-term reliable electrical contact the contact springs have to be kept clean at all times and should never be touched by hand.

The heat sink must fulfil the following specifications:

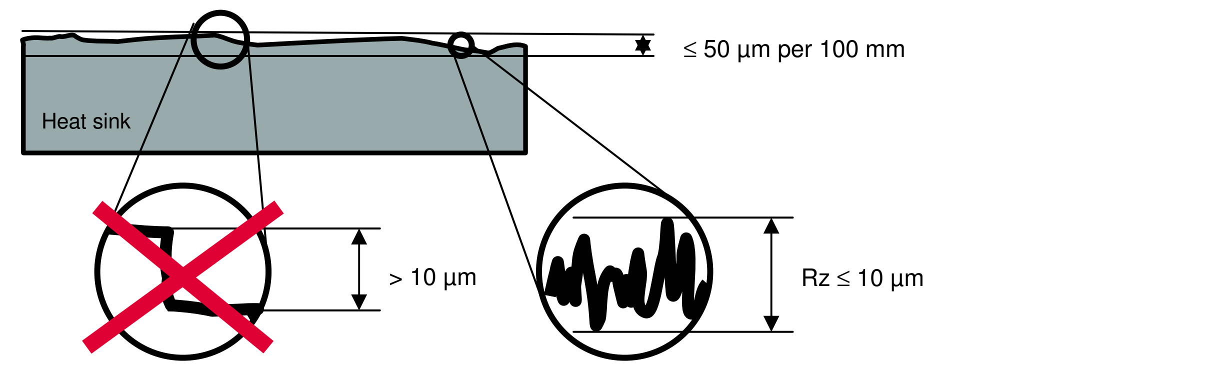



Fig. 9-1 Heat sink surface specifications

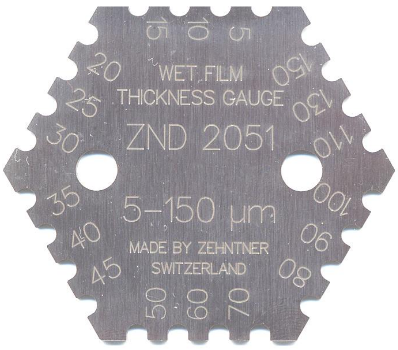
- The heat sink must be free from grease and particles
- Unevenness of heat sink mounting area must be ≤ 50 µm per 100 mm (DIN EN ISO 1101)
- Roughness “Rz” ≤ 10 µm (DIN EN ISO 4287)
- No steps > 10 µm (DIN EN ISO 4287)

## 9.2 Assembly

### 9.2.1 Applying Thermal Paste

A thin layer of thermal paste has to be applied onto the heat sink surface or the underside of the module. A layer thickness of 50 µm – 100 µm is recommended for Silicone Paste P 12 from WACKER CHEMIE.
The thickness of the layer can be determined using a measurement gauge as shown in Fig. 9-2.

SEMIKRON recommends using screen printing to apply thermal paste. In certain cases a hard rubber roller might be suitable for the application of thermal paste.




Supplier:

ELCOMETER GmbH
Himmlingstr. 18
D-73434 Aalen
Germany

Tel. +49-7366-919283

Fig. 9-2 Wet Film Thickness Gauge 5 – 150 µm

### 9.2.2 Mounting a SEMiX module to the Heat Sink

The SEMiX has to be placed on the appropriate heat sink area. Then the screws have to be pre-tightened with max. 1.0 Nm. Finally, the mounting torque $M_s$ (as given in the data sheets) has to be applied. During the assembly process the thermal paste shall spread evenly, ensuring that good and homogeneous thermal contact is achieved.

SEMIKRON recommends using the following type of screw:

- M5 - 8.8
- Strength of screw: 8.8
  - = Tensile strength - Rm = 800 N / mm²
  - = Yield point - Re = 640 N / mm²
- The mounting torque $M_s$ has to be between min. 3.0 Nm and max. 5.0 Nm (unless otherwise specified in the data sheet)
- To comply with the creepage and clearance distances as given in chapter 2.5, the height of the screw and washer must not exceed 6 mm + 1 mm. Refer also to Fig. 9-3.

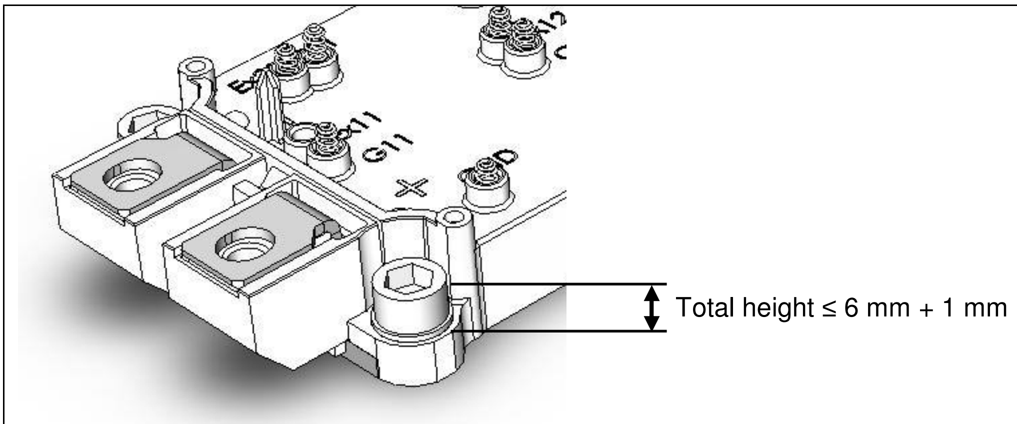



Fig. 9-3 Maximum height of screw plus washer

For modules with four screws the screws must be assembled in diagonal (crosswise) order. For six-pack modules in the “SEMiX 33c” case the screws have to be assembled in the order described in Fig. 9-4.

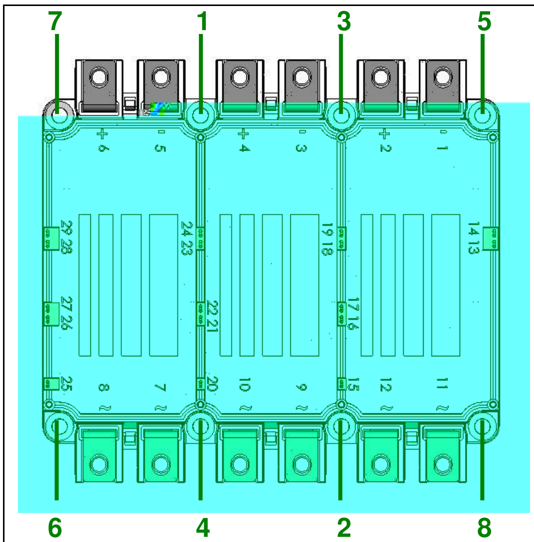



Fig. 9-4 Assembly order of screws for “SEMiX 33c” case (for assemble to the heat sink)

### 9.2.3 Mounting to the Main Terminals of SEMiX

Since SEMiX is a power-electric module and not part of the mechanical construction, the maximum mechanical forces on the main terminals as given in Fig. 9-5 must not be exceeded throughout the entire assembly procedure.

For the DC-link connection it is better to apply a slight pressure force in the –Z direction rather than pull forces in the +Z direction. In addition, the SEMiX module is not meant to support the DC-link, which is why additional mechanical components have to be arranged. Mechanical support is also needed for the AC-connection (e.g. motor cables) in order to keep mechanical forces and unnecessary vibration stress away from the module.

Fig. 9-5 Maximum forces at the main terminals

SEMIKRON recommends using the following type of screw:

- M6 - 8.8
- Strength of screw: 8.8
  = Tensile strength - Rm = 800 N / mm²
  = Yield point - Re = 640 N / mm²
- The depth of the screw in the module has to be between min. 6.5 mm and max. 10.0 mm.
- The mounting torque $M_t$ has to be between min. 2.5 Nm and max. 5.0 Nm
  (unless otherwise specified in the data sheet).

### Internal paralleling of AC-Terminals

Inside the SEMiX module the two AC-terminals are paralleled as shown in Fig. 9-6. This means it is not necessary to connect both terminals. Even with just one screw the terminal the maximum terminal current $I_{t(RMS)}$ as given in the data sheets can be achieved.

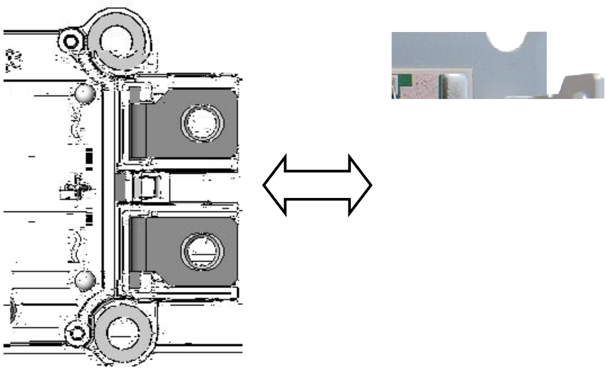


Fig. 9-6 Detail: AC terminal of SEMiX

### 9.2.4 Mounting the Printed Circuit Board to the SEMiX

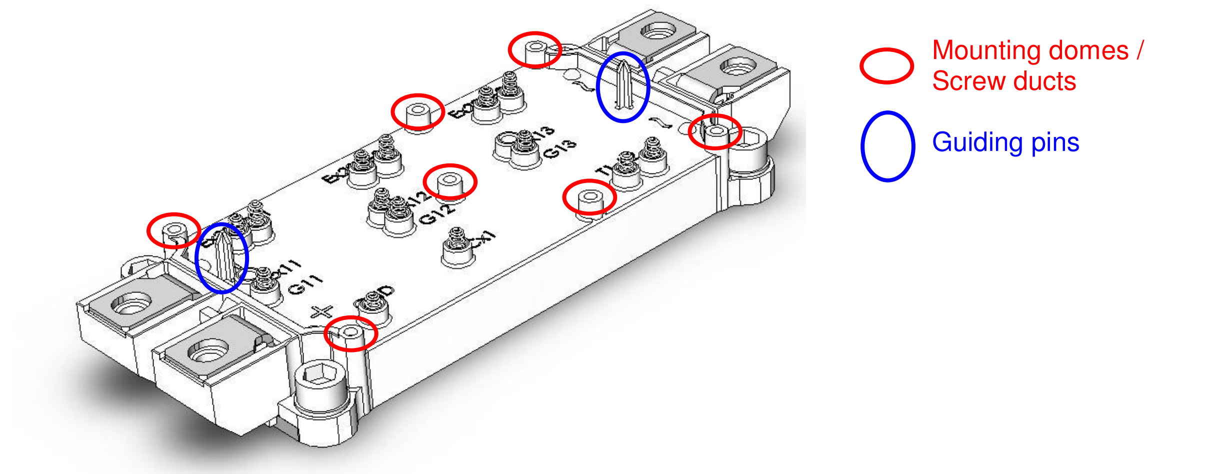



Fig. 9-7 SEMiX mounting domes and guiding pins

SEMIKRON recommends using the following type of screw:

- Self-tapping screws such as:
    - EJOT DELTA PT WN 5451 25x8
    - EJOT DELTA PT WN 5452 25x8 (alternative)
    - TORX T8 screw head
    - A2F surface specification
    - http://www.ejot.de/
- The depth of the screw in the module has to be between min. 6.0 mm and max. 7.5 mm. Please refer to the data sheet drawings for the detailed depth of the screw ducts.
- The mounting torque M has to be between min. 0.65 Nm and max. 0.85 Nm
- The number of times the driver may be assembled and disassembled depends very much on the screw surface and mounting torque. Under the aforementioned conditions, a driver can normally be assembled and disassembled three times.

The “SEMiX 3” case has 7 mounting domes. As shown in Fig. 9-7: four domes at the corners, one in the centre and two additional domes at the edges of the module. These two additional domes are meant for better resistance to shock and vibration. The use of these domes is optional.
For all other SEMiX modules it is necessary to use all available mounting domes to ensure a reliable connection between the contact springs and the PCB.

For the “SEMiX 33c” case (Fig. 9-4), the auxiliary contacts have to be soldered. During the solder process a maximum soldering temperature $T_{solder}$ = 265 °C and a maximum soldering time $t_{solder}$ = 10 sec must not be exceeded. For reasons of ESD protection, all soldering tools (e.g. soldering iron) have to be conductive grounded (refer also to chapter 9.3). Wave soldering is a valid soldering process in this context.
Since the electrical connections inside the “SEMiX 33c” are made using spring contacts, it is necessary to mount the module onto the heat sink (or a similar plate) before performing any electrical test. This also applies to any kind of incoming inspection.

### 9.2.5 Automated Screw Driver

The use of torque wrenches with automatic release is strongly recommended. These should be calibrated regularly.

For power screw drivers it is recommend that an electric power screw driver be used. With pneumatic systems, the behaviour of the clutch can lead to a shock and a torque overshoot which would damage the SEMiX module.

The screwing speed has to be limited to a maximum speed of 300 r.p.m. (revolutions per minute).

## 9.3 ESD Protection

SEMiX IGBT modules are sensitive to electrostatic discharge, because discharge of this kind can damage or destroy the sensitive MOS structure of the gate. All SEMiX modules are ESD protected in the shipment box by conductive plastic trays.
When handling and assembling the modules it is recommended that a conductive grounded wristlet be worn and a conductive grounded workplace be used. All staff should be suitably trained for correct ESD handling.

# 10 Laser Marking

## 10.1 Laser Marking on Modules

All SEMiX modules are laser marked. The marking contains the following items (see Fig. 10-1):

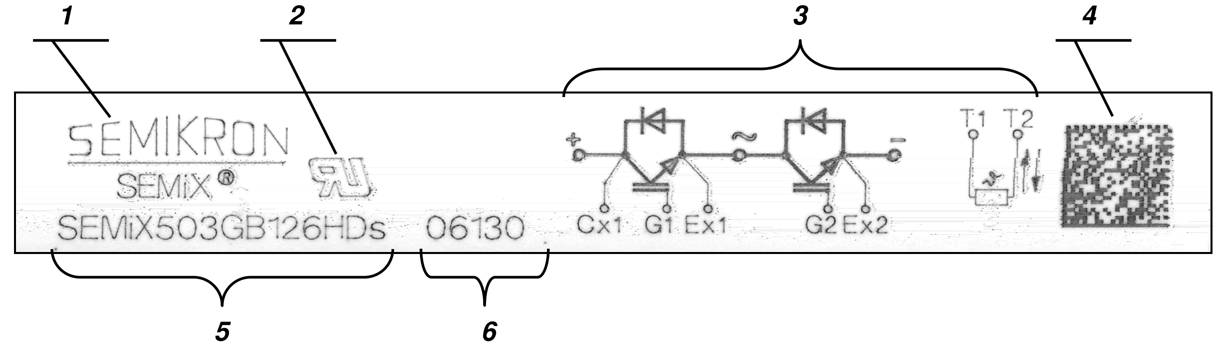



Fig. 10-1 Typical laser marking of SEMiX module

***1*** SEMIKRON logo, with product line designation SEMiX®
***2*** UL logo, SEMiX is UL recognised, file name: E63532
***3*** Circuit diagram
***4*** Data Matrix Code (refer also to chapter 10.2)
***5*** Type designation, for details refer to chapter 13 “Type Designation System”
***6*** Date code – 5 digits: YYMML (L = Lot of same type per week)
The date code might be followed by

- “R” to indicate that the module complies with the RoHS directive
- “E” for engineering samples

## 10.2 Data Matrix Code

The Data Matrix Code is described as follows:

- Type: EEC 200
- Standard: ISO / IEC 16022
- Cell size: 0.46 mm
- Field size: 24 x 24
- Dimensions: 11 x 11 mm plus a guard zone of 1 mm (circulating)
- The following data is coded:

| *1* | *2* | *3* | *4* | *5* | *6* | *7* | *8* | *9* | *10* | *11* |
|---|---|---|---|---|---|---|---|---|---|---|
| SEMiX503GB126HDs | | 27160012 | 6DE020381201 | | 0 | 1 | | 0001 | | 06130 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| *1* | 16 | digits | type designation | *7* | 1 | digit | line identifier (production) |
| *2* | 1 | digit | blank | *8* | 1 | digit | blank |
| *3* | 10 | digits | part number | *9* | 4 | digits | continuous number |
| *4* | 12 | digits | production tracking number | *10* | 1 | digit | blank |
| *5* | 1 | digit | blank | *11* | 5 | digits | date code |
| *6* | 1 | digit | measurement number | | | | |

Total: 53 digits

# 11 Bill of Materials

The SEMiX modules are made from various materials as given in Tab. 11-1.

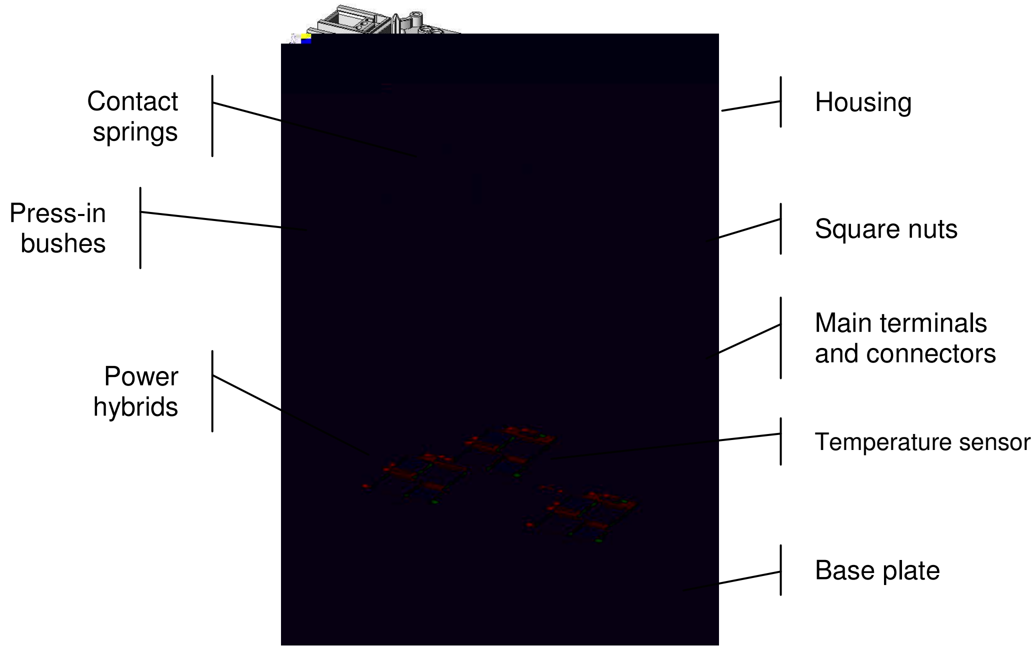



Fig. 11-1Sketch of SEMiX 3 as an example of the parts used

| | |
|---|---|
| Housing | Makrolon 9425 (Polycarbonate “PC” + 20 % glass fibre, contains no free halogens) |
| Contact springs | Copper alloy CuSn6 (DIN ISO 2076) with silver surface and tarnish protection “Silverbrite W ATPS” |
| Square nuts | Steel, zinc-plated |
| Press in bushes | Brass, nickel-plated |
| Soft mould | Silgel 612 silicone gel |
| Main terminals and connectors | Copper, silver-plated |
| Power hybrids | |
| ♦ Substrate | Copper, Al2O3, Copper.<br>A nickel metallization and gold finish is applied to the copper surface. |
| ♦ Wire bonds | Aluminium alloy |
| ♦ Chips | Silicon with Aluminium metallization on top side and silver metallization on bottom side |
| ♦ Temp. sensor | |
| ♦ Chip solder | SnAg alloy + organic flux (cleaned after soldering) |
| Base plate solder | SnCu alloy “No Flux” |
| Base plate | Copper, nickel plated |

Tab. 11-1 SEMiX – Bill of materials

Note: Even though SEMIKRON products are not subject to the electrical and electronic equipment law (ElektroG), SEMIKRON produces the SEMiX® product family in compliance with §5 of this regulation (on prohibited substances) as well as article 4 of directive 2002/95/EC of the European parliament (RoHS) on the restricted use of certain hazardous substances in electrical and electronic equipment. The ElektroG law is the German statutory equivalent of the European directive.

# 12 Packing Specifications

## 12.1 Packing Box

Standard packing boxes for SEMiX modules:

Fig. 12-1 Cardboard box with SEMiX in transparent ESD tray; dimensions: 350 x 280 x 50 mm³ (l x w x h)

| | | |
|---|---|---|
| Quantities per package | SEMiX 1s | 8 pcs |
| | SEMiX 2s | 6 pcs |
| | SEMiX 3s | 6 pcs |
| | SEMiX 4s | 4 pcs |
| | SEMiX 13s | 4 pcs |
| | SEMiX 33c | 2 pcs |
| Weight per package | ≤ 2.5 kg | |
| Bill of materials | Boxes: | Paper (cardboard) |
| | Trays: | ASK-PET/56 (not electrically chargeable) |

## 12.2 Marking Packing Boxes

All SEMiX packing boxes are marked with a sticker label.

This label is placed on the packing box as shown in Fig. 12-2:


Fig. 12-2: Place for label on SEMiX packing boxes

The label contains the following items (see Fig. 12-3)


Fig. 12-3 Label on SEMiX packing boxes

| | | |
|---|---|---|
| ***1*** | SEMIKRON Logo | |
| ***2*** | "Dat. Cd:" | Date code – 5 digits: YYMML (L=Lot of same type per week)<br>Suffix "R" stands for "RoHS compliant" |
| ***3*** | "Menge:" | Quantity of SEMiX modules inside the box – also as bar code |
| ***4*** | SEMiX type designation | |
| ***5*** | "Au.-Nr :" | Order Confirmation Number / Item Number on Order Confirmation |
| ***6*** | "Id.-Nr:" | SEMIKRON part number – also as bar code |
| ***7*** | ESD sign | SEMiX IGBT modules are sensitive to electrostatic discharge. Remove the ESD package and handle the modules only if the environment is guaranteed to be ESD proof. |

Bar Code:
- Standard: EEC 200
- Format: 19/9

# 13 Type Designation System

| *1* | *2* | *3* | *4* | *5* | *6* | *7* |
|---|---|---|---|---|---|---|
| SEMiX | 45 | 2 | GB | 12 | 6 | HDs |

***1*** SEMiX: Product name

***2*** Rated output current $I_C$ /10 (For OGBT product line "126", "128", "176")
Nominal chip current $I_{C,nom}$ /10 (For new product line "066", "12S2")
Rated output current $I_{FAV}$, $I_{FAV}$, $I_D$ /10 (For rectifier modules)

***3*** Housing size

| | | |
|---|---|---|
| 1 | = | 1, 1s, 13 |
| 2 | = | 2, 2s |
| 3 | = | 3, 3s, 33c |
| 4 | = | 4, 4s |

***4*** Circuit specification (examples)

| | | |
|---|---|---|
| GB | = | IGBT half bridge |
| GAL | = | IGBT low side chopper |
| GAR | = | IGBT high side chopper |
| GD | = | 3 ~ IGBT inverter, "six-pack" |
| KD | = | Diode rectifier half bridge |
| KH | = | Half controlled rectifier half bridge |
| KT | = | Controlled rectifier half bridge |
| D | = | 3 ~ rectifier bridge not controlled |
| DH | = | 3 ~ rectifier bridge half controlled |

***5*** Voltage class

| | | |
|---|---|---|
| 06 | = | 600 V |
| 12 | = | 1200 V |
| 16 | = | 1600 V (rectifier only) |
| 17 | = | 1700 V |

***6*** IGBT chip technology

| | | |
|---|---|---|
| 6 | = | Trench IGBT3 (600 V and 1200 V) |
| 8 | = | SPT IGBT (1200 V) |
| T4 | = | Trench IGBT4 (1200 V) |

***7*** Appendix (optional)

| | | |
|---|---|---|
| D | = | CAL Diode |
| HD | = | CAL HD Diode |
| s | = | Spring pin version of housing |
| c | = | Six-pack comparable with competitors |
| v1, v2,… | = | Exclusive, customised special version |

# 14 Figure Captions in the Datasheets

## 14.1 IGBT Modules

**Fig. 1** Collector current $I_C$ as a function of the collector- emitter voltage $V_{CE}$ (typical output characteristics) for $T_j$ = 25 °C and $T_j$ = 125 °C, Parameter: Gate-emitter voltage $V_{GE}$; Values at terminal level, including $R_{CC' + EE'}$

**Fig. 2** Maximum rated continuous DC collector current $I_C$ as a function of the case temperature $T_{case}$, terminal current $I_{cmax}$ = 600 A @ $T_{Terminal}$ = 100 °C

**Fig. 3** Typical turn-on and turn-off energy dissipation $E_{on}$ and $E_{off}$ of an IGBT element and turn-off energy dissipation $E_{rr}$ of a freewheeling diode as a function of the continuous collector current $I_C$ for inductive load

**Fig. 4** Typical turn-on and turn-off energy dissipation $E_{on}$ and $E_{off}$ of an IGBT element and turn-off energy dissipation $E_{rr}$ of a freewheeling diode as a function of the gate series resistance $R_G$ for inductive load

**Fig. 5** Typical transfer characteristic: continuous collector current $I_C$ as a function of the gate-emitter voltage $V_{GE;}$ Values at terminal level, including $R_{CC' + EE'}$

**Fig. 6** Typical gate charge characteristic: gate-emitter voltage $V_{GE}$ as a function of the gate charge $Q_G$

**Fig. 7** Typical IGBT switching times $t_{don}$, $t_r$ , $t_{doff}$ and $t_f$ as a function of the continuous collector current $I_C$ for inductive load and fixed gate series resistance $R_G$ for $T_j$ = 125 °C

**Fig. 8** Typical IGBT switching times $t_{don}$, $t_r$ , $t_{doff}$ and $t_f$ as a function of the gate series resistance $R_G$ for inductive load and fixed collector current $I_C$ for $T_j$ = 125 °C

**Fig. 9** Transient thermal impedance $Z_{th(j-c)}$ of the IGBT element and the diode element as single pulse expired following an abrupt change in power dissipation

**Fig. 10** Typical forward characteristics of the inverse diode (typical and maximum values) for $T_j$ = 25 °C and $T_j$ = 125 °C

**Fig. 11** Typical peak reverse recovery current $I_{RRM}$ of the inverse diode as a function of the fall rate $di_F/dt$ of the forward current with corresponding gate series resistance $R_G$ of the IGBT during turn-on

**Fig. 12** Typical recovery charge $Q_{rr}$ of the inverse diode as a function of the fall rate $di_F/dt$ of the forward current (Parameters: forward current $I_F$ and gate series resistance $R_G$ of the IGBT during turn-on)

## 14.2 Thyristor/Diode and Rectifier Modules

**Fig. 1 L** Mean power dissipation $P_{TAV}$ ($P_{FAV}$) of a single thyristor (diode) as a function of the mean on-state (forward) current $I_{TAV}$ ($I_{FAV}$) for DC-current (cont.), sinusoidal half waves (sin.180) and square-wave pulses (rec.15…180).

**Fig. 1 R** Maximum permissible power dissipation $P_{TAV}$ ($P_{FAV}$) as a function of the ambient temperature $T_a$ (temperature of the cooling air flow) for the total thermal resistance (junction to ambient air) $R_{th(j-a)}$ (typical values).

**Fig. 2 L** Total power dissipation $P_{TOT}$ of a SEMiX thyristor module used in an AC-controller application (W1C AC-converter) as a function of the maximum rated root mean square current $I_{RMS}$ at full conduction angle (typical values).

**Fig. 2 R** Maximum permissible power dissipation $P_{TOT}$ and resultant case temperature $T_c$ as a function of the ambient temperature $T_a$, plotted for different values of the thermal resistance $R_{th(c-a)}$ (case to ambient air). For the power dissipation given on the left vertical axis the corresponding case temperatures on the right vertical axis are not to be exceeded.

**Fig. 3 L** Total power dissipation $P_{TOT}$ of two SEMiX thyristor/diode modules in a two-pulse bridge connection (B2C) as a function of the direct output current $I_D$ either for resistive (R) or inductive (L) load. For thyristor modules the curve for operation at full conduction angle is shown (typical values).

**Fig. 3 R** Maximum permissible power dissipation $P_{TOT}$ and resultant case temperature $T_c$ as a function of the ambient temperature $T_a$, plotted for different values of the thermal resistance $R_{th(c-a)}$ (case to ambient). For the power dissipation given on the left vertical axis the corresponding case temperatures on the right vertical axis are not to be exceeded.

**Fig. 4 L** Total power dissipation $P_{TOT}$ of one SEMiX bridge rectifier module or three SEMiX thyristor/diode modules in a six-pulse bridge connection (B6C) as a function of the direct output current $I_D$. For a possible AC-controller connection (W3C) the total power dissipation is plotted over the root mean square current $I_{RMS}$. For thyristor modules the curves for operation at full conduction angle are shown (typical values).

**Fig. 4 R** Maximum permissible power dissipation $P_{TOT}$ and resultant case temperature $T_c$ as a function of the ambient temperature $T_a$, plotted for different thermal resistance values $R_{th(c-a)}$ (case to ambient). For the power dissipation given on the left vertical axis the corresponding case temperatures on the right vertical axis are not to be exceeded.

**Fig. 5** Typical recovery charge $Q_{rr}$ for the max. permissible junction temperature as a function of the rate of fall of the forward current $-di_T/dt$ and the peak on-state current $I_{TM}$ before commutation,

**Fig. 6** Transient thermal impedances $Z_{th(j-c)}$ (junction to case) and $Z_{th(j-s)}$ (junction to sink) for a single thyristor/diode chip as a function of the time t elapsed after a step change in power dissipation.

**Fig. 7** Forward characteristics: on-state voltage $V_T$ (forward voltage $V_F$) as a function of the on-state current $I_T$ (forward current $I_F$); typical and maximum values for $T_{vj}$=25°C and $T_{vjmax}$.

**Fig. 8** Surge current characteristics: ratio of the permissible overload on-state current $I_{T(OV)}$ ($I_{F(OV)}$) to the surge on-state current $I_{TSM}$ ($I_{FSM}$) as a function of the load period t and the ratio of $V_R$ / $V_{RRM}$ , where $V_R$ denotes the reverse voltage applied between the sinusoidal half waves and $V_{RRM}$ is the peak reverse voltage.

**Fig. 9** Thyristor modules only: gate voltage $V_G$ as a function of the gate current $I_G$, indicating the regions of possible (BMZ) and certain (BSZ) triggering for various virtual junction temperatures $T_{vj}$. The current and voltage values of the triggering pulses must lie within the range of certain (BSZ) triggering, but must not exceed the peak pulse power $P_G$ given for the pulse duration $t_p$. Curve 20 V; 20Ω is the output characteristic of suitable trigger equipment.

# 15 Disclaimer

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