

RE01 Group Products with 1.5-Mbyte Flash Memory

R01DS0363EJ0110

Renesas Microcomputers

Rev.1.10

64 MHz, 32-bit Arm® Cortex®-M0+, 1.5-Mbyte flash memory supporting background operation,

May 29, 2020

256-Kbyte SRAM, energy harvesting control circuit, MIP LCD controller, 2D graphic engine,

14-bit ultra-low power A/D converter, reference voltage generation circuit, RTC, sub-clock correction circuit

(theoretical regulation), security function (optional), USB 2.0 full-speed module, SPI, quad SPI

Features

■ Arm® Cortex®-M0+ core incorporated

- Maximum operating frequency: 64 MHz (boost mode)
- ARM® Memory Protection Unit (MPU)
- CoreSight™ debug port: SW-DP

■ Power-saving functions

- Back-bias control function based on silicon-on-thin-buried-oxide (SOTB™) process technology
- Operation at ultra-low power-supply voltages (from 1.62 V to 3.6 V)
- Four power control modes based on the operating frequency
- Four low power consumption modes
- Three power supply modes

■ On-chip code flash memory

- 1.5-Mbyte code flash memory
- Background programming/erasing
- No cycles of waiting for access in operation at or below 32 MHz; one cycle of waiting at frequencies above 32 MHz
- Function for area protection prevents erroneous overwriting or tampering

■ On-chip SRAM

- 256-Kbyte SRAM with no access wait cycles

■ Data transfer

- Four DMA controllers
- Single data transfer controller (DTC)

■ Reset and supply management

- Power-on reset circuit (POR)
- Low voltage detection (LVD) can be set.

■ Multiple clock sources

- External crystal oscillator (main clock): 8 to 32 MHz
- External crystal oscillator (sub-clock): 32.768 kHz
- High-speed on-chip oscillator (HOCO): 24, 32, 48, or 64 MHz
- Middle-speed on-chip oscillator (MOCO): 2 MHz
- Low-speed on-chip oscillator (LOCO): 32 kHz
- Independent watchdog timer on-chip oscillator: 16 kHz
- PLL frequency synthesizer

■ Energy harvesting control

- A power generation element is directly connectable.
- High-speed startup is possible without having to wait for the charging of a secondary battery.
- Function to prevent a secondary battery from overcharging

■ Independent watchdog timer

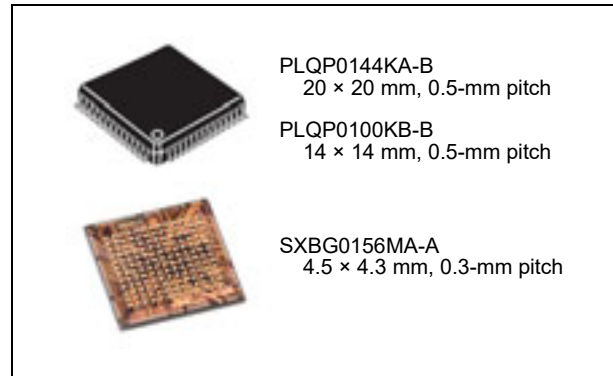
- 14-bit counter, 16-kHz (1/2 LOCO clock frequency) operation

■ Sub-clock correction circuit (CCC)

- The CCC corrects the accuracy of oscillation every 16 seconds (theoretical regulation).
- Events can be generated per second in deep software standby mode.

■ Communication functions

- Single USB 2.0 full-speed host/function module with PHY layer
- Two serial peripheral interfaces
- Single 128-bit buffer for which up to eight commands can be specified
- Single 32-bit buffer for which one command can be specified
- Single quad serial peripheral interface connectable to an external flash memory
- Two I²C bus interfaces
- Five serial communications interfaces (SCIg)
- Asynchronous, clock-synchronous, simple I²C, simple SPI, and smart card interfaces, and IrDA interface version 1.0 (the latter is only applicable to SCI0)
- Two serial communication interfaces (SCi) each having a 16-byte FIFO



■ Various analog circuits

- Single 14-bit successive approximation A/D converter
- High precision: 7 channels, standard precision: 11 channels
- Single 12-bit D/A converter with a buffer amplifier
- Single analog comparator (ACMP)
- Single temperature sensor for measuring the internal temperature of the chip
- Reference voltage generation circuit for the 14-bit A/D converter
- Single motor driver control circuit (MTDV)
- The MTDV can drive up to three motors.
- Single constant current (1 mA or 0.5 mA) source circuit with three channels that can drive three external LEDs

■ Various timer circuits

- Six general PWM timers (GPT)
- Two 32-bit counters
- Four 16-bit counters
- Two asynchronous general-purpose timers (AGT) that can be used in standby mode
- Two 8-bit timers (TMR)
- Single realtime clock (RTC)
- Single watchdog timer (WDT)
- Single low-speed timer (LST) that operates at 1 kHz
- A circuit for converting hexadecimal numbers to decimal numbers for use as a stopwatch
- Single low-speed pulse generator (LPG)
- Pulse output at two frequencies (2.048 or 4.096 kHz) is possible.

■ Human machine interfaces

- Single memory-in-pixel (MIP) LCD controller (MLCD)
- Parallel interface is supported.
- Single 2D graphics data conversion circuit (GDT)

■ Security functions (optional)

- Single Trusted Secure IP Lite (TSIP-Lite)
 - AES (128- or 256-bit key length, supporting ECB, CBC, CMAC, GCM, and others)
 - Key wrapping protects against the leakage of the encryption keys of users.
 - An access management circuit disables illicit access to the encryption engine.
 - Using the other security functions together with area protection enables secure booting and secure over-the-air (OTA) software updates.

■ Operating voltage and temperature range

- VCC = IOVCC = 1.62 V to 3.6 V
- IOVCCn and AVCCn can each be independently set to a voltage within the range between 1.62 V and 3.6 V.
- T_a: -40 to +85°C

1. Overview

1.1 Outline of Specifications

Table 1.1 shows the specifications in outline.

The specifications in the table are the maximum specifications, and the number of peripheral modules and channels in some cases depends on the number of pins of the package. For details, see Table 1.3, Function Comparison.

Table 1.1 Outline of Specifications (1/10)

Classification	Feature	Description
CPU	Central processing unit	<ul style="list-style-type: none"> Maximum operating frequency: 64 MHz Arm® Cortex®-M0+ <ul style="list-style-type: none"> - Revision: r0p1-00rel0 - Arm®v6-M architecture profile - Single-cycle integer multiplier Arm® Memory Protection Units (MPUs) <ul style="list-style-type: none"> - Arm®v6 Protected Memory System Architecture - Eight protected memory areas SysTick timer <ul style="list-style-type: none"> - Driven by SYSTICCLK (LOCO clock) or ICLK
Memory	Code flash memory	<ul style="list-style-type: none"> Maximum 1.5 Mbytes No cycles of waiting for access in operation at or below 32 MHz; one cycle of waiting at frequencies above 32 MHz Prefetch function On-board programming (four types): <ul style="list-style-type: none"> - Programming in serial programming mode (SCI boot mode) - Programming in serial programming mode (USB boot mode) - Programming in on-chip debug mode - Programming by a routine for code flash memory programming within a user program
	SRAM	<ul style="list-style-type: none"> Maximum 256 Kbytes SRAM0: 2000 0000h to 2000 7FFFh SRAM1: 2000 8000h to 2003 FFFFh Both areas are available during low leakage current mode. 64 MHz, No cycles of waiting for access
Startup modes		Three startup modes: <ul style="list-style-type: none"> Normal startup mode Energy harvesting startup mode SCI/USB boot mode
Reset		The LSI chip supports 12 system resets and one power shutdown reset. [System resets] <ul style="list-style-type: none"> RES# pin reset Power-on reset Independent watchdog timer reset Watchdog timer reset Voltage monitor 0 reset Voltage monitor 1 reset Voltage monitor BAT reset Bus master MPU error reset Bus slave MPU error reset Stack pointer error reset Software reset Deep software standby reset [Power shutdown reset] <ul style="list-style-type: none"> MINPWON mode reset

Table 1.1 Outline of Specifications (2/10)

Classification	Feature	Description
Low-voltage detection circuits (LVD)		<p>The low-voltage detection circuits (LVD) monitors the voltage level input to the VCC pin or VBAT_EHC pin. The detection level can be selected using a program.</p> <ul style="list-style-type: none"> • Voltage detection circuit 0 <ul style="list-style-type: none"> - Target for monitoring: VCC pin - Capable of generating an internal reset - The option-setting memory can be used to enable or disable the low-voltage detection circuit. - Selectable from four different voltage detection levels (1.67 V, 1.92 V, 2.17 V, and 2.42 V) • Voltage detection circuit 1 <ul style="list-style-type: none"> - Target for monitoring: VCC pin - The register setting can be used to enable or disable the low-voltage detection circuit. - Selectable from eight different voltage detection levels (1.67 V, 1.84 V, 2.00 V, 2.17 V, 2.33 V, 2.50 V, 2.66 V, and 2.83 V) - Digital filtering is available (1/2, 1/4, 1/8, and 1/16 LOCO frequency). - Detection of voltage rising above and falling below thresholds is selectable. - Capable of generating an internal reset - Two types of timing are selectable for release from reset. - An internal interrupt can be requested. - A maskable or non-maskable interrupt is selectable. - Voltage detection monitoring is available. - Event linking is available. • Voltage detection circuit BAT <ul style="list-style-type: none"> - Target for monitoring: VBAT_EHC pin - The register setting can be used to enable or disable the low-voltage detection circuit. - Selectable from five different voltage detection levels (1.67 V, 1.84 V, 2.00 V, 2.17 V, and 2.33 V) - Digital filtering is available (1/2, 1/4, 1/8, and 1/16 LOCO frequency). - Detection of voltage rising above and falling below thresholds is selectable. - Capable of generating an internal reset - Two types of timing are selectable for release from reset. - An internal interrupt can be requested. - A maskable or non-maskable interrupt is selectable. - Voltage detection monitoring is available.
Clock		<ul style="list-style-type: none"> • The LSI chip has the following clock generation circuits. <ul style="list-style-type: none"> - Main clock oscillator (MOSC) - Sub-clock oscillator (SOSC) - High-speed on-chip oscillator (HOCO) - Middle-speed on-chip oscillator (MOCO) - Low-speed on-chip oscillator (LOCO) - PLL frequency synthesizer - IWDI-dedicated on-chip oscillator (IWDILOCO) • Clock output support <ul style="list-style-type: none"> - CLKOUT pin (capable of the output of all types of clock signals) - CLKOUT32K pin (capable of the output of the SOSC clock signal)

Table 1.1 Outline of Specifications (3/10)

Classification	Feature	Description
Clock frequency accuracy measurement circuit (CAC)		<p>The CAC checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. Event signals can be generated when the frequency does not match or measurement ends. This function is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications.</p> <ul style="list-style-type: none"> • Target clocks for measurement <ul style="list-style-type: none"> - Main clock - Sub-clock - HOCO clock - MOCO clock - LOCO clock - CCC2K clock - IWDI-dedicated clock - Peripheral module clock B (PCLKB) • Reference clocks for measurement <ul style="list-style-type: none"> - External clock input to the CACREF pin - Main clock - Sub-clock - HOCO clock - MOCO clock - LOCO clock - CCC2K clock - IWDI-dedicated clock - Peripheral module clock B (PCLKB) • Digital filtering is selectable.
Low power consumption	Power-saving functions	<p>The LSI chip has several functions for power saving, such as setting clock dividers, stopping modules, selecting power control mode in operating mode, transitioning to low power consumption mode, and power supply mode per domain.</p> <ul style="list-style-type: none"> • Three power control modes based on the operating frequency <ul style="list-style-type: none"> - Boost mode (up to 64 MHz) - Normal mode - High-speed mode (up to 32 MHz) - Low-speed mode (up to 2 MHz) - Subosc-speed mode (this LSI chip can be placed in the low leakage current mode at 32.768 kHz.) - Low leakage current mode (32.768 kHz) • Five low-power consumption modes <ul style="list-style-type: none"> - Operating mode - Sleep mode - Software standby mode - Snooze mode - Deep software standby mode • Three power supply modes <ul style="list-style-type: none"> - All-power supply mode (ALLPWON) - Flash-excluded power supply mode (EXFPWON) - Minimum power supply mode (MINPWON)
	Back-bias voltage control*1 (VBBC) function	Program control of the back bias voltage enables low leakage current operation in the low leakage current mode.
Energy harvesting control circuit (EHC)		Starting up of this LSI chip in the power-saving mode is possible by controlling the power generating element, storage capacitor, and secondary battery.
Register write protection (RWP)		The register write protection function protects important registers from rewrites caused by software errors.
Memory protection units (MPUs) and stack pointer monitors		<ul style="list-style-type: none"> • Illicit memory access <ul style="list-style-type: none"> - CPU (attempt at access to an undefined address space) - CPU stack pointer monitors: Two regions • Memory protection <ul style="list-style-type: none"> - Arm® MPU: Eight areas - Bus master MPU: Four areas - Bus slave MPU • Security <ul style="list-style-type: none"> - Security MPU: Two secure program areas Three secure data areas (code flash memory, SRAM, and TSIP-Lite)

Table 1.1 Outline of Specifications (4/10)

Classification	Feature	Description
Interrupt	Interrupt controller unit (ICU)	<ul style="list-style-type: none"> Peripheral function interrupts: 168 sources External interrupts: 10 sources (pins IRQ0 to IRQ9) Non-maskable interrupts: Nine sources DMAC and DTC control: The DMAC and DTC can be activated by interrupt sources. Interrupts for NVIC: 32 sources
Key interrupt function (KINT)		An interrupt can be generated by inputting a rising or falling edge to the key interrupt input pins.
External bus		<ul style="list-style-type: none"> QSPI area: Connectable to the QSPI (external device interface)
DMA	Data transfer controller (DTC)	<ul style="list-style-type: none"> Transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: External interrupts and interrupt requests from peripheral functions Transfer channels: Multiple data units can be transferred on a single activation source (chain transfer).
	DMA controller (DMAC)	<p>A 4-channel DMA controller (DMAC) module is incorporated for transferring data without CPU intervention. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.</p> <ul style="list-style-type: none"> Transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
Event link controller (ELC)		The ELC uses the interrupt requests generated by various peripheral modules as event signals and connects them to different modules. This enables modules to function in combination with each other without CPU intervention.
Timers	General PWM timer (GPT)	<ul style="list-style-type: none"> Two 32-bit counters (GPT32), and four 16-bit counters (GPT16) Up-counting or down-counting (saw waves) or up-counting or down-counting (triangle waves) is selectable for each counter. Two input/output pins per channel Two output compare/input capture registers per channel For the two output compare/input capture registers of each channel, four buffer registers are provided and are capable of operating as comparison registers when buffering is not in use. In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) Generation of dead times in PWM operation Synchronous starting, stopping and clearing counters for arbitrary channels Based on the ELC settings, up to four ELC events can start or stop counting, clear the counter, drive counting up or down, or trigger input capture. The states of two input pins can be detected to start or stop counting, clear the counter, drive counting up or down, or trigger input capture. Up to two external triggers can start or stop counting, clear the counter, drive counting up or down, or trigger input capture. Output pin disable function in response to detecting short-circuits between output pins PWM waveforms for controlling brushless DC motors can be generated. Compare match A to D events, overflow or underflow events and input UVW edge events can be output to the ELC. A noise filter can be used for input capture input and hall sensor input.
	Port output enable for GPT (POE)	<ul style="list-style-type: none"> Output disabling in response to detection of the input level on the GTETRn pin Output disabling in response to a request from the GPT. Output disabling in response to detection of stopped oscillation. Output disabling in response to an ACMP interrupt request. Output disabling in response to software register settings. The GTETRn signals can be output to the GPT as external trigger signals after polarity and filter selection. An input filter can be used for the GTETRn pin.

Table 1.1 Outline of Specifications (5/10)

Classification	Feature	Description
Timers	Asynchronous general-purpose timer (AGT)	<p>The asynchronous general-purpose timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events.</p> <ul style="list-style-type: none"> • Two channels • Support for five operating modes <ul style="list-style-type: none"> - Timer mode - Pulse output mode - Event counter mode - Pulse width measurement mode - Pulse period measurement mode • The AGT supports the interrupt and event link functions for three sources, and the chip can return from software standby mode. <ul style="list-style-type: none"> - Underflow event signal/measurement complete event signal - Compare match A event signal - Compare match B event signal
	8-bit timers (TMR)	<ul style="list-style-type: none"> • (8 bits × 2 channels) × 1 unit • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal. • Capable of output of pulse with desired duty cycles or of PWM signals • The two channels can be cascaded to create a 16-bit timer. • Conversion start trigger for the 14-bit A/D converter can be generated. • Support of function for event linking by the ELC
	Realtime clock (RTC)	<p>The RTC has two counting modes: a calendar count mode and a binary count mode. These modes are controlled by the register settings.</p> <p>For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years.</p> <p>For binary count mode, the RTC counts seconds and retains the information as a serial value.</p> <p>Binary count mode can be used for calendars other than the Gregorian (western) calendar.</p> <ul style="list-style-type: none"> • Clock source: Sub-clock oscillator • Counting by either clock counters or 32-bit binary counters in second units is selectable. • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time capture function • Support of function for event linking by the ELC
	Clock correction circuit (CCC)	<p>The CCC corrects the oscillation accuracy every 16 seconds for the sub-clock (32.768 kHz).</p> <ul style="list-style-type: none"> • Clock output after correction: 2.048 kHz or 512 Hz • Signal output (CCCOUT): Selectable from 512 Hz, 1 Hz, and RTC output (1 Hz or 64 Hz) • Support of function for event linking by the ELC

Table 1.1 Outline of Specifications (6/10)

Classification	Feature	Description
Timers	Watchdog timer (WDT)	<p>The WDT can be used to reset the LSI chip when the system runs out of control. A non-maskable interrupt or interrupt can be generated by an underflow of the counter.</p> <ul style="list-style-type: none"> • 14 bits × 1 channel • Count clock (WDTCLK): Selectable from PCLKB and CCC_2K • Selectable counter clock signal: 6 types (WDTCLK/4, WDTCLK/64, WDTCLK/128, WDTCLK/512, WDTCLK/2048, WDTCLK/8192).
	Independent watchdog timer (IWDG)	<p>The IWDG is a 14-bit down-counter and operates with the clock (IWDGCLK) that is independent of the clock used by the system. It can reset the LSI chip if the system runs out of control. The IWDG provides functionality to reset the LSI chip or to generate a non-maskable interrupt or interrupt on a counter underflow.</p> <ul style="list-style-type: none"> • 14 bits × 1 channel • Counter-input clock: IWDGLOCO • IWDGLOCO/1, IWDGLOCO/16, IWDGLOCO/32, IWDGLOCO/64, IWDGLOCO/128, IWDGLOCO/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Support of function for event linking by the ELC
	Low-speed clock timer (LST)	<p>The low-speed clock timer (LST) is a 13-bit timer that consists of a 1-kHz timer-counter and a circuit for converting hexadecimal numbers to decimal numbers. The LST can be used to indicate a count that needs to be displayed in decimal.</p> <ul style="list-style-type: none"> • Capable of counting from 0.000 to 1.999 seconds (in units of 0.001 seconds) • The counted value can be directly stored in a register in decimal notation.
	Low-speed pulse generator (LPG)	<p>The LPG is a simple 4-bit timer that operates with a 32-kHz clock (SOSC clock, LOCO clock).</p> <ul style="list-style-type: none"> • Two types of pulse output are possible (4.096 kHz and 2.048 kHz). • Two duty cycles are selectable (1/4, 1/2).
	Motor driver control circuit (MTDV)	<p>The MTDV can drive up to three motors.</p> <ul style="list-style-type: none"> • Two-signal waveform output (three modes: PM1/PM2/PM3) • Three-signal waveform output (two modes: PM5/PM6) • Rotation detection function (PM1 mode only) • Polarity reversal function • Forward-/reverse-rotation control function • Support of function for event linking by the ELC

Table 1.1 Outline of Specifications (7/10)

Classification	Feature	Description
Communications interfaces	Serial communications interfaces (SCIg, SCli)	<p>Without FIFO (SCIg) × 5 channels, with FIFO (SCli) × 2 channels</p> <p>The SCI is configurable for five asynchronous and synchronous serial interfaces.</p> <ul style="list-style-type: none"> Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) 8-bit clock-synchronous interface Simple I²C (master-only) Simple SPI Smart card interface <p>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.</p> <p>SCI0 and SCI1 have 16-byte FIFO buffers to enable continuous and full-duplex communications.</p> <p>The data transfer speed can be configured independently using an on-chip baud rate generator.</p> <ul style="list-style-type: none"> Selectable as LSB-first or MSB-first transfer Support of function for event linking by the ELC (SCI2 only)
	IrDA interface (IrDA)	The IrDA interface sends and receives IrDA data communications waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0.
	I ² C bus interface (RIIC)	<p>The RIIC conforms with and provides a subset of the NXP I²C bus (Inter-Integrated Circuit bus) interface functions.</p> <ul style="list-style-type: none"> I²C bus format or SMBus format Two channels Master or slave selectable Automatic securing of the setup times, hold times, and bus-free times for the multi-master transfer rate Support of function for event linking by the ELC
	Serial peripheral interface (SPI)	<p>The SPI can handle high-speed and full-duplex synchronous serial communications with multiple processors and peripheral devices.</p> <ul style="list-style-type: none"> Up to eight commands/128-bit buffer × 1 channel (SPI0) One command/32-bit buffer × 1 channel (SPI1) Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). Transmit-only operation is available. Switching of RSPCK polarity Switching of RSPCK phase MSB-first or LSB-first selectable Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits 128-bit (SPI0) or 32-bit (SPI1) transmit and receive buffers Up to four frames can be transferred in one round of transmission or reception (each frame consisting of up to 32 bits). Double buffer configuration for the transmission and reception buffers Support of function for event linking by the ELC Communications with the MIP LCD controller of the three-wire serial type are possible (SPI0 only).
	Quad serial peripheral interface (QSPI)	<p>The QSPI is connectable to a serial ROM that has an SPI-compatible interface.</p> <ul style="list-style-type: none"> 1 channel Support for extended SPI, dual SPI, and quad SPI protocols Configurable to SPI mode 0 and SPI mode 3 Address width selectable from 8, 16, 24, or 32 bits.

Table 1.1 Outline of Specifications (8/10)

Classification	Feature	Description
Communications interfaces	USB 2.0 FS host/function module (USB)	<p>Full-speed USB controller that can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0.</p> <p>The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communications or based on your system.</p> <ul style="list-style-type: none"> • USB device controller (UDC) and USB 2.0 transceiver supporting host controller, device controller, and On-The-Go (OTG) functions (one channel) • Host and device controllers can be switched by the software. • Self-power mode or bus power mode can be selected. • When the host controller function is selected: Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • When the device controller function is selected: Full-speed transfer (12 Mbps)
Analog	14-bit A/D converter (S14AD)	<p>A 14-bit successive approximation A/D converter incorporated</p> <p>Up to 18 analog input channels are selectable. The analog input channels and the temperature sensor output are selectable for conversion. The A/D conversion accuracy is selectable between 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value.</p> <ul style="list-style-type: none"> • 14 bits × 18 channels (maximum value) (high accuracy: 7 channels, standard accuracy: 11 channels) • Resolution: 14 bits (14-bit or 12-bit conversion selectable) • Operating mode: <ul style="list-style-type: none"> Scan mode (single-scan mode, continuous-scan mode, or group-scan mode) • Group A priority control (only for group-scan mode) • Variable sampling state count • A/D-converted value addition mode or average mode selectable • Disconnection detection assist function • Double-trigger mode (duplication of A/D conversion data) • Support of function for event linking by the ELC • Automatic clear function of A/D data registers • Compare function for window A and window B • Digital compare function <ul style="list-style-type: none"> Comparison of values in the comparison register and the data register, and comparison between values in the data registers
	12-bit D/A converter (R12DA)	<p>A 12-bit D/A converter with an output amplifier incorporated</p> <ul style="list-style-type: none"> • 12 bits × 1 channel • Resolution: 12 bits • Support of function for event linking by the ELC
	Temperature sensor (TEMPS)	<p>The temperature sensor outputs the voltage that is directly proportional to the die temperature.</p> <p>The output voltage is converted to a digital value by the S14AD for conversion and can be further used by the end application.</p>
	Analog comparator (ACMP)	<p>The ACMP can be used to compare a reference input voltage and analog input voltage.</p> <ul style="list-style-type: none"> • 1 channel × 1 unit • Analog input: Input from the CMPIN pin • Reference voltage: Input from the CMPREF pin • Whether to use a noise filter and a sampling clock frequency can be selected.
	LED driver (LED)	<p>The LSI chip has a constant current source circuit that can drive three external LED channels.</p> <ul style="list-style-type: none"> • 3 channels × 1 unit • Output constant current: 1.0 mA (LED load: 1.4 kΩ), 0.5 mA (LED load: 2.8 kΩ) • Constant current temperature characteristics: 2000 ppm/°C (T_a = -20°C to 60°C)
	Reference voltage generation circuit (VREF)	<p>The circuit generates two types (1.25 V/2.5 V) of reference voltage.</p> <p>The generated voltage can be used as the reference voltage for the ADC.</p>

Table 1.1 Outline of Specifications (9/10)

Classification	Feature	Description
Human machine interfaces (HMI)	MIP LCD controller (MLCD)*2	MIP-method liquid crystal panel driver circuit incorporated
	2D graphics data conversion circuit (GDT)	<p>A graphic accelerator circuit that handles 2D image processing incorporated</p> <ul style="list-style-type: none"> • Handling of up to 32-byte image data. Up to 63 × 64 bits for conversion of glyph data into image data. • Rotations of 90-degree clockwise, 90-degree counterclockwise, vertical flip, and horizontal flip • Scaling down to 1/8, 2/8, 3/8, 4/8, 5/8, 6/8, or 7/8 by pixel averaging and to 1/2 by pixel skipping • Inversion allows bit-wise inversion of images; 1 is inverted to 0, and vice versa. • Monochrome compositing of a foreground image, background image, and trimming image • Color compositing of a foreground image and background image, and setting of priority color and transparent color • Scrolling of an image in 1-bit units • Conversion of glyph data into image data • Colorization of monochrome images by RGB values • Color data sorting allows separate R, G, and B images in memory to be sorted into a single area in order of R, G, and B. • Endian conversion
Data processing	Cyclic redundancy check (CRC) calculator	<p>The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communications. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require the CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.</p> <ul style="list-style-type: none"> • CRC code generated for any data in 8-bit/32-bit units • 8-bit data: One of three polynomials selectable [8-bit CRC] $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] $X^{16} + X^{15} + X^2 + 1$ (CRC-16) $X^{16} + X^{12} + X^5 + 1$ (CRC-16-CCITT) • 32-bit data: One of two polynomials selectable [32-bit CRC] $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) • The bit order of CRC calculation results can be switched for LSB- or MSB-first communications.
	Data operation circuit (DOC)	The DOC compares, adds, and subtracts 16-bit data.
	Divider (DIV)	<p>A circuit for handling high-speed division for signed 32-bit fixed point data</p> <ul style="list-style-type: none"> • Dividend: Signed 32-bit data • Divisor: Signed 32-bit data
	Data inversion circuit (DIL)	A circuit for inverting the values of input data is integrated.
Security	Trusted secure IP lite (TSIP-Lite)	<ul style="list-style-type: none"> • Access management circuit available • Security algorithms: <ul style="list-style-type: none"> - Common key cryptosystem (symmetrical cryptography): AES key length: 128 bits/256 bits - Encryption usage modes: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR, CCM • Other support features: <ul style="list-style-type: none"> - TRNG (true random number generation circuit) - Hash value generation: GHASH - Support for unique IDs (128-bit unique IDs)
Operating frequency		<p>Up to 32 MHz (normal mode) Up to 64 MHz (boost mode) Up to 32 kHz (low leakage current mode)</p>

Table 1.1 Outline of Specifications (10/10)

Classification	Feature	Description
Power supply voltages		VCC = IOVCC = 1.62 to 3.6 V, IOVCC0 = 1.62 to 3.6 V, IOVCC1 = 1.62 to 3.6 V, IOVCC2 = 1.62 to 3.6 V, IOVCC3 = 1.62 to 3.6 V, AVCC0 = 1.62 to 3.6 V, AVCC1 = 1.62 to 3.6 V, VCC_USB = 3.0 to 3.3 V, $1.62\text{ V} \leq \text{VREFH0} \leq \text{AVCC0}$
Operating ambient temperature		−40 to +85°C
Package		156-pin WLBGA (SXBG0156MA-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin LFQFP (PLQP0100KB-B)
On-chip debugging system		<ul style="list-style-type: none"> • Debug and trace: DWT, BPU, CoreSight™ MTB-M0+ • CoreSight debug port: SW-DP

Note 1. Voltage for charging the VBP and VBN pins

Note 2. General three-wire MIP can be supported by combining SPI0 and GDT.

1.2 Block Diagram

Figure 1.1 is a block diagram of this chip. Some individual devices within the group may have a subset of the features shown.

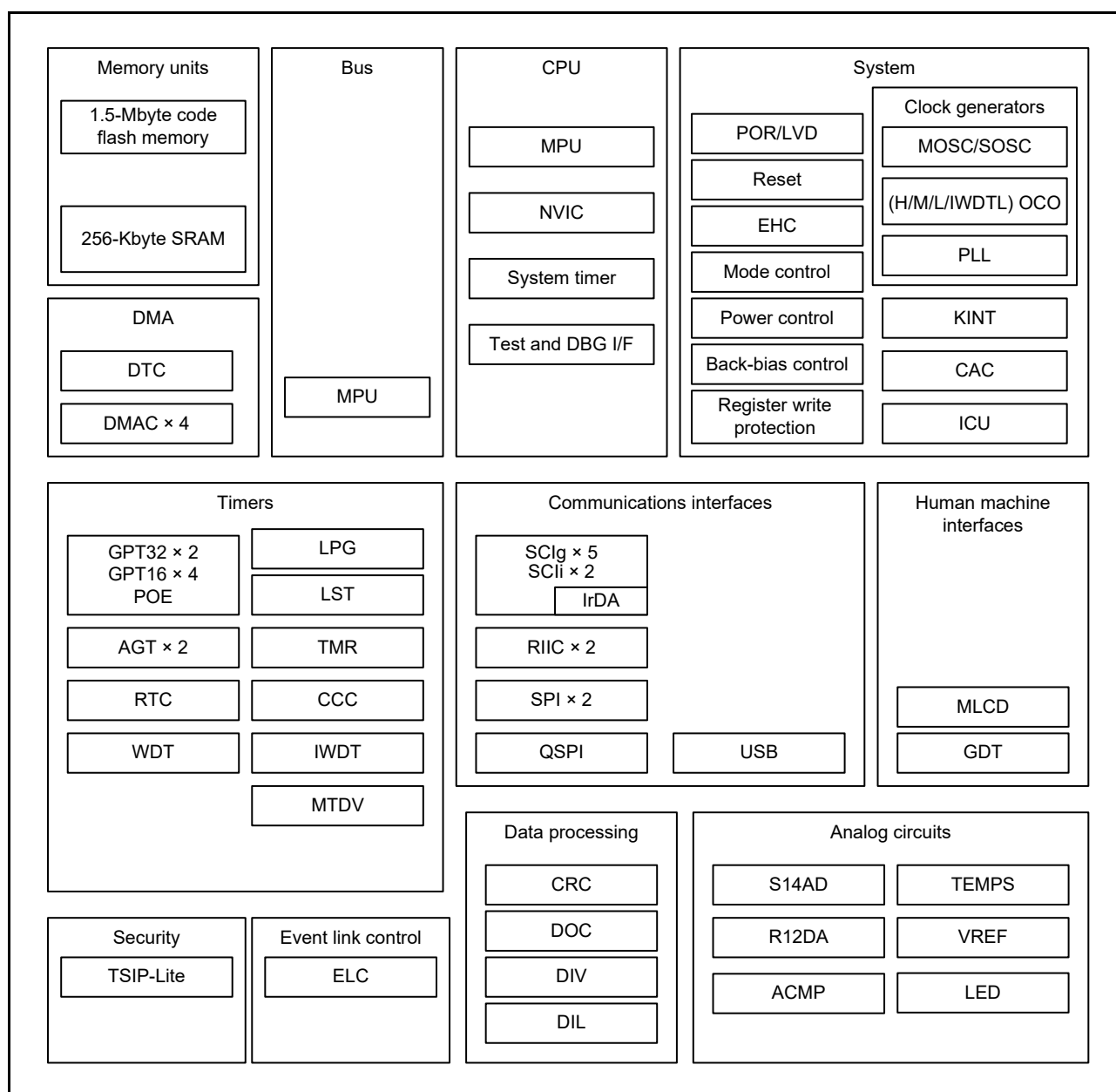


Figure 1.1 Block Diagram

1.3 List of Products

Table 1.2 List of Products

Part Number	Package	Code Flash Memory Capacity	SRAM Capacity	Support Status			
				USB	TSIP-Lite	MLCD	MTDV
R7F0E017D2DBN	SXBG0156MA-A	1.5 Mbytes	256 Kbytes	Supported	Supported	Supported	Supported
R7F0E016D2DBN	SXBG0156MA-A	1.5 Mbytes	256 Kbytes	Supported	Not supported	Supported	Supported
R7F0E015D2CFB	PLQP0144KA-B	1.5 Mbytes	256 Kbytes	Supported	Supported	Supported	Not supported
R7F0E014D2CFB	PLQP0144KA-B	1.5 Mbytes	256 Kbytes	Supported	Not supported	Supported	Not supported
R7F0E015D2CFP	PLQP0100KB-B	1.5 Mbytes	256 Kbytes	Supported	Supported	Supported	Not supported
R7F0E014D2CFP	PLQP0100KB-B	1.5 Mbytes	256 Kbytes	Supported	Not supported	Supported	Not supported

1.4 Function Comparison

Table 1.3 shows function comparison among products.

Table 1.3 Function Comparison (1/2)

Part Number			R7F0E017D2DBN	R7F0E016D2DBN	R7F0E015D2CFB	R7F0E014D2CFB	R7F0E015D2CFP	R7F0E014D2CFP
Total pin count			156		144		100	
Number of general-purpose I/O port pins	I/O port pins		102		109		66	
	Input port pin		1		1		1	
Package			WLBGA		LFQFP			
Code flash memory			1.5 Mbytes					
SRAM			256 Kbytes					
CPU operating frequency			32 MHz (normal mode) 64 MHz (boost mode) 32 kHz (low leakage current mode)					
Interrupt control	ICU		Yes					
	IRQ		Channels 0 to 9					
Key interrupt	KINT		8 channels					
DMA	DTC		Yes					
	DMAC		Channels 0 to 3					
Event control	ELC		Yes					
Energy harvesting	EHC		Yes					
Back-bias voltage control	VBBC		Yes					
Timers	GPT32		Channels 0 and 1					
	GPT16		Channels 2 to 5					
		POE	Yes					
	AGT		Channels 0 and 1					
	TMR		Channels 0 and 1					
	RTC		Yes					
	CCC		Yes					
	WDT		Yes					
	IWDT		Yes					
	MTDV		Yes (3 channels)		No			
	LST		Yes					
	LPG		Yes					
Communications function	SCIg	w/o FIFO	Channels 2 to 5, 9					
	SCLi	w/ FIFO	Channels 0 and 1					
		IrDA	Yes					
	RIIC		Channels 0 and 1					
	SPI	128-bit buffer	Channel 0					
		32-bit buffer	Channel 1					
	QSPI		Yes					
	USB		Yes					
Analog	S14AD	High precision	7 channels					
		Standard precision	11 channels				5 channels	
	R12DA		Yes (1 channel)					
	TEMPS		Yes (1 channel)					
	ACMP		Yes (1 channel)					
	VREF		Yes (1 channel)					
	LED		Yes				No	

Table 1.3 Function Comparison (2/2)

Part Number		R7F0E017D2DBN	R7F0E016D2DBN	R7F0E015D2CFB	R7F0E014D2CFB	R7F0E015D2CFP	R7F0E014D2CFP
HMI graphics	MLCD	Yes					
	GDT	Yes					
Data processing	CRC	Yes					
	DOC	Yes					
	DIV	Yes					
	DIL	Yes					
Security	TSIP-Lite	Yes	No	Yes	No	Yes	No

1.5 Pin Functions

Table 1.4 lists the pin functions. For details on how to connect smoothing capacitors, refer to examples of their connection shown and described in Appendix B.

Table 1.4 Pin Functions (1/6)

Function	Pin Name		I/O	Description
Power supply	VCC/ IOVCC	Normal startup mode	Input	Power supply pin. Connect it to the system power supply. Connect to VSS through a 0.1- μ F smoothing capacitor. Place the smoothing capacitor close to the pin.* ³ Apply the voltage to this pin before the voltage for the IOVCCn pin.
		Energy harvesting startup mode	Input	Power supply pin. Connect it to the system power supply. Connect to VSS through 0.1- μ F smoothing capacitor (1). Place the smoothing capacitor close to the pin. In addition, connect to VSS through smoothing capacitor (2) having capacity of 1/10 of capacity of a storage capacitor connected to the VCC_SU pin to improve robustness against external noise and obtain stable operation of the circuit. For instance, connect a 4.7- μ F smoothing capacitor in the case where a 47- μ F storage capacitor is connected to the VCC_SU pin. If placing the smoothing capacitor (2) close to this pin is possible, the smoothing capacitor (1) is not required. For more details, see Appendix B. Connecting the Capacitors to the Power Supply Pins.
	VSS		Input	Ground pin. Connect it to the system power supply (0 V).
	VCL		Input	Internal power supply stabilization pin. Connect the pin to VSS through a 4.7- μ F smoothing capacitor. Place the smoothing capacitor close to the pin.
	VCLH		Input	Internal power supply stabilization pin. Separately from the VCL pin, connect the VCLH pin to VSS through a 4.7- μ F smoothing capacitor. Place the smoothing capacitor close to the pin.
	VBN		—	Back-bias voltage stabilization pins. Connect the respective pins to VSS through a 1.0- μ F smoothing capacitor. Place the smoothing capacitor close to the pin.
	VBP		—	
	VSC_VCC	Normal startup mode	Input	Power supply pin supplied from a power generation element. Connect it to the system power supply (0 V) in normal startup mode.
		Energy harvesting startup mode	Input	Power supply pin supplied from a power generation element. Connect this pin to VSC_GND through a smoothing capacitor in parallel with the power generation element. Place the smoothing capacitor close to the pin. While a smoothing capacitor with a capacitance value of 4.7-nF to 47-nF is recommended, select a capacity value suitably in accordance with stability of a power generating element or the like.
	VCC_SU	Normal startup mode	I/O	Power supply pin supplied from a storage capacitor. Short it to VCC/IOVCC in normal startup mode.
		Energy harvesting startup mode	I/O	Power supply pin supplied from a storage capacitor. When using a photovoltaic cell as a power generating element, connect a storage capacitor with a capacitance value in accordance with an operating temperature, and with a value of at least 10 times VCC. A capacitance value of 47 μ F is required at 25°C. As a temperature becomes higher, a larger capacitance value is required. See the EHC characteristics in section 6.13, EHC Characteristics. Connect this pin to a 100- μ F storage capacitor in the case where other power generating elements are used.
	VSC_GND		Input	VSC_VCC ground pin. Connect it to the system power supply (0 V).
	VBAT_EHC	Normal startup mode	Input	Power supply pin supplied from a secondary battery. Connect it to VCC/IOVCC in normal startup mode.
		Energy harvesting startup mode	Input	Power supply pin supplied from a secondary battery. Connect a 2.6-V or 3.0-V secondary battery or a super capacitor in energy harvesting startup mode.

Table 1.4 Pin Functions (2/6)

Function	Pin Name	I/O	Description
Power supply	IOVCCn (n = 0 to 3)	Input	Power supply pin for input/output. Connect the pin to VSS through a 0.1-μF smoothing capacitor. Place the smoothing capacitor close to the pin.*3, *4 This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
Clock	XTAL	Input	Pins for connecting the MOSC resonator EXTAL is an external clock input pin.
	EXTAL	Output	
	XCIN	Input	Pins for connecting the SOSC resonator
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
	CLKOUT32K	Output	SOSC clock output pin
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Startup mode control	MD	Input	Pin for setting the startup mode. The signal level on this pin must not be changed during transition to the specified startup mode after release from the reset state.
	EHMD	Input	Pin for setting the energy harvesting mode
System control	RES#	Input	Reset signal input pin. The LSI chip enters the reset state when this signal goes low.
	BSCANP	Input	IOVCCn pin power supply forced input pin When the boundary scan function is in use, setting this pin to the high level while IOVCCn power is being supplied enables the supply of power to all I/O ports.
Interrupts	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ9, IRQ0_A_DS to IRQ3_A_DS	Input	Maskable interrupt request pins Pins that have "_DS" appended to their names can be used as triggers for release from deep software standby.
KINT	KRM00 to KRM07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
On-chip debugger	SWDIO	I/O	SWD data input/output pin
	SWCLK	Input	SWD clock input pin
Boundary scan	TMS	Input	Boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
GPT, POE	GTIOC0A to GTIOC5A, GTIOC0B to GTIOC5B	I/O	Input capture, output compare, or PWM output pins
	GTETRG, GTETRGA, GTETRQB, GTETRGB	Input	External trigger input pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

Table 1.4 Pin Functions (3/6)

Function	Pin Name	I/O	Description
AGT	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTEE0, AGTEE1	Input	External event input enable pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Compare match A output pins
	AGTOB0, AGTOB1	Output	Compare match B output pins
TMR	TMCi0, TMCi1	Input	Input pins for external clocks to be input to the counter
	TMRI0, TMRI1	Input	Input pins for the counter reset
	TMO0, TMO1	Output	Compare match output pins
RTC	RTCIC0 to RTCIC2	Input	Time capture event input pins
	RTCOU	Output	Output pin for 1-Hz or 64-Hz clock
CCC	CCCOU	Output	CCC clock output pin
LPG	LPGOU	Output	Low-speed pulse generator output pin
SCli	[Asynchronous mode/clock synchronous mode]		
	SCK0, SCK1	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1	Output	Output pins for transmit data (asynchronous mode/clock synchronous mode)
	CTS0, CTS1	Input	Input pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	RTS0, RTS1	Output	Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	[Simple I ² C mode]*1		
	SSCL0, SSCL1	I/O	Input/output pins for the I ² C clock (simple I ² C mode)
	SSDA0, SSDA1	I/O	Input/output pins for the I ² C data (simple I ² C mode)
	[Simple SPI mode]*1		
	SCK0, SCK1	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0, MISO1	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0, MOSI1	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0, SS1	Input	Chip-select input pins (simple SPI mode)
SClg	[Asynchronous mode/clock synchronous mode]		
	SCK2 to SCK5, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD2 to RXD5, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD2 to TXD5, TXD9	Output	Output pins for transmit data (asynchronous mode/clock synchronous mode)
	CTS2 to CTS5, CTS9	Input	Input pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	RTS2 to RTS5, RTS9	Output	Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	[Simple I ² C mode]		
	SSCL2 to SSCL5, SSCL9	I/O	Input/output pins for the I ² C clock (simple I ² C mode)
	SSDA2 to SSDA5, SSDA9	I/O	Input/output pins for the I ² C data (simple I ² C mode)
	[Simple SPI mode]		
	SCK2 to SCK5, SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO2 to MISO5, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI2 to MOSI5, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS2 to SS5, SS9	Input	Chip-select input pins (simple SPI mode)

Table 1.4 Pin Functions (4/6)

Function	Pin Name	I/O	Description
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pins
	MOSIA, MOSIB	I/O	Input/output pins for data output from the master
	MISOA, MISOB	I/O	Input/output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input/output pins for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data 0 to data 3
USB	VCC_USB	Input	Power supply pin for the USB. Connect the pin to VSS_USB through a 0.1-μF smoothing capacitor. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	VSS_USB	Input	Ground pin for the USB. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	USB_DP	I/O	D+ I/O pin for the on-chip USB transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin for the on-chip USB transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin state (connected or disconnected) can be detected when the USB module is operating as a device controller.
	USB_EXICEN	Output	Low-power consumption control signal for the external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for the external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the Micro-AB connector ID input signal to this pin during operation in OTG mode.

Table 1.4 Pin Functions (5/6)

Function	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog power supply pin for the 14-bit A/D converter, reference voltage generation circuit, and temperature sensor. Connect the pin to AVSS0 through a 1.0-μF smoothing capacitor. Place the smoothing capacitor close to the pin.* ⁵ This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	AVSS0	Input	Analog ground pin for the 14-bit A/D converter, reference voltage generation circuit, and temperature sensor. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	VREFH0	Input	Analog reference voltage pin for the 14-bit A/D converter. Connect the pin to VREFL0 through a 1.0-μF smoothing capacitor. Place the smoothing capacitor close to the pin.* ⁶ Connect this pin to AVCC0 when not using the A/D converter. Leave this pin open-circuit if AVCC0 is not to be supplied.
	AVTRO	Output	When using the output from the reference voltage generation circuit (VREF) as the reference voltage, connect this to VREFL0 through a 10-μF smoothing capacitor.
	VREFL0	Input	Analog reference ground pin for the 14-bit A/D converter. Connect this pin to AVSS0 when not using the A/D converter. Leave this pin open-circuit if AVCC0 is not to be supplied.
	AVCC1	Input	Analog power supply/reference voltage pin for the 12-bit D/A converter and the analog comparator. Connect the pin to AVSS1 through a 10-μF smoothing capacitor. Place the smoothing capacitor close to the pin. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	AVSS1	Input	Analog ground/reference ground pin for the 12-bit D/A converter and the analog comparator. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
S14AD	AN000 to AN006, AN016 to AN017, AN020 to AN028	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pin for the external trigger signal that starts A/D conversion
R12DA	DA0	Output	Output pin for the analog signals produced by the D/A converter
ACMP	CMPREF	Input	Reference voltage input pin
	CMPIN	Input	Analog voltage input pin
	VCOUT	Output	Comparator output pin
LED	LEDI1 to LEDI3	Input	Constant current input pins for turning on LEDs
MLCD	MLCD_VCOM	Output	Polarity signal pin for common electrode
	MLCD_XRST	Output	Output pin for LCD control
	MLCD_SCLK	Output	Communications serial output clock pin
	MLCD_DEN	Output	Data identification signal pin
	MLCD_ENBS	Output	Horizontal directional data enable pin
	MLCD_ENBG	Output	Vertical directional data enable pin
	MLCD_SI0 to MLCD_SI7	Output	Graphics data signal pins

Table 1.4 Pin Functions (6/6)

Function	Pin Name	I/O	Description
MTDV	VPM	Output	Voltage monitor pin The external load capacitance applied by VPM to VSS must be no greater than 30 pF. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	PM_RES_DRV0	Input	Back EMF detection pin
	MTDO1_DRV0 to MTDO2_DRV0, MTDO4_DRV1 to MTDO6_DRV1, MTDO7_DRV2 to MTDO9_DRV2	Output	Motor driver control pins
I/O ports	P000 to P015	I/O	16-bit input/output pins
	P100 to P114	I/O	15-bit input/output pins
	P200	Input	1-bit input-only pin. Multiplexed with the NMI pin function.
	P201 to P205, P207	I/O	6-bit input/output pins
	P300 to P315	I/O	16-bit input/output pins
	P404 to P411	I/O	8-bit input/output pins
	P412, P413	I/O	2-bit input/output pins. Multiplexed with the EXTAL and XTAL pin functions.
	P500 to P511	I/O	12-bit input/output pins
	P512 to P514	I/O	3-bit input/output 3-bit input/output pins.*2 Multiplexed with P-channel open-drain output.
	P600 to P610	I/O	11-bit input/output pins
	P700 to P704	I/O	5-bit input/output pins
	P800 to P815	I/O	16-bit input/output pins

Note: Use a laminated ceramic capacitor as a smoothing capacitor.

Note 1. For the SCLi and SCLg interfaces, each communications pin has multiple functions that work differently depending on the mode as follows: RXDn/SCLn/MISO_n, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn

Note 2. As output pins, these general-purpose port pins can only be used for output of the low level.

Note 3. In an environment where there is much external noise, optionally connect these pins to VSS through a 10-pF smoothing capacitor close to the respective current sources to improve robustness against external noise and obtain stable operation of the circuit.

Note 4. When some of the IOVCC0, IOVCC1, IOVCC2, and IOVCC3 pins are connected at the same voltage, a 10-μF smoothing capacitor can be shared. In the case where the pin is connected to VCC/IOVCC, a 10-μF smoothing capacitor is not necessary.

Note 5. In an environment where there is much external noise, optionally connect this pin to AVSS0 through a 10-pF smoothing capacitor close to the current source to improve robustness against external noise and obtain stable operation of the circuit.

Note 6. In an environment where there is much external noise, optionally connect this pin to VREFL0 through a 10-pF smoothing capacitor close to the current source to improve robustness against external noise and obtain stable operation of the circuit.

1.6 Pin Arrangement

Figure 1.2 to Figure 1.5 show pin arrangements.

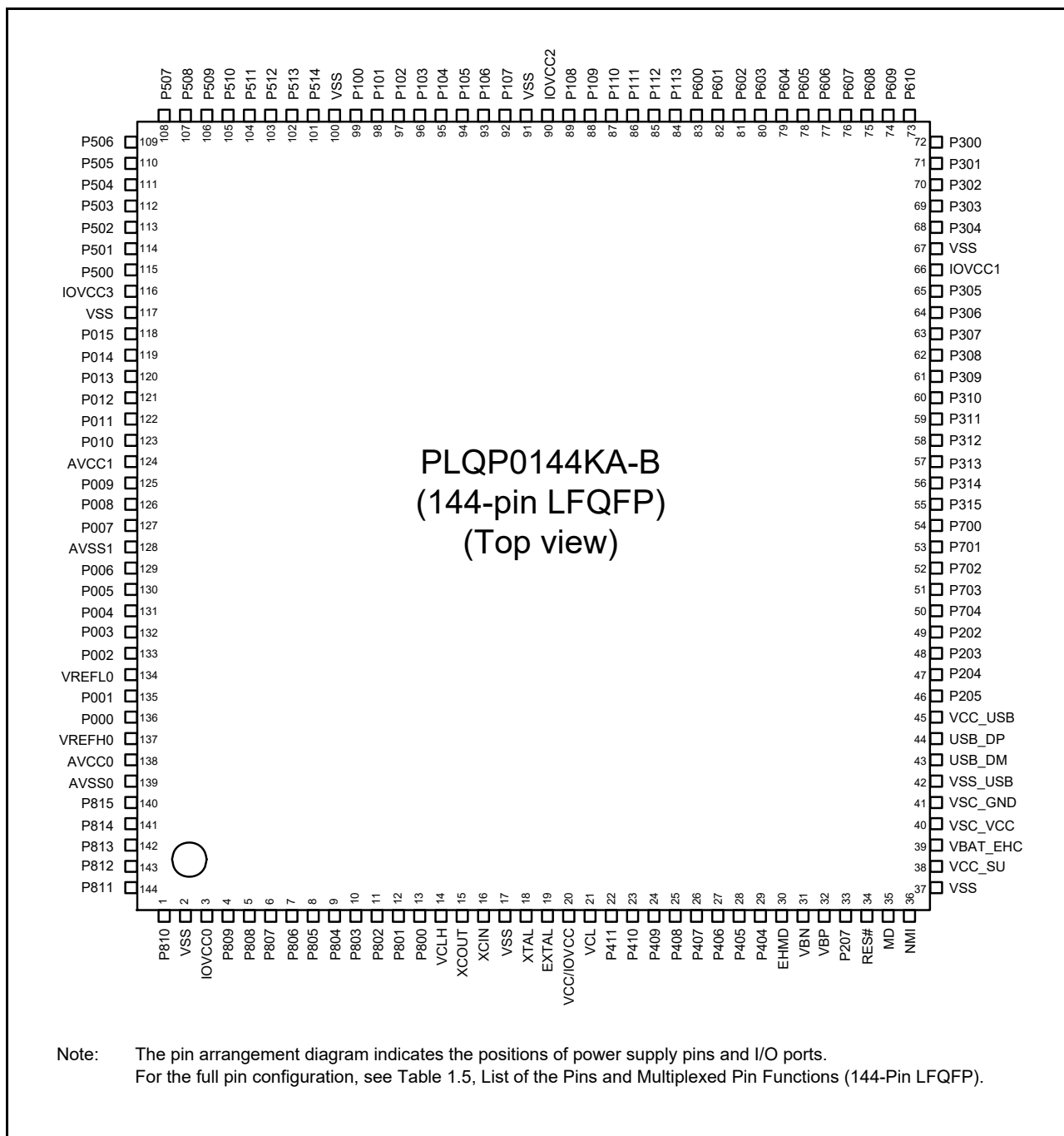


Figure 1.2 Pin Arrangement for 144-Pin LFQFP

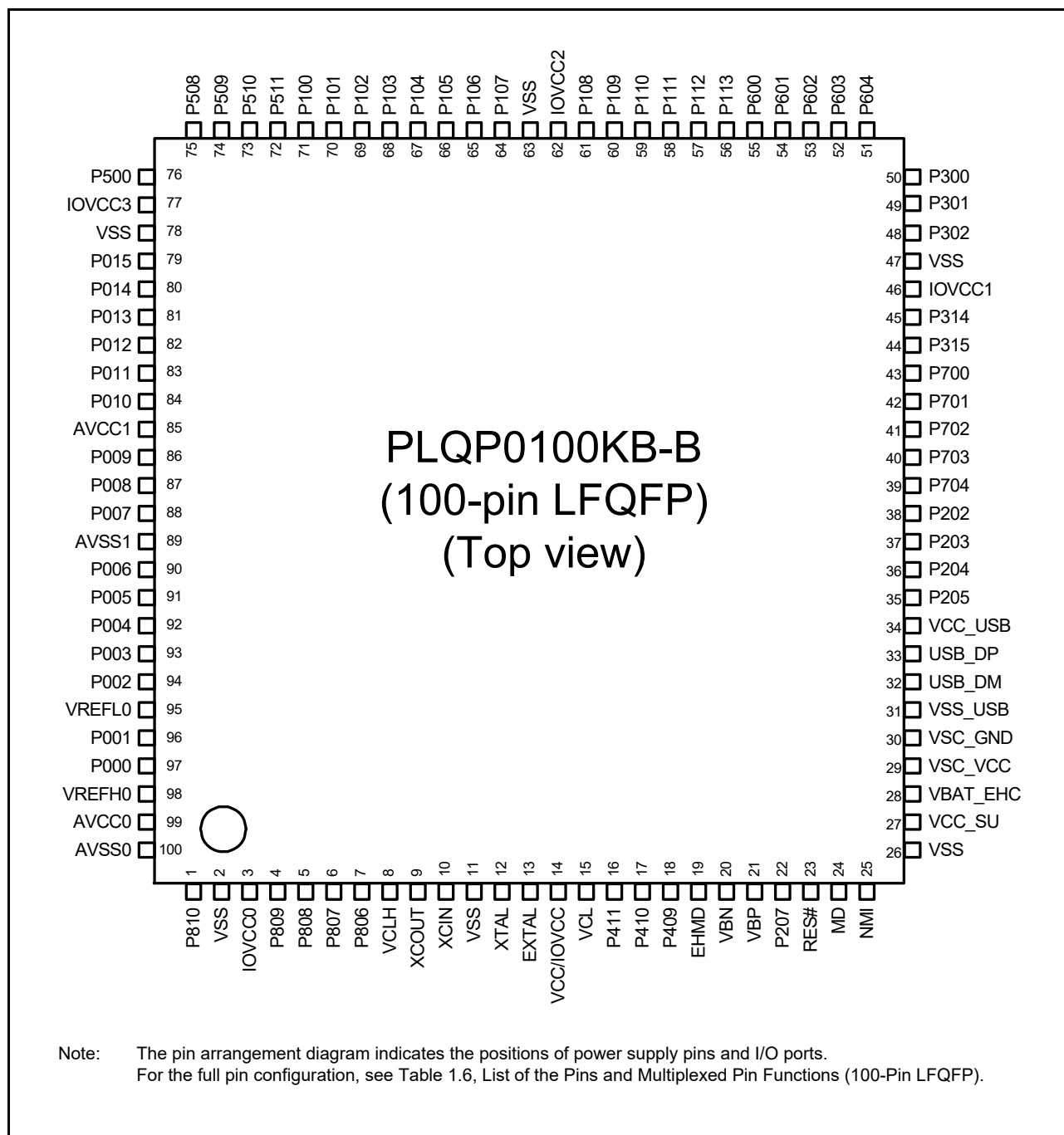


Figure 1.3 Pin Arrangement for 100-Pin LFQFP

SXBG0156MA-A (156-pin WLBGA) Ball surface (bottom view)

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	IOVCC0	P810	P815	AVSS0	P000	P004	P007	P010	P011	VSS	IOVCC3	P502	P506
2	P807	IOVCC0	VSS	AVCC0	VREFH0	P003	P008	P012	P015	P501	P505	P506	P511
3	P802	P808	P811	VREFL0	P001	P005	P009	P013	P500	P508	P509	P510	P100
4	XCOUT	P801	P809	P814	P006	AVSS1	AVCC1	P014	P507	P104	P103	P101	P102
5	XCIN	P800	P805	P813	P002	VSS	P503	P512	P513	P114	P107	P106	P105
6	VSS	VCLH	P804	P812	VSS	VSS	P504	P514	VSS	P113	P108	VSS	IOVCC2
7	XTAL	VCL	P410	P803	P806	VSS _USB	VCC _USB	VSS	P602	P605	P112	P110	P109
8	EXTAL	VCC /IOVCC	P409	P407	P405	USB _DM	USB _DP	P306	P610	P609	P604	P600	P111
9	P411	P408	P207	EHMD	P404	P703	P700	MTDO2_ DRV0	P305	P303	P608	P603	P601
10	P406	VBP	MD	VSS	VSC _VCC	P704	MTDO1_ DRV0	PM_RES _DRV0	MTDO7_ DRV2	MTDO9_ DRV2	P302	P607	P606
11	VBN	RES#	VCC _SU	VSC _GND	P204	P203	P702	MTDO4_ DRV1	MTDO5_ DRV1	MTDO8_ DRV2	VSS	P301	P300
12	VBP	NMI	VBAT_ EHC	BSCANP	P205	P202	P701	P308	MTDO6_ DRV1	VPM	IOVCC1	P304	VSS

Note: The pin arrangement diagram indicates the positions of power supply pins and I/O ports.
For the full pin configuration, see Table 1.7, List of the Pins and Multiplexed Pin Functions (WLBGA).

Figure 1.4 Pin Arrangement for 156-Pin WLBGA (Bottom View)

SXBG0156MA-A (156-pin WLBGA) Positions as seen through the chip (top view)

	A	B	C	D	E	F	G	H	J	K	L	M	N
12	VBP	NMI	VBAT_EHC	BSCANP	P205	P202	P701	P308	MTDO6_DRV1	VPM	IOVCC1	P304	VSS
11	VBN	RES#	VCC_SU	VSC_GND	P204	P203	P702	MTDO4_DRV1	MTDO5_DRV1	MTDO8_DRV2	VSS	P301	P300
10	P406	VBP	MD	VSS	VSC_VCC	P704	MTDO1_DRV0	PM_RES_DRV0	MTDO7_DRV2	MTDO9_DRV2	P302	P607	P606
9	P411	P408	P207	EHMD	P404	P703	P700	MTDO2_DRV0	P305	P303	P608	P603	P601
8	EXTAL	VCC_IOVCC	P409	P407	P405	USB_DM	USB_DP	P306	P610	P609	P604	P600	P111
7	XTAL	VCL	P410	P803	P806	VSS_USB	VCC_USB	VSS	P602	P605	P112	P110	P109
6	VSS	VCLH	P804	P812	VSS	VSS	P504	P514	VSS	P113	P108	VSS	IOVCC2
5	XCIN	P800	P805	P813	P002	VSS	P503	P512	P513	P114	P107	P106	P105
4	XCOUT	P801	P809	P814	P006	AVSS1	AVCC1	P014	P507	P104	P103	P101	P102
3	P802	P808	P811	VREFL0	P001	P005	P009	P013	P500	P508	P509	P510	P100
2	P807	IOVCC0	VSS	AVCC0	VREFH0	P003	P008	P012	P015	P501	P505	P506	P511
1	IOVCC0	P810	P815	AVSS0	P000	P004	P007	P010	P011	VSS	IOVCC3	P502	P506

Note: The pin arrangement diagram indicates the positions of power supply pins and I/O ports.
For the full pin configuration, see Table 1.7, List of the Pins and Multiplexed Pin Functions (WLBGA).

Figure 1.5 Pin Arrangement for 156-Pin WLBGA (Top View)

1.7 List of Pins

Table 1.5 to Table 1.7 are lists of the pins and multiplexed pin functions.

Table 1.5 List of the Pins and Multiplexed Pin Functions (144-Pin LFQFP) (1/5)

Pin Number 144 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
1		P810	CACREF_B/AGTIO0_A/ GTIOC2A_B	SCK3_B/SCL0				IOVCC0
2	VSS							
3	IOVCC0							
4		P809	AGTEE0_A/ GTETRGA_B/ GTIOC2B_B	TXD3_B/SSDA3_B/ MOSI3_B/SDA0				IOVCC0
5		P808	AGTO0_A/GTETRGA_B	RXD3_B/SSCL3_B/ MISO3_B		IRQ2_B		IOVCC0
6		P807	AGTOA0_A/GTIOC1A_B	CTS3_B/RTS3_B/ SS3_B/SSLB3_C		IRQ3_B	VCOUT_B	IOVCC0
7		P806	AGTOB0_A/GTIOC1B_B					IOVCC0
8		P805		MOSIB_C/QIO0_C				IOVCC0
9		P804	GTIU_C	MISOB_C/QIO1_C				IOVCC0
10		P803	GTIV_C	SSLB2_C/QIO2_C				IOVCC0
11		P802	GTIW_C	SSLB1_C/QIO3_C				IOVCC0
12		P801	GTOUUP_C	RSPCKB_C/ QSPCLK_C				IOVCC0
13		P800	GTOULO_C	SSLB0_C/QSSL_C				IOVCC0
14	VCLH							
15	XCOUT							IOVCC
16	XCIN							IOVCC
17	VSS							
18	XTAL	P413	GTETRGA_A/ GTIOC0A_A	TXD3_A/SSDA3_A/ MOSI3_A				IOVCC
19	EXTAL	P412	GTETRGA_B/ GTIOC0B_A	RXD3_A/SSCL3_A/ MISO3_A				IOVCC
20	VCC/IOVCC							
21	VCL							
22	CLKOUT32K_A /SWCLK	P411	TMCIO_A	TXD9_A/SSDA9_A/ MOSI9_A/SCK3_A		IRQ0_A_DS		IOVCC
23		P410	GTIOC3B_B			IRQ2_A_DS		IOVCC
24	CLKOUT32K_B	P409	GTIOC3A_B			IRQ3_A_DS		IOVCC
25		P408	GTOVUP_C			KRM07_B		IOVCC
26		P407	GTOVLO_C			KRM06_B		IOVCC
27		P406	GTOVUP_C					IOVCC
28		P405	GTOVLO_C					IOVCC
29		P404						IOVCC
30	EHMD							IOVCC
31	VCN							
32	VBP							
33	SWDIO	P207		USB_ID_A/RXD9_A/ SSCL9_A/MISO9_A/ CTS3_A/RTS3_A/ SS3_A		IRQ1_A_DS		IOVCC
34	RES#							IOVCC

Table 1.5 List of the Pins and Multiplexed Pin Functions (144-Pin LFQFP) (2/5)

Pin Number 144 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
35	MD	P201	TMRI0_A					IOVCC
36		P200	TMO0_A			NMI		IOVCC
37	VSS							
38	VCC_SU							
39	VBAT_EHC							
40	VSC_VCC							
41	VSC_GND							
42	VSS_USB							
43				USB_DM				VCC_USB
44				USB_DP				VCC_USB
45	VCC_USB							
46		P205		CTS4_B/RTS4_B/ SS4_B		IRQ8_B		IOVCC1
47		P204	ADTRG0_A/GTIU_A/ RTCIC0_B	USB_VBUS/SCK4_B		IRQ9_B		IOVCC1
48		P203	GTIV_A/RTCIC1_B	USB_OVRCURA_A/ TXD4_B/SSDA4_B/ MOSI4_B				IOVCC1
49		P202	CACREF_A/GTIW_A/ CCCOUT_B/RTCOUT_B	USB_OVRCURB_A/ RXD4_B/SSCL4_B/ MISO4_B		IRQ4_A		IOVCC1
50		P704	TMC11	CTS0_C/RTS0_C/ SS0_C				IOVCC1
51		P703		TXD0_C/SSDA0_C/ MOSI0_C				IOVCC1
52		P702		RXD0_C/SSCL0_C/ MISO0_C				IOVCC1
53		P701	TMRI1/RTCIC2_B	USB_VBUSEN_A/ SCL1				IOVCC1
54		P700	TMO1	SCK0_C/SDA1				IOVCC1
55		P315	GTIOC4A_B	TXD5_B/SSDA5_B/ MOSI5_B				IOVCC1
56		P314	GTIOC4B_B	RXD5_B/SSCL5_B/ MISO5_B				IOVCC1
57		P313		TXD1_B/SSDA1_B/ MOSI1_B/IRTXD1_B				IOVCC1
58		P312		RXD1_B/SSCL1_B/ MISO1_B/IRRXD1_B				IOVCC1
59		P311		CTS1_B/RTS1_B/ SS1_B				IOVCC1
60		P310		SCK1_B				IOVCC1
61		P309	AGTIO1_C					IOVCC1
62		P308	AGTO1_C					IOVCC1
63		P307	AGTOA1_C					IOVCC1
64		P306	AGTOB1_C					IOVCC1
65		P305	AGTEE1_C					IOVCC1
66	IOVCC1							
67	VSS							
68		P304		TXD5_C/SSDA5_C/ MOSI5_C		KRM05_B		IOVCC1
69		P303		RXD5_C/SSCL5_C/ MISO5_C		KRM04_B		IOVCC1

Table 1.5 List of the Pins and Multiplexed Pin Functions (144-Pin LQFP) (3/5)

Pin Number 144 LQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
70		P302	GTIU_B/TMCIO_B	CTS5_C/RTS5_C/ SS5_C/CTS5_B/ RTS5_B/SS5_B				IOVCC1
71		P301	GTIV_B/TMRI0_B/ CCCOUT_A/RTCCOUT_A	SCK5_C/SCK5_B				IOVCC1
72	CLKOUT32K_C	P300	GTIW_B/TMO0_B					IOVCC1
73		P610		SSLB0_B				IOVCC1
74		P609		TXD2_C/SSDA2_C/ MOSI2_C/MOSIB_B				IOVCC1
75		P608	GTETRG_A_C	RXD2_C/SSCL2_C/ MISO2_C/MISOB_B				IOVCC1
76		P607	GTETRGB_C	CTS2_C/RTS2_C/ SS2_C/RSPCKB_B				IOVCC1
77		P606		SCK2_C/SSLB2_B				IOVCC1
78		P605		TXD9_C/SSDA9_C/ MOSI9_C/SSLB1_B				IOVCC1
79		P604	GTIOC5B_B/RTIC0_A	TXD9_B/SSDA9_B/ MOSI9_B/SSLB3_B		IRQ5_B		IOVCC1
80		P603	GTIOC5A_B/RTIC1_A	RXD9_B/SSCL9_B/ MISO9_B/SSLB0_D				IOVCC1
81		P602	GTOUUP_B/RTIC2_A	SCK9_B/QSPCLK_A				IOVCC1
82		P601	GTOULO_B	CTS9_B/RTS9_B/ SS9_B/QSSL_A				IOVCC1
83		P600	LPGOUT	SCK9_C				IOVCC1
84		P113	AGTEE1_A/ GTOWUP_A/ GTIOC3A_A	TXD4_A/SSDA4_A/ MOSI4_A/SSLB2_A/ QIO0_B	MLCD_VCOM	IRQ5_A		IOVCC2
85		P112	AGTEE0_B/ GTOWLO_A/ GTIOC3B_A	RXD4_A/SSCL4_A/ MISO4_A/SSLB3_A/ QIO1_B	MLCD_XRST	IRQ6_A		IOVCC2
86		P111	AGTO0_B/GTOUUP_A/ GTIOC2A_A	CTS4_A/RTS4_A/ SS4_A/RXD5_A/ SSCL5_A/MISO5_A/ SSLB1_A/QIO2_B	MLCD_SCLK			IOVCC2
87		P110	AGTOA0_B/GTOULO_A/ GTIOC2B_A	SCK9_A/SCK5_A/ MOSIB_A/QIO3_B	MLCD_DEN			IOVCC2
88		P109	AGTOB0_B/GTOVUP_A	CTS9_A/RTS9_A/ SS9_A/CTS5_A/ RTS5_A/SS5_A/ MISOB_A/ QSPCLK_B	MLCD_ENBS			IOVCC2
89		P108	AGTIO0_B/GTOVLO_A	SCK4_A/TXD5_A/ SSDA5_A/MOSI5_A/ RSPCKB_A/QSSL_B	MLCD_ENBG			IOVCC2
90	IOVCC2							
91	VSS							
92	TMS	P107	AGTOB1_A/GTIOC1A_A	CTS0_A/RTS0_A/ SS0_A/RSPCKA_A	MLCD_SI0	IRQ7_A/ KRM07_A		IOVCC2
93	TDO	P106	AGTOA1_A/GTIOC1B_A	TXD0_A/SSDA0_A/ MOSI0_A/SSLB0_A	MLCD_SI1	IRQ0_B/ KRM06_A	VCOUT_A	IOVCC2
94	TDI	P105	AGTO1_A/GTIOC4A_A	USB_EXICEN/ RXD0_A/SSCL0_A/ MISO0_A/MISOA_A	MLCD_SI2	IRQ8_A/ KRM05_A		IOVCC2
95	TCK	P104	AGTIO1_A/GTIOC4B_A	SCK0_A/MOSIA_A	MLCD_SI3	IRQ9_A/ KRM04_A		IOVCC2

Table 1.5 List of the Pins and Multiplexed Pin Functions (144-Pin LFQFP) (4/5)

Pin Number 144 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
96		P103	GTIOC5A_A	CTS2_A/RTS2_A/ SS2_A/CTS1_A/ RTS1_A/SS1_A/ SSLA0_A	MLCD_SI4	KRM03_A		IOVCC2
97		P102	GTIOC5B_A	TXD2_A/SSDA2_A/ MOSI2_A/TXD1_A/ SSDA1_A/MOSI1_A/ IRTXD1_A/SSLA1_A	MLCD_SI5	KRM02_A		IOVCC2
98		P101	GTIOC0A_B	RXD2_A/SSCL2_A/ MISO2_A/RXD1_A/ SSCL1_A/MISO1_A/ IRRXD1_A/SSLA2_A	MLCD_SI6	KRM01_A		IOVCC2
99		P100	GTIOC0B_B	SCK2_A/SCK1_A/ SSLA3_A	MLCD_SI7	KRM00_A		IOVCC2
100	VSS							
101		P514			LEDI1			IOVCC3
102		P513			LEDI2			IOVCC3
103		P512			LEDI3			IOVCC3
104		P511	GTOVUP_B/ GTIOC1B_C			KRM03_B		IOVCC3
105		P510	GTOVLO_B/ GTIOC1A_C			KRM02_B		IOVCC3
106		P509		USB_OVRCURB_B		KRM01_B		IOVCC3
107		P508	GTIOC2B_C			IRQ4_B		IOVCC3
108		P507	GTIOC2A_C	USB_ID_B		KRM00_B		IOVCC3
109		P506				IRQ0_C	AN028	IOVCC3
110		P505				IRQ1_C	AN027	IOVCC3
111		P504		USB_VBUSEN_B/ CTS2_B/RTS2_B/ SS2_B			AN026	IOVCC3
112		P503		USB_OVRCURA_B/ SCK2_B			AN025	IOVCC3
113		P502		RXD2_B/SSCL2_B/ MISO2_B/ RSPCKA_C			AN024	IOVCC3
114		P501	AGTOA1_B	TXD2_B/SSDA2_B/ MOSI2_B/MOSIA_C		IRQ1_B	AN023	IOVCC3
115		P500	ADTRG0_B/AGTOB1_B/ GTOWUP_B/ GTIOC4B_C	CTS0_B/RTS0_B/ SS0_B/MISOA_B/ QIO0_A			AN022	IOVCC3
116	IOVCC3							
117	VSS							
118		P015	AGTIO1_B/GTOWLO_B/ GTIOC4A_C	SCK0_B/SSLA3_B/ QIO1_A		IRQ7_B	AN021	IOVCC3
119		P014	AGTEE1_B/GTIOC3B_C	RXD0_B/SSCL2_B/ MISO2_B/SSLA2_B/ QIO2_A		IRQ6_B	AN020	IOVCC3
120		P013	AGTO1_B/GTIOC3A_C	TXD0_B/SSDA0_B/ MOSI0_B/SSLA1_B/ QIO3_A				IOVCC3
121		P012		SSLA0_B				IOVCC3
122	CLKOUT	P011		RSPCKA_B			AN017	IOVCC3
123		P010		MOSIA_B			AN016	IOVCC3
124	AVCC1							
125		P009					CMPREF	AVCC1

Table 1.5 List of the Pins and Multiplexed Pin Functions (144-Pin LFQFP) (5/5)

Pin Number 144 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
126		P008					CMPIN	AVCC1
127		P007					DA0	AVCC1
128	AVSS1							
129		P006					AN006	AVCC0
130		P005					AN005	AVCC0
131		P004					AN004	AVCC0
132		P003					AN003	AVCC0
133		P002					AN002	AVCC0
134	VREFL0							
135		P001					AN001	AVCC0
136		P000					AN000	AVCC0
137	VREFH0/ AVTRO							
138	AVCC0							
139	AVSS0							
140		P815	GTIOC5A_C	CTS4_C/RTS4_C/ SS4_C				IOVCC0
141		P814	GTIOC5B_C	SCK4_C				IOVCC0
142		P813		RXD4_C/SSCL4_C/ MISO4_C				IOVCC0
143		P812	GTIOC0A_C	TXD4_C/SSDA4_C/ MOSI4_C				IOVCC0
144		P811	GTIOC0B_C					IOVCC0

Note: Note the following points with regard to pin names.

- For the SCLi and SCLg interfaces, each communications pin has multiple functions that work differently depending on the mode as follows:
RXDn/SCLn/MISO_n, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
- We recommend using the sets of pins that have the same letter (“_A”, “_B”, “_C” to indicate group membership) appended to their names.
For the SPI, QSPI, and SCI interfaces, the AC portion of the electrical characteristics is measured per group.
- Pin functions that have “_DS” appended to their names can be used as inputs for trigger signals for release from deep software standby.

Table 1.6 List of the Pins and Multiplexed Pin Functions (100-Pin LFQFP) (1/4)

Pin Number 100 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
1		P810	CACREF_B/AGTIO0_A/ GTIOC2A_B	SCK3_B/SCL0				IOVCC0
2	VSS							
3	IOVCC0							
4		P809	AGTEE0_A/ GTETRGA_B/ GTIOC2B_B	TXD3_B/SSDA3_B/ MOSI3_B/SDA0				IOVCC0
5		P808	AGTO0_A/GTETRGA_B	RXD3_B/SSCL3_B/ MISO3_B		IRQ2_B		IOVCC0
6		P807	AGTOA0_A/GTIOC1A_B	CTS3_B/RTS3_B/ SS3_B/SSLB3_C		IRQ3_B	VCOUT_B	IOVCC0
7		P806	AGTOB0_A/GTIOC1B_B					IOVCC0
8	VCLH							
9	XCOUT							IOVCC
10	XCIN							IOVCC
11	VSS							
12	XTAL	P413	GTETRGA_A/ GTIOC0A_A	TXD3_A/SSDA3_A/ MOSI3_A				IOVCC
13	EXTAL	P412	GTETRGA_B/ GTIOC0B_A	RXD3_A/SSCL3_A/ MISO3_A				IOVCC
14	VCC/IOVCC							
15	VCL							
16	CLKOUT32K_A /SWCLK	P411	TMCIO_A	TXD9_A/SSDA9_A/ MOSI9_A/SCK3_A		IRQ0_A_DS		IOVCC
17		P410	GTIOC3B_B			IRQ2_A_DS		IOVCC
18	CLKOUT32K_B	P409	GTIOC3A_B			IRQ3_A_DS		IOVCC
19	EHMD							IOVCC
20	VBIN							
21	VBP							
22	SWDIO	P207		USB_ID_A/RXD9_A/ SSCL9_A/MISO9_A/ CTS3_A/RTS3_A/ SS3_A		IRQ1_A_DS		IOVCC
23	RES#							IOVCC
24	MD	P201	TMRIO_A					IOVCC
25		P200	TMO0_A			NMI		IOVCC
26	VSS							
27	VCC_SU							
28	VBAT_EHC							
29	VSC_VCC							
30	VSC_GND							
31	VSS_USB							
32				USB_DM				VCC_USB
33				USB_DP				VCC_USB
34	VCC_USB							
35		P205		CTS4_B/RTS4_B/ SS4_B		IRQ8_B		IOVCC1
36		P204	ADTRG0_A/GTIOU_A/ RTIC0_B	USB_VBUS/SCK4_B		IRQ9_B		IOVCC1
37		P203	GTIV_A/RTIC1_B	USB_OVRCURA_A/ TXD4_B/SSDA4_B/ MOSI4_B				IOVCC1

Table 1.6 List of the Pins and Multiplexed Pin Functions (100-Pin LFQFP) (2/4)

Pin Number 100 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
38		P202	CACREF_A/GTIW_A/ CCCOUT_B/RTCCOUT_B	USB_OVRCURB_A/ RXD4_B/SSCL4_B/ MISO4_B		IRQ4_A		IOVCC1
39		P704	TMC1	CTS0_C/RTS0_C/ SS0_C				IOVCC1
40		P703		TXD0_C/SSDA0_C/ MOSI0_C				IOVCC1
41		P702		RXD0_C/SSCL0_C/ MISO0_C				IOVCC1
42		P701	TMR1/RTCCIC2_B	USB_VBUSEN_A/ SCL1				IOVCC1
43		P700	TMO1	SCK0_C/SDA1				IOVCC1
44		P315	GTIOC4A_B	TXD5_B/SSDA5_B/ MOSI5_B				IOVCC1
45		P314	GTIOC4B_B	RXD5_B/SSCL5_B/ MISO5_B				IOVCC1
46	IOVCC1							
47	VSS							
48		P302	GTIU_B/TMCIO_B	CTS5_C/RTS5_C/ SS5_C/CTS5_B/ RTS5_B/SS5_B				IOVCC1
49		P301	GTIV_B/TMRI0_B/ CCCOUT_A/RTCCOUT_A	SCK5_C/SCK5_B				IOVCC1
50		P300	GTIW_B/TMO0_B					IOVCC1
51		P604	GTIOC5B_B/RTCCIC0_A	TXD9_B/SSDA9_B/ MOSI9_B/SSLB3_B		IRQ5_B		IOVCC1
52		P603	GTIOC5A_B/RTCCIC1_A	RXD9_B/SSCL9_B/ MISO9_B/SSLB0_D				IOVCC1
53		P602	GTOUUP_B/RTCCIC2_A	SCK9_B/QSPCLK_A				IOVCC1
54		P601	GTOULO_B	CTS9_B/RTS9_B/ SS9_B/QSSL_A				IOVCC1
55		P600	LPGOUT	SCK9_C				IOVCC1
56		P113	AGTEE1_A/ GTOWUP_A/ GTIOC3A_A	TXD4_A/SSDA4_A/ MOSI4_A/SSLB2_A/ QIO0_B	MLCD_VCOM	IRQ5_A		IOVCC2
57		P112	AGTEE0_B/ GTOWLO_A/ GTIOC3B_A	RXD4_A/SSCL4_A/ MISO4_A/SSLB3_A/ QIO1_B	MLCD_XRST	IRQ6_A		IOVCC2
58		P111	AGTO0_B/GTOUUP_A/ GTIOC2A_A	CTS4_A/RTS4_A/ SS4_A/RXD5_A/ SSCL5_A/MISO5_A/ SSLB1_A/QIO2_B	MLCD_SCLK			IOVCC2
59		P110	AGTOA0_B/GTOULO_A/ GTIOC2B_A	SCK9_A/SCK5_A/ MOSI9_A/QIO3_B	MLCD_DEN			IOVCC2
60		P109	AGTOB0_B/GTOVUP_A	CTS9_A/RTS9_A/ SS9_A/CTS5_A/ RTS5_A/SS5_A/ MISOB_A/ QSPCLK_B	MLCD_ENBS			IOVCC2
61		P108	AGTIO0_B/GTOVLO_A	SCK4_A/TXD5_A/ SSDA5_A/MOSI5_A/ RSPCKB_A/QSSL_B	MLCD_ENBG			IOVCC2
62	IOVCC2							
63	VSS							
64	TMS	P107	AGTOB1_A/GTIOC1A_A	CTS0_A/RTS0_A/ SS0_A/RSPCKA_A	MLCD_SI0	IRQ7_A/ KRM07_A		IOVCC2
65	TDO	P106	AGTOA1_A/GTIOC1B_A	TXD0_A/SSDA0_A/ MOSI0_A/SSLB0_A	MLCD_SI1	IRQ0_B/ KRM06_A	VCOUT_A	IOVCC2

Table 1.6 List of the Pins and Multiplexed Pin Functions (100-Pin LFQFP) (3/4)

Pin Number 100 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
66	TDI	P105	AGTO1_A/GTIOC4A_A	USB_EXICEN/ RXD0_A/SSCL0_A/ MISO0_A/MISOA_A	MLCD_SI2	IRQ8_A/ KRM05_A		IOVCC2
67	TCK	P104	AGTIO1_A/GTIOC4B_A	SCK0_A/MOSIA_A	MLCD_SI3	IRQ9_A/ KRM04_A		IOVCC2
68		P103	GTIOC5A_A	CTS2_A/RTS2_A/ SS2_A/CTS1_A/ RTS1_A/SS1_A/ SSLA0_A	MLCD_SI4	KRM03_A		IOVCC2
69		P102	GTIOC5B_A	TXD2_A/SSDA2_A/ MOSI2_A/TXD1_A/ SSDA1_A/MOSI1_A/ IRTXD1_A/SSLA1_A	MLCD_SI5	KRM02_A		IOVCC2
70		P101	GTIOC0A_B	RXD2_A/SSCL2_A/ MISO2_A/RXD1_A/ SSCL1_A/MISO1_A/ IRRXD1_A/SSLA2_A	MLCD_SI6	KRM01_A		IOVCC2
71		P100	GTIOC0B_B	SCK2_A/SCK1_A/ SSLA3_A	MLCD_SI7	KRM00_A		IOVCC2
72		P511	GTOVUP_B/ GTIOC1B_C			KRM03_B		IOVCC3
73		P510	GTOVLO_B/ GTIOC1A_C			KRM02_B		IOVCC3
74		P509		USB_OVRCURB_B		KRM01_B		IOVCC3
75		P508	GTIOC2B_C			IRQ4_B		IOVCC3
76		P500	ADTRG0_B/AGTOB1_B/ GTOWUP_B/ GTIOC4B_C	CTS0_B/RTS0_B/ SS0_B/MISOA_B/ QIO0_A			AN022	IOVCC3
77	IOVCC3							
78	VSS							
79		P015	AGTIO1_B/GTOWLO_B/ GTIOC4A_C	SCK0_B/SSLA3_B/ QIO1_A		IRQ7_B	AN021	IOVCC3
80		P014	AGTEE1_B/GTIOC3B_C	RXD0_B/SSCL0_B/ MISO0_B/SSLA2_B/ QIO2_A		IRQ6_B	AN020	IOVCC3
81		P013	AGTO1_B/GTIOC3A_C	TXD0_B/SSDA0_B/ MOSI0_B/SSLA1_B/ QIO3_A				IOVCC3
82		P012		SSLA0_B				IOVCC3
83	CLKOUT	P011		RSPCKA_B			AN017	IOVCC3
84		P010		MOSIA_B			AN016	IOVCC3
85	AVCC1							
86		P009					CMPREF	AVCC1
87		P008					CMPIN	AVCC1
88		P007					DA0	AVCC1
89	AVSS1							
90		P006					AN006	AVCC0
91		P005					AN005	AVCC0
92		P004					AN004	AVCC0
93		P003					AN003	AVCC0
94		P002					AN002	AVCC0
95	VREFL0							
96		P001					AN001	AVCC0
97		P000					AN000	AVCC0
98	VREFH0/ AVTRO							
99	AVCC0							

Table 1.6 List of the Pins and Multiplexed Pin Functions (100-Pin LFQFP) (4/4)

Pin Number 100 LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	Applicable Power Supply
100	AVSS0							

Note: Note the following points with regard to pin names.

- For the SCli and SClg interfaces, each communications pin has multiple functions that work differently depending on the mode as follows:
RXDn/SCLn/MISO_n, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
- We recommend using the sets of pins that have the same letter ("_A", "_B", "_C" to indicate group membership) appended to their names.
For the SPI, QSPI, and SCI interfaces, the AC portion of the electrical characteristics is measured per group.
- Pin functions that have "_DS" appended to their names can be used as inputs for trigger signals for release from deep software standby.

Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA) (1/6)

Pin Number	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, RIIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	MTDV	Applicable Power Supply
B1		P810	CACREF_B/ AGTIO0_A/ GTIOC2A_B	SCK3_B/SCL0					IOVCC0
C2	VSS								
B2	IOVCC0								
C4		P809	AGTEE0_A/ GTETRG_A_B/ GTIOC2B_B	TXD3_B/ SSDA3_B/ MOSI3_B/SDA0					IOVCC0
B3		P808	AGTO0_A/ GTETRGA_B	RXD3_B/ SSCL3_B/ MISO3_B		IRQ2_B			IOVCC0
A2		P807	AGTOA0_A/ GTIOC1A_B	CTS3_B/ RTS3_B/SS3_B/ SSLB3_C		IRQ3_B	VCOUT_B		IOVCC0
E7		P806	AGTOB0_A/ GTIOC1B_B						IOVCC0
C5		P805		MOSIB_C/ QIO0_C					IOVCC0
C6		P804	GTIU_C	MISOB_C/ QIO1_C					IOVCC0
D7		P803	GTIV_C	SSLB2_C/ QIO2_C					IOVCC0
A3		P802	GTIW_C	SSLB1_C/ QIO3_C					IOVCC0
B4		P801	GTOUUP_C	RSPCKB_C/ QSPCLK_C					IOVCC0
B5		P800	GTOULO_C	SSLB0_C/ QSSL_C					IOVCC0
B6	VCLH								
A4	XCOUT								IOVCC
A5	XCIN								IOVCC
A6	VSS								
A7	XTAL	P413	GTETRG_A/ GTIOC0A_A	TXD3_A/ SSDA3_A/ MOSI3_A					IOVCC
A8	EXTAL	P412	GTETRGA_A/ GTIOC0B_A	RXD3_A/ SSCL3_A/ MISO3_A					IOVCC
B8	VCC/IOVCC								
B7	VCL								
A9	CLKOUT32K_A/ SWCLK	P411	TMCIO_A	TXD9_A/ SSDA9_A/ MOSI9_A/ SCK3_A		IRQ0_A_DS			IOVCC
C7		P410	GTIOC3B_B			IRQ2_A_DS			IOVCC
C8	CLKOUT32K_B	P409	GTIOC3A_B			IRQ3_A_DS			IOVCC
B9		P408	GTOVUP_C			KRM07_B			IOVCC
D8		P407	GTOVLO_C			KRM06_B			IOVCC
A10		P406	GTOVUP_C						IOVCC
E8		P405	GTOVLO_C						IOVCC
E9		P404							IOVCC
D9	EHMD								IOVCC
A11	VBIN								

Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA) (2/6)

Pin Number	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	MTDV	Applicable Power Supply
B10	VBP								
C9	SWDIO	P207		USB_ID_A/ RXD9_A/ SSCL9_A/ MISO9_A/ CTS3_A/ RTS3_A/SS3_A		IRQ1_A_DS			IOVCC
B11	RES#								IOVCC
C10	MD	P201	TMRI0_A						IOVCC
B12		P200	TMO0_A			NMI			IOVCC
D10	VSS								
C11	VCC_SU								
C12	VBAT_EHC								
E10	VSC_VCC								
D11	VSC_GND								
D12	BSCANP								IOVCC
F7	VSS_USB								
F8				USB_DM					VCC_USB
G8				USB_DP					VCC_USB
G7	VCC_USB								
E12		P205		CTS4_B/ RTS4_B/SS4_B		IRQ8_B			IOVCC1
E11		P204	ADTRG0_A/ GTIU_A/RTCIC0_B	USB_VBUS/ SCK4_B		IRQ9_B			IOVCC1
F11		P203	GTIV_A/RTCIC1_B	USB_OVRCURA_A/ TXD4_B/ SSDA4_B/ MOSI4_B					IOVCC1
F12		P202	CACREF_A/ GTIW_A/ CCCOU_T_B/ RTCOU_T_B	USB_OVRCURB_A/ RXD4_B/ SSCL4_B/ MISO4_B		IRQ4_A			IOVCC1
F10		P704	TMCI1	CTS0_C/ RTS0_C/SS0_C					IOVCC1
F9		P703		TXD0_C/ SSDA0_C/ MOSI0_C					IOVCC1
G11		P702		RXD0_C/ SSCL0_C/ MISO0_C					IOVCC1
G12		P701	TMRI1/RTCIC2_B	USB_VBUSEN_A/ SCL1					IOVCC1
G9		P700	TMO1	SCK0_C/SDA1					IOVCC1
G10								MTDO1_DR V0	VPM
H10								PM_RES1_D RV0	VPM
H9								MTDO2_DR V0	VPM
H11								MTDO4_DR V1	VPM
J11								MTDO5_DR V1	VPM
J12								MTDO6_DR V1	VPM
K12	VPM								

Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA) (3/6)

Pin Number	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, RIIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	MTDV	Applicable Power Supply
H12		P308	AGTO1_C						IOVCC1
J10								MTDO7_DR V2	VPM
K11								MTDO8_DR V2	VPM
H8		P306	AGTOB1_C						IOVCC1
K10								MTDO9_DR V2	VPM
J9		P305	AGTEE1_C						IOVCC1
L12	IOVCC1								
L11	VSS								
M12		P304		TXD5_C/ SSDA5_C/ MOSI5_C		KRM05_B			IOVCC1
K9		P303		RXD5_C/ SSCL5_C/ MISO5_C		KRM04_B			IOVCC1
L10		P302	GTIU_B/TMCI0_B	CTS5_C/ RTS5_C/SS5_C/ CTS5_B/ RTS5_B/SS5_B					IOVCC1
M11		P301	GTIV_B/TMRI0_B/ CCCOUT_A/ RTCCOUT_A	SCK5_C/ SCK5_B					IOVCC1
N11		P300	GTIW_B/TMO0_B						IOVCC1
J8	CLKOUT32K_C	P610		SSLB0_B					IOVCC1
K8		P609		TXD2_C/ SSDA2_C/ MOSI2_C/ MOSIB_B					IOVCC1
L9		P608	GTETRG_A_C	RXD2_C/ SSCL2_C/ MISO2_C/ MISOB_B					IOVCC1
M10		P607	GTETRGB_C	CTS2_C/ RTS2_C/SS2_C/ RSPCKB_B					IOVCC1
N10		P606		SCK2_C/ SSLB2_B					IOVCC1
K7		P605		TXD9_C/ SSDA9_C/ MOSI9_C/ SSLB1_B					IOVCC1
L8		P604	GTIOC5B_B/ RTCIC0_A	TXD9_B/ SSDA9_B/ MOSI9_B/ SSLB3_B		IRQ5_B			IOVCC1
M9		P603	GTIOC5A_B/ RTCIC1_A	RXD9_B/ SSCL9_B/ MISO9_B/ SSLB0_D					IOVCC1
J7		P602	GTOUUP_B/ RTCIC2_A	SCK9_B/ QSPCLK_A					IOVCC1
N9		P601	GTOULO_B	CTS9_B/ RTS9_B/SS9_B/ QSSL_A					IOVCC1
M8		P600	LPGOUT	SCK9_C					IOVCC1

Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA) (4/6)

Pin Number	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, RIIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	MTDV	Applicable Power Supply
K6		P113	AGTEE1_A/ GTOWUP_A/ GTIOC3A_A	TXD4_A/ SSDA4_A/ MOSI4_A/ SSLB2_A/ QIO0_B	MLCD_VCOM	IRQ5_A			IOVCC2
L7		P112	AGTEE0_B/ GTOWLO_A/ GTIOC3B_A	RXD4_A/ SSCL4_A/ MISO4_A/ SSLB3_A/ QIO1_B	MLCD_XRST	IRQ6_A			IOVCC2
N8		P111	AGTO0_B/ GTOWUP_A/ GTIOC2A_A	CTS4_A/ RTS4_A/SS4_A/ RXD5_A/ SSCL5_A/ MISO5_A/ SSLB1_A/ QIO2_B	MLCD_SCLK				IOVCC2
M7		P110	AGTOA0_B/ GTOWLO_A/ GTIOC2B_A	SCK9_A/ SCK5_A/ MOSIB_A/ QIO3_B	MLCD_DEN				IOVCC2
N7		P109	AGTOB0_B/ GTOWUP_A	CTS9_A/ RTS9_A/SS9_A/ CTS5_A/ RTS5_A/SS5_A/ MISOB_A/ QSPCLK_B	MLCD_ENBS				IOVCC2
L6		P108	AGTIO0_B/ GTOWLO_A	SCK4_A/ TXD5_A/ SSDA5_A/ MOSI5_A/ RSPCKB_A/ QSSL_B	MLCD_ENBG				IOVCC2
K5		P114							IOVCC2
N6	IOVCC2								
M6	VSS								
L5	TMS	P107	AGTOB1_A/ GTIOC1A_A	CTS0_A/ RTS0_A/SS0_A/ RSPCKA_A	MLCD_SI0	IRQ7_A/ KRM07_A			IOVCC2
M5	TDO	P106	AGTOA1_A/ GTIOC1B_A	TXD0_A/ SSDA0_A/ MOSI0_A/ SSLB0_A	MLCD_SI1	IRQ0_B/ KRM06_A	VCOUT_A		IOVCC2
N5	TDI	P105	AGTO1_A/ GTIOC4A_A	USB_EXICEN/ RXD0_A/ SSCL0_A/ MISO0_A/ MISOA_A	MLCD_SI2	IRQ8_A/ KRM05_A			IOVCC2
K4	TCK	P104	AGTIO1_A/ GTIOC4B_A	SCK0_A/ MOSIA_A	MLCD_SI3	IRQ9_A/ KRM04_A			IOVCC2
L4		P103	GTIOC5A_A	CTS2_A/ RTS2_A/SS2_A/ CTS1_A/ RTS1_A/SS1_A/ SSLA0_A	MLCD_SI4	KRM03_A			IOVCC2
N4		P102	GTIOC5B_A	TXD2_A/ SSDA2_A/ MOSI2_A/ TXD1_A/ SSDA1_A/ MOSI1_A/ IRTXD1_A/ SSLA1_A	MLCD_SI5	KRM02_A			IOVCC2

Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA) (5/6)

Pin Number	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, RIIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	MTDV	Applicable Power Supply
M4		P101	GTIOC0A_B	RXD2_A/ SSCL2_A/ MISO2_A/ RXD1_A/ SSCL1_A/ MISO1_A/ IRRXD1_A/ SSLA2_A	MLCD_SI6	KRM01_A			IOVCC2
N3		P100	GTIOC0B_B	SCK2_A/ SCK1_A/ SSLA3_A	MLCD_SI7	KRM00_A			IOVCC2
J6	VSS								
H6		P514			LEDI1				IOVCC3
J5		P513			LEDI2				IOVCC3
H5		P512			LEDI3				IOVCC3
N2		P511	GTOVUP_B/ GTIOC1B_C			KRM03_B			IOVCC3
M3		P510	GTOVLO_B/ GTIOC1A_C			KRM02_B			IOVCC3
L3		P509		USB_OVRCURB_B		KRM01_B			IOVCC3
K3		P508	GTIOC2B_C			IRQ4_B			IOVCC3
J4		P507	GTIOC2A_C	USB_ID_B		KRM00_B			IOVCC3
M2		P506				IRQ0_C	AN028		IOVCC3
L2		P505				IRQ1_C	AN027		IOVCC3
G6		P504		USB_VBUSEN_B/ CTS2_B/ RTS2_B/SS2_B			AN026		IOVCC3
G5		P503		USB_OVRCURA_B/ SCK2_B			AN025		IOVCC3
M1		P502		RXD2_B/ SSCL2_B/ MISO2_B/ RSPCKA_C			AN024		IOVCC3
K2		P501	AGTOA1_B	TXD2_B/ SSDA2_B/ MOSI2_B/ MOSIA_C		IRQ1_B	AN023		IOVCC3
J3		P500	ADTRG0_B/ AGTOB1_B/ GTOWUP_B/ GTIOC4B_C	CTS0_B/ RTS0_B/SS0_B/ MISOA_B/ QIO0_A			AN022		IOVCC3
L1	IOVCC3								
K1	VSS								
J2		P015	AGTIO1_B/ GTOWLO_B/ GTIOC4A_C	SCK0_B/ SSLA3_B/ QIO1_A		IRQ7_B	AN021		IOVCC3
H4		P014	AGTEE1_B/ GTIOC3B_C	RXD0_B/ SSCL0_B/ MISO0_B/ SSLA2_B/ QIO2_A		IRQ6_B	AN020		IOVCC3
H3		P013	AGTO1_B/ GTIOC3A_C	TXD0_B/ SSDA0_B/ MOSI0_B/ SSLA1_B/ QIO3_A					IOVCC3
H2		P012		SSLA0_B					IOVCC3
J1	CLKOUT	P011		RSPCKA_B			AN017		IOVCC3
H1		P010		MOSIA_B			AN016		IOVCC3

Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA) (6/6)

Pin Number	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC, LPG)	Communications (SCI, SPI, IIC, USB, QSPI)	Display (MLCD, LED)	Interrupts (IRQ, KINT)	Analog (S14AD, R12DA, ACMP)	MTDV	Applicable Power Supply
G4	AVCC1								
G3		P009					CMPREF		AVCC1
G2		P008					CMPIN		AVCC1
G1		P007					DA0		AVCC1
F4	AVSS1								
E4		P006					AN006		AVCC0
F3		P005					AN005		AVCC0
F1		P004					AN004		AVCC0
F2		P003					AN003		AVCC0
E5		P002					AN002		AVCC0
D3	VREFL0								
E3		P001					AN001		AVCC0
E1		P000					AN000		AVCC0
E2	VREFH0/AVTRO								
D2	AVCC0								
D1	AVSS0								
C1		P815	GTIOC5A_C	CTS4_C/ RTS4_C/SS4_C					IOVCC0
D4		P814	GTIOC5B_C	SCK4_C					IOVCC0
D5		P813		RXD4_C/ SSCL4_C/ MISO4_C					IOVCC0
D6		P812	GTIOC0A_C	TXD4_C/ SSDA4_C/ MOSI4_C					IOVCC0
C3		P811	GTIOC0B_C						IOVCC0
A1	IOVCC0*1								
A12	VBP*1								
E6	VSS*1								
F5	VSS*1								
F6	VSS*1								
H7	VSS*1								
N1		P506*1							
N12	VSS*1								

Note: Note the following points with regard to pin names.

- For the SCI and SCIG interfaces, each communications pin has multiple functions that work differently depending on the mode as follows:
RXDn/SCLn/MISO_n, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
- We recommend using the sets of pins that have the same letter ("A", "B", "C" to indicate group membership) appended to their names.
For the SPI, QSPI, and SCI interfaces, the AC portion of the electrical characteristics is measured per group.
- Pin functions that have "_DS" appended to their names can be used as inputs for trigger signals for release from deep software standby.

Note 1. If connection of any among the A1, A12, E6, F5, F6, H7, N1, and N12 pins is not possible for space-related reasons, the pins can be handled as N.C. (not connected).

2. CPU

This LSI chip is based on the Arm® Cortex®-M0+ CPU core.

2.1 Overview

2.1.1 CPU

- Arm® Cortex-M0+
 - Revision: r0p1-00rel0
 - Arm®v6-M architecture profile
 - Single-cycle integer multiplier
- Memory Protection Units (MPU)
 - Arm®v6 Protected Memory System Architecture
 - Eight protected regions
- SysTick timer
 - Driven by LOCO clock (32.768 kHz ± 30%)

For details, see reference 1. and reference 2. in section 2.8.

2.1.2 Debug

- Arm® CoreSight™ MTB-M0+
 - Revision: r0p1-00rel0
 - Buffer size: 32-Kbyte MTB RAM
- Data Watchpoint Unit (DWT)
 - Two comparators for watchpoints
- Breakpoint Unit (BPU)
 - Four instruction comparators
- CoreSight Debug Access Port (DAP)
 - Serial Wire Debug Port (SW-DP)
- Debug Register Module (DBGREG)
 - Reset control
 - Stop control

For details, see reference 1. and reference 2. in section 2.8.

2.1.3 Operating Frequency

- CPU core: maximum 64 MHz
- Serial Wire Data (SWD) interface: maximum 12.5 MHz

Figure 2.1 shows the block diagram of the Cortex-M0+ CPU.

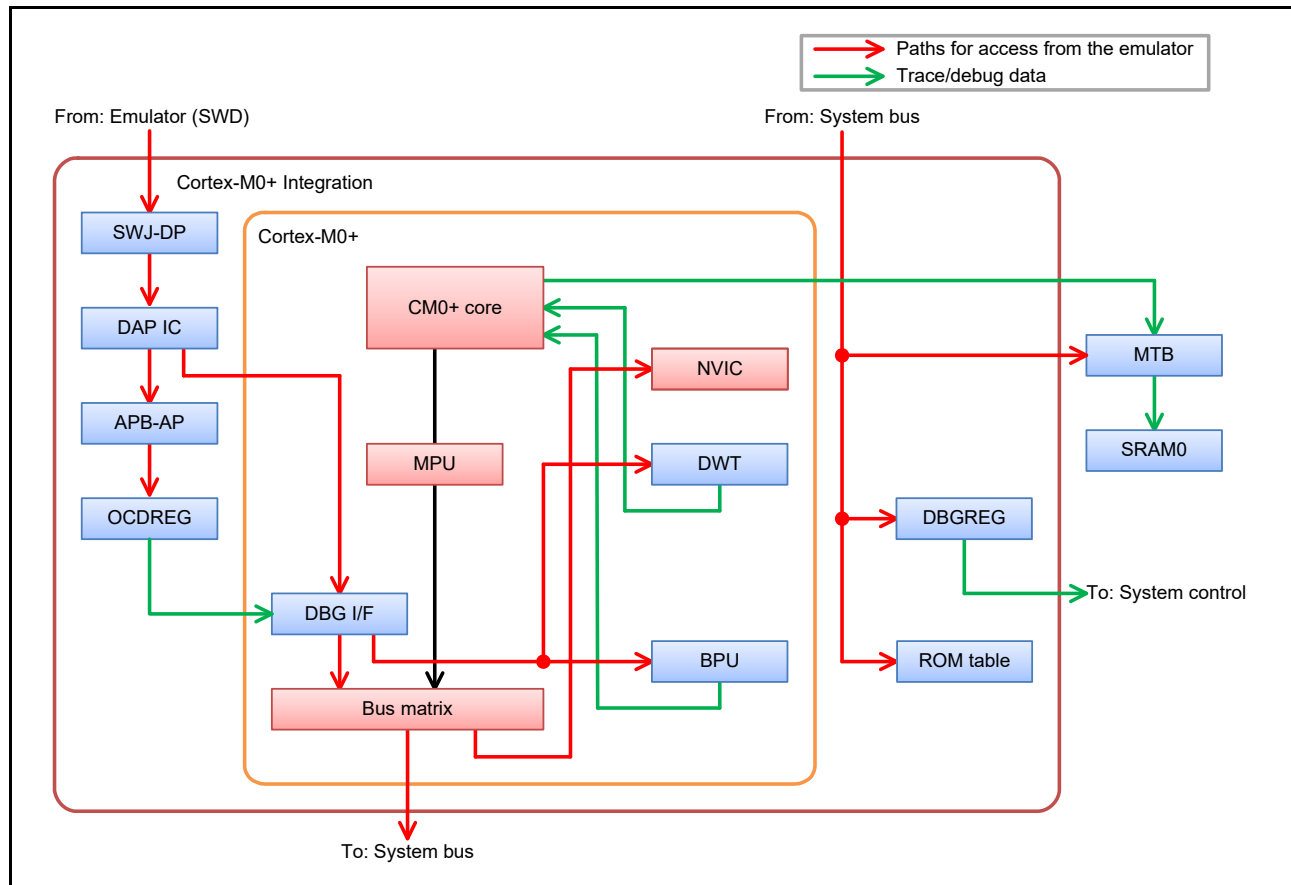


Figure 2.1 Cortex-M0+ CPU Block Diagram

2.2 Implementation Options

Table 2.1 Implementation Options

Option	Implementation
MPU	Included, 8 memory protection regions
Single-cycle multiplier	Included
Number of interrupts	32
Sleep mode power saving	Sleep mode and other low power consumption modes are supported. For details, see section 12, Power-Saving Functions in the User's Manual: Hardware. Note: SCB.SCR.SLEEPDEEP is ignored.
Endianness	Little endian
SysTick timer	See reference 3. in section 2.8.
System reset request output	The SYSRESETREQ bit in the application interrupt and reset control register causes a CPU reset.
Vector table offset register	Included

For details, see reference 3. in section 2.8.

2.3 SWD Interface

The LSI chip supports the SWD interface as a debug interface.

Table 2.2 lists the SWD pins.

Table 2.2 SWD Pins

Pin Name	I/O	Function	When not in Use
SWCLK	Input	Serial wire clock input pin	Pull-up
SWDIO	I/O	Serial wire data I/O pin	Pull-up

2.4 Debug Mode

2.4.1 Debug Mode Definition

Table 2.3 shows the debug modes and conditions.

Table 2.3 Debug Modes and Conditions

Conditions		Mode	
Connection with the Emulator	SWD Authentication	Debug Mode	Debug Authentication
Not connected	—	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	On-chip debug (OCD) mode	Enabled

Note: Whether the emulator is connected or not can be determined from the value of the CDBGPWRUPREQ bit in the SWJ-DP register. The bit can only be written by the emulator. Read the DBGSTR.CDBGPWRUPREQ bit to confirm the value of this bit.

Note: Debug authentication is defined by the Arm®v6-M architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both of them are not permitted.

2.4.2 Effects of Debug Mode

The debug mode effects occur both internal and external to the CPU. This section describes the effects of the debug mode.

2.4.2.1 Low Power Consumption Mode

All CoreSight debug components can store the register settings even when the CPU enters software standby, snooze, or deep software standby mode. However, AHB-AP cannot respond to on-chip debug (OCD) access in these low power consumption modes. It means the emulator must wait for cancellation of the low power consumption mode to access the CoreSight debug components. In this case, the emulator can request low power consumption mode cancellation by using the DBIRQ bit in the MCUCTRL register. For details, see section 2.5.6.3, MCU Control Register (MCUCTRL).

2.4.2.2 Resets

In OCD mode, the effectiveness of some types of reset depends on the state of the CPU at the time and the settings of bits of the DBGSTOPCR register.

Table 2.4 Reset or Interrupt and Mode Setting

Reset or Interrupt Name	Control in On-chip Debug (OCD) Mode	
	OCD Break Mode	OCD Run Mode
RES# pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on the settings of bits of the DBGSTOPCR register.
Watchdog timer reset/interrupt	Does not occur*1	Depends on the settings of bits of the DBGSTOPCR register.
Voltage monitor 0 reset	Depends on the settings of bits of the DBGSTOPCR register.	
Voltage monitor 1 reset/interrupt	Depends on the settings of bits of the DBGSTOPCR register.	
Voltage monitor BAT reset/interrupt	Depends on the settings of bits of the DBGSTOPCR register.	
Bus master MPU reset/interrupt	Same as user mode	
Bus slave MPU reset/interrupt	Same as user mode	
Stack pointer error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
MINPWON mode reset	Same as user mode	
Software reset	Same as user mode	

Note: OCD break mode means that the CPU is halted, and OCD run mode means that the CPU is not halted.

Note 1. The IWDT and WDT always stop in OCD break mode.

2.5 Programmers Model

2.5.1 Address Spaces

The debugging system in this LSI chip has two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD-dedicated registers.

Figure 2.2 shows the block diagram of the AP connection and address spaces.

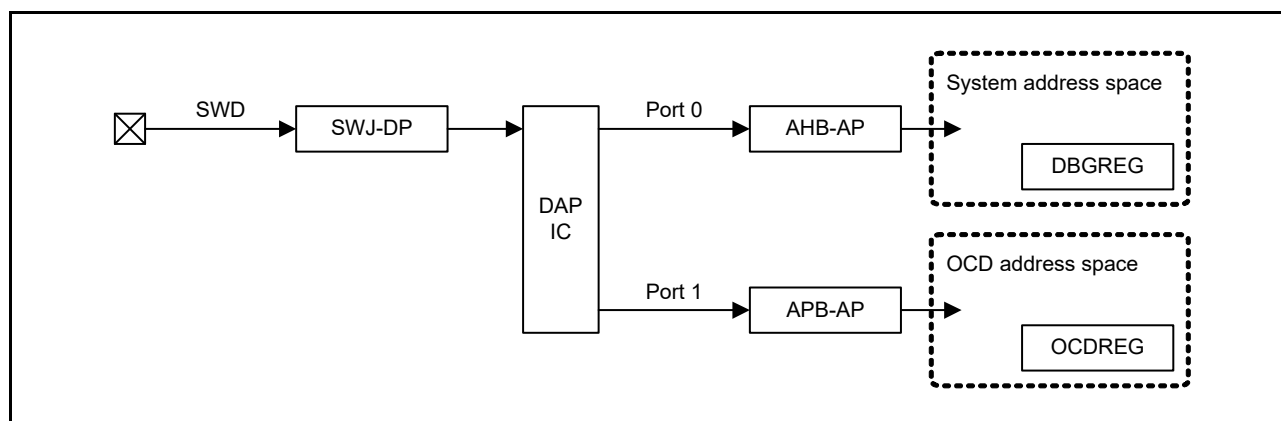


Figure 2.2 Block Diagram of the AP Connection and Address Spaces

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the emulator, the CPU, and other bus masters in the chip. OCDREG is located in the OCD address space and can be accessed only from the emulator. The CPU and other bus masters cannot access the OCD-dedicated registers.

2.5.2 Cortex-M0+ Peripheral Address Map

In system address space, the Cortex-M0+ has a Private Peripheral Bus (PPB), which can be accessed only from the CPU and emulator. Table 2.5 shows the Cortex-M0+ peripheral address map.

Table 2.5 Peripheral Address Map

Component Name	Start Address	End Address	Note
DWT	E000 1000h	E000 1FFFh	See reference 2. in section 2.8.
BPU	E000 2000h	E000 2FFFh	See reference 2. in section 2.8.
SCS	E000 E000h	E000 EFFFh	See reference 2. in section 2.8.
ROM table	E00F F000h	E00F FFFFh	See section 2.5.4, CoreSight ROM Table and reference 5. in section 2.8.

2.5.3 External Debug Address Map

In the system address space, the Cortex-M0+ core has external debug components. These components can be accessed from the CPU and other bus masters through the system bus. Table 2.6 shows the address map of the Cortex-M0+ external debug components.

Table 2.6 Address Map of External Debug Components

Component Name	Start Address	End Address	Note
MTB (RAM area)	2000 0000h	2000 7FFFh	The Micro Trace Buffer (MTB) has 32 Kbytes of available RAM. See reference 6. in section 2.8.
MTB (SFR area)	4001 9000h	4001 9FFFh	See reference 6. in section 2.8.
ROM table	4001 A000h	4001 AFFFh	See reference 6. in section 2.8.

2.5.4 CoreSight ROM Table

This LSI chip has two CoreSight ROM tables. One ROM table holds a list of external debug components and a pointer to Arm® components. The other ROM table holds a list of Arm® components.

2.5.4.1 ROM Entries

Table 2.7 shows the ROM table which contains the pointers to the Arm® system area and user area component information.

Table 2.8 shows the ROM table which contains Arm® system area component information. For details, see references 5. and 6. in section 2.8.

Table 2.7 ROM Table (1)

Address	Access Size	R/W	Value	Target Component
4001 A000h	32 bits	R	A00E 5003h	Arm® Cortex-M0+ processor
4001 A004h	32 bits	R	FFFF F003h	MTB
4001 A008h	32 bits	R	0000 0000h	(End marker for the ROM tables)

Table 2.8 ROM Table (2)

Address	Access Size	R/W	Value	Target Component
E00F F000h	32 bits	R	FFF0 F003h	The SCS is mounted here.
E00F F004h	32 bits	R	FFF0 2003h	The DWT is mounted here.
E00F F008h	32 bits	R	FFF0 3003h	The BPU is mounted here.
E00F F00Ch	32 bits	R	0000 0000h	(End marker for the ROM tables)

2.5.4.2 CoreSight Registers

The CoreSight ROM table has CoreSight registers defined in the Arm® CoreSight architecture. Table 2.9 and Table 2.10 show the registers. See reference 5. in section 2.8 for details on each register.

Table 2.9 CoreSight Registers in the CoreSight ROM Table (Renesas Unique ID)

Name	Address	Access Size	R/W	Initial Value
Arm® CM0+	4001 A000h	32 bits	R	A00E 5003h
MTB	4001 A004h	32 bits	R	FFFF F003h
PID4	4001 AFD0h	32 bits	R	0000 0004h
PID5	4001 AFD4h	32 bits	R	0000 0000h
PID6	4001 AFD8h	32 bits	R	0000 0000h
PID7	4001 AFDCh	32 bits	R	0000 0000h
PID0	4001 AFE0h	32 bits	R	0000 002Ah
PID1	4001 AFE4h	32 bits	R	0000 0030h
PID2	4001 AFE8h	32 bits	R	0000 000Ah
PID3	4001 AFECCh	32 bits	R	0000 0000h
CID0	4001 AFF0h	32 bits	R	0000 000Dh
CID1	4001 AFF4h	32 bits	R	0000 0010h
CID2	4001 AFF8h	32 bits	R	0000 0005h
CID3	4001 AFFCh	32 bits	R	0000 00B1h

Table 2.10 CoreSight Registers in the CoreSight ROM Table (CoreSight-ID)

Name	Address	Access Size	R/W	Initial Value
SCS	E00F F000h	32 bits	R	FFF0 F003h
DWT	E00F F004h	32 bits	R	FFF0 2003h
BPU	E00F F008h	32 bits	R	FFF0 3003h
PID4	E00F FFD0h	32 bits	R	0000 0004h
PID5	E00F FFD4h	32 bits	R	0000 0000h
PID6	E00F FFD8h	32 bits	R	0000 0000h
PID7	E00F FFDCCh	32 bits	R	0000 0000h
PID0	E00F FFE0h	32 bits	R	0000 00C0h
PID1	E00F FFE4h	32 bits	R	0000 00B4h
PID2	E00F FFE8h	32 bits	R	0000 000Bh
PID3	E00F FFECCh	32 bits	R	0000 0000h
CID0	E00F FFF0h	32 bits	R	0000 000Dh
CID1	E00F FFF4h	32 bits	R	0000 0010h
CID2	E00F FFF8h	32 bits	R	0000 0005h
CID3	E00F FFFCh	32 bits	R	0000 00B1h

2.5.5 DBGREG

DBGREG is a register module that controls the debug functions. DBGREG is implemented as a CoreSight-compliant component.

Table 2.11 lists the DBGREG registers excluding the CoreSight registers.

Table 2.11 DBGREG Registers Other than CoreSight

Name		DAP Port	Address	Access Size	R/W
Debug status register	DBGSTR	Port 0	4001 B000h	32 bits	R
Debug stop control register	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W

2.5.5.1 Debug Status Register (DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPW RUPACK	CDBGPW RUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0.	R
b28	CDBGPW PREQ	Debug Power-up Request	0: The emulator is not requesting debug power-up. 1: The emulator is requesting debug power-up.	R
b29	CDBGPW PACK	Debug Power-up Acknowledge	0: A debug power-up request is being received. 1: A debug power-up request is not being received.	R
b31, b30	—	Reserved	These bits are read as 0.	R

This register is a status register which indicates the state of the debug power-up request to the chip from the emulator.

2.5.5.2 Debug Stop Control Register (DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_LVDBAT	DBGSTOP_LVD1	DBGSTOP_LVD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	DBGSTOP_IWDT	Mask Bit for IWDT Reset/Interrupt	0: Enable IWDT reset/interrupt. 1: Mask IWDT reset/interrupt and stop IWDT count.	R/W
b1	DBGSTOP_WDT	Mask Bit for WDT Reset/Interrupt	0: Enable WDT reset/interrupt. 1: Mask WDT reset/interrupt and stop WDT count.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DBGSTOP_LVD0	Mask Bit for LVD0 Reset	0: Enable LVD0 reset. 1: Mask LVD0 reset.	R/W
b17	DBGSTOP_LVD1	Mask Bit for LVD1 Reset/Interrupt	0: Enable LVD1 reset/interrupt. 1: Mask LVD1 reset/interrupt.	R/W
b18	DBGSTOP_LVDBAT	Mask Bit for LVDBAT Reset/Interrupt	0: Enable LVDBAT reset/interrupt. 1: Mask LVDBAT reset/interrupt.	R/W
b31 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The debug stop control register (DBGSTOPCR) controls certain resets and interrupts in the OCD mode. In user mode, the settings of the bits in this register do not affect the operation of the chip.

2.5.5.3 DBGREG CoreSight Registers

DBGREG has CoreSight registers defined in the Arm® CoreSight architecture. Table 2.12 lists these registers. See reference 5. in section 2.8 for details on each register.

Table 2.12 DBGREG CoreSight Registers

Name	Address	Access Size	R/W	Initial Value
PID4	4001 BFD0h	32 bits	R	0000 0004h
PID5	4001 BFD4h	32 bits	R	0000 0000h
PID6	4001 BFD8h	32 bits	R	0000 0000h
PID7	4001 BFDCh	32 bits	R	0000 0000h
PID0	4001 BFE0h	32 bits	R	0000 0005h
PID1	4001 BFE4h	32 bits	R	0000 0030h
PID2	4001 BFE8h	32 bits	R	0000 001Ah
PID3	4001 BFECh	32 bits	R	0000 0000h
CID0	4001 BFF0h	32 bits	R	0000 000Dh
CID1	4001 BFF4h	32 bits	R	0000 00F0h
CID2	4001 BFF8h	32 bits	R	0000 0005h
CID3	4001 BFFCh	32 bits	R	0000 00B1h

2.5.6 OCDREG

The OCDREG registers are only accessible by the emulator. OCDREG is implemented as a CoreSight-compliant component.

Table 2.13 lists the OCDREG registers.

Table 2.13 OCDREG Registers

Name		DAP Port	Address	Access Size	R/W
ID authentication code register 0	IAUTH0	Port 1	8000 0000h	32 bits	W
ID authentication code register 1	IAUTH1	Port 1	8000 0100h	32 bits	W
ID authentication code register 2	IAUTH2	Port 1	8000 0200h	32 bits	W
ID authentication code register 3	IAUTH3	Port 1	8000 0300h	32 bits	W
MCU status register	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU control register	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

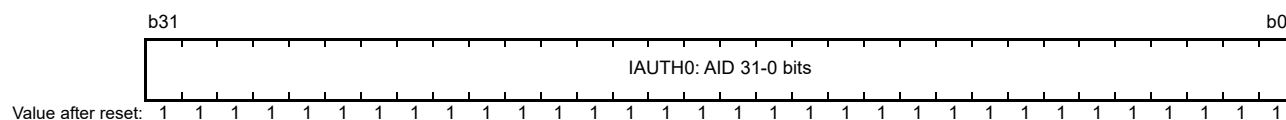
Note: OCDREG is located in dedicated OCD address space. This address space is independent of the system address space.

2.5.6.1 ID Authentication Code Register (IAUTH0 to IAUTH3)

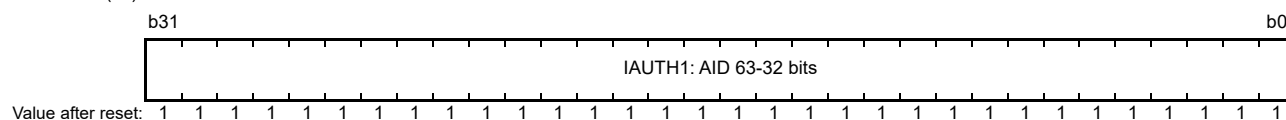
These registers are authentication registers used for the writing of a 128-bit key. These registers must be written in sequential order from IAUTH0 register to IAUTH3 register.

The initial value of the registers is all FFFF FFFFh. This means that SWD access is initially permitted when ID code in the OSIS register has the initial value. See section 2.7.1, Unlock ID Code.

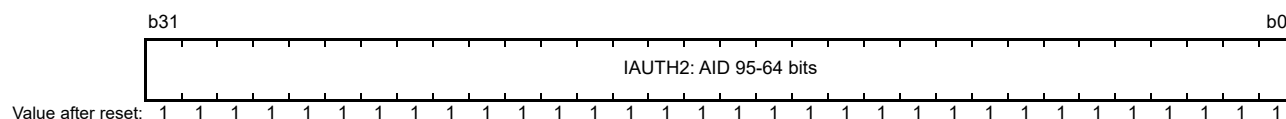
Address(es): IAUTH0 8000 0000h



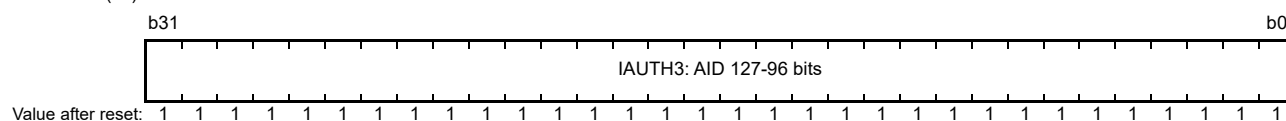
Address(es): IAUTH1 8000 0100h



Address(es): IAUTH2 8000 0200h



Address(es): IAUTH3 8000 0300h



2.5.6.2 MCU Status Register (MCUSTAT)

Address(es): MCUSTAT 8000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0 *1	1/0 *1	0

Bit	Symbol	Bit Name	Description	R/W
b0	AUTH	Debugger Authentication Flag	0: Authentication failed. 1: Authentication succeeded.	R
b1	CPUSLEEP	Sleep Status Flag	0: CPU is not in sleep mode. 1: CPU is in sleep mode.	R
b2	CPUSTOPCLK	Stop Status Flag	0: The clock is being supplied to the CPU. 1: Supply of the clock to the CPU is stopped.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Note 1. Depends on the state of this chip.

2.5.6.3 MCU Control Register (MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EDBGRQ	External Debug Request	0: Debug event not requested. 1: Debug event requested. Writing 1 to this bit causes a CPU halt. This bit is cleared by either of the following conditions. • Writing 0 to the EDBGRQ bit • CPU is halted.	R/W
b7 to b1	—	Reserved	These bits are read as 0.	R
b8	DBIRQ	Debug Interrupt Request	0: Debug interrupt not requested. 1: Debug interrupt requested. Writing 1 to this bit wakes up the chip from low power consumption mode.	R/W
b31 to b9	—	Reserved	These bits are read as 0.	R

Note: Set the DBIRQ and EDBGRQ bits to the same value.

2.5.6.4 OCDREG CoreSight Registers

OCDREG has CoreSight registers defined in the Arm® CoreSight architecture.

Table 2.14 lists these registers. See reference 5. in section 2.8 for details on each register.

Table 2.14 OCDREG CoreSight Registers

Name	Address	Access Size	R/W	Initial Value
PID4	8000 0FD0h	32 bits	R	0000 0004h
PID5	8000 0FD4h	32 bits	R	0000 0000h
PID6	8000 0FD8h	32 bits	R	0000 0000h
PID7	8000 0FDCh	32 bits	R	0000 0000h
PID0	8000 0FE0h	32 bits	R	0000 0004h
PID1	8000 0FE4h	32 bits	R	0000 0030h
PID2	8000 0FE8h	32 bits	R	0000 000Ah
PID3	8000 0FECh	32 bits	R	0000 0000h
CID0	8000 0FF0h	32 bits	R	0000 000Dh
CID1	8000 0FF4h	32 bits	R	0000 00F0h
CID2	8000 0FF8h	32 bits	R	0000 0005h
CID3	8000 0FFCh	32 bits	R	0000 00B1h

2.6 SysTick Timer

This LSI chip has a SysTick timer that provides a simple 24-bit down counter. The timer can select ICLK or SYSTICCLK reference clock.

For details, see section 9, Clock Generation Circuit in the User's Manual: Hardware and reference 1. in section 2.8.

2.7 Connection with the Emulator

This LSI chip has an SWD authentication mechanism to check permission for access to chip resources for debugging. Permission for full debug functionality requires passing the authentication process.

Figure 2.3 shows the block diagram of the authentication mechanism.

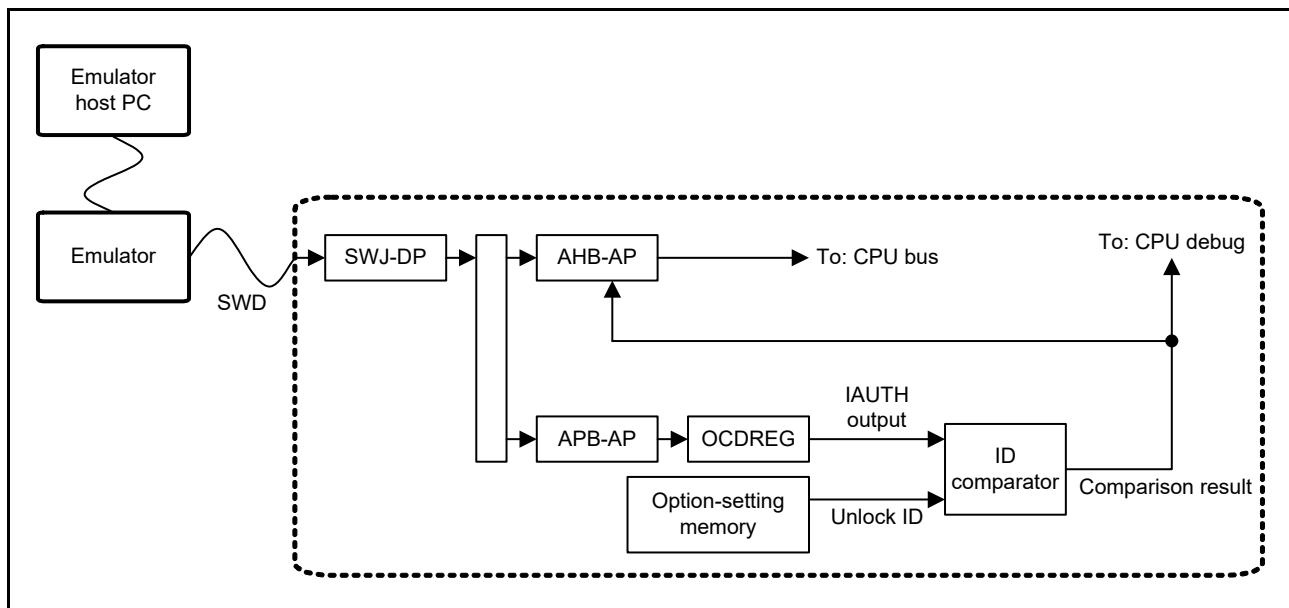


Figure 2.3 SWD Authentication Mechanism Block Diagram

The LSI chip includes an ID comparator for use in SWD authentication. The comparator compares the 128-bit IAUTH output value from the given registers in the OCDREG space with the 128-bit unlock ID code written in the OCD/serial programmer ID setting register (OSIS) in the option-setting memory. The two outputs being identical represents a pass in SWD authentication and use of the CPU debug functions and system bus access from the emulator are permitted. After passing SWD authentication, the emulator must set the DBGEN bit in the system control OCD control register (SYOCDCR). In addition, the emulator must clear the DBGEN bit before disconnection. See the description of the SYOCDCR register in section 12, Power-Saving Functions in the User's Manual: Hardware.

2.7.1 Unlock ID Code

The unlock ID code is used for checking permissions for the CPU debug functions and system bus access. If the unlock ID code matches the 128-bit data written in the IAUTH0 to IAUTH3 registers, the SWD debugger obtains access permission. Unlock ID code is written in the OCD/serial programmer ID setting register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFFh). For details on the OSIS register, see section 7, Option-Setting Memory in the User's Manual: Hardware.

2.7.2 Restrictions on Connecting an Emulator

To start a SWD connection from an emulator, the chip must be able to enter OCD mode. To do so, however, there are some restrictions depending on the current chip state. Table 2.15 lists in which mode and power consumption state the chip can transition to OCD mode.

Since the chip cannot transition to OCD mode while in EXFPWON and normal modes, MINPWON and normal modes, or VBB mode, change the chip to OCD mode while in ALLPWON and normal modes, and then change it to EXFPWON and normal modes, MINPWON and normal modes, or VBB mode in order to carry out debugging in EXFPWON and normal modes, MINPWON and normal modes, or VBB mode. For details, see section 12, Power-Saving Functions in the User's Manual: Hardware.

Table 2.15 State of the LSI Chip That can Transition to OCD Mode

Current Operating Mode before Transitioning to OCD Mode			Transition to OCD Mode
Power Control Mode	Power Supply Mode	Low Power Consumption Modes	
Boost mode	—	Operating mode	Possible*1
		Sleep mode	Possible*1
Normal mode	ALLPWON mode	Operating mode	Possible*1
		Sleep mode	Possible*1
		Snooze mode	Impossible
		Software standby mode	Impossible
		Deep software standby mode	Impossible
	EXFPWON mode MINPWON mode	All modes	Impossible
VBB mode	ALLPWON mode EXFPWON mode MINPWON mode	All modes	Impossible
Mode transition period			Impossible

Note 1. After transition to the OCD mode, set 1 to the SYOCDCCR.DBGEN bit (on-chip debugger enable). For details on the SYOCDCCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCCR) in the User's Manual: Hardware.

2.7.2.1 Mode Transitions while in OCD Mode

Some restrictions apply to mode transitions while in OCD mode. Table 2.16 lists availability of mode transitions between the power control modes.

Table 2.16 Availability of Mode Transitions between the Power Control Modes while in OCD Mode

Current Power Control Mode	Power Control Mode to Transition to	Availability of Mode Transitions between the Power Control Modes
Boost mode	Normal mode	Impossible
Normal mode	Boost mode	Impossible
	VBB mode	Possible*1, *2
VBB mode	Normal mode	Possible*1

Note 1. Although power control mode transition between normal and VBB modes is possible, the state of the power in normal mode is maintained in order to continue debugging. Functions such as state flagging can be emulated.

Note 2. After transition to the OCD mode while in ALLPWON and normal modes, set the SYOCDCCR.DBGEN bit to 1 (on-chip debugger enable) before transition to the VBB mode. For details on the SYOCDCCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCCR) in the User's Manual: Hardware.

After transition to the OCD mode while in ALLPWON and normal modes, set the SYOCDCCR.DBGEN bit to 1 (on-chip debugger enable) before transition to EXFPWON or MINPWON mode. For details on the SYOCDCCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCCR) in the User's Manual: Hardware.

2.7.2.2 Entering Low Power Consumption Mode while in OCD Mode

The chip can enter low power consumption mode even while it is in OCD mode.

After transition to the OCD mode, set the SYOCDRCR.DBGEN bit to 1 (on-chip debugger enable) before transition to low power consumption mode. For details on the SYOCDRCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDRCR) in the User's Manual: Hardware.

If system bus access is required and the chip is in software standby, snooze, or deep software standby mode, set the MCUCTRL.DBIRQ bit in OCDREG to 1 to wake the chip up from the low power consumption mode. Simultaneously, using the MCUCTRL.EDBGRQ bit in OCDREG, the emulator can wake up the chip without starting CPU execution. Table 2.17 lists availability of access to system bus while in OCD mode.

Table 2.17 Availability of Access to System Bus while in OCD Mode

Current Mode	Current Low Power Consumption Mode	Access to System Bus
Boost mode	Operating mode	Possible
	Sleep mode	Possible
Normal mode	Operating mode	Possible
	Sleep mode	Possible
	Snooze mode	Impossible
	Software standby mode	Impossible
	Deep software standby mode	Impossible
VBB mode	Operating mode	Possible
	Sleep mode	Possible
	Snooze mode	Impossible
	Software standby mode	Impossible
	Deep software standby mode	Impossible
Mode transition period		Impossible

2.7.2.3 Modifying the Unlock ID Code in the OSIS Register

Modifying the unlock ID code in the OSIS register requires placing the chip in the reset state by asserting the signal on the RES# pin or setting the SYSRESETREQ bit of the application interrupt and reset control register in the system control block to 1. The modified unlock ID code is reflected after the reset. For the system control block, see reference 2. listed in section 2.8.

The emulator must set the modified unlock ID code in the IAUTH0 to IAUTH3 registers immediately before the chip is placed in the reset state. When the IAUTH0 to IAUTH3 registers have been overwritten, writing to the SYSRESETREQ bit is not possible. Place the chip in the reset state by asserting the signal on the RES# pin.

2.7.2.4 Connecting Sequence and SWD Authentication

Protection of the connection with the emulator by the SWD authentication mechanism means that input of an unlock ID code to the SWD authentication registers will be required in some cases. The value for the OSIS register in the option-setting memory decides whether the input of an unlock ID code is required or not. After de-asserting the signal on the RES# pin, a waiting time is required before comparison with the OSIS register value following cold start. For the waiting time after de-assertion of the signal on the RES# pin, see section 6.3.3, Reset Timing in section 6, Electrical Characteristics.

The SWD authentication process is described in detail below.

- (1) When MSB of the OSIS register is 0 (bit 127 = 0)

The ID code is always mismatching, and the connection to the emulator is prohibited.

- (2) When bits in the OSIS register are all 1s (the initial value)

ID authentication is not required and the emulator can use AHB-AP without the authentication.

For details of the settings for using the AHB-AP, see reference 4. in section 2.8.

1. Connect the emulator to the chip through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the emulator must assert CDBGPWRUPREQ in the SWJ-DP control status register, then must wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up AHB-AP to access the system address space. AHB-AP is connected to the DAP bus port 0.
4. Start accessing the system bus using AHB-AP.

- (3) When the value in the OSIS register becomes “ALeRASE” in ASCII code

Data in the flash memory are deleted. For details, see section 57, Flash Memory in the User’s Manual: Hardware.

1. Set the ASCII code “ALeRASE” (414C 6552 4153 45FF FFFF FFFF FFFF FFFFh) in the IAUTH0 to IAUTH3 registers.
2. Place the chip in the reset state.
3. Wait until MCUSTAT.CPUSTOPCLK = 1 (deletion completed).
4. Reset the chip then release it from the reset state so that it enters the OCD mode.
5. Confirm that all bits of the unlock ID code are 1 (the code is FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFFh).

- (4) When bits in the OSIS register are not all 1s

ID authentication is required and the emulator must write the 128-bit unlock ID code to the IAUTH0 to IAUTH3 registers in OCDREG before using AHB-AP.

1. Connect the emulator to the chip through the SWD interface.
2. Set up the SWJ-DP to access the DAP bus. In the setup, the emulator must assert CDBGPWRUPREQ in the SWJ-DP control status register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up APB-AP to access OCDREG. APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit unlock ID code to the IAUTH0 to IAUTH3 registers in OCDREG using APB-AP.
5. If the 128-bit unlock ID code matches the OSIS register value, AHB-AP is authorized to issue an AHB transaction. The authentication result can be confirmed in the AUTH bit in the MCUSTAT register or the DbgStatus bit in the AHB-AP control status word register.
 - When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
 - When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.
6. Set up AHB-AP to access the system address space. AHB-AP is connected to the DAP bus port 0.
7. Start accessing the CPU debug resources using AHB-AP.

2.8 References

1. ARM® v6-M Architecture Reference Manual (ARM DDI 0419E)
2. Cortex™-M0+ Technical Reference Manual (ARM DDI 0484C)
3. Cortex™-M0+ Devices Generic User Guide (ARM DUI 0662B)
4. Arm® CoreSight™ SoC-400 Technical Reference Manual (ARM DDI 0480G)
5. Arm® CoreSight™ Architecture Specification (ARM IHI 0029E)
6. CoreSight™ MTB-M0+ Technical Reference Manual (ARM DDI 0486B)

3. Startup Modes

3.1 Types and Selection of Startup Mode

Table 3.1 shows the startup modes selected by the levels on the mode setting pins (MD and EHMD). For details on each of the startup modes, see section 3.2, Details of Startup Modes.

Table 3.1 Types of Startup Mode Selected by the Levels on the Startup Mode Setting Pin and Energy Harvesting Mode Setting Pin

Mode Setting Pins		Startup Mode
MD	EHMD	
High	High	Energy harvesting startup mode
	Low	Normal startup mode
Low	—	SCI/USB boot mode

3.2 Details of Startup Modes

3.2.1 Normal Startup and Energy Harvesting Startup Modes

In normal startup and energy harvesting startup modes, all input and output pins are available for use as input or output ports, inputs or outputs for peripheral functions, or as interrupt inputs. When release from the reset state proceeds while the MD pin is high, the LSI chip starts in normal startup or energy harvesting startup mode and starts running the program in the code flash memory. The EHMD pin can be used to select normal startup or energy harvesting startup. For details, see section 3.3.2, Power-up Sequence.

3.2.2 Serial Programming Mode

3.2.2.1 SCI Boot Mode

In this mode, the code flash memory modifying program (boot program) stored in a dedicated area within the chip is started up. The code flash memory can be modified from outside the chip by using the asynchronous interface (SCIg). For details, see section 57, Flash Memory in the User's Manual: Hardware.

The LSI chip starts in the serial programming mode if the MD pin is held low on release from the reset state. After startup in the serial programming mode, the boot program selects the SCI.

3.2.2.2 USB Boot Mode

In this mode, the code flash memory modifying program (boot program) stored in a dedicated area within the chip is started up. The code flash memory can be modified from outside the chip by using the USB. For details, see section 57, Flash Memory in the User's Manual: Hardware.

The chip starts in the serial programming mode if the MD pin is held low on release from the reset state. After startup in the serial programming mode, the boot program selects the USB.

3.2.3 On-chip Debug Mode

In this mode, the chip can be externally controlled by connecting an external emulator or flash memory programmer through the SWD interface.

3.3 Startup Mode Transitions

3.3.1 Startup Mode Determined by the Mode Setting Pins

Figure 3.1 shows startup mode transitions determined by the settings of the MD pin and the EHMD pin.

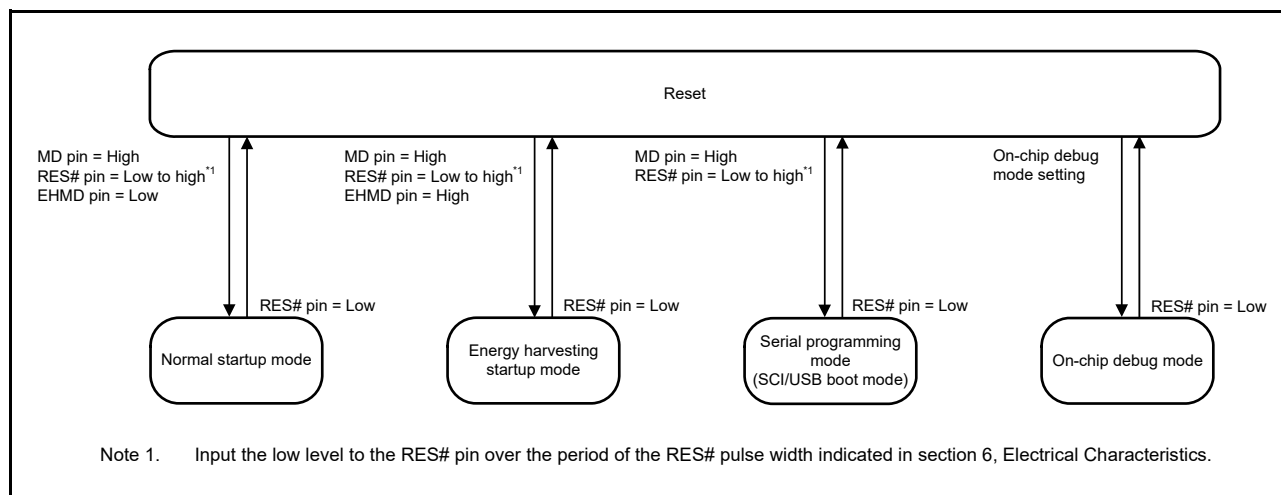


Figure 3.1 Startup Mode Determined by Levels on the Startup Mode Setting Pin and Energy Harvesting Mode Setting Pin

3.3.2 Power-up Sequence

The normal startup or energy harvesting startup mode is selected by the state of the EHMD pin on release from the reset state as shown in Table 3.2.

Table 3.2 Types of Startup Mode Selected by the State of the EHMD Pin

EHMD Pin State	Startup Mode
Low	Normal startup mode
High	Energy harvesting startup mode

The procedure for using the low leakage current mode as one of power control modes depends on the selected startup mode.

In the normal startup mode, the LSI chip starts with the back bias voltage control (VBBC) circuit disabled. Using the low leakage current mode after normal startup requires waiting for completion of the startup setting and initial setup of the VBBC circuit after release from the internal reset state. The initial setup of the VBBC circuit is the operation of charging an external capacitor connected between VBP and VBN. Setting the back bias voltage control (VBBC) enable bit (VBBCR.VBBEN) to 1 starts this initial setup. When the initial setup is completed, the back bias voltage control (VBBC) initial setup completion flag (VBBST.VBBSTUP) is set to 1. Transition to the low leakage current mode becomes possible when the VBBST.VBBSTUP flag is 1.

In the energy harvesting startup mode, the initial setup of the VBBC circuit starts and is completed during the internal reset period. Consequently, the chip can enter the low leakage current mode immediately, since the VBBCR.VBBEN bit and the VBBST.VBBSTUP flag will be 1 at the time of release from the internal reset state. Although the internal reset period for the energy harvesting startup mode is longer than that for the normal startup mode, the amount of current drawn is reduced during the initial setup of the VBBC circuit.

For details on the low leakage current mode, see section 12, Power-Saving Functions in the User's Manual: Hardware.

4. Address Space

4.1 Address Space

This LSI chip supports a 4-Gbyte linear address space from 0000 0000h to FFFF FFFFh, that can contain both programs and data.

Figure 4.1 shows the memory map.

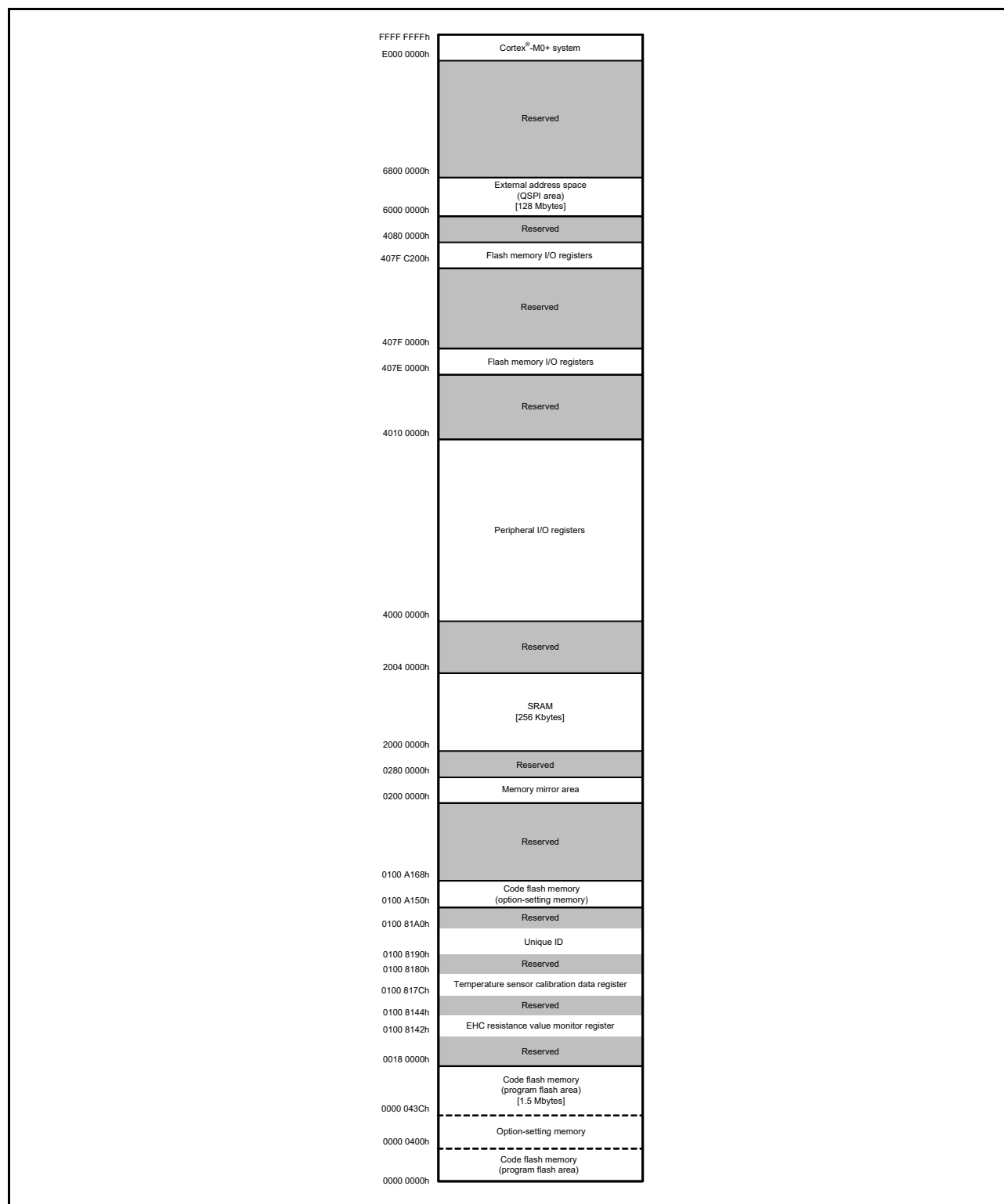


Figure 4.1 Memory Map

4.2 External Address Space

The QSPI area is provided as external address space. The QSPI area is divided into two areas, the QSPI I/O registers, and external SPI device space.

Figure 4.2 shows the address ranges associated with the QSPI area.

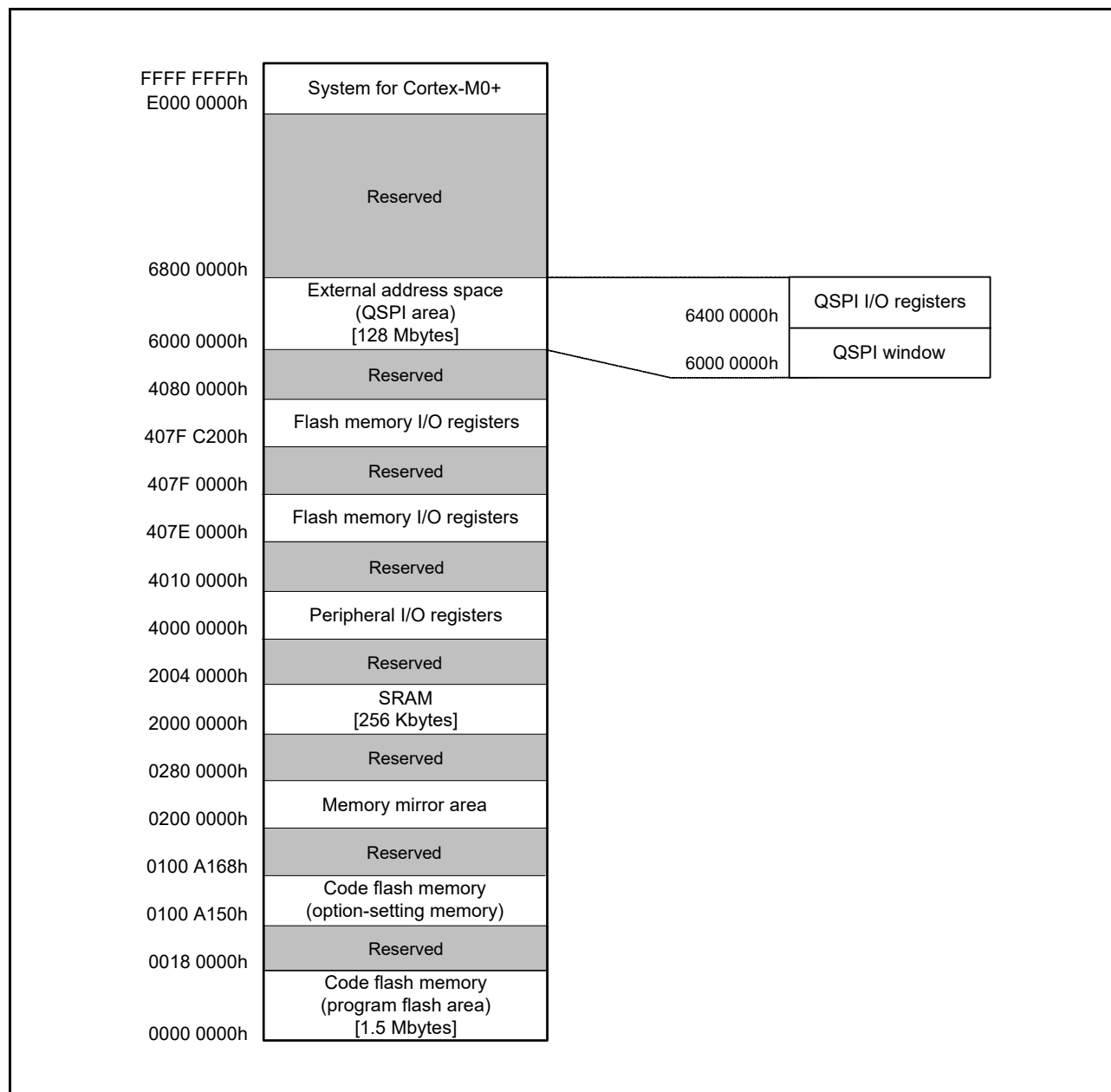


Figure 4.2 External Address Space

5. I/O Registers

This section describes I/O register addresses and access cycles by function.

5.1 Address Information

Table 5.1 lists the address information for I/O registers in this product.

Table 5.1 I/O Register Address (1/2)

Start Address	End Address	Module Symbol	Description
4000 0000h	4000 4FFFh	MPU, MMF, BUS	Memory Protection Unit, memory mirror function, bus control
4000 5000h	4000 5FFFh	DMAC, DTC	DMA controller, data transfer controller
4000 6000h	4000 6FFFh	ICU	Interrupt controller
4001 9000h	4001 9FFFh	MTB	Debug function (MTB)
4001 A000h	4001 AFFFh	FLASH	Flash memory
4001 B000h	4001 BFFFh	DBG	Debug function
4001 E000h	4001 EFFFh	SYSTEM	System control
4004 0000h	4004 001Fh	PORT0	Port 0 control register
4004 0020h	4004 003Fh	PORT1	Port 1 control register
4004 0040h	4004 005Fh	PORT2	Port 2 control register
4004 0060h	4004 007Fh	PORT3	Port 3 control register
4004 0080h	4004 009Fh	PORT4	Port 4 control register
4004 00A0h	4004 00BFh	PORT5	Port 5 control register
4004 00C0h	4004 00DFh	PORT6	Port 6 control register
4004 00E0h	4004 00FFh	PORT7	Port 7 control register
4004 0100h	4004 011Fh	PORT8	Port 8 control register
4004 0800h	4004 0CFFh	PFS	Port mn pin function select register
4004 0D00h	4004 0FFFh	PMISC	Miscellaneous port control register
4004 1000h	4004 10FFh	ELC	Event link controller
4004 1240h	4004 125Fh	SCI2	Serial communication interface 2
4004 1260h	4004 127Fh	SCI3	Serial communication interface 3
4004 1280h	4004 129Fh	SCI4	Serial communication interface 4
4004 12A0h	4004 12BFh	SCI5	Serial communication interface 5
4004 1320h	4004 133Fh	SCI9	Serial communication interface 9
4004 2000h	4004 20FFh	POE0	Port output enable 0
4004 2100h	4004 21FFh	POE1	Port output enable 1
4004 4000h	4004 40FFh	RTC	Realtime clock
4004 4200h	4004 42FFh	WDT	Watchdog timer
4004 4400h	4004 44FFh	IWDT	Independent watchdog timer
4004 4600h	4004 46FFh	CAC	Clock frequency accuracy measurement circuit
4004 7000h	4004 70FFh	MSTP	Module stop control registers B, C, D
4005 2000h	4005 207Fh	TMR	8-bit timer
4005 3000h	4005 30FFh	RIIC0	I ² C bus interface 0
4005 3100h	4005 31FFh	RIIC1	I ² C bus interface 1
4005 4100h	4005 41FFh	DOC	Data operation circuit
4005 5000h	4005 50FFh	GPT320	General PWM timer 0 (32 bits)
4005 5100h	4005 51FFh	GPT321	General PWM timer 1 (32 bits)
4005 5200h	4005 52FFh	GPT162	General PWM timer 2 (16 bits)

Table 5.1 I/O Register Address (2/2)

Start Address	End Address	Module Symbol	Description
4005 5300h	4005 53FFh	GPT163	General PWM timer 3 (16 bits)
4005 5400h	4005 54FFh	GPT164	General PWM timer 4 (16 bits)
4005 5500h	4005 55FFh	GPT165	General PWM timer 5 (16 bits)
4005 5FF0h	4005 5FFFh	GPT_OPS	Output phase switch control
4005 C000h	4005 C1FFh	S14AD	14-bit A/D converter
4005 D000h	4005 D0FFh	TEMPS	Temperature sensor
4005 E000h	4005 E0FFh	R12DA	12-bit D/A converter
4007 0000h	4007 001Fh	SCI0	Serial communication interface 0
4007 0020h	4007 003Fh	SCI1	Serial communication interface 1
4007 0200h	4007 03FFh	MLCD	MIP LCD controller
4007 0800h	4007 0DFFh	GDT	2D graphics data conversion circuit
4007 0F00h	4007 0FFFh	IrDA	Infrared communication
4007 2000h	4007 20FFh	SPI0	Serial peripheral interface 0 (128 bits)
4007 2100h	4007 21FFh	SPI1	Serial peripheral interface 1 (32 bits)
4007 4000h	4007 40FFh	CRC	CRC calculator
4008 0000h	4008 00FFh	KINT	Key interrupt function
4008 0400h	4008 04FFh	CCC	Clock correction circuit
4008 4000h	4008 40FFh	AGT0	Asynchronous general-purpose timer 0
4008 4100h	4008 41FFh	AGT1	Asynchronous general-purpose timer 1
4008 4400h	4008 44FFh	LST	Low-speed clock timer
4008 4500h	4008 457Fh	DIL	Data inversion circuit
4008 4600h	4008 467Fh	LPG	Low-speed pulse generator
4008 4680h	4008 46FFh	DIV	Divider
4008 4800h	4008 49FFh	MTDV	Motor driver control circuit
4008 5000h	4008 50FFh	ACMP	Analog comparator
4008 6900h	4008 69FFh	LED	LED driver
4008 6A80h	4008 6AFFh	VREF	Reference voltage generation circuit
4009 0400h	4009 04FFh	USB	USB2.0FS host/function module
400C 0000h	400C 01FFh	TSIP-Lite	Security function
6400 0000h	67FF FFFFh	QSPI	Quad-serial peripheral interface

5.2 Access Cycle

Table 5.2 lists the access cycle information of the I/O registers in this LSI chip. The following statements apply to Table 5.2:

- Registers are grouped by corresponding modules.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the I/O register area, reserved addresses that are not allocated to registers must not be accessed. If access is attempted, further operation cannot be guaranteed.
- The number of access cycles for I/O registers depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency between ICLK and PCLK. “PCLK” refers to both PCLKA and PCLKB. For the internal peripheral bus, see section 18, Buses in the User’s Manual: Hardware.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, 1 cycle of PCLK is added to the divided clock synchronization cycles.
- The numbers of cycles are applicable when access by the CPU does not conflict with bus access by another bus master (the DMAC or DTC).

Table 5.2 I/O Register Access Cycle (1/2)

Function	Start Address	End Address	ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related Function
			Read	Write	Read	Write		
CPU, MPU, MMF, Bus, DMAC, DTC, ICU, FLASH, DBG	4000 0000h	4000 6FFFh	3	3	—	—	ICLK	CPU, Memory Protection Unit, memory mirror function, bus control, DMA controller, data transfer controller, interrupt controller, flash memory, debug function
	4001 A000h	4001 BFFFh			—	—		
MTB	4001 9000h	4001 9FFFh	2	2	—	—	ICLK	Debug function (MTB)
System control*4	4001 E000h	4001 E3FFh	3	3	—	—	ICLK	Low power consumption function, resets, clock generation function, register write protection function, low voltage detection, energy harvesting control circuit
	4001 E400h	4001 E412h	5	5	—	—		
	4001 E413h	4001 E413h	3	3	—	—		
	4001 E414h	4001 E420h	5	5	—	—		
	4001 E421h	4001 E421h	3	3	—	—		
	4001 E422h	4001 E4E0h	5	5	—	—		
	4001 E4E1h	4001 E4E1h	3	3	—	—		
	4001 E4E2h	4001 E4FFh	5	5	—	—		
	4001 E500h	4001 EFFFh	3	3	—	—		
GPIO*5	4004 0000h	4004 10FFh	3	3	2-3	2-3	PCLKB	I/O ports, event link controller
SCI2 to SCI5, and SCI9	4004 1240h	4004 133Fh	3	3	2-3*2	2-3*2	PCLKB	Serial communications interface
POE0 and POE1	4004 2000h	4004 21FFh	3	3	2-3	2-3	PCLKB	Port output enable
RTC, WDT, IWDT, CAC, MSTP	4004 4000h	4004 70FFh	3	3	2-3	2-3	PCLKB	Realtime clock, watchdog timer, independent watchdog timer, clock frequency accuracy measurement circuit, module stop control
TMR	4005 2000h	4005 207Fh	3	3	2-3	2-3	PCLKB	8-bit timer
RIIC0 and RIIC1	4005 3000h	4005 31FFh	3	3	2-3	2-3	PCLKB	I ² C bus interface
DOC	4005 4100h	4005 41FFh	3	3	2-3	2-3	PCLKB	Data operation circuit

Table 5.2 I/O Register Access Cycle (2/2)

Function	Start Address	End Address	ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related Function
			Read	Write	Read	Write		
GPT0 to GPT5*6, and GPT_OPS	4005 5000h	4005 5FFFh	6	4	5-6	3-4	PCLKB	General PWM timer
S14AD	4005 C000h	4005 C1FFh	3	3	2-3	2-3	PCLKB	14-bit A/D converter
TEMPS	4005 D000h	4005 D0FFh	3	3	2-3	2-3	PCLKB	Temperature sensor
R12DA	4005 E000h	4005 E0FFh	3	3	2-3	2-3	PCLKB	12-bit D/A converter
SCI0 and SCI1	4007 0000h	4007 003Fh	3	3	—	—	PCLKA	Serial communications interface
MLCD and GDT	4007 0200h	4007 0DFFh	3	3	—	—	PCLKA	MIP LCD controller, 2D graphics data conversion circuit
IrDA	4007 0F00h	4007 0FFFh	3	3	—	—	PCLKA	Infrared communication
SPI0 and SPI1	4007 2000h	4007 21FFh	3	3	—	—	PCLKA	Serial peripheral interface
CRC	4007 4000h	4007 40FFh	3	3	—	—	PCLKA	CRC calculator
KINT	4008 0000h	4008 00FFh	3	3	2-3	2-3	PCLKB	Key interrupt function
CCC	4008 0400h	4008 04FFh	4	4	3-4	3-4	PCLKB	Clock correction circuit
AGT0 and AGT1	4008 4000h	4008 41FFh	4	4	3-4	3-4	PCLKB	Asynchronous general-purpose timer
LST	4008 4400h	4008 44FFh	4	4	3-4	3-4	PCLKB	Low-speed clock timer
DIL	4008 4500h	4008 457Fh	4	4	3-4	3-4	PCLKB	Data inversion circuit
LPG	4008 4600h	4008 467Fh	4	4	3-4	3-4	PCLKB	Low-speed pulse generator
DIV	4008 4680h	4008 46FFh	4	4	3-4	3-4	PCLKB	Divider
MTDV	4008 4800h	4008 49FFh	4	4	3-4	3-4	PCLKB	Motor driver control circuit
ACMP	4008 5000h	4008 50FFh	3	3	2-3	2-3	PCLKB	Analog comparator
LED	4008 6900h	4008 69FFh	4	4	3-4	3-4	PCLKB	LED driver
VREF	4008 6A80h	4008 6AFFh	4	4	3-4	3-4	PCLKB	Reference voltage generation circuit
USB	4009 0400h	4009 04FFh	3	3	2-3	2-3	PCLKB	USB2.0FS host/function module
TSIP-Lite	400C 0000h	400C 01FFh	3	3	—	—	PCLKA	Security function
QSPI	6400 0000h	67FF FFFFh	4*3	14*3	—	—	PCLKA	Quad-serial peripheral interface

Note 1. If the number of PCLK cycles is a non-integer (for example 1.5), the minimum value is rounded down to an integer, and the maximum value is rounded off to an integer. For example, 1.5 to 2.5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 5.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 5.2.

Note 3. The access cycles depend on the QSPI bus cycles.

Note 4. These values indicate the minimum numbers of cycles for access by the CPU. They do not include the cycles required for changes in the source of the ICLK clock and frequency after changes to the SCKSCR and SCKDIVCR registers.

Note 5. GPIO indicates PORT0 to PORT8, PFS, PMISC, and the ELC.

Note 6. GPT0 to GPT5 indicates GPT320, GPT321, GPT162, GPT163, GPT164, and GPT165.

6. Electrical Characteristics

The electrical characteristics of the LSI chip are defined under the following conditions unless otherwise specified:

$VCC = AVCC0 = AVCC1 = IOVCC0 = IOVCC1 = IOVCC2 = IOVCC3 = 1.62 \text{ to } 3.6 \text{ V}$

$VCC_USB = 3.0 \text{ to } 3.6 \text{ V}$

$1.62 \text{ V} \leq VREFH0 \leq AVCC0$

$VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 \text{ V}$

$T_a = T_{opr}$

The load capacitance of each I/O pin is 30 pF.

When measuring the power consumption, low CL4 (SOMCR.SODRV = 1 and SOMCR.SODRV0 = 0) was selected for the driving ability of the sub-clock oscillator.

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage	Power supply voltage	VCC	-0.3 to 4.6	V
	Input voltage for EHC	VSC_VCC	-0.3 to 4.6	V
	Secondary battery input voltage for EHC	VBAT_EHC	-0.3 to 4.6	V
	Power supply voltage for USB	VCC_USB	-0.3 to 4.6	V
	Power supply voltage for I/O pins	IOVCC, IOVCC0 to IOVCC3	-0.3 to 4.6	V
Input voltage		V_{in}	-0.3 to VCC + 0.3 (max. 4.6 V)	V
Reference power supply voltage		VREFH0	-0.3 to AVCC0 + 0.3 (max. 4.6 V)	V
		VREFL0	-0.3 to AVSS0 + 0.3	V
Analog power supply voltage		AVCC0, AVCC1	-0.3 to 4.6	V
Junction temperature		T_j	-40 to +95	°C
Storage temperature		T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI chip might result if absolute maximum ratings are exceeded.

Table 6.2 Recommended Operating Conditions

Item	Symbol		Min.	Typ.	Max.	Unit
Power supply voltage	VCC		1.62	—	3.6	V
	VSS		—	0	—	V
Input voltage for EHC	VSC_VCC		1.62	—	3.6	V
Secondary battery input voltage for EHC	VBAT_EHC*1		1.62	—	3.6	V
Power supply voltage for USB	VCC_USB		3.0	—	3.6	V
	VSS_USB		—	0	—	V
Analog power supply voltage	AVCC0, AVCC1		1.62	—	3.6	V
	AVSS0, AVSS1		—	0	—	V
	VREFH0		1.62	—	AVCC0	V
	VREFL0		—	0	—	V
Power supply voltage for I/O pins	IOVCC, IOVCC0, IOVCC1, IOVCC3		1.62	—	3.6	V
	IOVCC2	When MLCD is not in use	1.62	—	3.6	V
		When MLCD is in use	2.7	3.0	3.3	V
Operating temperature	T _{opr}		−40	—	85	°C

Note 1. The voltage of the secondary battery to be connected to VBAT_EHC is 2.6 V or 3.0 V.

6.2 DC Characteristics

6.2.1 Input Characteristics of I/O Pins (V_{IH} and V_{IL})

Table 6.3 Input Characteristics of I/O Pins (V_{IH} and V_{IL})

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RES#, NMI, and IRQ pins and input pins of on-chip peripheral functions other than those of the RIIC	V_{IH}	$VCC \times 0.8$	—	—	V	—
		V_{IL}	—	—	$VCC \times 0.2$		
		ΔV_T	0.3	—	—		
	RIIC	V_{IH}	$VCC \times 0.7$	—	—		VCC = 3.0 to 3.6 V
		V_{IL}	—	—	$VCC \times 0.3$		
		ΔV_T	$VCC \times 0.05$	—	—		
Input voltage other than that for the Schmitt trigger input pins	EXTAL, MD, EHMD, and general-purpose I/O ports	V_{IH}	$VCC \times 0.8$	—	—		—
		V_{IL}	—	—	$VCC \times 0.2$		

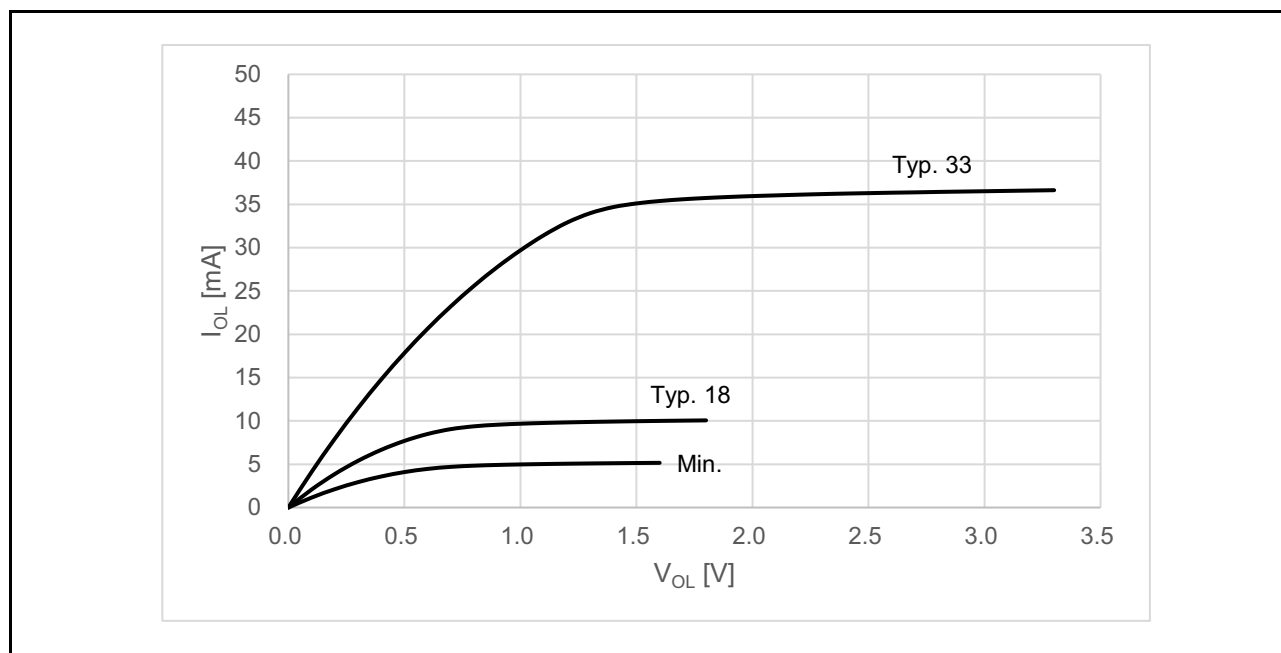
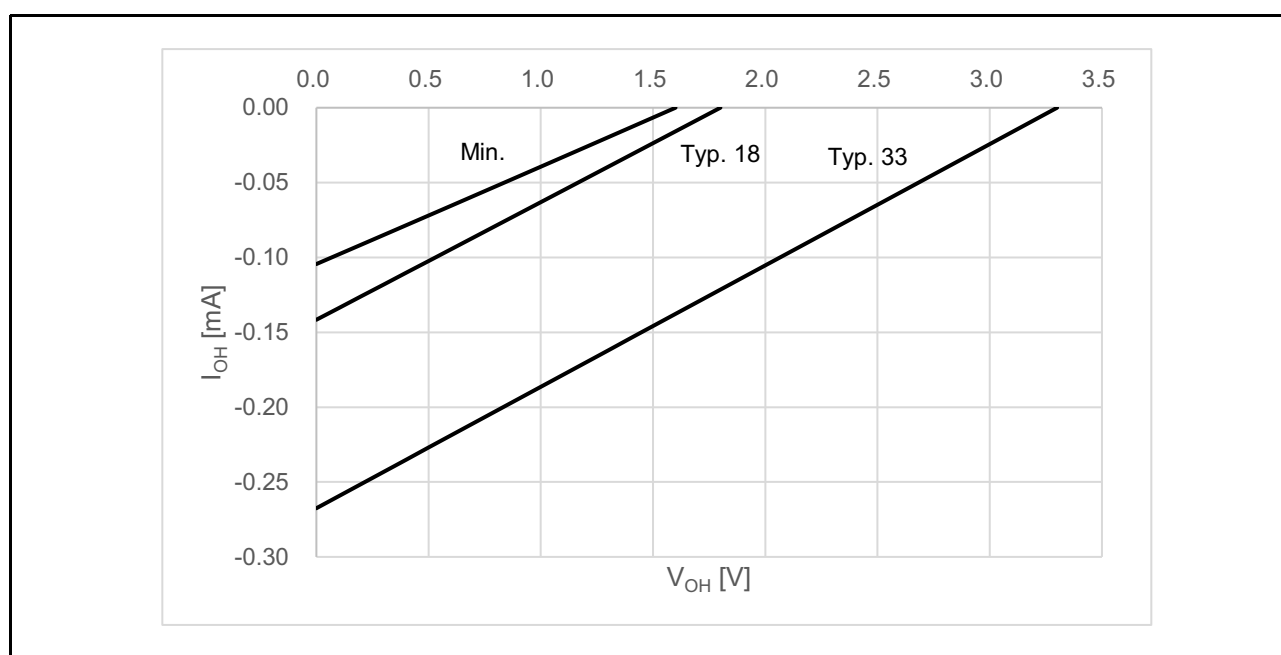
6.2.2 Output Characteristics of I/O Pins (V_{OH} and V_{OL}) (1)

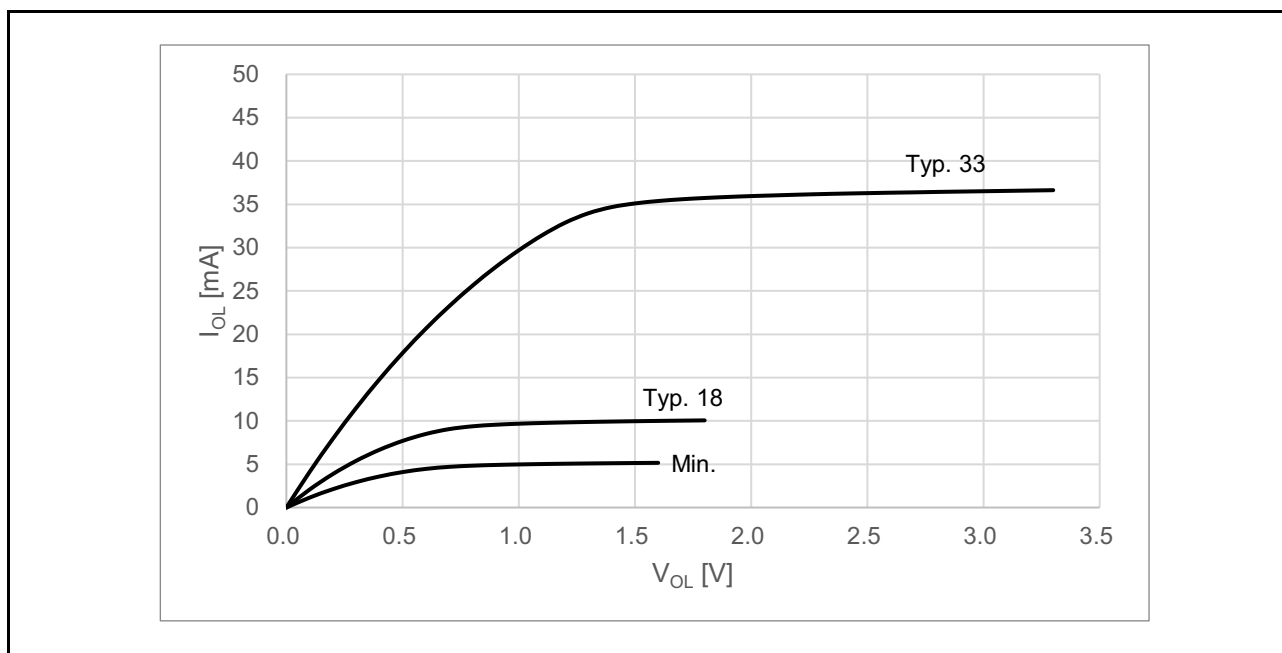
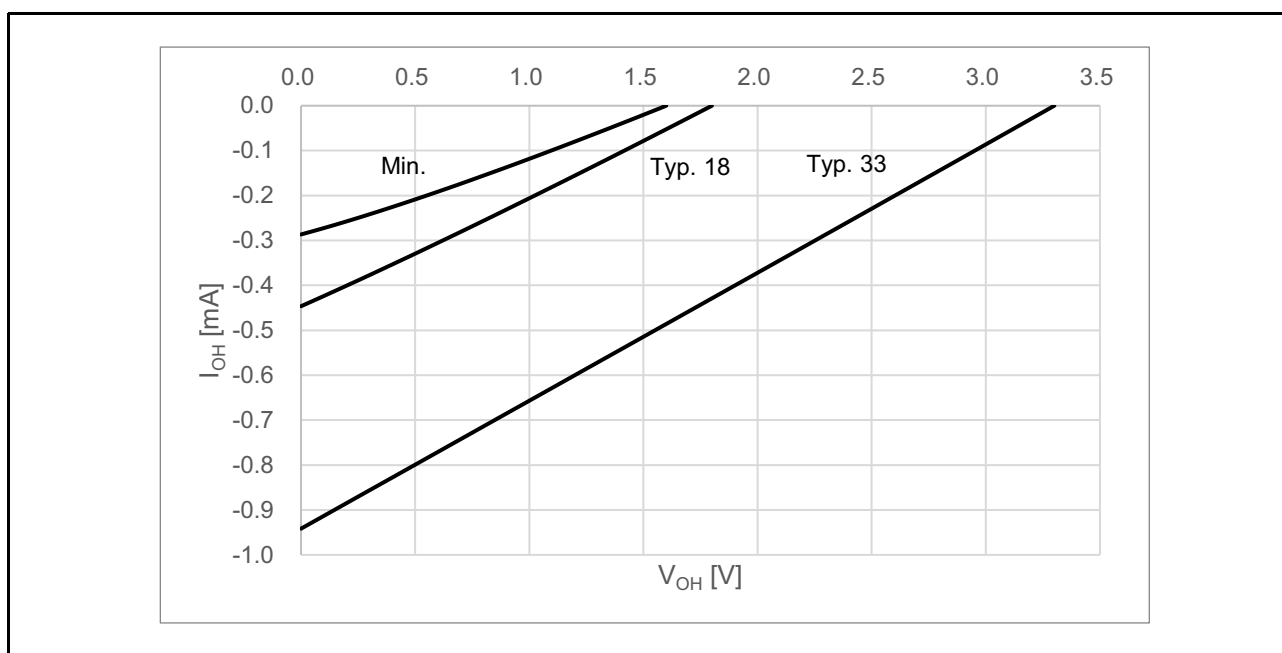
Table 6.4 Output Characteristics of I/O Pins (V_{OH} and V_{OL})

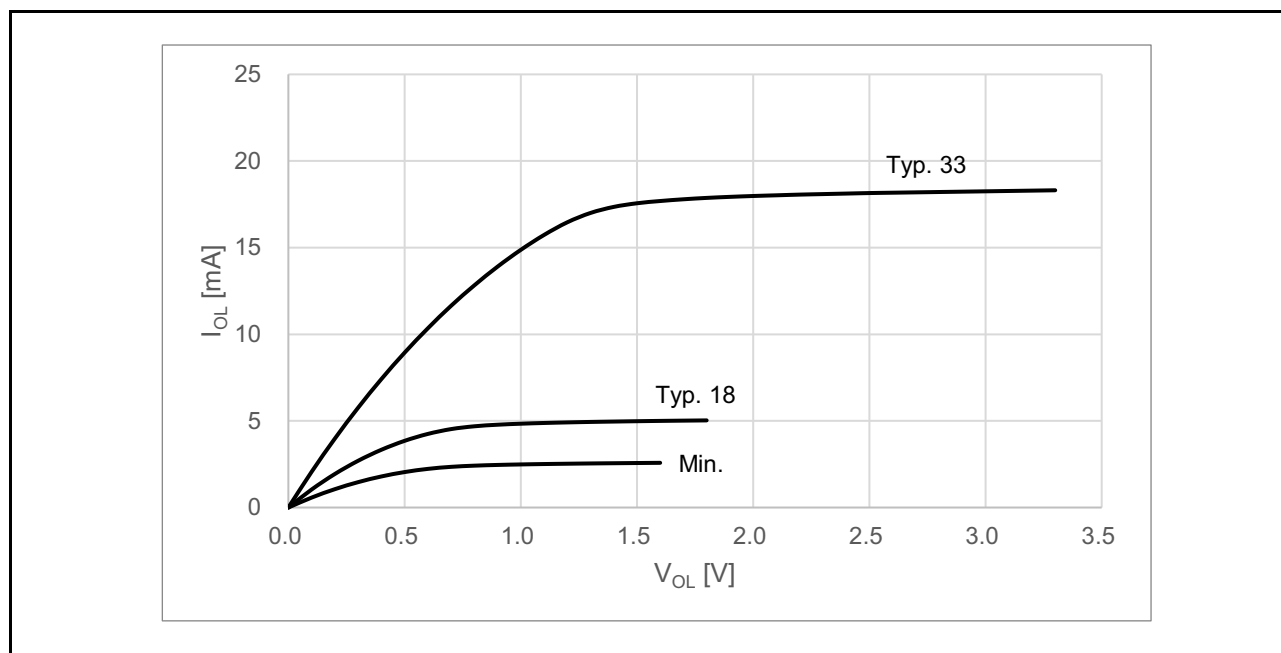
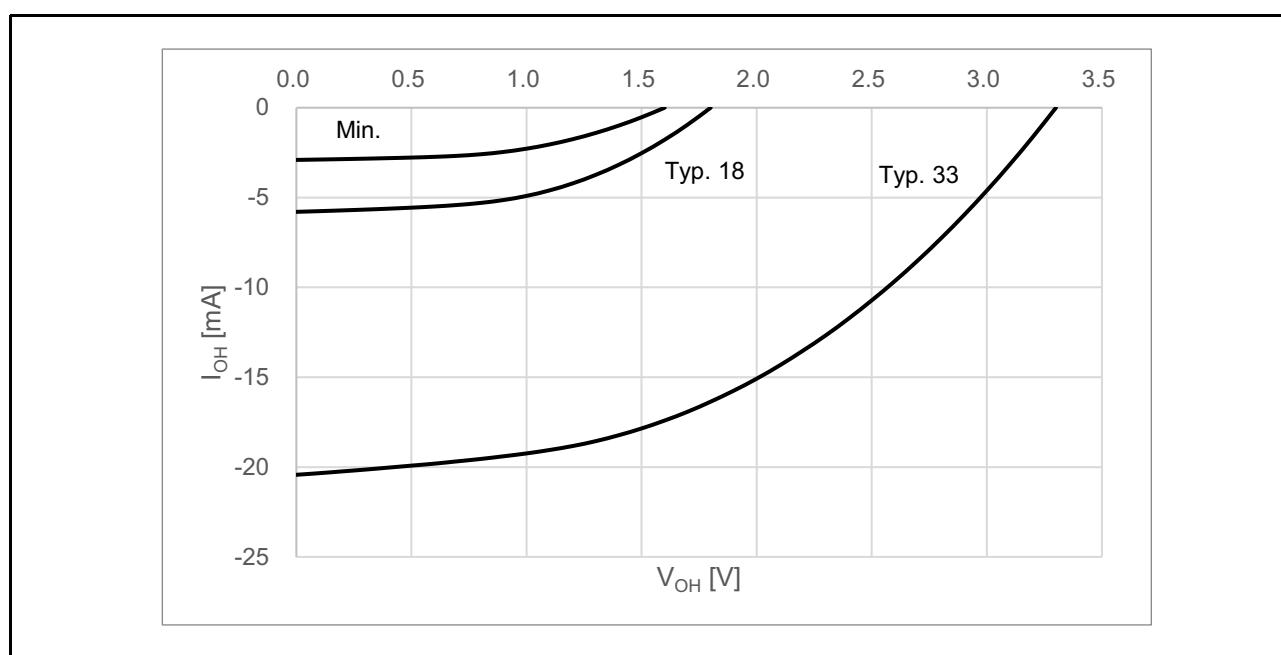
Item	Setting of the Register	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high-level voltage	Low driving ability (PmnPFS.DSCR[1:0] = 00b)	V_{OH}	$VCC - 0.5$	—	—	V	$I_{OH} = 10 \mu A$
	Middle driving ability (PmnPFS.DSCR[1:0] = 01b)		$VCC - 0.5$	—	—		$I_{OH} = 10 \mu A$
	Standard driving ability (PmnPFS.DSCR[1:0] = 10b)		$VCC - 0.6$	—	—		$I_{OH} = 2 \text{ mA}$
	High driving ability (PmnPFS.DSCR[1:0] = 11b)		$VCC - 0.5$	—	—		$I_{OH} = 2 \text{ mA}$
Output low-level voltage	Low driving ability (PmnPFS.DSCR[1:0] = 00b)	V_{OL}	—	—	0.5		$I_{OL} = 2 \text{ mA}$
	Middle driving ability (PmnPFS.DSCR[1:0] = 01b)		—	—	0.5		$I_{OL} = 2 \text{ mA}$
	Standard driving ability (PmnPFS.DSCR[1:0] = 10b)		—	—	0.6		$I_{OL} = 2 \text{ mA}$
	High driving ability (PmnPFS.DSCR[1:0] = 11b)		—	—	0.5		$I_{OL} = 2 \text{ mA}$

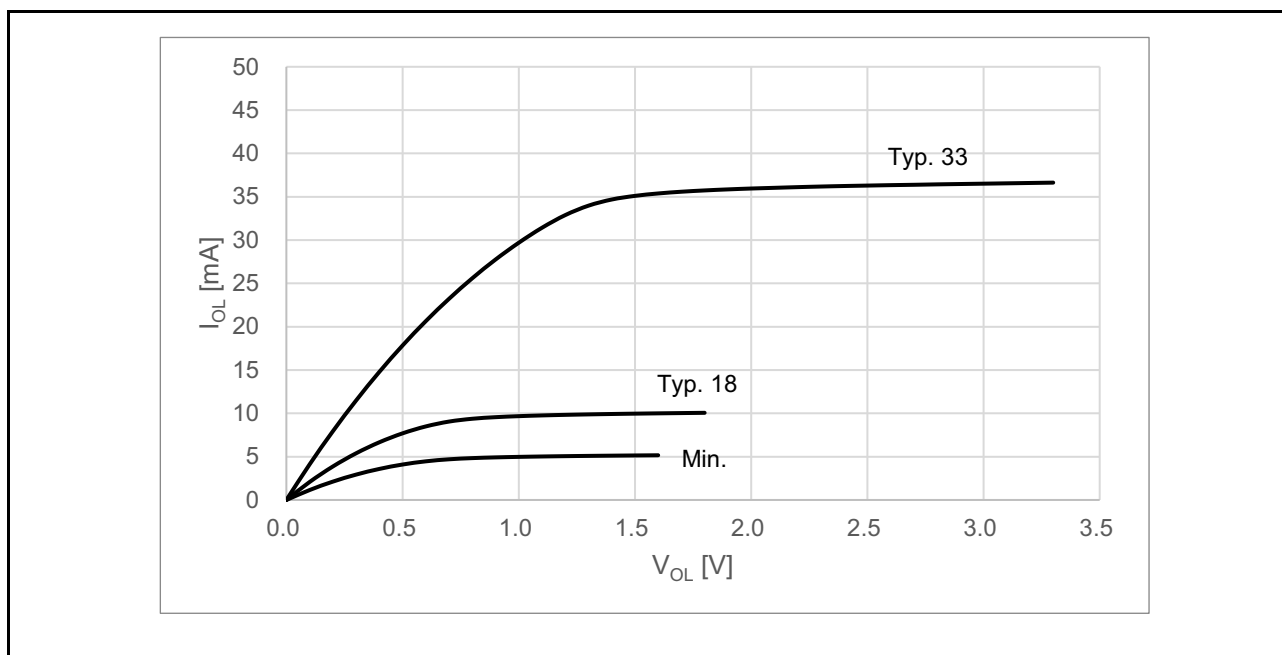
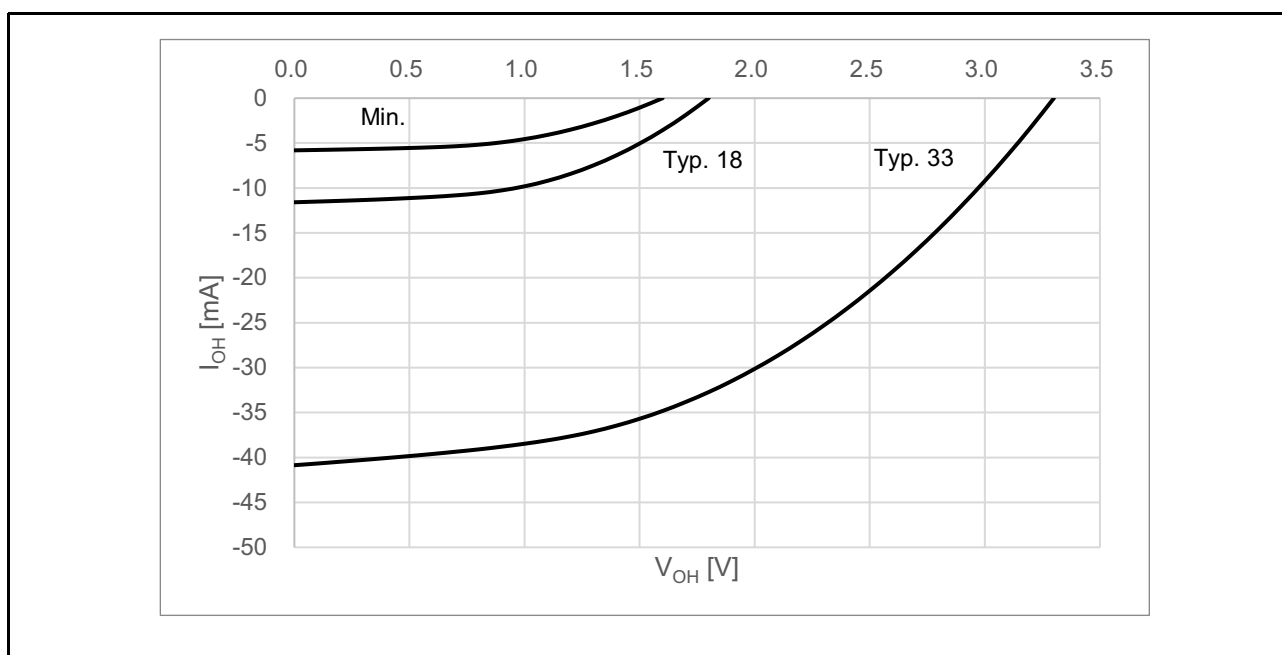
Table 6.5 Conditions for Testing I/O Characteristics

	Typ. 33	Typ. 18	Min.	Unit
VCC	3.3	1.8	1.6	V
Temperature	25	25	125	°C

Figure 6.1 V_{OL} vs. I_{OL} Characteristics (Low Driving Ability)Figure 6.2 V_{OH} vs. I_{OH} Characteristics (Low Driving Ability)

Figure 6.3 V_{OL} vs. I_{OL} Characteristics (Middle Driving Ability)Figure 6.4 V_{OH} vs. I_{OH} Characteristics (Middle Driving Ability)

Figure 6.5 V_{OL} vs. I_{OL} Characteristics (Standard Driving Ability)Figure 6.6 V_{OH} vs. I_{OH} Characteristics (Standard Driving Ability)

Figure 6.7 V_{OL} vs. I_{OL} Characteristics (High Driving Ability)Figure 6.8 V_{OH} vs. I_{OH} Characteristics (High Driving Ability)

6.2.3 Output Characteristics of I/O Pins (V_{OL}) (2)

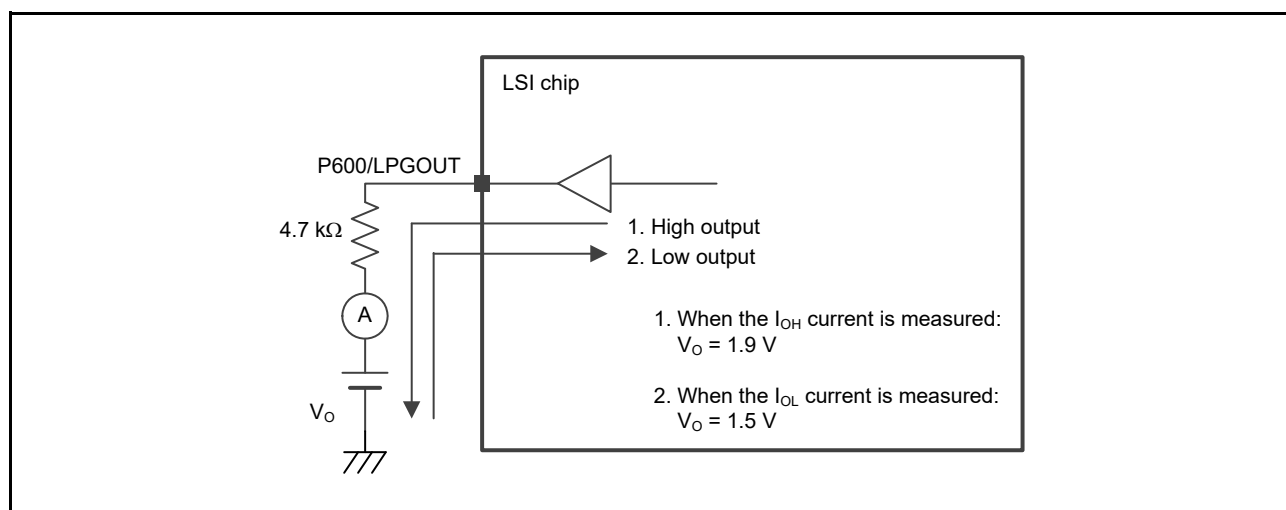
Table 6.6 Output Characteristics of I/O Pins (V_{OL})Conditions: $V_{CC} = 3.0$ to 3.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low-level voltage	RIIC	V_{OL}	—	—	0.4	V	$I_{OL} = 3$ mA
			—	—	0.6		$I_{OL} = 6$ mA

6.2.4 Output Characteristics of the LPG Pin (I_{OH} and I_{OL})

Table 6.7 Output Characteristics of the LPG Pin (I_{OH} and I_{OL})Conditions: $IOVCC1 = 2.2$ V, $T_a = 25^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output current	P600	I_{OL}	50	160	200	μA	P600PFS.DSCR[1:0] = 00b
			50	110	200		P600PFS.DSCR[1:0] = 01b
		I_{OH}	—	10	—		P600PFS.DSCR[1:0] = 00b

Figure 6.9 Output Characteristics of the LPG Pin (I_{OH} and I_{OL})

6.2.5 Pull-up and Pull-down Resistors

Table 6.8 Pull-up and Pull-down Resistors

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Pull-up resistor	I_P	120	200	—	kΩ	$V_{CC} = 2.5$ V
Pull-down resistor	I_P	120	200	—		$V_{CC} = 2.5$ V

6.2.6 Pin Capacitance

Table 6.9 Pin Capacitance

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RIIC-related pins	P809, P810, P701, P700	C_{in}	—	—	8	pF	—
DA0	P007						
LEDI1 to LEDI3	P512, P513, P514						
MTDV-related pins	MTDO*_DRV*, PM_RES_DRV0						
EXTAL, XTAL	P412, P413						
USB-related pins	USB_DP, USB_DM						
All other pins			—	—	16		

Note: For details, see Table 1.4, Pin Functions in section 1, Overview.

6.2.7 Characteristics of Motor Driver I/O Pins

Table 6.10 Characteristics of Motor Driver I/O Pins

Conditions: IOVCC1 = 1.8 V (for measuring the detection pin's internal resistor), $T_a = -20$ to $+60^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection pin's internal resistor	mtRs	23.5	25	26.5	k Ω	RESREG.PM1RES[2:0] = 001b
		47	50	53		RESREG.PM1RES[2:0] = 010b
		71	75	80		RESREG.PM1RES[2:0] = 011b
		94	100	106		RESREG.PM1RES[2:0] = 100b
		141	150	159		RESREG.PM1RES[2:0] = 101b
		165	175	186		RESREG.PM1RES[2:0] = 110b
		188	200	212		RESREG.PM1RES[2:0] = 111b
Temperature characteristic of the internal resistor	R/dT	-1200	—	1200	ppm/ $^\circ\text{C}$	—

Note: Applicable motor driving pins:
PM_RES_DRV0, MTDO1_DRV0, MTDO2_DRV0, MTDO4_DRV1, MTDO5_DRV1, MTDO6_DRV1, MTDO7_DRV2,
MTDO8_DRV2, MTDO9_DRV2

6.2.8 Operating Current and Standby Current

Table 6.11 Operating Current and Standby Current (1/6)

Maximum test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit		
All power supply mode (ALLPWON) The code is executed from within the flash memory.	BOOST	Maximum operation*1		ICLK/PCLKB = 64/32 MHz	HOCO	—	18	mA		
				ICLK/PCLKB = 32/16 MHz	HOCO	—	11*3			
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 64/32 MHz	MOSC + PLL	7.4	—			
				ICLK/PCLKB = 32/16 MHz	MOSC	4.1	—			
				ICLK/PCLKB = 64/32 MHz	HOCO	8.2	—			
				ICLK/PCLKB = 32/16 MHz		4.4	—			
		CoreMark (peripheral clock signal stopped*2)		ICLK/PCLKB = 64/1 MHz	HOCO	3.5	—			
				ICLK/PCLKB = 32/0.5 MHz	HOCO	2.0	—			
		while(1) operation (peripheral clock signal stopped*2)		ICLK/PCLKB = 64/1 MHz	HOCO	3.0	—			
				ICLK/PCLKB = 32/0.5 MHz	HOCO	1.7	—			
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 64/1 MHz	HOCO	1.2	—			
				ICLK/PCLKB = 32/0.5 MHz	HOCO	1.0	—			
		Increases with background operation (BGO)		During programming					0.24	—
				During erasure					0.23	—
	NORMAL	High-Speed mode	Maximum operation*1		ICLK/PCLKB = 32/32 MHz	MOSC	—	10	mA	
					ICLK/PCLKB = 16/16 MHz		—	8.0*3		
			while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32/32 MHz	MOSC	3.9	9.0		
					ICLK/PCLKB = 16/16 MHz		2.0	7.0*3		
					ICLK/PCLKB = 32/32 MHz	HOCO	4.3	9.0		
					ICLK/PCLKB = 16/16 MHz		2.4	7.0*3		
CoreMark (peripheral clock signal stopped*2)			ICLK/PCLKB = 32/0.5 MHz	MOSC	1.5	—				
			ICLK/PCLKB = 16/0.25 MHz		0.83	—				
while(1) operation (peripheral clock signal stopped*2)			ICLK/PCLKB = 32/0.5 MHz	MOSC	1.1	6.0				
			ICLK/PCLKB = 16/0.25 MHz		0.65	—				
Sleep mode (peripheral clock signal stopped*2)			ICLK/PCLKB = 32/0.5 MHz		0.64	—				
			ICLK/PCLKB = 16/0.25 MHz		0.41	—				
Increases with background operation (BGO) during programming					0.23	—				
Increases with background operation (BGO) during erasure					0.15	—				

Table 6.11 Operating Current and Standby Current (2/6)

Maximum test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
All power supply mode (ALLPWON) The code is executed from within the flash memory.	NORMAL	Low-Speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	5.0	mA
				ICLK/PCLKB = 1/1 MHz		—	5.0*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 2/2 MHz	MOSC	0.36	5.0*3	
				ICLK/PCLKB = 1/1 MHz		0.24	—	
				ICLK/PCLKB = 2/2 MHz	MOCO	0.36	—	
				ICLK/PCLKB = 1/1 MHz		0.24	—	
			CoreMark (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz	MOSC	0.20	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.15	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz		0.18	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.15	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz		0.15	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.13	—	
		Subosc-Speed mode	while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	93	4700*3	μA
				ICLK/PCLKB = 32.7/0.51 kHz		92	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/0.51 kHz		91	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/0.51 kHz		90	—	
	VBB	Maximum operation*1		ICLK/PCLKB = 32.7/32.7 kHz	LOCO	—	200*3	μA
				ICLK/PCLKB = 32.7/32.7 kHz		38	—	
				ICLK/PCLKB = 32.7/0.51 kHz		34	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (standard CL)	38	—	
				ICLK/PCLKB = 32.768/0.512 kHz		34	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (low CL)	37	—	
				ICLK/PCLKB = 32.768/0.512 kHz		33	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/0.512 kHz				

Table 6.11 Operating Current and Standby Current (3/6)

Maximum test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Condition: The FLSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Flash excluded power supply mode (EXFPWON) The code is executed from SRAM.	NORMAL	High-Speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	9.8*3	mA
				ICLK/PCLKB = 16/16 MHz		—	7.8*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32/32 MHz		3.9	—	
				ICLK/PCLKB = 16/16 MHz		2.0	—	
				ICLK/PCLKB = 32/32 MHz	HOCO	4.3	—	
				ICLK/PCLKB = 16/16 MHz		2.4	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	1.1	—	
				ICLK/PCLKB = 16/0.25 MHz		0.61	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	0.59	—	
				ICLK/PCLKB = 16/0.25 MHz		0.36	—	
		Low-Speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	4.8*3	
				ICLK/PCLKB = 1/1 MHz		—	4.8*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 2/2 MHz	MOSC	0.29	—	
				ICLK/PCLKB = 1/1 MHz		0.18	—	
				ICLK/PCLKB = 2/2 MHz	MOCO	0.29	—	
				ICLK/PCLKB = 1/1 MHz		0.18	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz	MOSC	0.13	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.10	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz		0.09	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.08	—	
		Subosc-Speed mode	while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	52	4500*3	μA
				ICLK/PCLKB = 32.7/0.51 kHz		51	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/0.51 kHz		50	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/0.51 kHz		49	—	

Table 6.11 Operating Current and Standby Current (4/6)

Maximum test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Flash excluded power supply mode (EXFPWON) The code is executed from SRAM.	NORMAL	Software standby mode*5	VCC = 3.3 V		LOCO	29	—	μA
			VCC = 1.8 V			29	—	
			VCC = 3.3 V		SOSC (standard CL)	29	—	
			VCC = 1.8 V			29	—	
			VCC = 3.3 V		SOSC (low CL)	28	—	
			VCC = 1.8 V			28	—	
	VBB	Maximum operation*1		ICLK/PCLKB = 32.7/ 32.7 kHz	LOCO	—	30*3	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.7/ 32.7 kHz		6.8	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.7/ 0.51 kHz		3.1	—	
		Software standby mode*5	VCC = 3.3 V/3.6 V			2.1	25*3	
			VCC = 1.8 V			1.9	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/ 32.768 kHz	SOSC (standard CL)	6.5	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/ 0.512 kHz		2.9	—	
		Software standby mode*5	VCC = 3.3 V			2.0	—	
			VCC = 1.8 V			1.9	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/ 32.768 kHz	SOSC (low CL)	5.8	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/ 0.512 kHz		2.2	—	
		Software standby mode*5	VCC = 3.3 V			1.3	—	
			VCC = 1.8 V			1.2	—	
Minimum power supply mode (MINPWON) The code is executed from SRAM	NORMAL	High-Speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz		MOSC	—	7.0*3
				ICLK/PCLKB = 16/16 MHz	—		5.5*3	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	1.1	4.6*3	
				ICLK/PCLKB = 16/0.5 MHz		0.8	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	0.58	—	
				ICLK/PCLKB = 16/0.5 MHz		0.42	—	

Table 6.11 Operating Current and Standby Current (5/6)

Maximum test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Condition: The FLSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit		
Minimum power supply mode (MINPWON) The code is executed from SRAM	NORMAL	Low-Speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	3700*3	μA		
				ICLK/PCLKB = 1/1 MHz		—	3700*3			
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz	MOSC	110	—			
				ICLK/PCLKB = 1000/31.25 kHz		80	—			
				ICLK/PCLKB = 2000/31.25 kHz	MOCO	105	—			
				ICLK/PCLKB = 1000/31.25 kHz		75	—			
				Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/31.25 kHz	MOCO	70		—	
					ICLK/PCLKB = 1000/31.25 kHz		60		—	
			Subosc-Speed mode	while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	40	3500*3	μA	
					ICLK/PCLKB = 32.7/0.51 kHz		40	—		
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.7/32.7 kHz	39		—			
				ICLK/PCLKB = 32.7/0.51 kHz	39		—			
		Software standby mode*5	VCC = 3.3 V			LOCO	20	—	μA	
			VCC = 1.8 V				19	—		
			VCC = 3.3 V			SOSC (standard CL)	20	—		
			VCC = 1.8 V				20	—		
			VCC = 3.3 V			SOSC (low CL)	19	—		
			VCC = 1.8 V				19	—		
		VBB	while(1) operation (peripheral clock signal supplied)			ICLK/PCLKB = 32.768/32.768 kHz	SOSC (standard CL)	3.3	22*3	μA
			Sleep mode (peripheral clock signal stopped*2)			ICLK/PCLKB = 32.768/0.512 kHz		1.8	—	
	Software standby mode*5		VCC = 3.3 V			1.4		—		
			VCC = 1.8 V			1.2		—		
	while(1) operation (peripheral clock signal supplied)			ICLK/PCLKB = 32.7/32.7 kHz	LOCO	3.3	15*3	μA		
	Sleep mode (peripheral clock signal stopped*2)			ICLK/PCLKB = 32.7/0.51 kHz		1.8	14*3			
	Software standby mode		VCC = 3.3 V (typ.)/3.6 V (max.)			1.4	12			
			VCC = 1.8 V			1.2	10*3			
	while(1) operation (peripheral clock signal supplied)			ICLK/PCLKB = 32.768/32.768 kHz	SOSC (low CL)	2.6	—	μA		
Sleep mode (peripheral clock signal stopped*2)			ICLK/PCLKB = 32.768/0.512 kHz	1.1		—				
Software standby mode*5	VCC = 3.3 V			0.7		—				
	VCC = 1.8 V			0.5		—				
Minimum power supply mode (MINPWON) The code is executed from SRAM	VBB		Software standby mode Increases when peripheral modules are in use (independent of VCC)	Increase for using the IWDG (OFS0.IWDGSTRT = 0)			81	—	nA	
				Increase for using the AGT (AGTCR.TSTART = 1)			43	—		
				Increase for each 32 Kbytes of SRAM in use (set by the RAMSDCR register)			12	—		

Table 6.11 Operating Current and Standby Current (6/6)

Maximum test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode	Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Deep software standby mode	VCC = 3.3 V (typ.)/3.6 V (max.)	—	—	140	2000*3	nA
	VCC = 1.8 V	—	—	120	500*3	
	Increase for using the SOSC (VCC = 3.3 V)	—	SOSC (low CL)	160	—	
	Increase for using the SOSC (VCC = 1.8 V)	—		100	—	
Increases when peripheral modules are in use in standby mode (independent of VCC)	Increase for using the LVD0 (OFS1.LVDAS = 0)			48	—	nA
	Increase for using the LVD1 (LVCMPCR.LVD1E = 1)			66	—	
	Increase for using the LVDBAT (LVCMPCR.LVDBATE = 1)			66	—	
	Increase for using the CCC (CADJUSCEN = 1 and ADJUSTEN = 1)			35	—	
	Increase for using the MTDV			100*4	—	

Note 1. The value for current in a “Maximum operation” row is for a case where the DMAC is handling transfer in every cycle and the CPU is repeatedly executing a multiply instruction while all modules are released from the module-stop state. The value does not include the current during background operation (BGO) and the supply of current for the pins.

Note 2. The value for current in a row with a label that includes “peripheral clock signal stopped” is for a case where the peripheral circuits have been placed in the module-stop state following the settings for frequency-division of ICLK and PCLKB.

Note 3. We do not inspect this value before shipment. The values presented in this manual are only for reference.

Note 4. This is the design value obtained by measuring current for 2 ms while the PM2 forward-rotation waveform is being output.

Note 5. The supply of the clock signals is stopped in this mode regardless of the operating frequency settings.

Table 6.12 Analog Operating Current (AVCC0) and Standby Current

Maximum test conditions: VCC = AVCC0 = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, T_a = T_{opr} = 25°C (when the VREF is not in use)Typical test conditions: VCC = AVCC0 = 3.3 V, AVTRO = 1.25 V, T_a = T_{opr} = 25°C (when the VREF is in use)

Item	Operating Circuit			Symbol	Typ.	Max.	Unit	Test Conditions
	A/D	Temperature Sensor	VREF					
AVCC0 power supply current	During conversion	During operation	During operation	I _{AVCC0}	81	—	μA	PCLKB = 16 MHz Sampling interval is 1 μs. (ADSSTRn.SST[7:0] = 10h)
		Stopped	During operation		77	—		
		During operation	Stopped		69	—		
		Stopped	Stopped		53	—		
		Stopped	Stopped		0.19	—		
	Waiting for conversion	Stopped	Stopped		22	—	nA	PCLKB = 16 MHz*1
	On standby*2				22	1900		Clock supply is stopped.
	Reference power supply current	During conversion	Stopped		Stopped	I _{REFH0}	18	—
0.08				—			PCLKB = 32.768 kHz	
Waiting for conversion		Stopped	Stopped	22	—		nA	PCLKB = 16 MHz*1
On standby			22	—	Clock supply is stopped.			

Note 1. This indicates that the clock signal is being supplied to the A/D converter but A/D conversion is not in progress.

Note 2. We measured the AVCC0 and AVCC1 pins at the same time.

Table 6.13 Analog Operating Current (AVCC1)

Maximum test conditions: VCC = AVCC1 = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = AVCC1 = 3.3 V, T_a = T_{opr} = 25°C

Item	Operating Circuit			Symbol	Typ.	Max.	Unit	Test Conditions
	D/A	D/A Amplifier	ACMP					
AVCC1 power supply current	During conversion	During operation	Stopped	I _{AVCC1}	44	68	μA	PCLKB = 32 MHz
		Stopped	Stopped		9.2	13		PCLKB = 32 MHz
	Waiting for conversion	Stopped	During operation		8.4	22		PCLKB = 32 MHz
		Stopped	Stopped		22	1900	nA	PCLKB = 32 MHz

Table 6.14 USB Operating Current

Maximum test conditions: VCC = VCC_USB = 3.6 V, T_a = T_{opr} = 85°CTypical test conditions: VCC = VCC_USB = 3.3 V, T_a = T_{opr} = 25°C

Item		Symbol	Typ.	Max.	Unit	Test Conditions
USB operating current	When the full-speed transfer is selected in the host controller mode	I _{USBHF}	3.9	4.5	mA	—
	When the full-speed transfer is selected in the device controller mode	I _{USBDF}	4.6	5.4		—
	When the low-speed transfer is selected in the host controller mode	I _{USBHL}	2.4	3.1		—
USB waiting current		I _{USBST}	7.2	—	nA	—

Table 6.15 IOVCC Waiting Current

Maximum test conditions: $V_{CC} = IOVCCn = 3.6\text{ V}$, $T_a = T_{opr} = 85^\circ\text{C}$ Typical test conditions: $V_{CC} = IOVCCn = 3.3\text{ V}$, $T_a = T_{opr} = 25^\circ\text{C}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
IOVCC0 waiting current	$I_{IOVCC0ST}$	8.6	—	nA	—
IOVCC1 waiting current	$I_{IOVCC1ST}$	16	—		—
IOVCC2 waiting current	$I_{IOVCC2ST}$	9.2	—		—
IOVCC3 waiting current	$I_{IOVCC3ST}$	21	—		—
IOVCC0 to IOVCC3 waiting current (total)	$I_{IOVCCST}$	—	900		—

6.2.9 Gradients of VCC Rising and Falling

Table 6.16 Characteristics for Gradients of VCC Rising and Falling

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Range of gradients for VCC rising at the time power is supplied	$SrVCC$	0.02	—	20	ms/V	—
Allowable range of fluctuations in the gradients for the voltage rising and falling	$dt/dVCC$	2	—	20	ms/V	—

6.2.10 On-chip Linear Regulator Characteristics

Table 6.17 On-chip Linear Regulator Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LDO startup time	t_{LDO}	3000	—	—	μs	Figure 6.10
LDO stabilization time	t_{LDOWT}	300	—	—	μs	Figure 6.10

Note: To ensure stable operation of the LSI chip, avoid operations that draw large amounts of current during the LDO stabilization time and the LDO stabilization period after no externally applied voltage is being supplied.

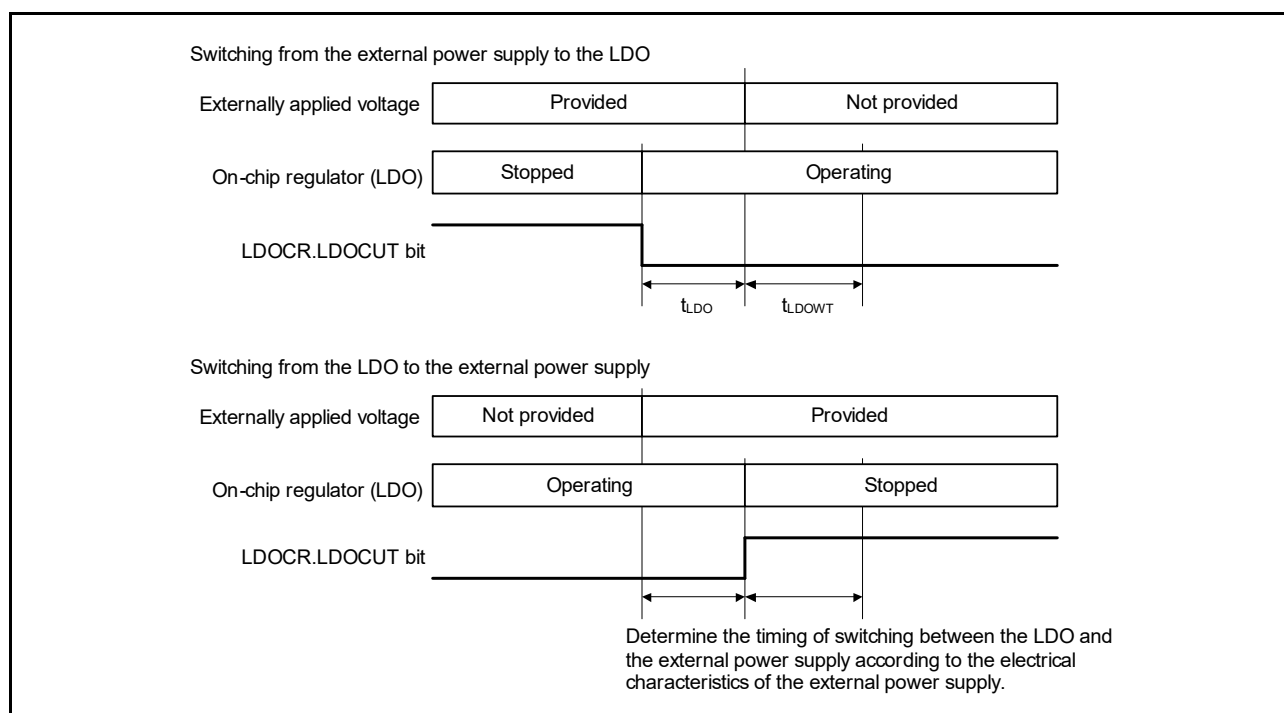


Figure 6.10 Timing of Switching between the External Power Supply and the LDO

6.3 AC Characteristics

6.3.1 Operating Frequency

Table 6.18 Operating Frequencies in the Various Modes

Power Control Mode		Clock Source	Symbol	Min.	Typ.	Max.	Unit	
BOOST		System clock (ICLK)	f	—	—	64	MHz	
		Peripheral module clock A (PCLKA)		—	—	64		
		Peripheral module clock B (PCLKB)		—	—	32		
NORMAL	High-speed	System clock (ICLK)		—	—	32		
		Peripheral module clock A (PCLKA)		—	—	32		
		Peripheral module clock B (PCLKB)		—	—	32		
	Low-speed	System clock (ICLK)		—	*1	2.3		
		Peripheral module clock A (PCLKA)		—	*1	2.3		
		Peripheral module clock B (PCLKB)		—	*1	2.3		
		Subosc-speed		System clock (ICLK)	—	*2	37.6	kHz
				Peripheral module clock A (PCLKA)	—	*2	37.6	
				Peripheral module clock B (PCLKB)	—	*2	37.6	
VBB		System clock (ICLK)		—	*2	37.6		
		Peripheral module clock A (PCLKA)		—	*2	37.6		
		Peripheral module clock B (PCLKB)		—	*2	37.6		

Note: Reading, programming, and erasing the code flash memory requires that operation be within a specific range of frequencies. See Table 57.3 in section 57, Flash Memory in the User's Manual: Hardware.

Note: For the required relationships between the frequencies of clock signals, see the note under Table 9.2 in section 9, Clock Generation Circuit in the User's Manual: Hardware.

Note 1. The value is 2.0 MHz when the MOCO is selected as the clock source and the frequency is not being divided.

Note 2. The value is 32.768 kHz when the sub-clock oscillator is selected as the clock source and the frequency is not being divided.

6.3.2 Clock Timing

Table 6.19 Timing of the Clock Signals other than the Sub-clock Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXCyc}	35	—	—	ns	Figure 6.11
EXTAL external clock input high pulse width	t_{EXH}	14	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	14	—	—	ns	
EXTAL external clock input rising time	t_{EXr}	—	—	3.5	ns	
EXTAL external clock input falling time	t_{EXf}	—	—	3.5	ns	
Main clock oscillator frequency	f_{MAIN}	8	—	32	MHz	—
Waiting time till the main clock oscillation is stable (crystal)*1	$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 6.12
LOCO clock oscillation frequency	f_{LOCO}	27.8	32.7	37.6	kHz	—
Waiting time till the LOCO clock oscillation is stable	t_{LOCOWT}	—	—	130	μs	Figure 6.13
IWDT-dedicated clock oscillation frequency	$f_{IWDTLOCO}$	13.9	16.35	18.8	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	1.4	2	2.3	MHz	—
Waiting time till the MOCO clock oscillation is stable	t_{MOCOWT}	—	—	16	μs	—
HOCO clock oscillation frequency*3	f_{HOCO24}	23.52	24	24.96	MHz	$0^{\circ}\text{C} \leq T_a \leq +85^{\circ}\text{C}$
	f_{HOCO32}	31.36	32	33.28		
	f_{HOCO48}	47.04	48	49.92		
	f_{HOCO64}	62.72	64	66.56		
	f_{HOCO24}	22.80	24	24.96		$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$
	f_{HOCO32}	30.40	32	33.28		
	f_{HOCO48}	45.60	48	49.92		
	f_{HOCO64}	60.80	64	66.56		
HOCO clock oscillation stabilization wait time*2	t_{HOCOWT}	—	—	700	μs	—
PLL output clock frequency	f_{PLL}	32	—	64	MHz	PLLCCR.FSEL0 = 1
		32	—	48		PLLCCR.FSEL0 = 0
Waiting time till the PLL output clock oscillation is stable	t_{PLLWT}	—	—	1020	μs	Figure 6.14 Includes the stabilization waiting time for LOCO clock oscillation

Note 1. For setting up the main clock oscillator, we recommend consulting the oscillator manufacturer regarding the results of oscillation evaluation and use the results for the oscillation stabilization time. The value of the MOSCWTCR register should correspond to at least that value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time period between when HOCOCCR.HCSTP is changed to 0 and when OSCSF.HOCOSF is changed to 1.

Note 3. The guaranteed values stated for this item apply to products in packages. If you are using WLPGA samples, note that the characteristics deteriorate once the device has been mounted on your system due to fluctuations in stress.

Table 6.20 Timing of the Sub-clock Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 6.15

Note 1. For setting up the sub-clock oscillator, we recommend consulting the oscillator manufacturer regarding the results of oscillation evaluation and use the results for the oscillation stabilization time. After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. We recommend using two times the value of the results of oscillation evaluation by the oscillator manufacturer.

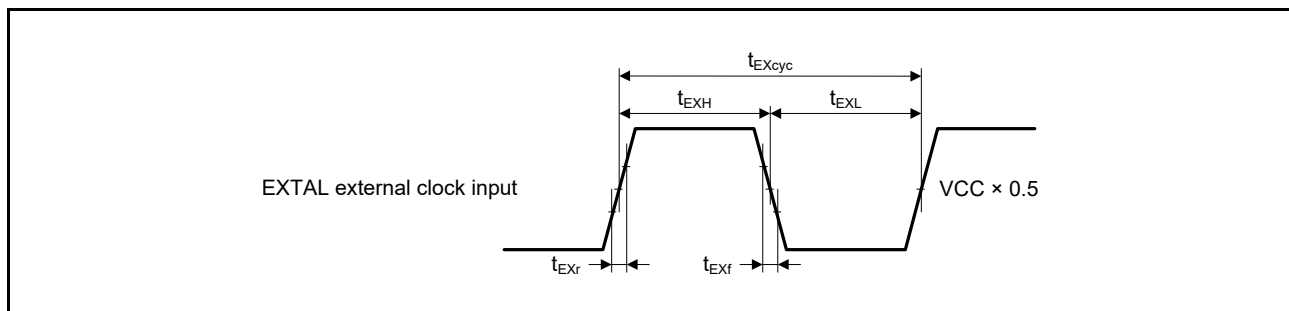


Figure 6.11 EXTAL External Clock Input Timing

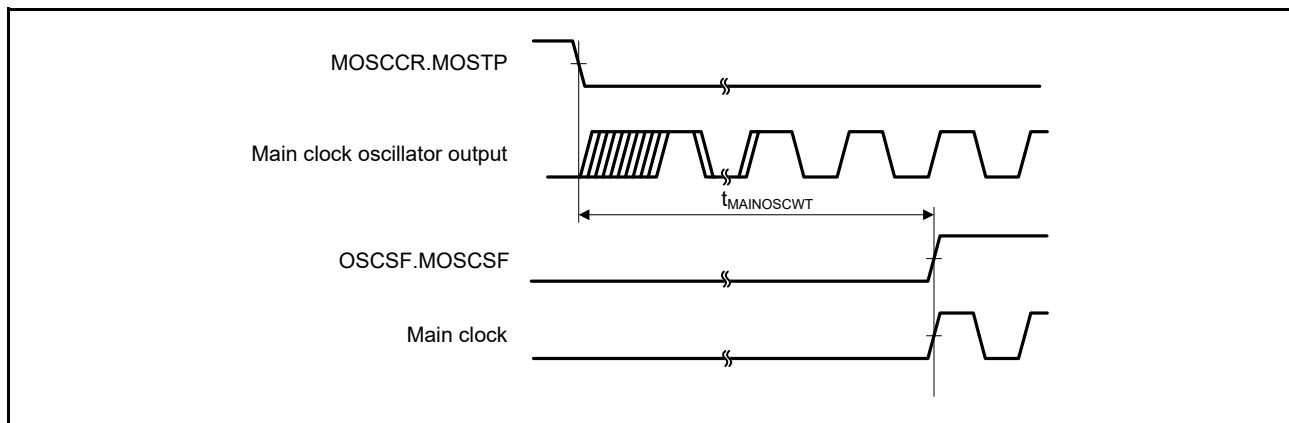


Figure 6.12 Main Clock Oscillation Start Timing

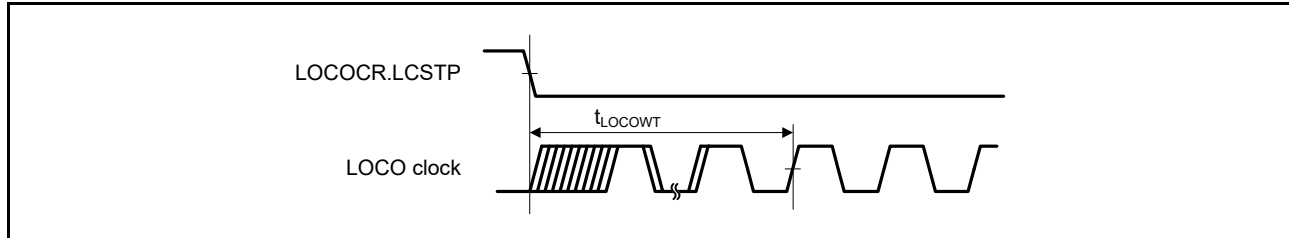


Figure 6.13 LOCO Clock Oscillation Start Timing

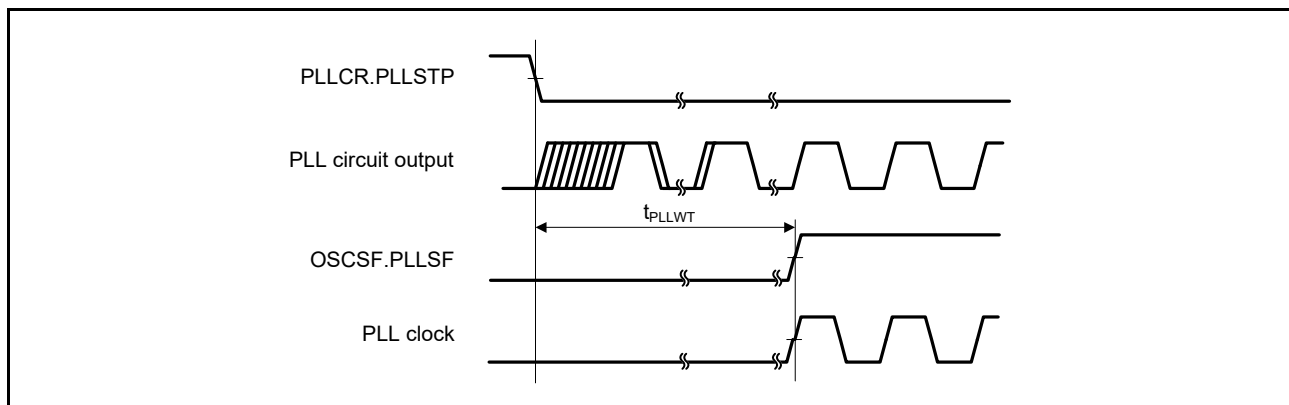


Figure 6.14 PLL Clock Oscillation Start Timing

Note: Start the PLL after the main clock oscillation is stabilized.

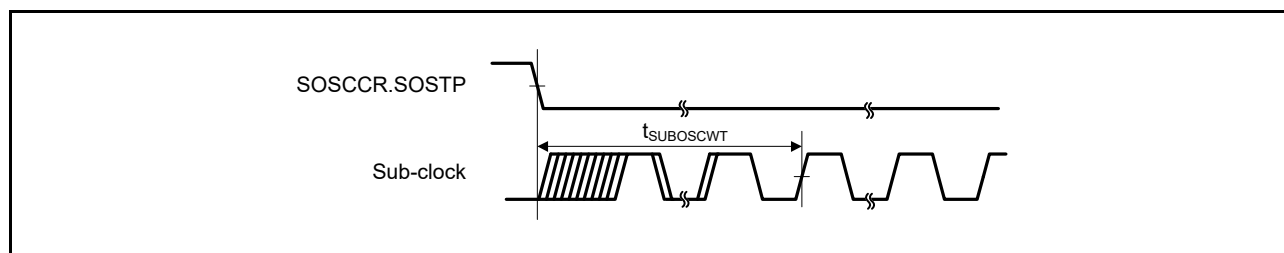


Figure 6.15 Sub-clock Oscillation Start Timing

6.3.3 Reset Timing

Table 6.21 Reset Timing

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
RES# pulse width	Power-on (in the normal startup mode)		t _{RESWP}	44	—	—	ms	Figure 6.16	
	Deep software standby mode (in the normal startup mode)		t _{RESWD}	13	—	—	ms	Figure 6.17	
	Software standby mode, Subosc-speed mode		t _{RESWS}	7.0	—	—	ms		
	ALLPWON	Operation in boost mode	t _{RESW}	0.9	—	—	ms		
		Operation in normal mode	t _{RESW}	0.6	—	—	ms		
		Operation in low leakage current mode	t _{RESW}	1.6	—	—	ms		
		Transition from boost mode to normal mode in progress	t _{RESW}	0.6	—	—	ms		
		Transition from normal mode to boost mode in progress	t _{RESW}	1.8	—	—	ms		
		Transition from normal mode to low leakage current mode in progress	t _{RESW}	2.1	—	—	ms		
		Transition from low leakage current mode to normal mode in progress	t _{RESW}	1.2	—	—	ms		
		EXFPWON	Operation in normal mode	t _{RESW}	1.9	—	—		ms
			Operation in low leakage current mode	t _{RESW}	2.0	—	—		ms
	Transition from normal mode to low leakage current mode in progress		t _{RESW}	2.4	—	—	ms		
	Transition from low leakage current mode to normal mode in progress		t _{RESW}	2.1	—	—	ms		
	MINPWON	Operation in normal mode	t _{RESW}	2.3	—	—	ms		
		Operation in low leakage current mode	t _{RESW}	2.5	—	—	ms		
		Transition from normal mode to low leakage current mode in progress	t _{RESW}	6.1	—	—	ms		
		Transition from low leakage current mode to normal mode in progress	t _{RESW}	2.6	—	—	ms		
	Transition between ALLPWON and EXFPWON modes in normal mode in progress		t _{RESW}	2.5	—	—	ms		
	Transition between EXFPWON and MINPWON modes in normal mode in progress		t _{RESW}	2.0	—	—	ms		
	Transition between ALLPWON and EXFPWON modes in VBB mode in progress		t _{RESW}	3.0	—	—	ms		
	Transition between EXFPWON and MINPWON modes in VBB mode in progress		t _{RESW}	6.5	—	—	ms		
	Waiting time after release from the RES# pin reset			t _{RESWT}	—	19	22		ms

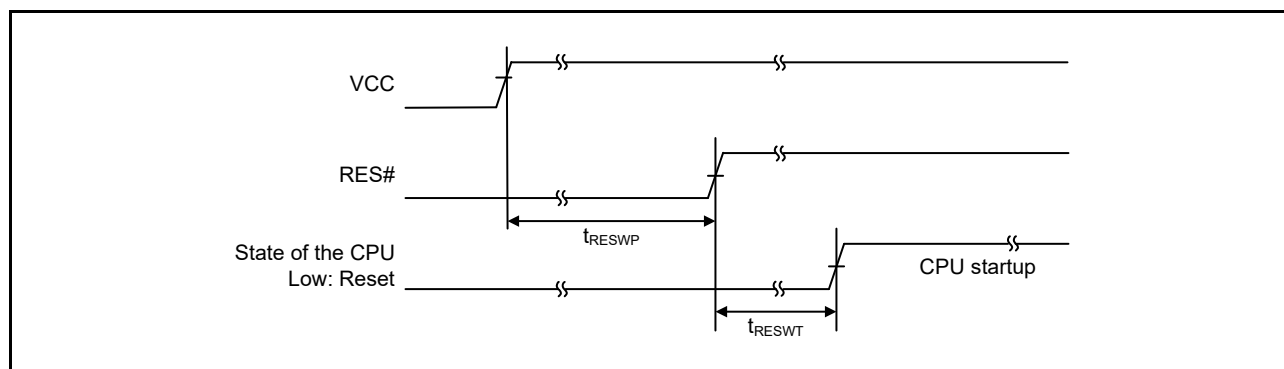


Figure 6.16 Timing of Input through the Reset Pin when Power is Supplied

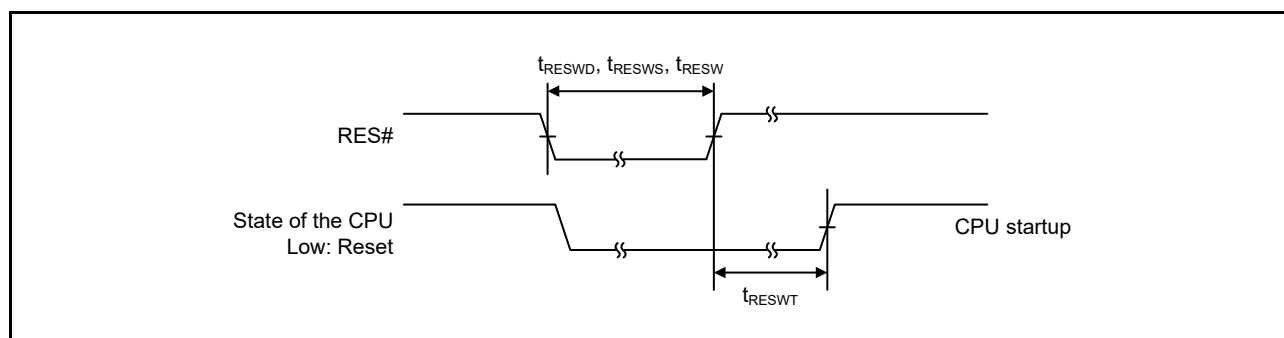


Figure 6.17 Reset Input Timing

6.3.4 Wakeup Timing

Table 6.22 Timing of Return from Low Power Consumption (Standby) Mode

Item	Power Control Mode before and after the Mode Transition	System Clock Source	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Time to return to operating mode (ALLPWON) from software standby (EXFPWON)*1	VBB	SOSC	t _{SBYSC}	—	—	6.0	ms	All oscillators have the same frequency divisor of 1. Measurement was in the ALLPWON power supply mode.
		LOCO	t _{SBYLO}	—	—	6.2	ms	
Time to return to operating mode (EXFPWON) from software standby (EXFPWON)*1	VBB	SOSC	t _{SBYSC}	—	—	1.2	ms	All oscillators have the same frequency divisor of 1. Measurement was in the EXFPWON power supply mode.
		LOCO	t _{SBYLO}	—	—	1.1	ms	
Time to return to operating mode (MINPWON) from software standby (MINPWON)*1	VBB	SOSC	t _{SBYSC}	—	—	1.2	ms	All oscillators have the same frequency divisor of 1. Measurement was in the MINPWON power supply mode.
		LOCO	t _{SBYLO}	—	—	1.1	ms	
Time to return from deep software standby (in normal startup mode)			t _{DSBY}	—	—	9	ms	Figure 6.18
Waiting time following release from deep software standby			t _{DSBYWT}	—	—	22	ms	

Note 1. The system clock source determines the time return takes. If multiple oscillators are started, the time return takes can be calculated from the following expression. Total time for return = time for return of the oscillator that serves as the system source clock + maximum oscillation stabilization time of an oscillator that requires more stabilization time than the system source clock + 2 cycles of LOCO (if LOCO is to operate) + 3 cycles of SOSC (if the sub-clock oscillator is to operate and MSTPCRC.MSTPC0 = 0 (releasing the CAC from the module-stop state)).

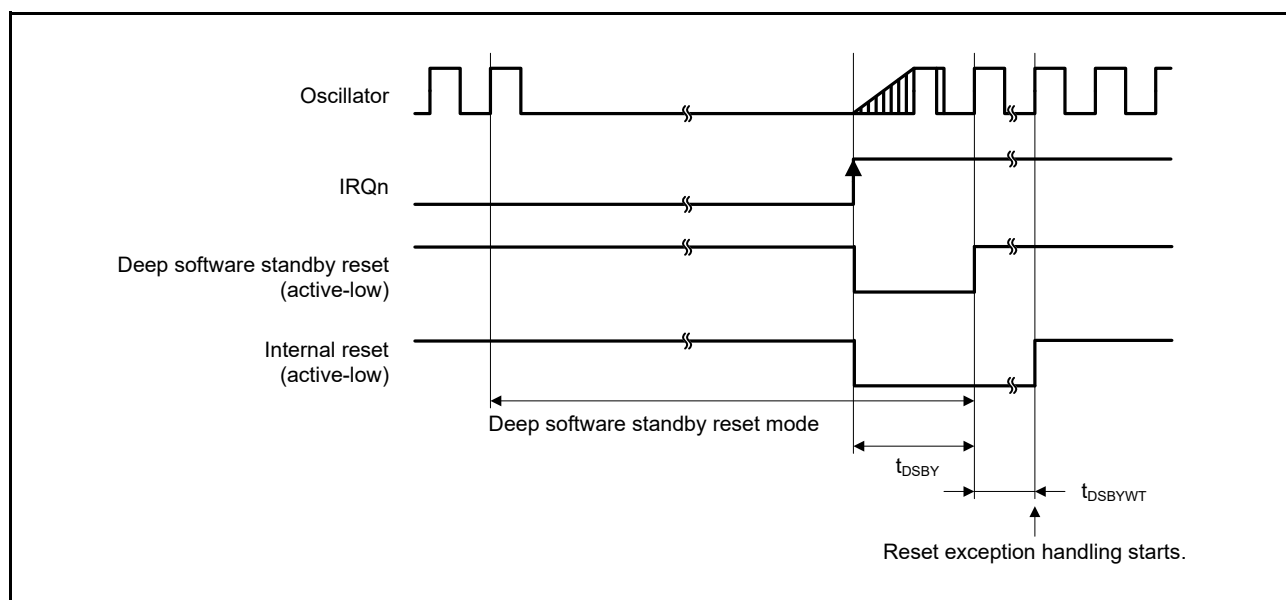


Figure 6.18 Timing of Release from Deep Software Standby

6.3.5 Interrupt Input Timing

Table 6.23 Interrupt Input Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	6000	—	—	ns	Software standby in low leakage current mode
		1000	—	—		Software standby when not in low leakage current mode
		300	—	—		In deep software standby mode
		4	—	—	t_{Pcyc}^{*1}	Other than above
IRQn pulse width	t_{IRQW}	6000	—	—	ns	Software standby in low leakage current mode
		1000	—	—		Software standby when not in low leakage current mode
		300	—	—		In deep software standby mode
		4	—	—	t_{Pcyc}^{*1}	Other than above IRQCRI.IRQMD[1:0] = 00b, 01b
		5	—	—		Other than above IRQCRI.IRQMD[1:0] = 10b
KINT pulse width	t_{KINTW}	6000	—	—	ns	Software standby in low leakage current mode
		1000	—	—		Software standby when not in low leakage current mode
		4	—	—	t_{Pcyc}^{*1}	In deep software standby mode

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKB.

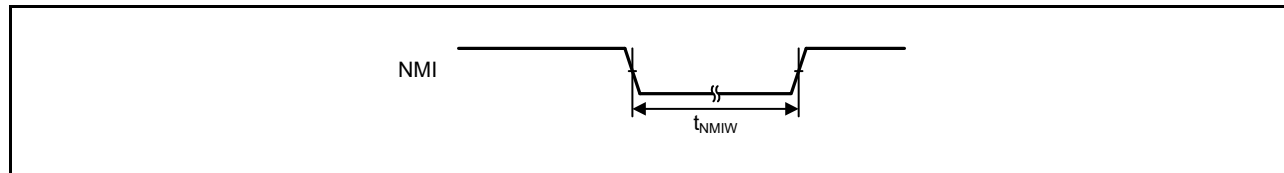


Figure 6.19 NMI Interrupt Input Timing

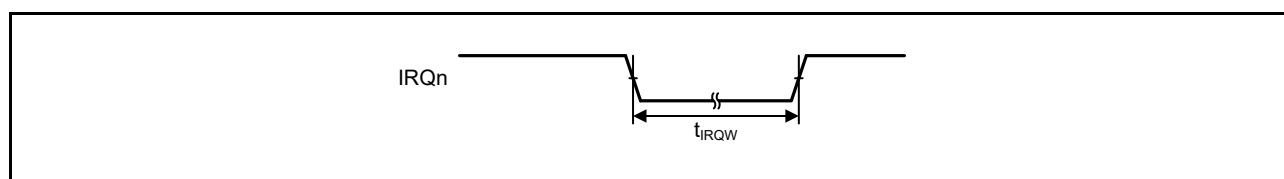


Figure 6.20 IRQn Interrupt Input Timing

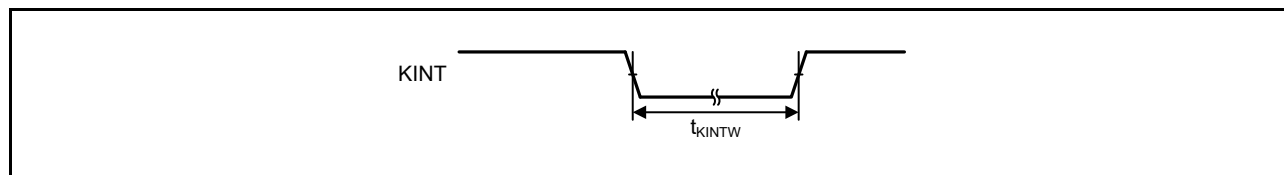


Figure 6.21 Key Interrupt Input Timing

6.3.6 I/O Ports, POE, GPT, AGT, and S14AD Trigger Timing

Table 6.24 I/O Ports, POE, GPT, AGT, and S14AD Trigger Timing

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	2.5	—	—	t _{Pcyc}	Figure 6.22
	ELC event pulse input width			4	—	—		
POE	POE input trigger pulse width		t _{POEW}	1.5	—	—	t _{Pcyc}	Figure 6.23
GPT	Input capture pulse width	Single edge	t _{GTICW}	1.5	—	—	t _{Pcyc}	Figure 6.24
		Both edges		2.5	—	—		
AGT	AGTIO _n input cycles		t _{ACYC}	4	—	—	t _{Pcyc}	Figure 6.25 AGTMR1.TEDGPL = 0 AGTMR1.TMOD[2:0] = 010b
				9	—	—		Figure 6.25 AGTMR1.TEDGPL = 1 AGTMR1.TMOD[2:0] = 010b
	AGTIO _n input high- and low-level width		t _{ACKWH} , t _{ACKWL}	1	—	—		Figure 6.25 AGTMR1.TEDGPL = 0 AGTMR1.TMOD[2:0] = 010b
				4	—	—		Figure 6.25 AGTMR1.TEDGPL = 1 AGTMR1.TMOD[2:0] = 010b
	AGTEEn input high- and low-level width		t _{ACKWH} , t _{ACKWL}	—	1	—	t _{ACYC}	Figure 6.25 AGTMR1.TEDGPL = 0 AGTMR1.TMOD[2:0] = 010b
				4	—	—	t _{Pcyc}	Figure 6.25 AGTMR1.TEDGPL = 1 AGTMR1.TMOD[2:0] = 010b
S14AD	14-bit A/D converter trigger input pulse width		t _{TRGW}	1.5	—	—	t _{Pcyc}	Figure 6.26

(n = 0, 1)

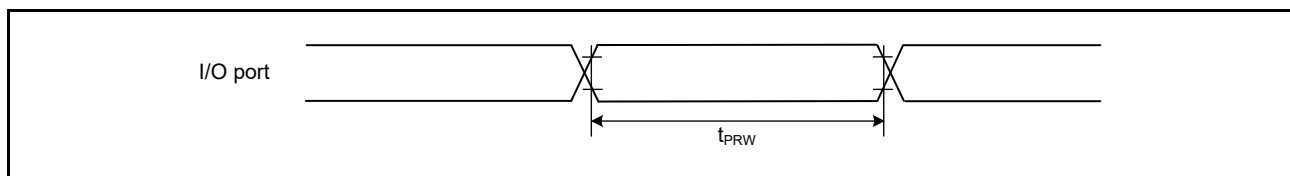
Note 1. t_{Pcyc} refers to the period of a cycle of PCLKA for the GPT, and that of PCLKB for the I/O ports, POE, AGT, and S14AD.

Figure 6.22 I/O Port Input Data Pulse Width

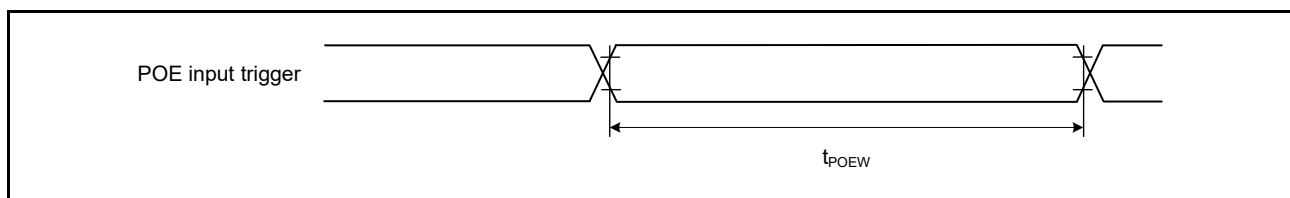


Figure 6.23 POE Input Trigger Pulse Width

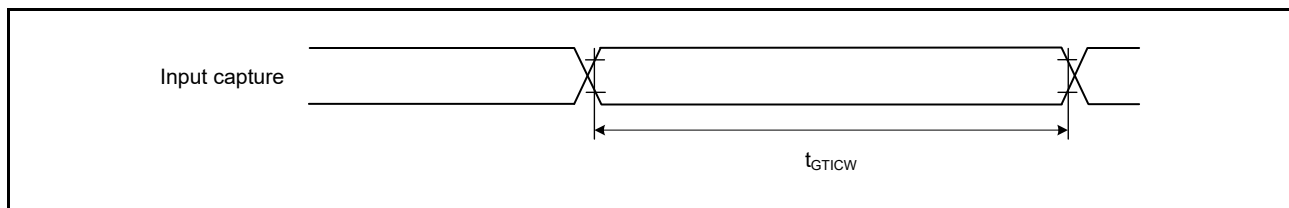


Figure 6.24 GPT Input Capture Pulse Width

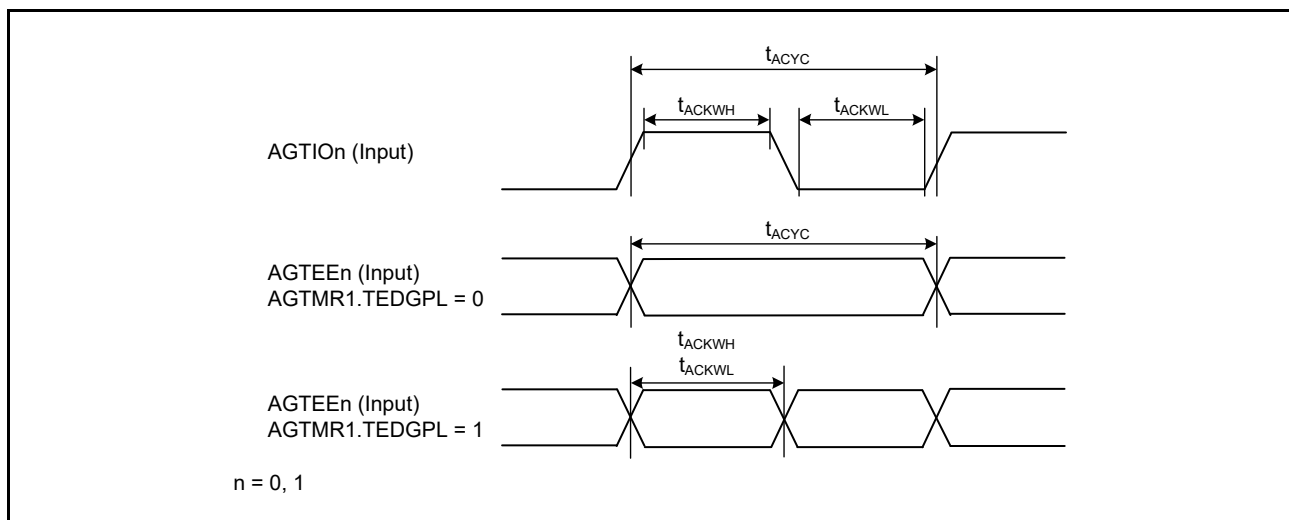


Figure 6.25 AGT I/O Timing

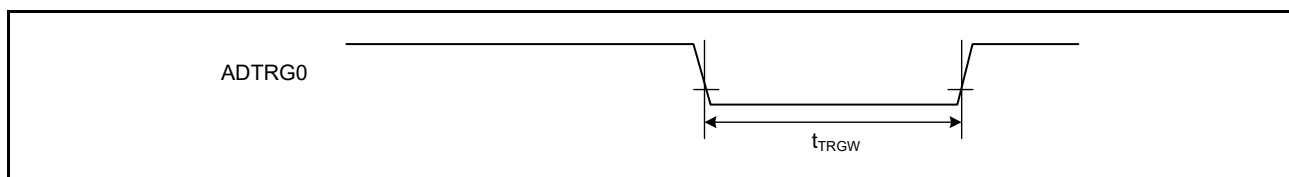


Figure 6.26 S14AD Trigger Input Timing

6.3.7 CAC Timing

Table 6.25 CAC Timing

Item			Symbol	Min.	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{P_{cyc}}^{*1} \leq t_{cac}^{*2}$	t_{CACREF}	$4.5t_{cac} + 3t_{P_{cyc}}$	—	ns	—
		$t_{P_{cyc}}^{*1} > t_{cac}^{*2}$		$5t_{cac} + 6.5t_{P_{cyc}}$	—	ns	

Note 1. $t_{P_{cyc}}$ refers to the period of a cycle of PCLKB.

Note 2. t_{cac} refers to the period of a cycle of the CAC count clock source.

6.3.8 SCI Timing

Table 6.26 SCI Timing (1)

Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
SCI	Frequency (SCI0, SCI1)		BOOST	pclkfmax	—	64	MHz	—
			NORMAL		—	32		
	Frequency (other than SCI0, SCI1)		—		32			
	Input clock cycle	Asynchronous	t _{Scyc}	4	—	t _{Pcyc}	Figure 6.27	
		Clock synchronous		6	—			
	Input clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}		
	Input clock rise time		t _{SCKr}	—	1 × t _{Pcyc}	ns		
	Input clock fall time		t _{SCKf}	—	1 × t _{Pcyc}	ns		
	Output clock cycle	Asynchronous	t _{Scyc}	6	—	t _{Pcyc}		
		Clock synchronous		4	—			
	Output clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}		
	Output clock rise time		t _{SCKr}	—	1 × t _{Pcyc}	ns		
	Output clock fall time		t _{SCKf}	—	1 × t _{Pcyc}	ns		
	Transmit data delay time	Master	t _{TXD}	—	40	ns	Figure 6.28	
		Slave		—	55			
	Receive data setup time	Master	t _{RXS}	45	—	ns		
		Slave		27	—			
	Receive data hold time	Master	t _{RXH}	5	—	ns		
		Slave		40	—			

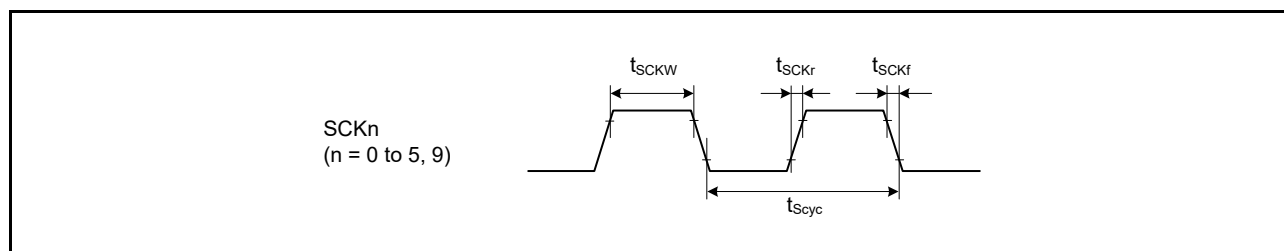
Note 1. t_{Pcyc} refers to the period of a cycle of PCLKA in the SCI0 and SCI1, and that of PCLKB in the SCI2 to SCI5 and SCI9.

Figure 6.27 SCK Clock Input Timing

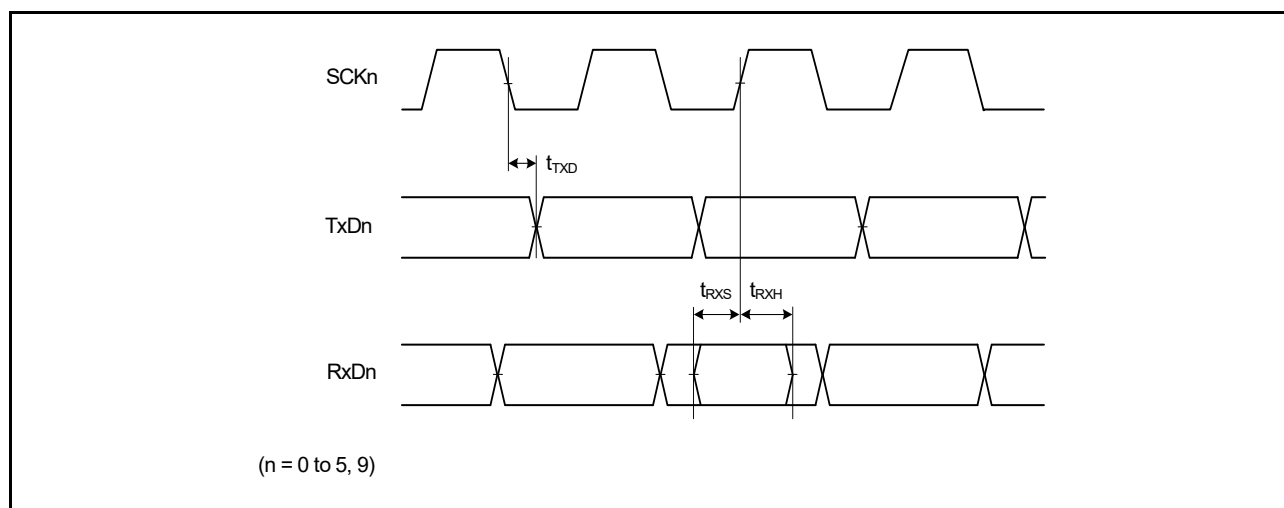


Figure 6.28 SCI Input and Output Timing in Clock Synchronous Mode

Table 6.27 SCI Timing (2)

Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
Simple SPI	Frequency (SCI0, SCI1)		BOOST	pclkfmax	—	64	MHz	—
			NORMAL		—	32		
	Frequency (other than SCI0, SCI1)		—		32			
	SCK clock cycle	Master	t _{SPcyc}	4	65536	t _{Pcyc}	Figure 6.29	
		Slave		6	—			
	SCK clock high pulse width		t _{SPCKWH}	0.4	0.6	t _{SPcyc}		
	SCK clock low pulse width		t _{SPCKWL}	0.4	0.6	t _{SPcyc}		
	SCK clock rise/fall time		t _{SPCKr} , t _{SPCKf}	—	1 × t _{Pcyc}	ns		
	Data input setup time	Master	t _{SU}	45	—	ns	Figure 6.30 to Figure 6.33	
		Slave		27	—			
	Data input hold time	Master	t _H	33.3	—	ns		
		Slave		40	—			
	SS input setup time		t _{LEAD}	1	—	t _{SPcyc}		
	SS input hold time		t _{LAG}	1	—	t _{SPcyc}		
	Data output delay time	Master	t _{OD}	—	40	ns		
		Slave		—	65			
	Data output hold time	Master	t _{OH}	−10	—	ns		
Slave		−10		—				
Data rise/fall time		t _{Dr} , t _{Df}	—	1 × t _{Pcyc}	ns			
Slave access time	BOOST	t _{SA}	—	8	t _{Pcyc}	Figure 6.32, Figure 6.33		
	NORMAL		—	6				
Slave output release time	BOOST	t _{REL}	—	8	t _{Pcyc}			
	NORMAL		—	6				

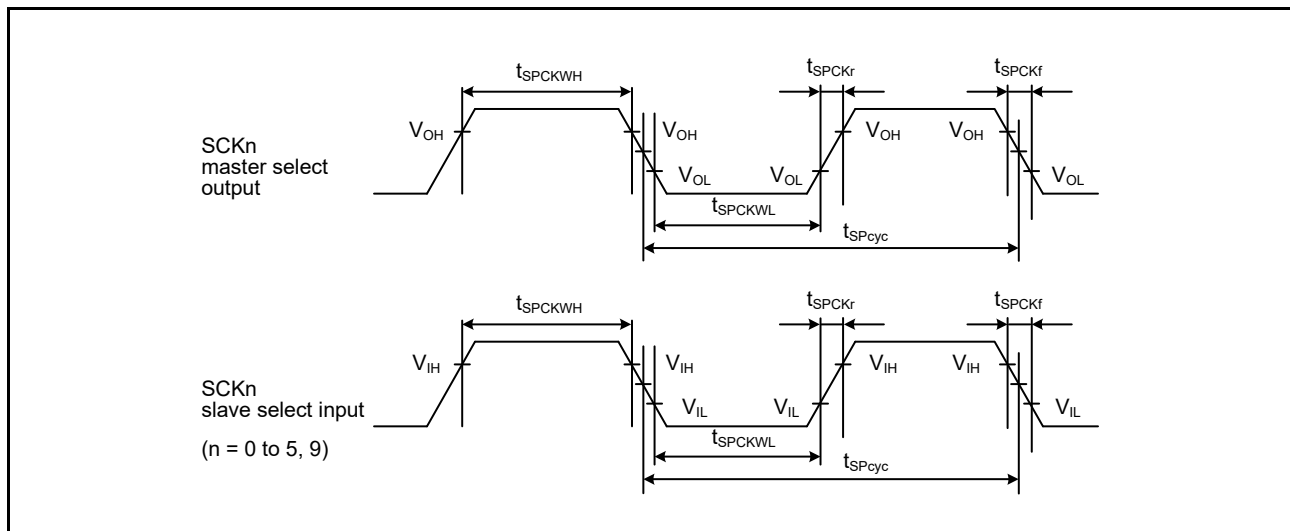
Note 1. t_{PCyc} refers to the period of a cycle of PCLKA in the SCI0 and SCI1, and that of PCLKB in the SCI2 to SCI5 and SCI9.

Figure 6.29 SCK Clock Input and Output Timing (Simple SPI Mode)

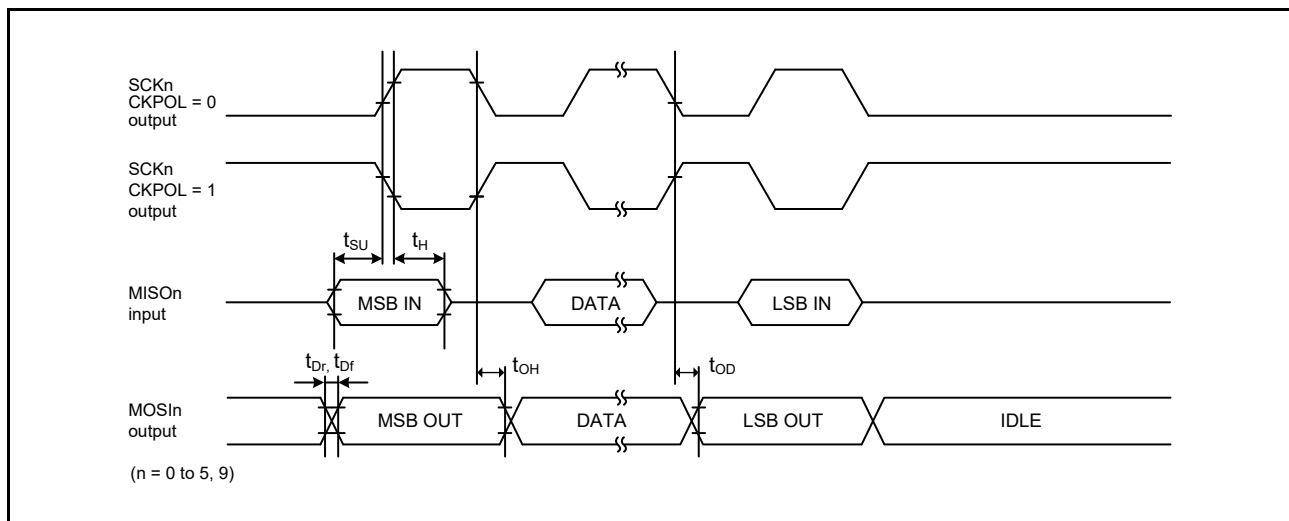


Figure 6.30 SCK Input and Output Timing (Simple SPI Mode) (Master, SPMR.CKPH = 1)

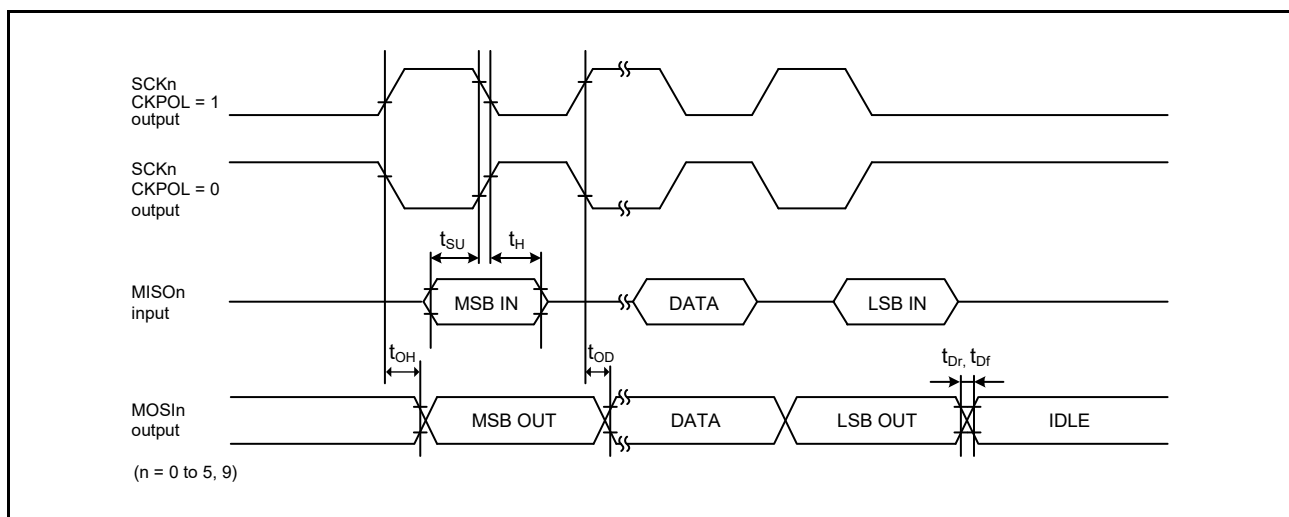


Figure 6.31 SCK Input and Output Timing (Simple SPI Mode) (Master, SPMR.CKPH = 0)

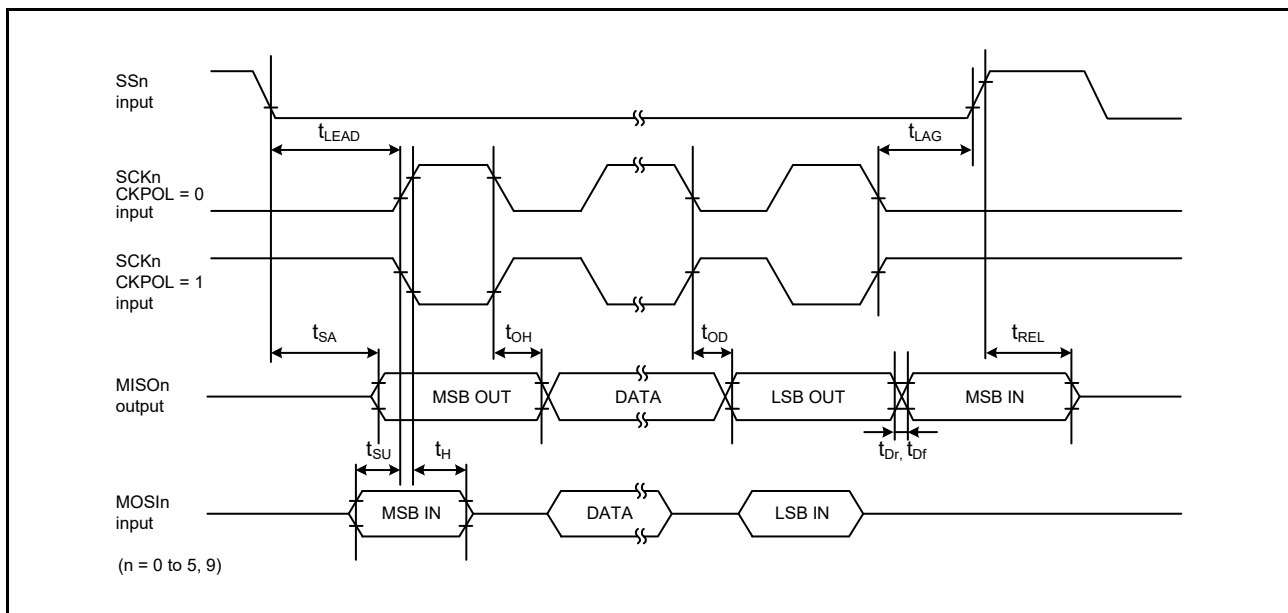


Figure 6.32 SCK Input and Output Timing (Simple SPI Mode) (Slave, SPMR.CKPH = 1)

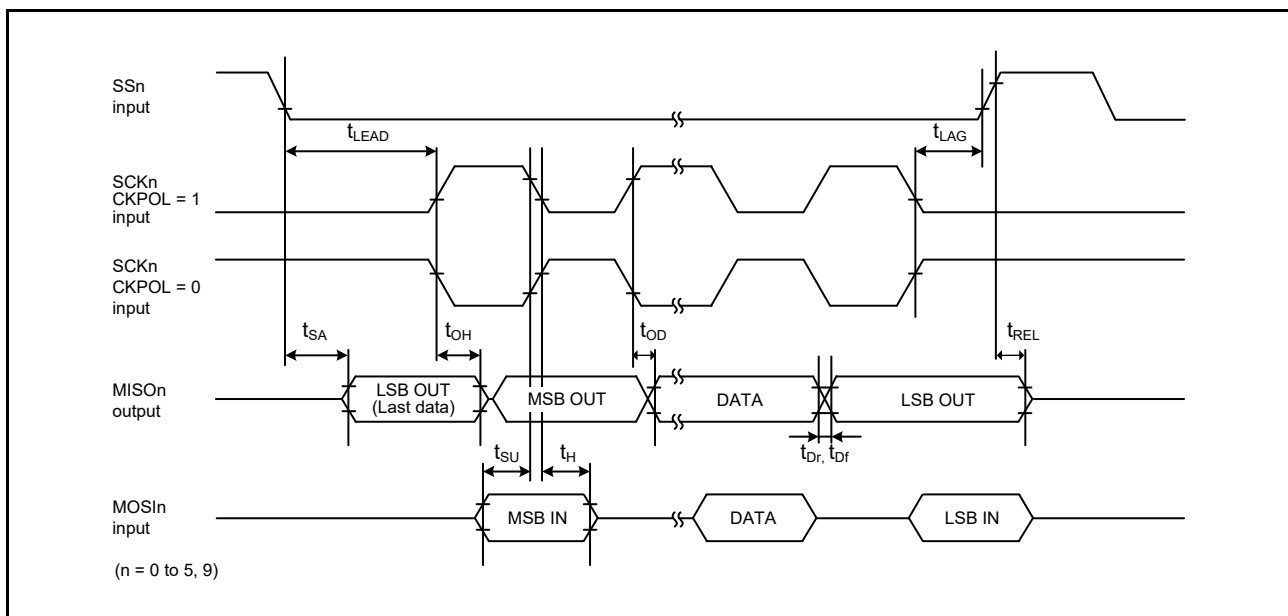
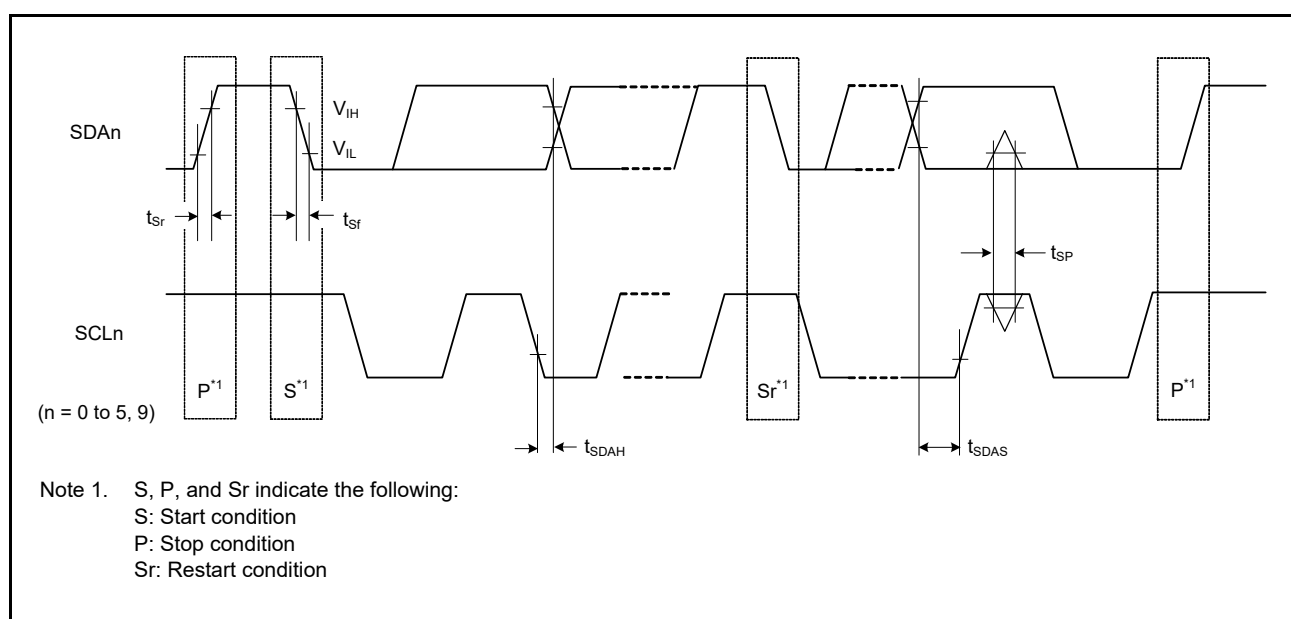


Figure 6.33 SCK Input and Output Timing (Simple SPI Mode) (Slave, SPMR.CKPH = 0)

Table 6.28 SCI Timing (3)

Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item			Symbol	Min.	Max. ^{*2}	Unit	Test Conditions
Simple IIC (standard mode)	Frequency (SCI0, SCI1)	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	Frequency (other than SCI0, SCI1)			—	32		
	SDA input rise time		t_{Sr}	—	1000	ns	Figure 6.34
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time		t_{SP}	0	4	t_{Pcyc}	Figure 6.34 SMR.CKS[1:0] = 00b, SNFR.NFCS[2:0] = 001b
					1024		Figure 6.34 SMR.CKS[1:0] = 11b, SNFR.NFCS[2:0] = 100b
	Data input setup time		t_{SDAS}	250	—	ns	Figure 6.34
	Data input hold time		t_{SDAH}	0	—	ns	
	SCI and SDA load capacitance		C_b^{*1}	—	400	pF	
Simple IIC (fast mode)	Frequency (SCI0, SCI1)	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	Frequency (other than SCI0, SCI1)			—	32		
	SCL and SDA input rise time		t_{Sr}	—	300	ns	Figure 6.34
	SCL and SDA input fall time		t_{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time		t_{SP}	0	4	t_{Pcyc}	Figure 6.34 SMR.CKS[1:0] = 00b, SNFR.NFCS[2:0] = 001b
					1024		Figure 6.34 SMR.CKS[1:0] = 11b, SNFR.NFCS[2:0] = 100b
	Data input setup time		t_{SDAS}	100	—	ns	Figure 6.34
	Data input hold time		t_{SDAH}	0	—	ns	
	SCI and SDA load capacitance		C_b^{*1}	—	400	pF	

Note 1. C_b refers to the total capacitance of the bus line.Note 2. t_{Pcyc} refers to the period of a cycle of PCLKA in the SCI0 and SCI1, and that of PCLKB in the SCI2 to SCI5 and SCI9.Figure 6.34 SCK Input and Output Timing (Simple I²C Mode)

6.3.9 SPI Timing

Table 6.29 SPI Timing

Conditions: High driving ability output is selected by the port drive capability in the PmnPFS register.

Item			Symbol	Min.	Max.	Unit	Test Conditions
SPI	Frequency	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	RSPCK clock cycle	Master	t_{SPCyc}	4	4096	t_{Pcyc}	Figure 6.35
		BOOST		2	4096		
		NORMAL		6	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$3 \times t_{Pcyc}$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$3 \times t_{Pcyc}$	—		
	RSPCK clock rise and fall time	Output	t_{SPCKr}	—	10	ns	Figure 6.35 IOVCCn ≥ 2.7 V
		Input	t_{SPCKf}	—	1	μ s	
	Data input setup time	Master	t_{SU}	25	—	ns	Figure 6.36 to Figure 6.41
		BOOST		15	—		
		NORMAL		10	—		
	Data input hold time	Master	t_{HF}	0	—	ns	Figure 6.36 to Figure 6.41 The PCLKA division ratio is set to 1/2.
				1	—	t_{Pcyc}	
		Slave		20	—	ns	
	SSL setup time	Master	t_{LEAD}	$-30 + N \times t_{SPCyc}^{*1}$	—	ns	Figure 6.36 to Figure 6.41
		Slave		$6 \times t_{Pcyc}$	—	ns	
	SSL hold time	Master	t_{LAG}	$-30 + N \times t_{SPCyc}^{*2}$	—	ns	Figure 6.36 to Figure 6.41
		Slave		$6 \times t_{Pcyc}$	—	ns	
	Data output delay time	Master	t_{OD}	—	14	ns	Figure 6.36 to Figure 6.41 IOVCCn ≥ 2.7 V
		Slave		—	50		
	Data output hold time	Master	t_{OH}	0	—	ns	Figure 6.36 to Figure 6.41
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPCyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPCyc} + 2 \times t_{Pcyc}$	ns	Figure 6.36 to Figure 6.41
		Slave		$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	10	ns	Figure 6.36 to Figure 6.41 IOVCCn ≥ 2.7 V
		Input		—	1	μ s	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	10	ns	Figure 6.36 to Figure 6.41 IOVCCn ≥ 2.7 V
		Input		—	1	μ s	
	Slave access time		t_{SA}	—	$2 \times t_{Pcyc} + 100$	ns	Figure 6.40, Figure 6.41 IOVCCn ≥ 2.7 V
	Slave output release time		t_{REL}	—	$2 \times t_{Pcyc} + 100$	ns	

Note: t_{Pcyc} refers to the period of a cycle of PCLKA.

Note 1. N indicates the RSPCK delay set in the SPCKD register.

Note 2. N indicates the RSPCK delay set in the SSLND register.

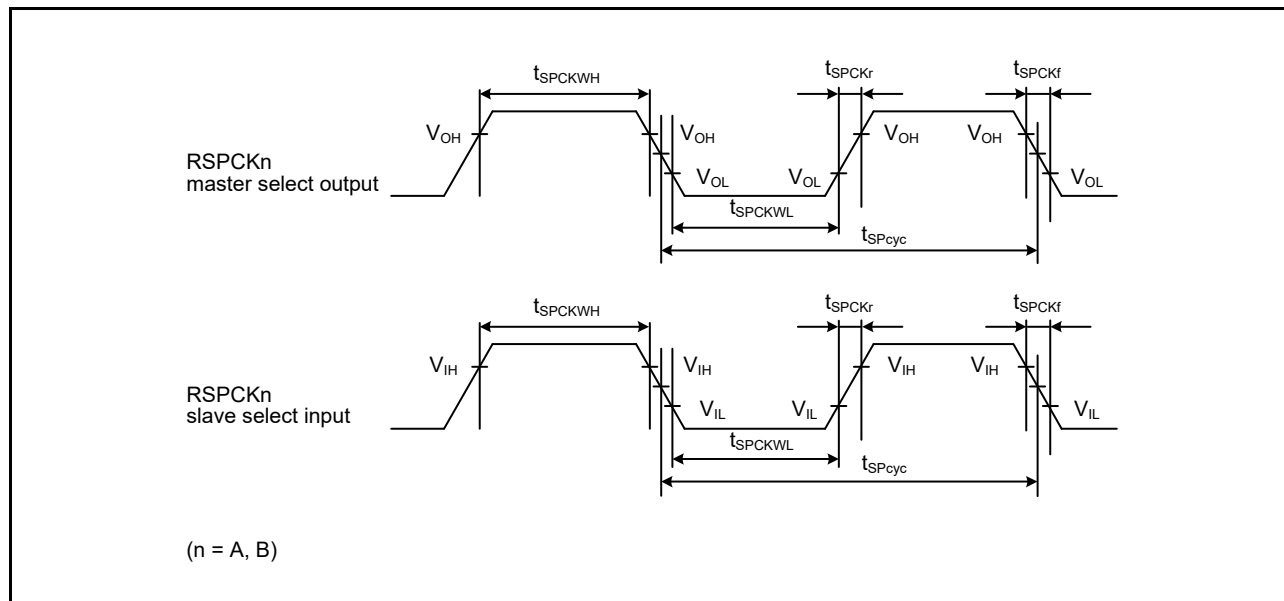


Figure 6.35 SPI Clock Timing

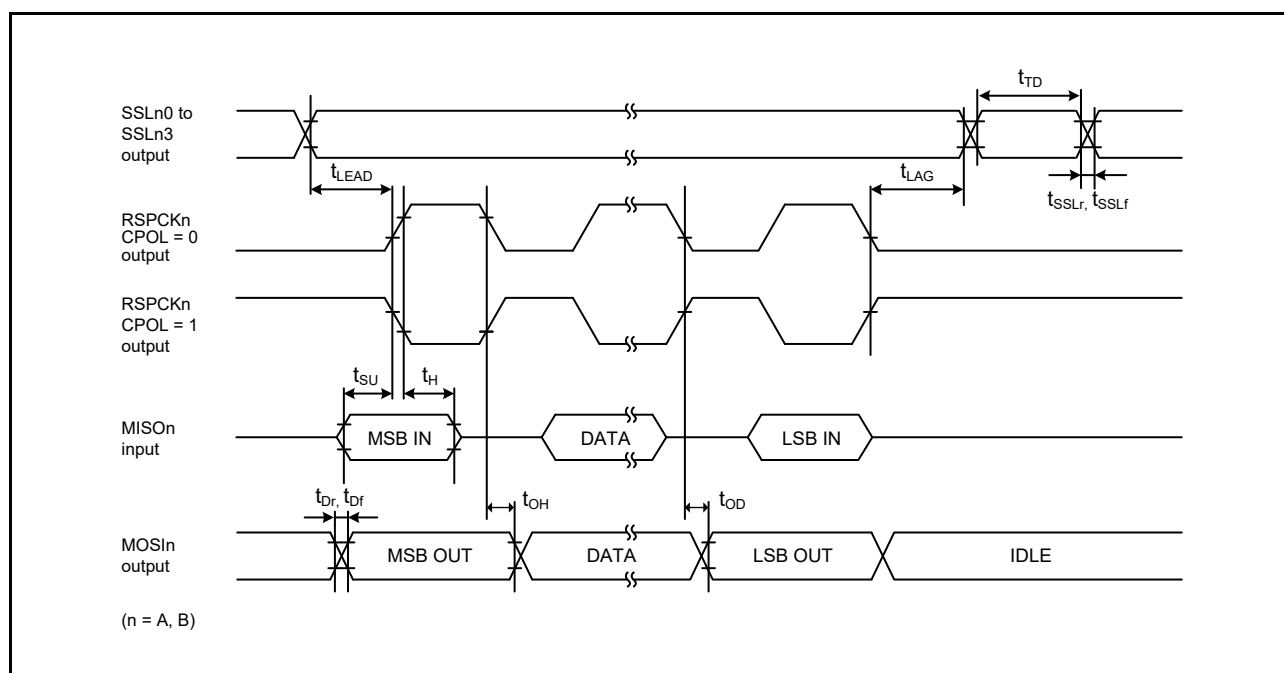


Figure 6.36 SPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio is Set to Any Value Other than 1/2)

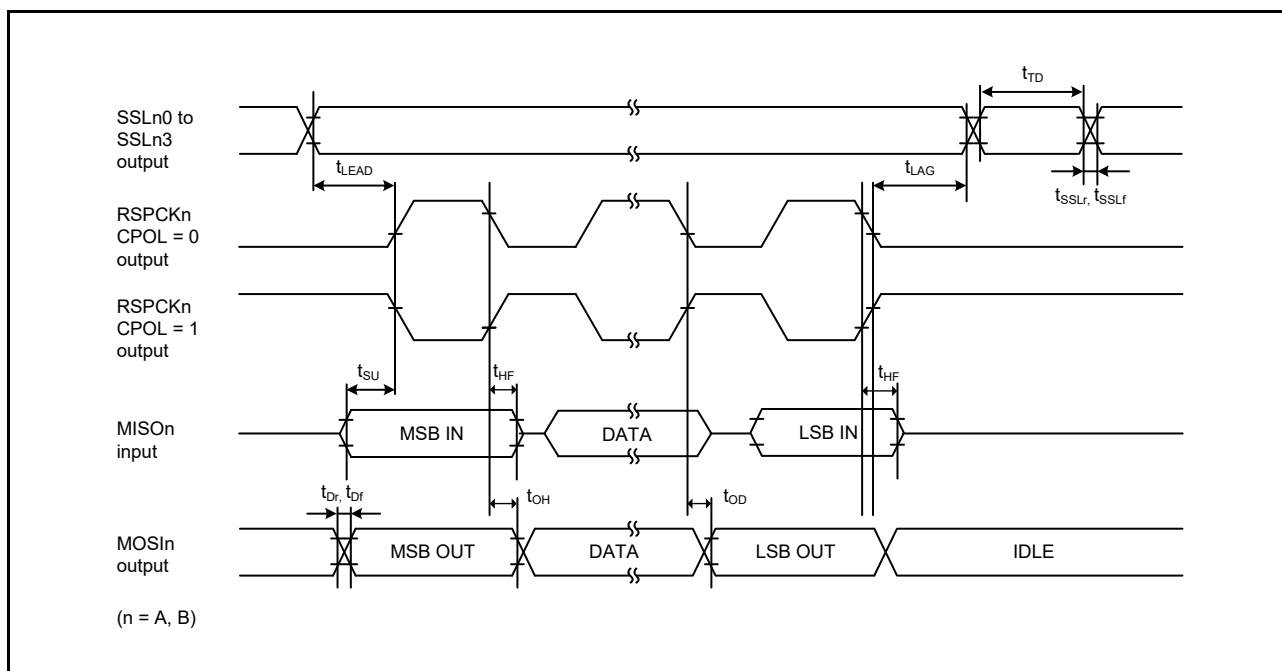


Figure 6.37 SPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio is Set to 1/2)

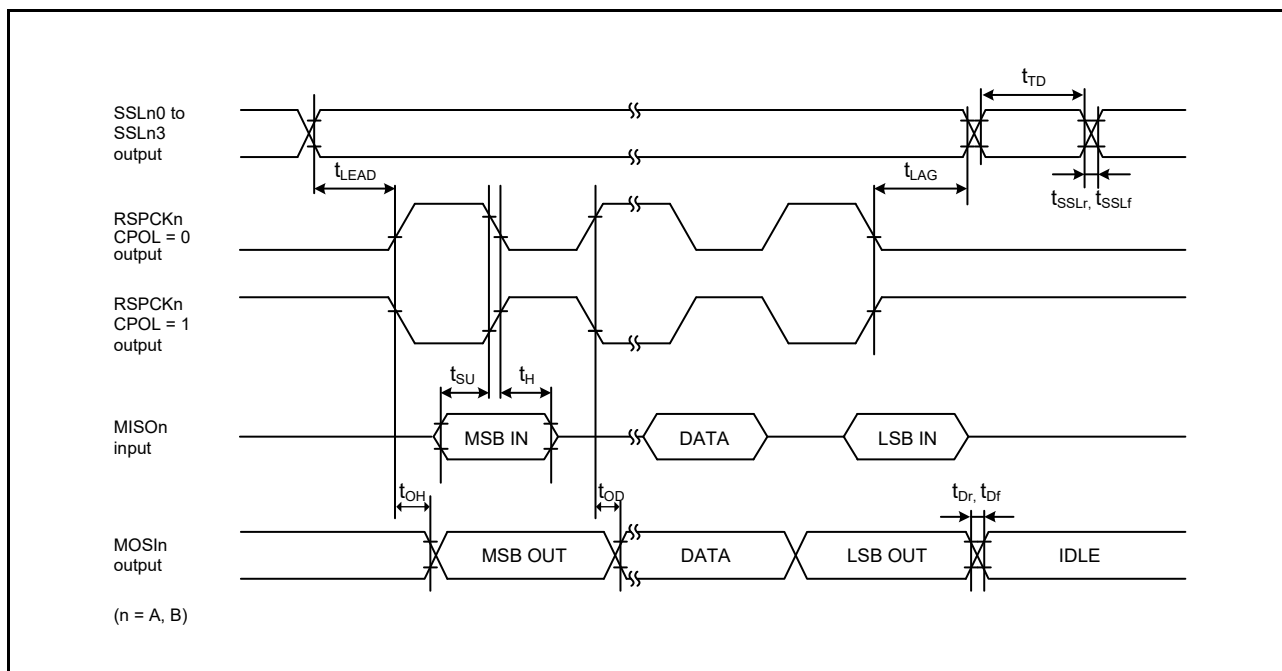


Figure 6.38 SPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio is Set to Any Value Other than 1/2)

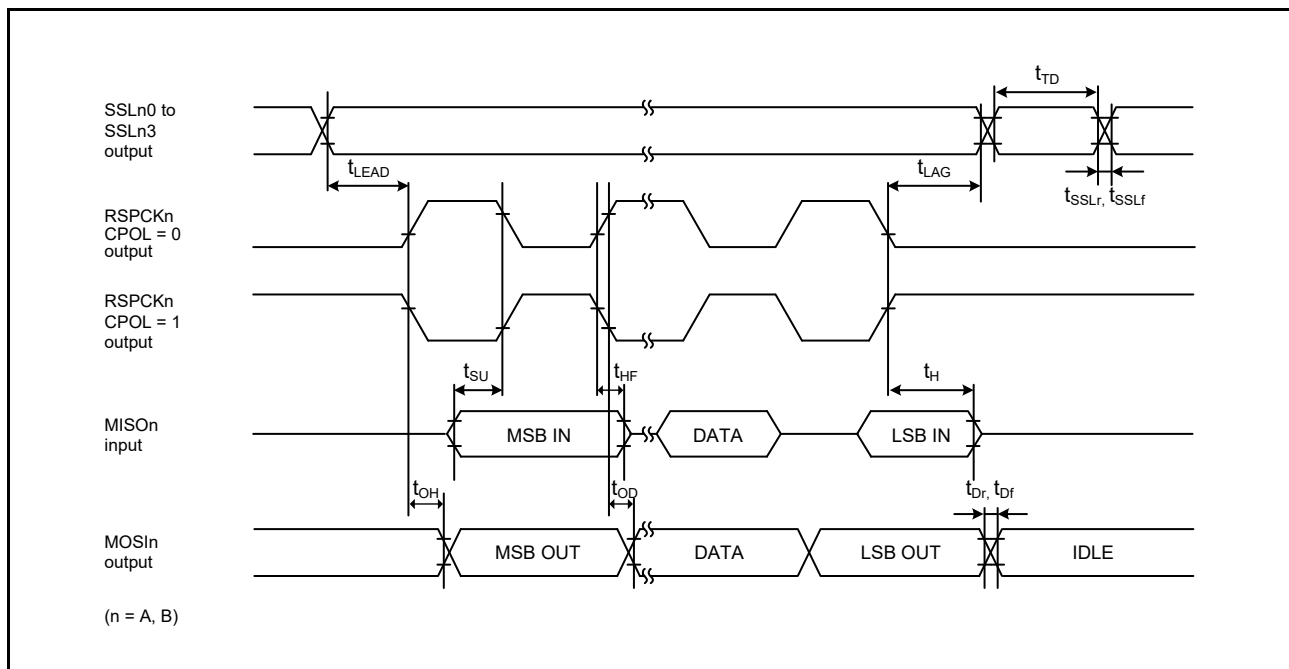


Figure 6.39 SPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio is Set to 1/2)

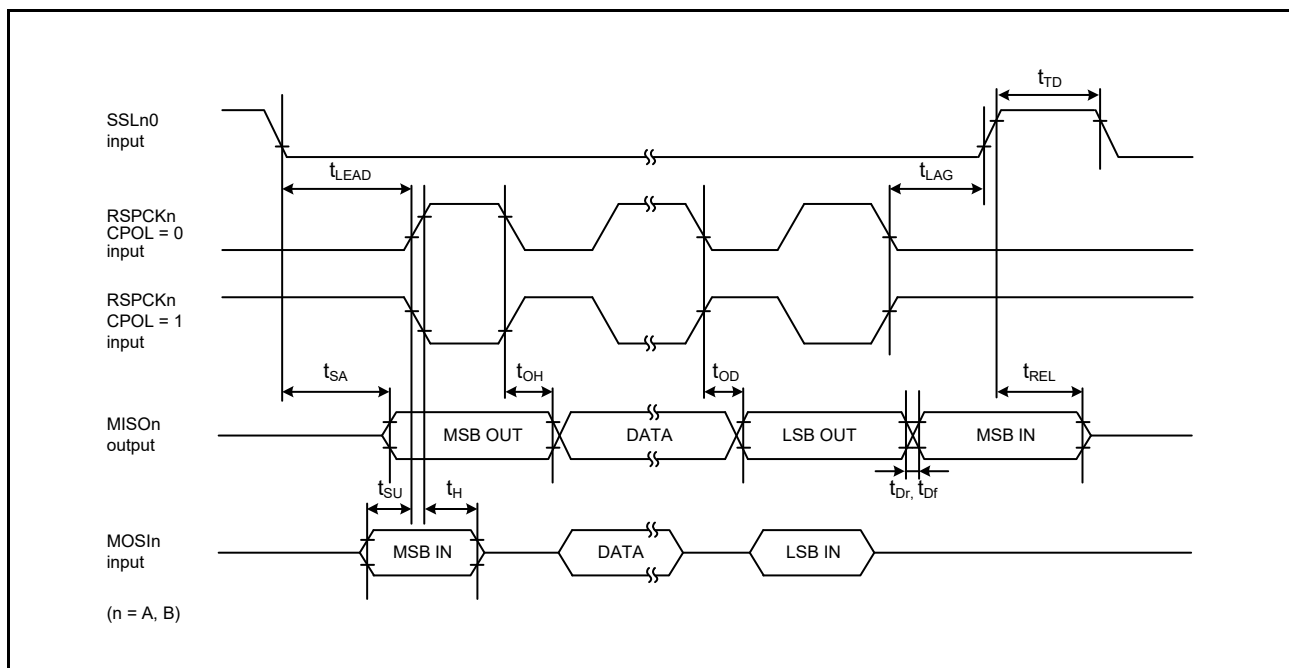


Figure 6.40 SPI Timing (Slave, CPHA = 0)

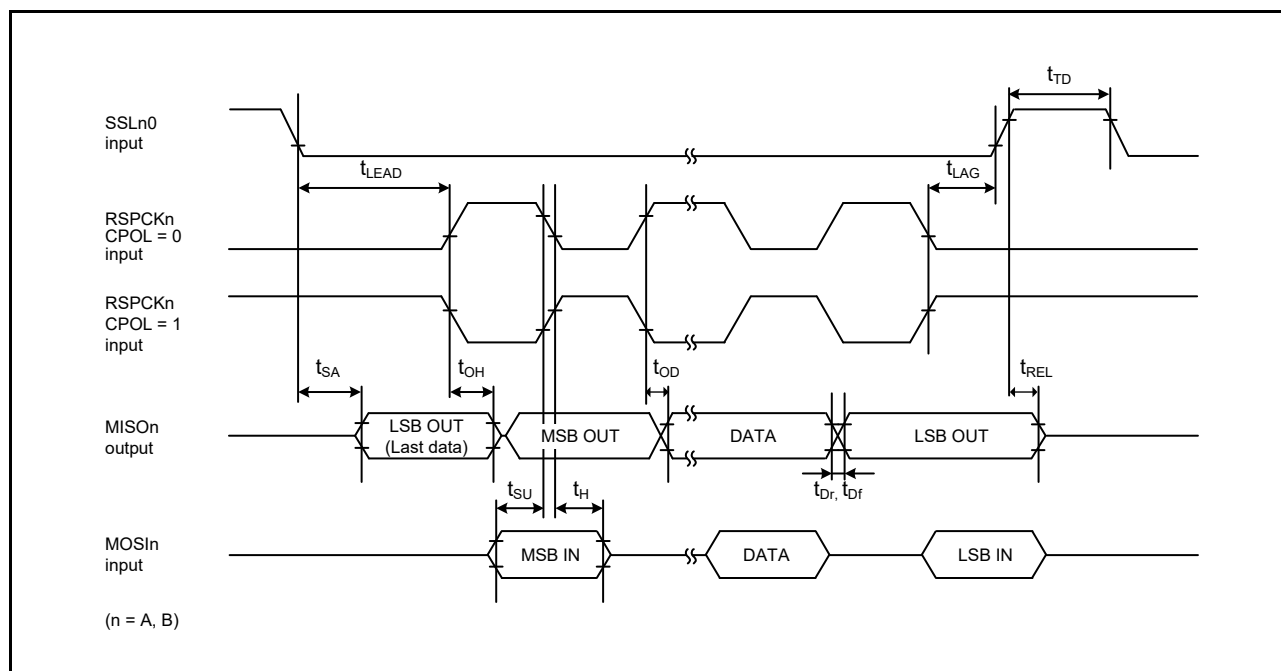


Figure 6.41 SPI Timing (Slave, CPHA = 1)

6.3.10 QSPI Timing

Table 6.30 QSPI Timing

Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
QSPI	QSPCLK clock cycle (PCLKA > 48 MHz)	t _{QScyc}	3	4080	t _{Pcyc}	Figure 6.42
	QSPCLK clock cycle (PCLKA ≤ 48 MHz)		2	4080		
	QSPCLK clock high-level pulse width	t _{QSWH}	t _{QScyc} × 0.4	—	ns	
	QSPCLK clock low-level pulse width	t _{QSWL}	t _{QScyc} × 0.4	—		
Data input setup time		t _{SU}	25	—	ns	Figure 6.43
Data input hold time		t _H	12	—	ns	
QSSL setup time		t _{LEAD}	(L + 0.5) × t _{QScyc} − M*2	—	ns	
QSSL hold time		t _{LAG}	(N + 0.5) × t _{QScyc} − M*3	—	ns	
Data output delay time		t _{OD}	−3.3	14	ns	
Successive transmission delay time		t _{TD}	1	16	t _{QScyc}	

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKA.

Note 2. The setting of the SFMSSC.SFMSSLD bit determines the value of L. The value of M is 10 in the boost mode or 15 in the normal mode.

Note 3. The setting of the SFMSSC.SFMSSHD bit determines the value of N. The value of M is 10 in the boost mode or 15 in the normal mode.

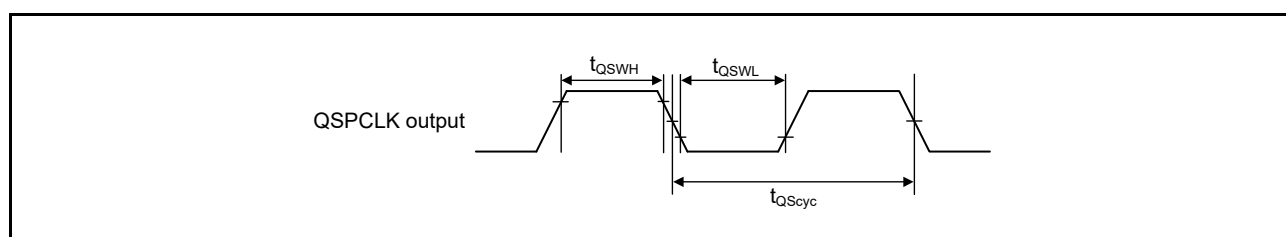


Figure 6.42 QSPI Clock Timing

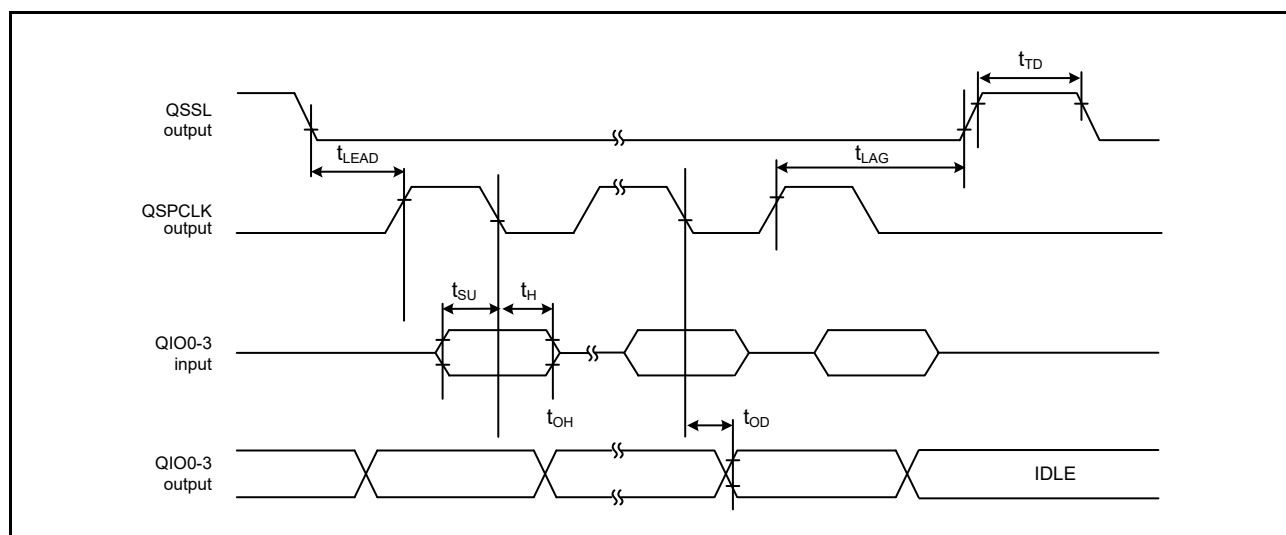


Figure 6.43 QSPI I/O Timing

6.3.11 IIC Timing

Table 6.31 IIC Timing

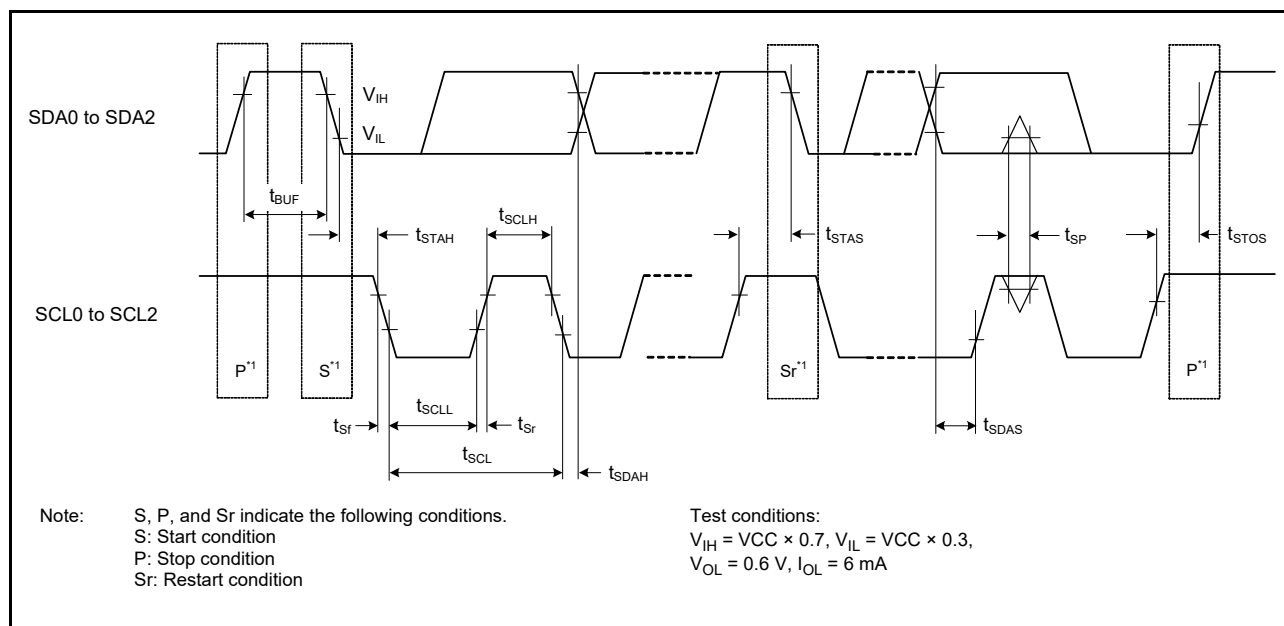
Conditions: $V_{CC} = 3.0$ to 3.6 V, $V_{IH} = V_{CC} \times 0.7$, $V_{IL} = V_{CC} \times 0.3$, $V_{OL} = 0.6$ V, $I_{OL} = 6$ mA
 Standard driving ability output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
IIC (standard mode)	SCL input cycle time	t _{SCL}	6(12) × t _{IICcyc} + 1300	—	ns	Figure 6.44
	SCL input high pulse width	t _{SCLH}	3(6) × t _{IICcyc} + 300	—	ns	
	SCL input low pulse width	t _{SCLL}	3(6) × t _{IICcyc} + 300	—	ns	
	SCL and SDA input rise time	t _{Sr}	—	1000	ns	
	SCL and SDA input fall time	t _{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time	t _{SP}	0	1(4) × t _{IICcyc}	ns	
	SDA input bus free time	t _{BUF}	3(6) × t _{IICcyc} + 300	—	ns	
	Start condition input hold time	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Restart condition input setup time	t _{STAS}	1000	—	ns	
	Stop condition input setup time	t _{STOS}	1000	—	ns	
	Data input setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL and SDA load capacitance*2	C _b	—	400	pF	
	IIC (fast mode)	SCL input cycle time	t _{SCL}	6(12) × t _{IICcyc} + 1300	—	
SCL input high pulse width		t _{SCLH}	3(6) × t _{IICcyc} + 300	—	ns	
SCL input low pulse width		t _{SCLL}	3(6) × t _{IICcyc} + 300	—	ns	
SCL and SDA input rise time		t _{Sr}	—	300	ns	
SCL and SDA input fall time		t _{Sf}	—	300	ns	
SCL and SDA input spike pulse removal time		t _{SP}	0	1(4) × t _{IICcyc}	ns	
SDA input bus free time		t _{BUF}	3(6) × t _{IICcyc} + 300	—	ns	
Start condition input hold time		t _{STAH}	t _{IICcyc} + 300	—	ns	
Restart condition input setup time		t _{STAS}	300	—	ns	
Stop condition input setup time		t _{STOS}	300	—	ns	
Data input setup time		t _{SDAS}	t _{IICcyc} + 50	—	ns	
Data input hold time		t _{SDAH}	0	—	ns	
SCL and SDA load capacitance*2		C _b	—	400	pF	

Note: t_{IICcyc} refers to the period of a cycle of IIC internal reference clock (IIC ϕ).

Note 1. The values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled by setting the ICFER.NFE bit to 1.

Note 2. C_b refers to the total capacitance of the bus line.

Figure 6.44 I²C Bus Interface Input and output Timing

6.3.12 MLCD Timing

Table 6.32 MLCD Timing

Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item	Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
MLCD_SCLK pin output high pulse width	t_{wSCLKH}	1	—	255	t_{Pcyc}	Figure 6.45
MLCD_SCLK pin output low pulse width	t_{wSCLKL}	1	—	255	t_{Pcyc}	
Data transmit wait time	t_{wNOP}	—	1	—	t_{Pcyc}	
MLCD_SI pin output setup time	t_{sSI}	1	—	255	t_{Pcyc}	
MLCD_SI pin output hold time	t_{hSI}	1	—	255	t_{Pcyc}	
MLCD_DEN pin output setup time	t_{sDEN}	1	—	255	t_{Pcyc}	
MLCD_DEN pin output hold time	t_{hDEN}	1	—	255	t_{Pcyc}	
MLCD_ENBG and MLCD_ENBS pins output high pulse width	t_{wENBH}	2	—	1023	t_{Pcyc}	
Time from MLCD_SCLK pin output rise to MLCD_ENBG and MLCD_ENBS pins output rise	t_{oENB}	3	—	255	t_{Pcyc}	
Time from MLCD_ENBG and MLCD_ENBS pins output fall to MLCD_SCLK pin output rise	t_{bENB}	3	—	255	t_{Pcyc}	
MLCD_VCOM pin output duty ratio	—	—	50	—	%	
MLCD_VCOM pin output high/low pulse time	t_{cVCOM}	500	—	5000	ms	

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKA.

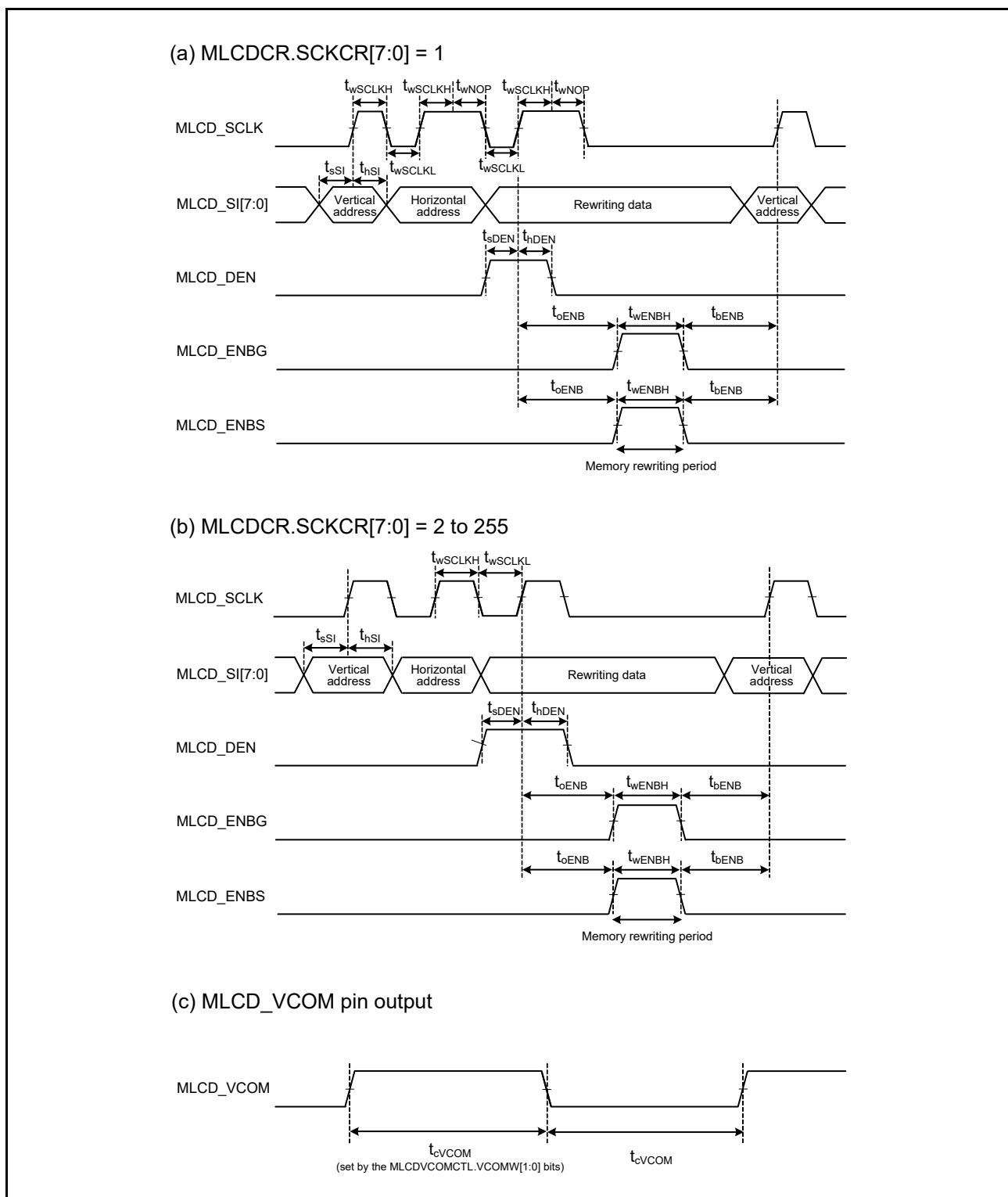


Figure 6.45 MLCD Output Timing

6.3.13 CLKOUT Timing

Table 6.33 CLKOUT Timing

Item			Symbol	Min.	Max.	Unit	Test Conditions
CLKOUT	CLKOUT pin output cycle*1	IOVCCn \geq 2.7 V	t_{Cyc}	31.25	—	ns	Figure 6.46
		IOVCCn < 2.7 V		62.5	—		
CLKOUT32	CLKOUT pin output cycle		t_{Cyc}	30.5	—	μ s	

Note 1. When the CLKOUT output is being derived from the external EXTAL clock input or the sub-clock oscillator and the frequency divisor is 1 (CKOCR.CKOSSEL[2:0] = 011b and CKOCR.CKODIV[2:0] = 000b), the input duty cycle must be in the range from 45 to 55% to satisfy the values above.

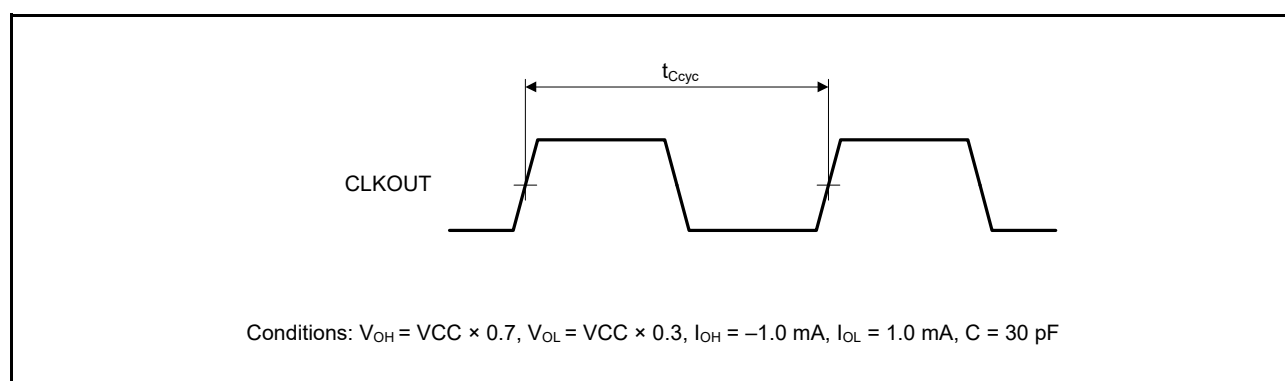


Figure 6.46 CLKOUT Output Timing

6.3.14 TMR Timing

Table 6.34 TMR Timing

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
TMR	Pulse width of the timer clock	Single edge specified	t_{TMCWH} , t_{TMCWL}	1.5	—	—	t_{Pcyc}	Figure 6.47
		Both edges specified		2.5	—	—		

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKB.

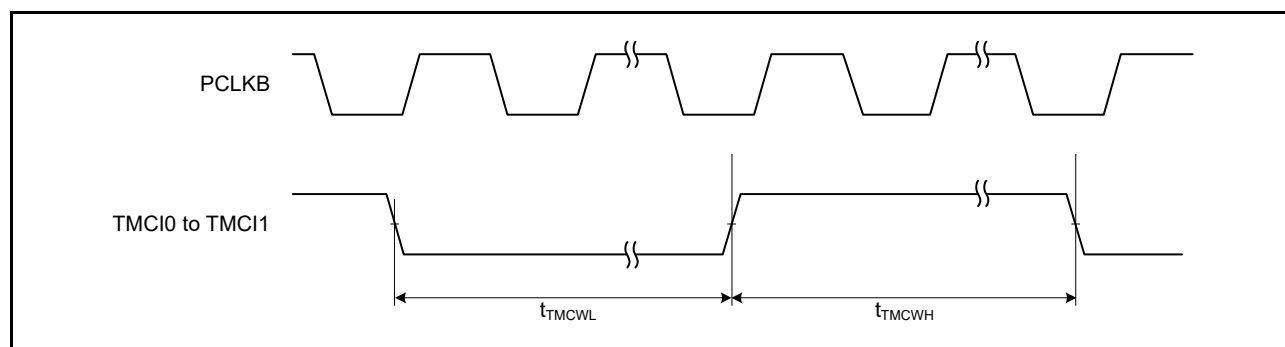


Figure 6.47 TMR Clock Input Timing

6.4 USB Characteristics

6.4.1 USB Timing

Table 6.35 USB Characteristics

Item			Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V	—
	Input low level voltage		V_{IL}	—	0.8	V	—
	Differential input sensitivity		V_{DI}	0.2	—	V	USB_DP – USB_DM
	Differential common mode range		V_{CM}	0.8	2.5	V	—
Output characteristics	Output high level voltage		V_{OH}	2.8	3.6	V	$I_{OH} = -200\ \mu A$
	Output low level voltage		V_{OL}	0.0	0.3	V	$I_{OL} = 2\ mA$
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 6.48 to Figure 6.50
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	
Characteristics of the pull-up and pull-down resistors	Pull-down resistor		R_{PD}	14.25	24.80	k Ω	When the host is selected.
	Pull-up resistor		R_{PUI}	0.9	1.575	k Ω	In the idle state
			R_{PUA}	1.425	3.09	k Ω	During reception

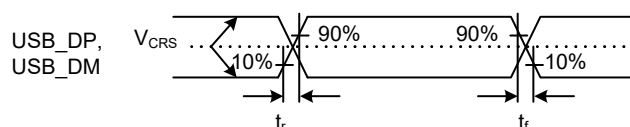


Figure 6.48 USB_DP and USB_DM Output Timing

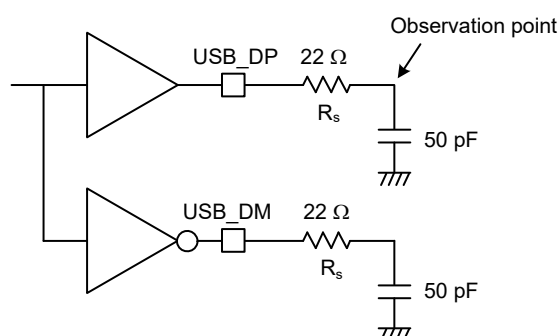


Figure 6.49 Test Circuit for Full-speed (FS) Connection

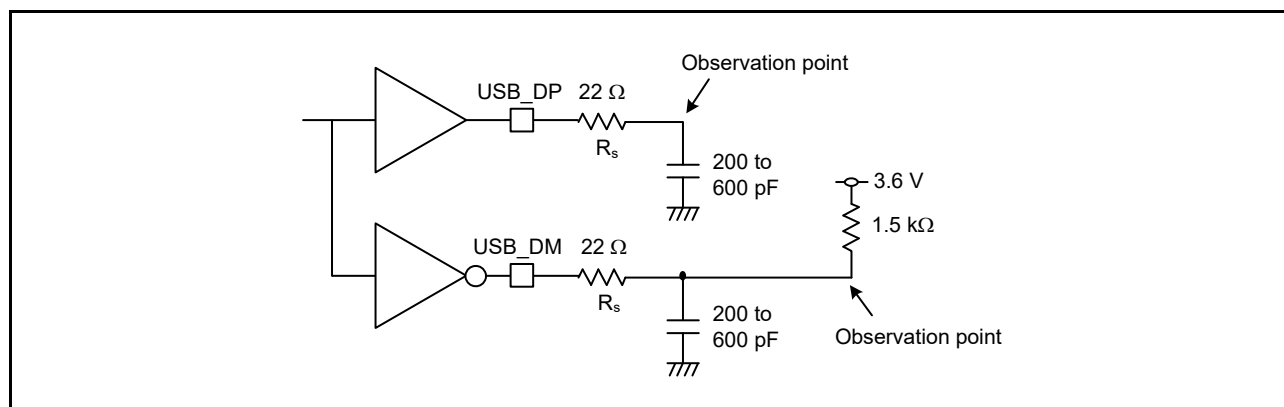


Figure 6.50 Test Circuit for Low-speed (LS) Connection

6.5 A/D Conversion Characteristics

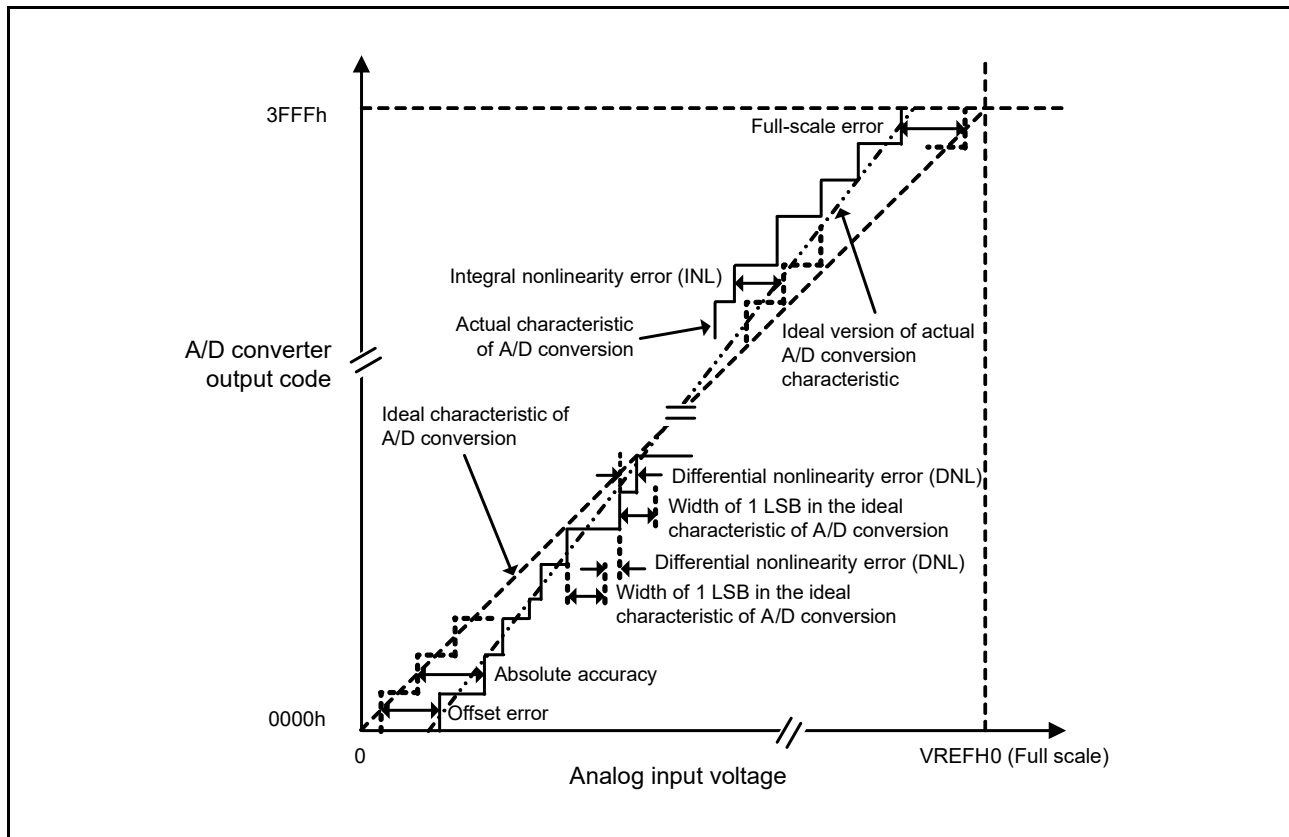


Figure 6.51 Terminology for Characteristics of an A/D Converter

Absolute accuracy

Absolute accuracy is a measure of the difference between the output codes which would be produced by an ideal A/D converter and the codes output by the actual A/D converter. Absolute accuracy is measured by the differences between the codes at the central points (within 1 LSB) of the ranges of analog input voltage for which given digital codes would be expected in ideal A/D conversion. For example, when the resolution is 14 bits and the reference voltage (V_{REFH0}) is 3.276 V, the width of 1 LSB is 0.2 mV, and analog inputs including 0, 0.2, 0.4 mV, and so on, can be used.

An absolute accuracy of ± 5 LSB means that where an ideal A/D converter would output 0008h when the analog input voltage is 1.6 mV, the result from the actual A/D converter can be any value in the range from 0003h to 000Dh.

Integral nonlinearity error (INL)

Integral nonlinearity error is a measure of the maximum deviation between the ideal linear variation in output values with voltage and the actual measured output codes when the measured offset error and full-scale error are 0.

Differential nonlinearity error (DNL)

Differential nonlinearity error is a measure of the difference between the width of 1 LSB in an ideal A/D converter and the actual measured output codes.

Offset error

Offset error is a measure of the difference between the point at which the first ideal output code changes and the first actual measured output code.

Full-scale error

Full-scale error is a measure of the difference between the point at which the ideal output code changes to the last code and the last actual measured code.

We do not inspect the characteristics of the A/D converter before shipment unless otherwise stated. The values presented in this manual are only for reference. The electrical characteristics values that are given are categorized into the following seven groups.

- (1) $AVCC0 = VREFH0 = 2.7$ to 3.6 V

Note that the values in the column “Max.” in Table 6.36 only apply in the case of a normal distribution with $\pm 3\sigma$ variation from the mean.

- (2) $AVCC0 = VREFH0 = 2.7$ to 3.6 V

- (3) $AVCC0 = VREFH0 = 2.4$ to 3.6 V

- (4) $AVCC0 = VREFH0 = 1.8$ to 3.6 V

- (5) $AVCC0 = VREFH0 = 1.62$ to 3.6 V

- (6) $AVCC0 = 3.3$ V, $AVTRO = 2.5$ V (the output of the reference voltage generator is used for reference)

- (7) $AVCC0 = 1.8$ V, $AVTRO = 1.25$ V (the output of the reference voltage generator is used for reference)

Some points to note regarding the electrical characteristics of the A/D converter are listed below.

- (1) The characteristics do not include the quantization error (± 0.5 LSB).

- (2) The characteristics are the values after offset calibration.

- (3) The characteristics only apply when the 14-bit A/D converter pins are in use for A/D conversion, and not for any other functions.

- (4) The conversion time (t_{CONV}) is the sum of the sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}).

The values in parentheses in the conversion time indicate the sampling time.

Table 6.36 A/D Conversion Characteristics (1)

Conditions: $AVCC0 = VREFH0 = 2.7$ to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	1.0 (0.46875)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		1.5 (0.96875)	—	—	μs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		−1.2	—	1.2	mV	High-precision channel
Full-scale error*1		−1.2	—	1.2	mV	High-precision channel
Absolute accuracy*1		—	±4.0*2	±11	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.5	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5	±4.0	LSB	High-precision channel
ENOB (effective number of bits) error*1, *2		—	13	—	Bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).

Note 2. The value applies when $AVCC0 = VREFH0 = 3.3$ V.

Note 3. If $AVCC0 \neq VREFH0$, the condition $AVCC0 \geq VREFH0 \geq 2.7$ V applies.

Table 6.37 A/D Conversion Characteristics (2)

Conditions: $AVCC0 = VREFH0 = 2.7$ to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32*3	MHz	ADCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	1.0 (0.46875)	—	—	μs	High-precision channel ADCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		1.5 (0.96875)	—	—	μs	Standard-precision channel ADCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	μs	ADCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		−1.7	—	1.7	LSB	High-precision channel
Full-scale error*1		−1.7	—	1.7	LSB	High-precision channel
Absolute accuracy*1		—	±4.0*2	±14	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.7	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5	±5.0	LSB	High-precision channel
ENOB (effective number of bits) error*1, *2		—	13	—	Bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).

Note 2. The value applies when $AVCC0 = VREFH0 = 3.3$ V.

Note 3. If $AVCC0 \neq VREFH0$, the condition $AVCC0 \geq VREFH0 \geq 2.7$ V applies.

Table 6.38 A/D Conversion Characteristics (3)

Conditions: $AVCC0 = VREFH0 = 2.4$ to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16*3	MHz	ADCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.9375)	—	—	μs	High-precision channel ADCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		3.0 (1.9375)	—	—	μs	Standard-precision channel ADCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	μs	ADCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		−1.7	—	1.7	mV	High-precision channel
Full-scale error*1		−1.7	—	1.7	mV	High-precision channel
Absolute accuracy*1		—	±4.0*2	±14	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.7	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5	±5.0	LSB	High-precision channel
ENOB (effective number of bits) error*1, *2		—	13	—	Bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).

Note 2. The value applies when $AVCC0 = VREFH0 = 3.3$ V.

Note 3. If $AVCC0 \neq VREFH0$, the condition $AVCC0 \geq VREFH0 \geq 2.4$ V applies.

Table 6.39 A/D Conversion Characteristics (4)

Conditions: AVCC0 = VREFH0 = 1.8 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8*2	MHz	ADSCCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	3.75 (1.875)	—	—	μs	High-precision channel ADSCCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		5.75 (3.875)	—	—	μs	Standard-precision channel ADSCCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		531.25 (60.98)	—	—	μs	ADSCCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		−1.7	—	1.7	mV	High-precision channel
Full-scale error*1		−1.7	—	1.7	mV	High-precision channel
Absolute accuracy*1		—	±2.0	±7.0	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0	±2.0	LSB	High-precision channel
INL integral nonlinearity error*1		—	±1.0	±3.0	LSB	High-precision channel

Note 1. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 00h).

Note 2. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 1.8 V applies.

Table 6.40 A/D Conversion Characteristics (5)

Conditions: AVCC0 = VREFH0 = 1.62 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8*3	MHz	ADSCCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution*1		—	—	10	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	3.75 (1.875)	—	—	μs	High-precision channel ADSCCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		5.75 (3.875)	—	—	μs	Standard-precision channel ADSCCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		531.25 (60.98)	—	—	μs	ADSCCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*2		−1.7	—	1.7	mV	High-precision channel
Full-scale error*2		−1.7	—	1.7	mV	High-precision channel
Absolute accuracy*2		—	±0.5	±2.5	LSB	High-precision channel
DNL differential nonlinearity error*2		—	±0.5	±1.5	LSB	High-precision channel
INL integral nonlinearity error*2		—	±0.5	±1.5	LSB	High-precision channel

Note 1. Due to selection of the 12-bit resolution, ignore the two lower-order bits of the 14-bit result of A/D conversion (in the ADDRy registers).

Note 2. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 00h).

Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 1.62 V applies.

Table 6.41 Characteristics of A/D Conversion when the Output Value from the Reference Voltage Generation Circuit is in Use as the Reference Voltage (1)

Conditions: AVCC0 = 3.3 V, AVTRO = 2.50 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.9375)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		3.0 (1.9375)	—	—	μs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		−1.7	—	1.7	mV	High-precision channel
DNL differential nonlinearity error*1		—	±1.5	—	LSB	High-precision channel
INL integral nonlinearity error*1		—	±3.0	—	LSB	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).

Table 6.42 Characteristics of A/D Conversion when the Output Value from the Reference Voltage Generation Circuit is in Use as the Reference Voltage (2)

Conditions: AVCC0 = 1.8 V, AVTRO = 1.25 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	ADCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADCLKCR.SCLKEN = 1
Dynamic range	A _{in}	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	3.75 (1.875)	—	—	μs	High-precision channel ADCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		5.75 (3.875)	—	—	μs	Standard-precision channel ADCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		531.25 (60.98)	—	—	μs	ADCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		−1.7	—	1.7	mV	High-precision channel
DNL differential nonlinearity error*1		—	±1.0	—	LSB	High-precision channel
INL integral nonlinearity error*1		—	±1.0	—	LSB	High-precision channel

Note 1. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 00h).

6.6 Analog Comparator Characteristics

Table 6.43 Analog Comparator Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Conversion time	T_{conv}	—	0.5	2	μs	
Comparison precision	Acc	−100	—	100	mV	
Stabilization wait time	T_{start}	—	1.2	7	μs	

Note: We do not inspect the characteristics of the analog comparator before shipment. The values presented in this manual are only for reference.

6.7 D/A Conversion Characteristics

Table 6.44 D/A Conversion Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	12	12	12	Bit	—
Output without buffer	Differential nonlinearity error	DNL	—	±1.0	LSB	—
	Integral nonlinearity error	INL	—	±4.0	LSB	—
	Output resistance	R_O	—	94	k Ω	—
	Conversion time	t_s	—	50	μs	External capacitance: 20 pF
Buffer output	Load resistance	R_L	5	—	k Ω	—
	Load capacitance	C_L	—	40	pF	—
	Output voltage range	V_O	0.18	$AVCC1 - 0.18$	V	$AVCC1 \geq 2.7 V$
	Differential nonlinearity error	DNL	—	±1.0	LSB	$AVCC1 \geq 2.7 V$
	Integral nonlinearity error	INL	—	±2.0	LSB	$AVCC1 \geq 2.7 V$
	Offset error	—	—	±20	mV	$AVCC1 \geq 2.7 V$
	Full-scale error	—	—	±20	mV	$AVCC1 \geq 2.7 V$
	Conversion time	t_s	—	50	μs	$AVCC1 \geq 2.0 V$

Note: We do not inspect the characteristics of the analog D/A converter before shipment. The values presented in this manual are only for reference.

6.8 Temperature Sensor Characteristics

Table 6.45 Temperature Sensor Characteristics

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±5	—	°C	$AVCC0 \geq 2.6 V$
	—	±6	—	°C	$AVCC0 < 2.6 V$
Temperature gradient	—	1.6	—	mV/°C	—
Temperature sensor activation time	—	30	120	μs	—
Sampling time	—	2	7	μs	—

Note: We do not inspect the characteristics of the temperature sensor before shipment. The values presented in this manual are only for reference.

6.9 VREF Characteristics

Table 6.46 VREF Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage	AVTRO	1.17	1.25	1.33	V	AVCC0 \geq 2.8 V VREF.AVCR.AVSEL = 0
	AVTRO	2.34	2.50	2.66	V	AVCC0 \geq 2.8 V VREF.AVCR.AVSEL = 1
	AVTRO	1.17	1.25	1.33	V	AVCC0 < 2.8 V VREF.AVCR.AVSEL = 0
Waiting time till the circuit activates and operation is stable	t_{VRSTUP}	—	—	50	ms	—

Note: We do not inspect the VREF characteristics before shipment. The values presented in this manual are only for reference.

6.10 LED Characteristics

Table 6.47 LED Characteristics

Conditions: $T_a = -20$ to $+65^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LED constant current*1	I_{led}	0.95	1.00	1.05	mA	LED load = 1.4 k Ω LED.LECO.LESn = 1 (n = 1, 2, 3)
		0.48	0.50	0.53		LED load = 2.8 k Ω LED.LECO.LESn = 0 (n = 1, 2, 3)
Rise time*2	T_{set}	—	—	150	μs	—

Note: A voltage supplied to an external LED to be used must be equivalent to IOVCC3.

Note 1. Input current value for one LEDIn pin (n = 1, 2, 3). Plural pins must not be simultaneously enabled. Set the LECO.LEOn bit of the LED to enable or disable the desired pin.

Note 2. Time required for the LED current to reach the target value after the LEPSR.LEPS bit is set to 1 (constant current circuit on). We do not inspect this characteristic before shipment. This value is only for reference.

6.11 Oscillation Stop Detection Circuit Characteristics

Table 6.48 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	30	μs	Figure 6.52

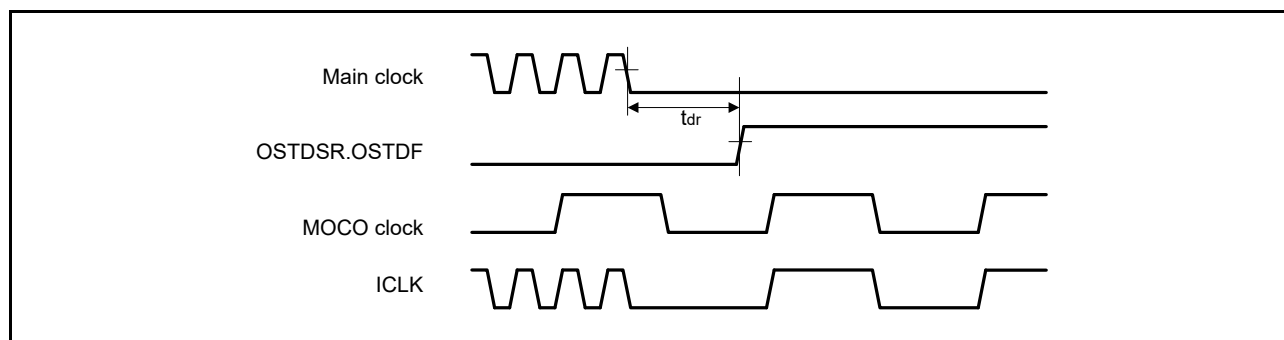


Figure 6.52 Oscillation Stop Detection Timing

6.12 Characteristics of Power-on Reset Circuit and Low Voltage Detection Circuit

Table 6.49 Characteristics of Power-on Reset Circuit and Low Voltage Detection Circuit

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset circuit (POR)	Rising	V _{POR}	1.40	1.50	1.60	V	Figure 6.53
		Falling	V _{PORL}	1.30	1.40	1.50		
	Voltage monitoring 0 circuit (LVD0)		V _{det0_0}	2.34	2.42	2.50	V	Figure 6.54
			V _{det0_1}	2.10	2.17	2.24		
			V _{det0_2}	1.86	1.92	1.98		
			V _{det0_3}	1.62	1.67	1.72		
	Voltage monitoring 1 circuit (LVD1)		V _{det1_0}	2.74	2.83	2.92	V	Figure 6.55
			V _{det1_1}	2.58	2.66	2.74		
			V _{det1_3}	2.42	2.50	2.58		
			V _{det1_5}	2.26	2.33	2.40		
			V _{det1_7}	2.10	2.17	2.24		
			V _{det1_9}	1.94	2.00	2.06		
			V _{det1_B}	1.78	1.84	1.90		
			V _{det1_D}	1.62	1.67	1.72		
	Voltage monitoring BAT circuit (LVDBAT)		V _{detBAT_5}	2.26	2.33	2.40	V	Figure 6.56
			V _{detBAT_7}	2.10	2.17	2.24		
			V _{detBAT_9}	1.94	2.00	2.06		
			V _{detBAT_B}	1.78	1.84	1.90		
			V _{detBAT_D}	1.62	1.67	1.72		
Internal reset time	LVD0 reset time		t _{LVD0}	—	3.10	—	ms	Figure 6.54
	LVD1 reset time		t _{LVD1}	—	1.38	—	ms	Figure 6.55
	LVDBAT reset time		t _{LVDBAT}	—	1.38	—	ms	Figure 6.56
Minimum VCC down time*1			t _{VOFF}	4	—	—	ms	Figure 6.53 to Figure 6.56
LVD0 response delay time			t _{det}	—	150	300	μs	Figure 6.54 to Figure 6.56
LVD1 response delay time			t _{det}	—	150	300	μs	
LVDBAT response delay time (when the VCC and VBAT_EHC pins are connected)			t _{det}	—	150	300	μs	
LVDBAT response delay time (when the VCC and VBAT_EHC pins are not connected)			t _{det}	—	400	800	μs	
LVD1 operation stabilization time (after the LVD circuit is enabled)			t _{d(E-A)}	—	—	600	μs	Figure 6.55, Figure 6.56
LVDBAT operation stabilization time (when the VCC and VBAT_EHC pins are connected)			t _{d(E-A)}	—	—	600	μs	
LVDBAT operation stabilization time (when the VCC and VBAT_EHC pins are not connected)			t _{d(E-A)}	—	—	1000	μs	
Hysteresis width (LVD1)			V _{LVH} *2	—	60	—	mV	
Hysteresis width (LVD1)			V _{LVH} *3	—	55	—	mV	
Hysteresis width (LVD1)			V _{LVH} *4	—	50	—	mV	
Hysteresis width (LVD1)			V _{LVH} *5	—	45	—	mV	
Hysteresis width (LVD1)			V _{LVH} *6	—	40	—	mV	
Hysteresis width (LVD1)			V _{LVH} *7	—	35	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the lowest value among voltage detection levels V_{POR} , V_{det1} , and V_{detBAT} for the power-on reset circuit and low-voltage detection circuit.

Note 2. When V_{det0_0} is selected.

Note 3. When V_{det0_1} and V_{det0_3} are selected.

Note 4. When V_{det1_5} is selected.

Note 5. When V_{det1_7} is selected.

Note 6. When V_{det1_9} and V_{det1_B} are selected.

Note 7. When V_{det1_D} is selected.

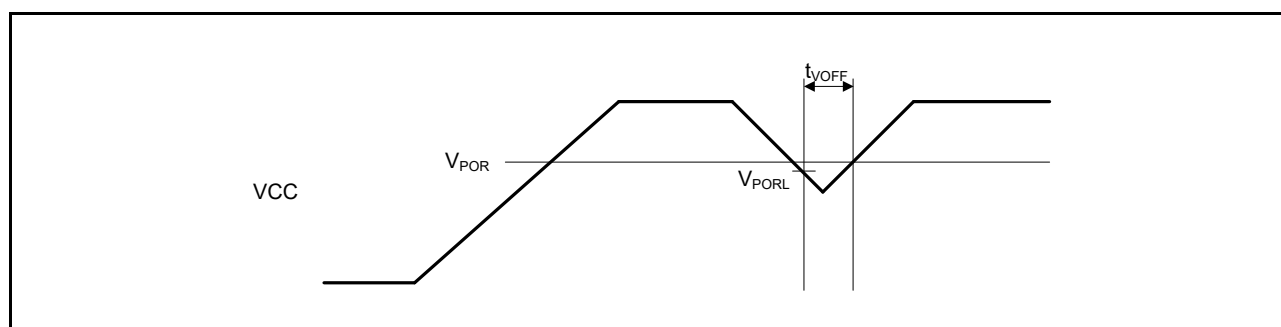
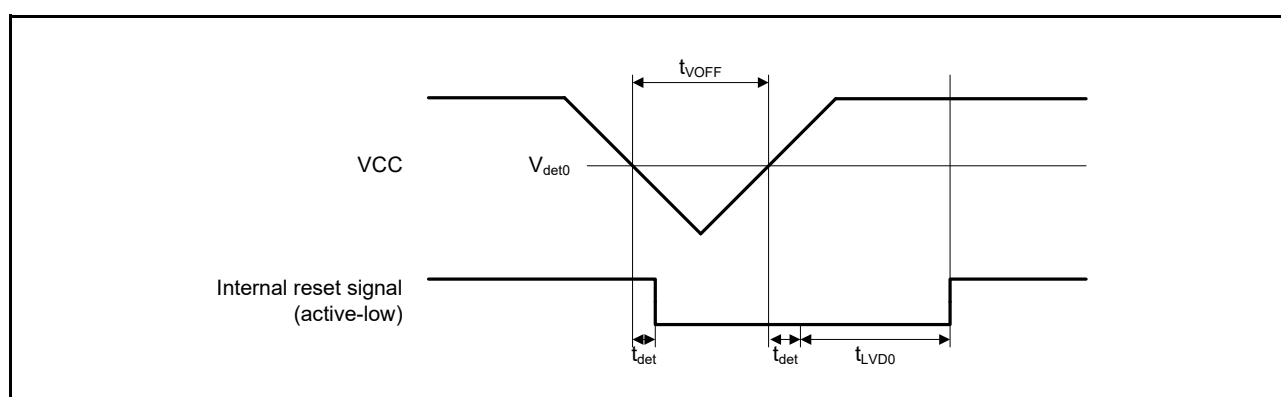
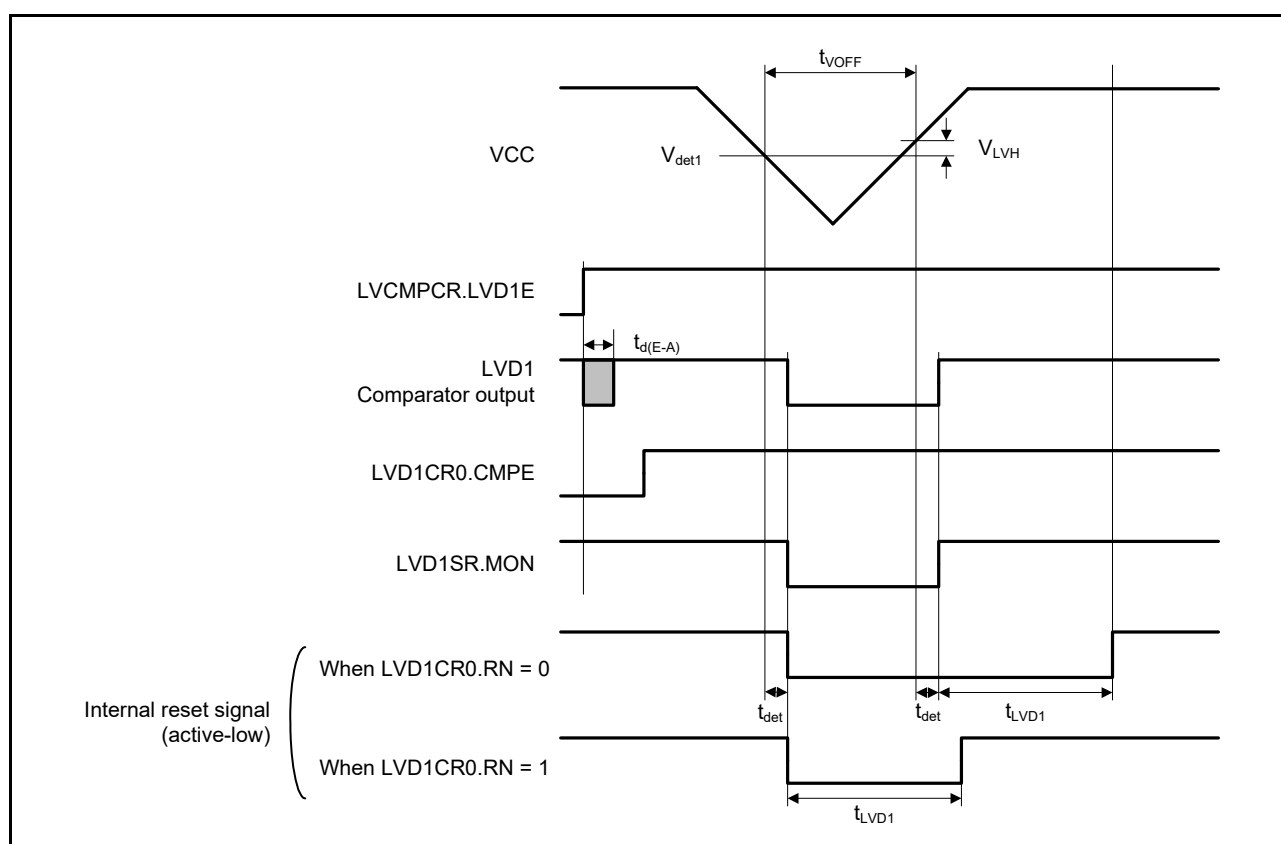
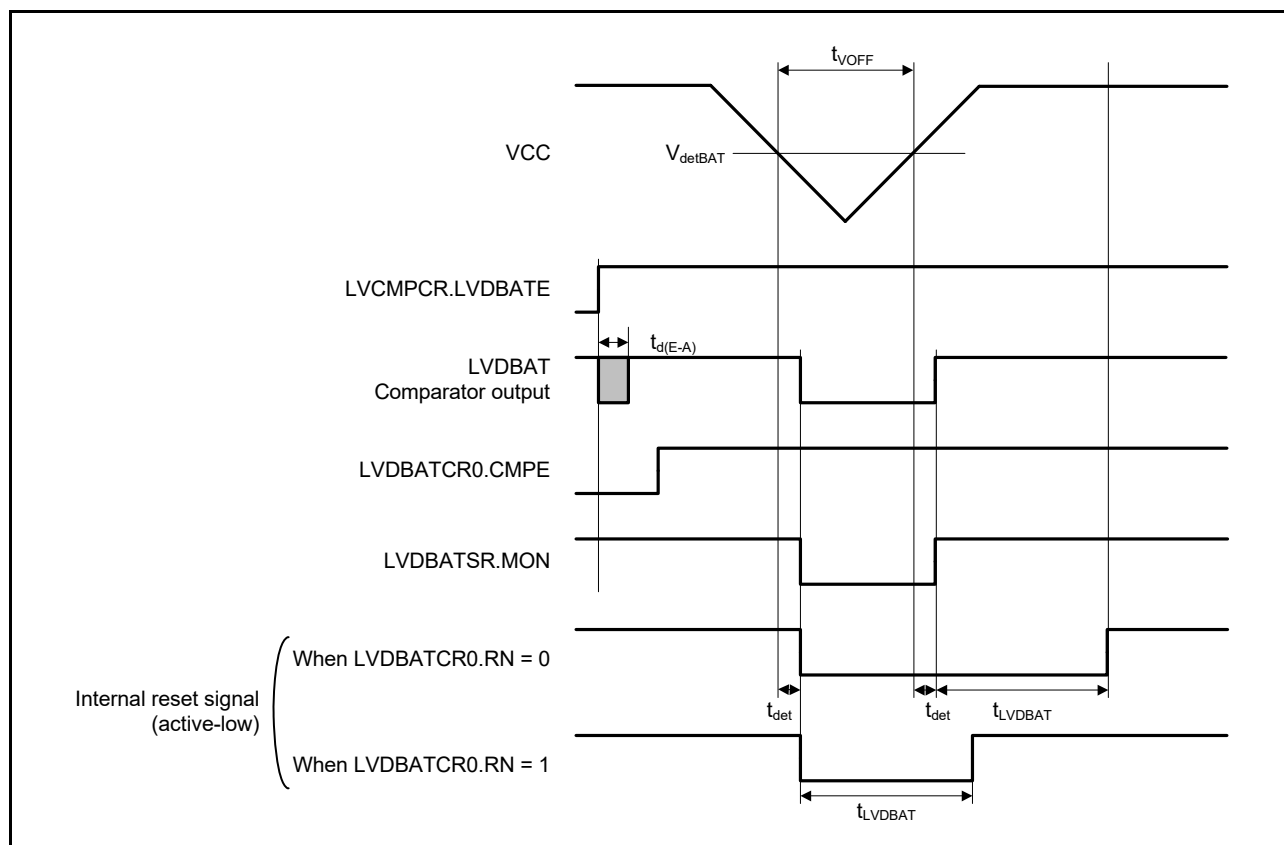


Figure 6.53 Power-on Reset Timing

Figure 6.54 Timing of Voltage Detection by Voltage Monitoring Circuit 0 (V_{det0})Figure 6.55 Timing of Voltage Detection by Voltage Monitoring Circuit 1 (V_{det1})

Figure 6.56 Timing of Voltage Detection by Voltage Monitoring BAT Circuit (V_{detBAT})

6.13 EHC Characteristics

Table 6.50 EHC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current during reset	I_{CCEHC}	—	0.02	—	μA	$V_{CC} = V_{SC_VCC} = 0\text{ V}$, $V_{CC_SU} = V_{BAT_EHC} = 2.5\text{ V}$ $T_a = 25^\circ\text{C}$
Capacitance of the storage capacitor connected to $V_{CC_SU}^{*1, *3}$	C_{VCCSU}	—	100	—	μF	EHMD = 1 $T_a = -40\text{ to }60^\circ\text{C}$
		—	47	—		EHMD = 0 $T_a = -40\text{ to }50^\circ\text{C}$
		—	150	—		EHMD = 1 $T_a = -40\text{ to }85^\circ\text{C}$
Capacitance of the smoothing capacitor connected to V_{CC}^{*1}	C_{VCC}	—	10	—		$T_a = -40\text{ to }85^\circ\text{C}$
Current that can flow from V_{SC_VCC} into LSI chip (when the secondary battery of 2.6 V is used)	I_{SC}	—	—	10	mA	$V_{SC_VCC} \leq 3.6\text{ V}$
Current that can flow from V_{SC_VCC} into LSI chip (when the secondary battery of 3.0 V is used)		—	—	6	mA	$V_{SC_VCC} \leq 3.6\text{ V}$
Current that can flow from V_{BAT_EHC} to $IOVCCn^{*2}$	I_{VBAT}	—	—	30	mA	—
Current that can flow from $V_{CC}/IOVCC$ to $IOVCCn^{*2}$	I_{VCC}	—	—	30	mA	—
Permissible value of output impedance on the V_{BAT_EHC} side	R_{VBAT}	—	—	10	Ω	$V_{SC_VCC} \leq 3.6\text{ V}$
V_{BAT} threshold voltage for secondary battery overcharging protection (when a 2.6-V secondary battery is in use)	V_{BAT_CHG}	2.535	2.585	2.635	V	$I_{SC} = 3\text{ }\mu\text{A to }10\text{ mA}$, $V_{SC_VCC} = V_{BAT_EHC}$
V_{BAT} threshold voltage for secondary battery overcharging protection (when a 3.0-V secondary battery is in use)	V_{BAT_CHG}	2.925	2.975	3.025	V	$I_{SC} = 3\text{ }\mu\text{A to }6\text{ mA}$, $V_{SC_VCC} = V_{BAT_EHC}$
V_{CC} threshold voltage for secondary battery overcharging protection	V_{CC_CHG}	2.925	2.975	3.025	V	$I_{SC} = 3\text{ }\mu\text{A to }10\text{ mA}$, $V_{SC_VCC} = V_{CC}$
High threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 2.6-V secondary voltage is in use)	$V_{CC_SU_H}$	—	2.62	—	V	Value at V_{CC} rise when $V_{SC_VCC} = V_{CC}$
Low threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 2.6-V secondary voltage is in use)	$V_{CC_SU_L}$	—	2.32	—	V	Value at V_{CC} fall when $V_{SC_VCC} = V_{CC}$
High threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 3.0-V secondary voltage is in use)	$V_{CC_SU_H}$	—	2.83	—	V	Value at V_{CC} rise when $V_{SC_VCC} = V_{CC}$
Low threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 3.0-V secondary voltage is in use)	$V_{CC_SU_L}$	—	2.51	—	V	Value at V_{CC} fall when $V_{SC_VCC} = V_{CC}$
Threshold voltage in activation of the LSI chip in the energy harvesting mode	$V_{CC_SU_H}$	—	2.62	—	V	$I_{SC} = 3\text{ }\mu\text{A to }10\text{ mA}$
Threshold voltage for the power generating element status flag	V_{ENOUT}	—	0.5	—	V	$V_{CC_SU} = 2.5\text{ V}$
Minimum activating current required in energy harvesting startup mode	I_{SC}	—	3	—	μA	$T_a = 25^\circ\text{C}$, V_{CC_SU} and V_{CC} are connected to 100- μF and 10- μF capacitors, respectively.

Note 1. See Figure 13.1 in the User's Manual: Hardware.

Note 2. $IOVCCn$ refers to $IOVCC0$, $IOVCC1$, $IOVCC2$, and $IOVCC3$.

Note 3. Figure 6.58 shows the relation between the upper limit on temperature and the capacitance of the storage capacitor connected to V_{CC_SU} . When the capacitance becomes insufficient for the temperature at which the capacitor is to be used, an activation current is required shown in Figure 6.59.

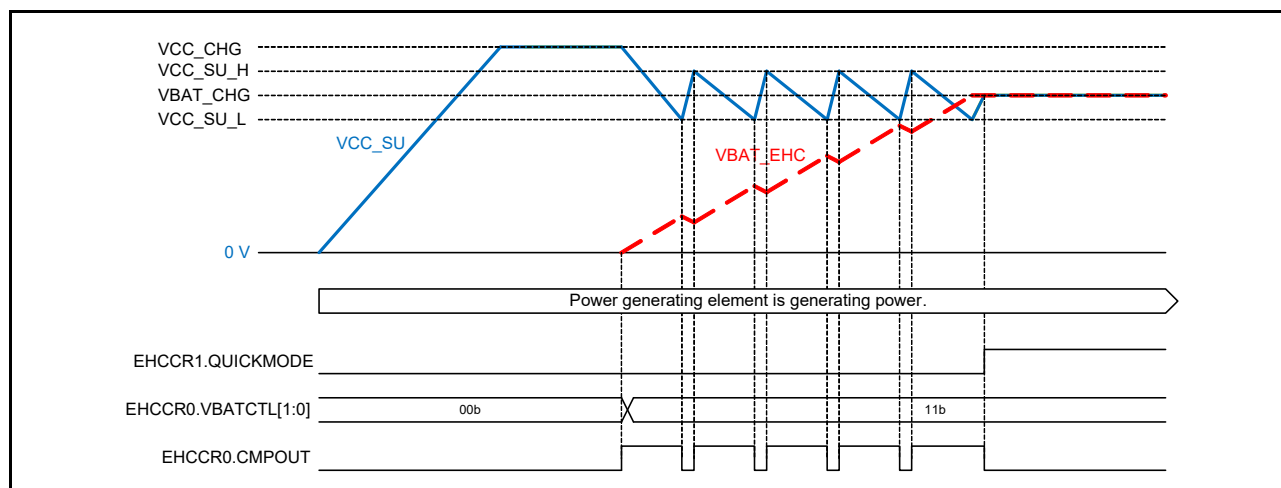


Figure 6.57 Charging Operations for the VBAT_EHC Pin in High-speed Activation of the LSI chip by Using EHC Capacitor Charging

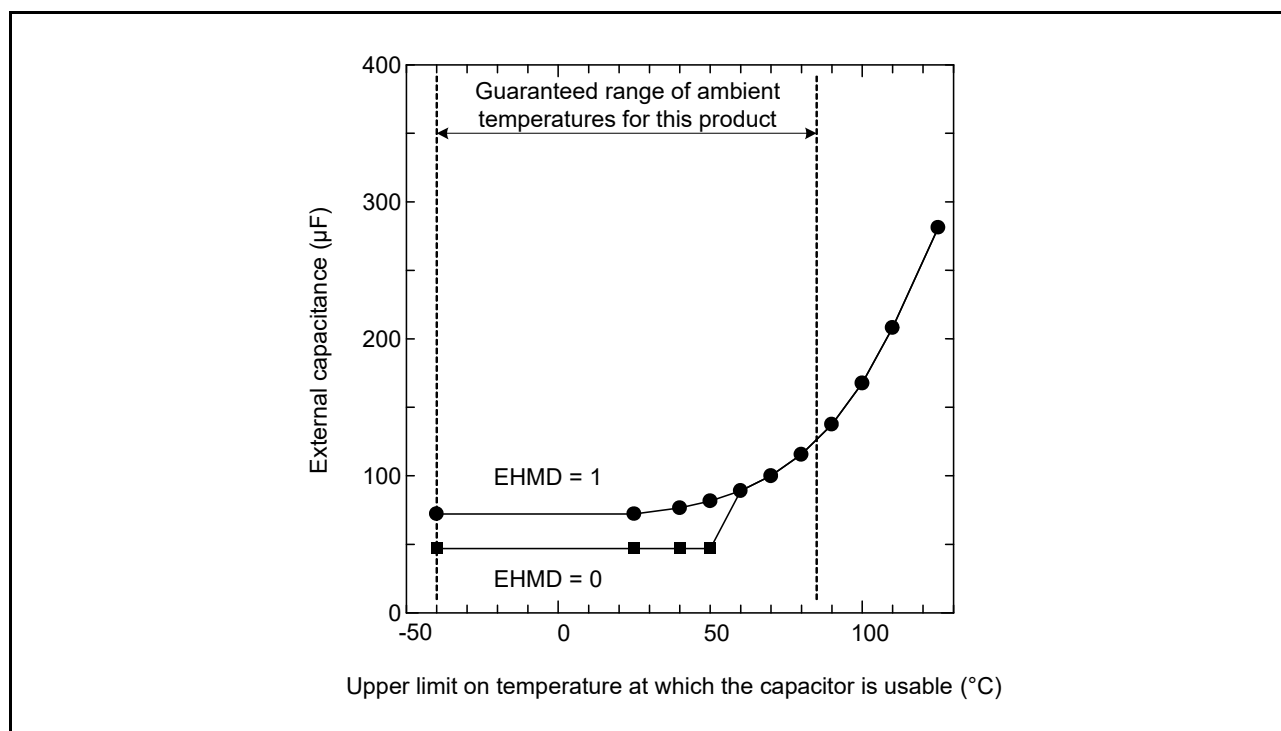


Figure 6.58 Relation between the Upper Limit on Temperature and Capacitance of the Storage Capacitor Connected to VCC_SU

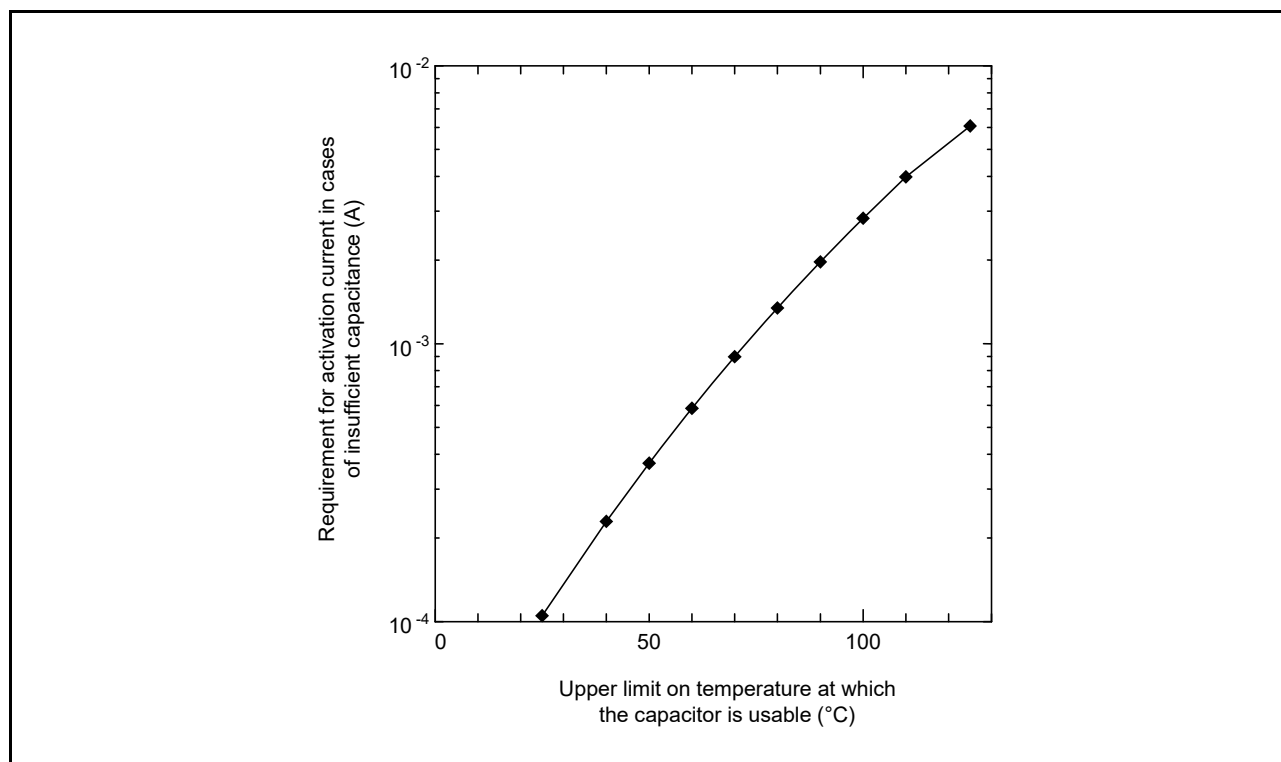


Figure 6.59 Relation between the Upper Limit of a Temperature and an Activation Current in the Case where Capacitance is Insufficient

6.14 Back Bias Voltage Control (VBBC) Circuit Characteristics

Table 6.51 VBBC Initial Setup Time

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VBBC initial setup time*1	t_{VBBSUP}	—	300*2	600*2, *3	ms	Figure 6.60
Internal voltage discharge time	t_{VBBDIS}	1	—	—	ms	Figure 6.61

Note 1. This is the time period between when 1 is written to VBBCR.VBBEN and when VBBST.VBBSTUP is changed to 1.

Note 2. This is the time when the value of the smoothing capacitor connected between the VBP and VBN pins is $1.0\text{ F} \pm 20\%$.

Note 3. We do not inspect the characteristics of the back-bias voltage control circuit before shipment. The values presented in this manual are only for reference.

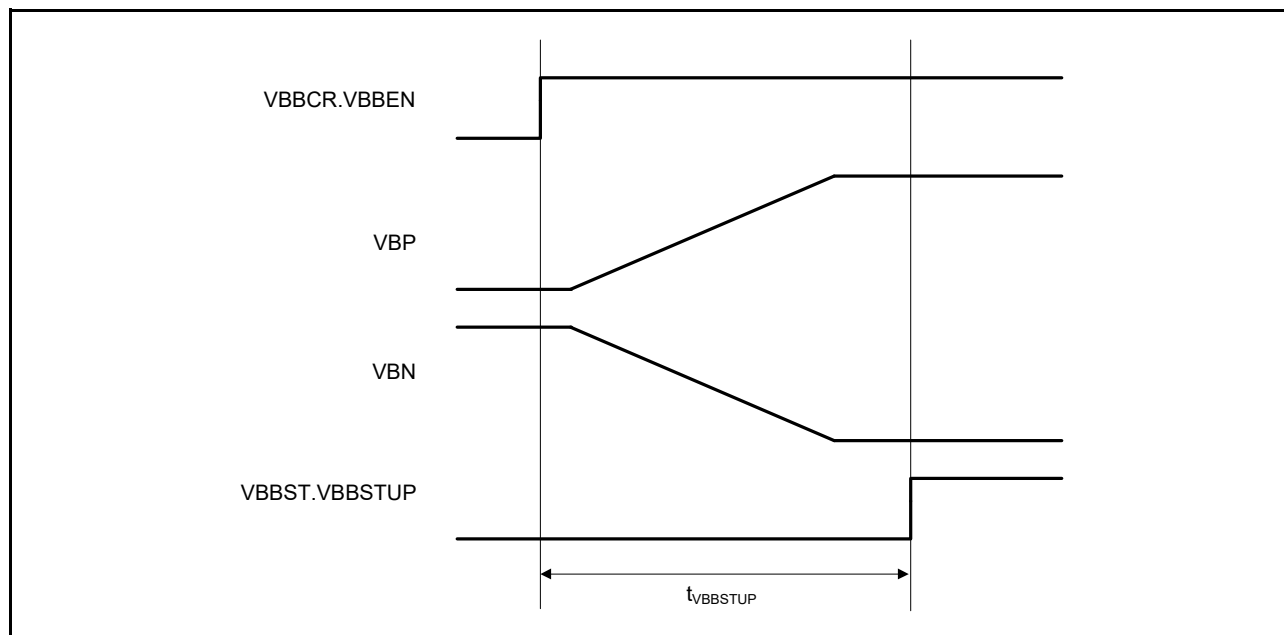


Figure 6.60 VBBC Initial Setup Timing

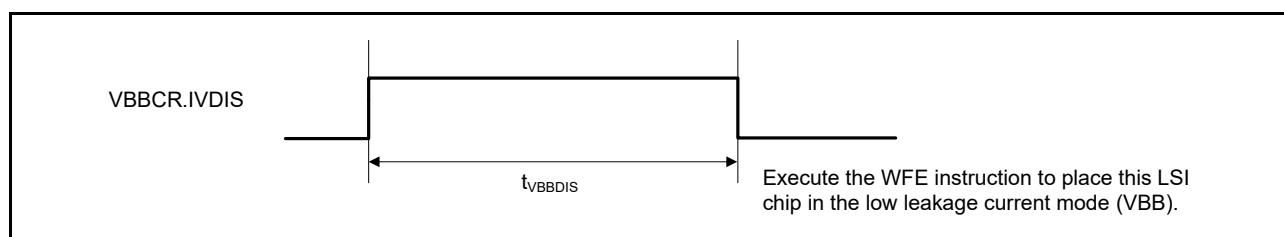


Figure 6.61 Internal Voltage Discharge Time

6.15 MTDV Characteristics

Table 6.52 Characteristics of Rotation Detection

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Threshold voltage 1 (rotation detection)	V_{THP1}	1.0	—	1.3	V	$T_a = -40$ to $+85^{\circ}\text{C}$ $\text{IOVCC1} = 1.65$ to 3.6 V
Threshold voltage 2 (magnetic field detection)	V_{THP2}	$0.42 \times \text{IOVCC1}$	—	$0.54 \times \text{IOVCC1}$	V	$T_a = -10$ to $+60^{\circ}\text{C}$ $\text{IOVCC1} = 1.8$ to 3.4 V

Table 6.53 Delay Characteristics of the Driving Waveform

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input signal delay time 1	t_{DELAY1}	6.00	7.60	9.20	μs	$T_a = -10$ to $+60^{\circ}\text{C}$

Note: The values indicate the delay time for a single delay cell circuit. The number of delay cell circuits actually in use can be checked by reading the PM1STA.PM1BIT[3:0] bits.

Table 6.54 VPM Characteristics (1/2)
 Conditions: $T_a = -20$ to $+60^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage 1	VPM	1.57	—	1.63	V	IOVCC1 = 1.65 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 000b (with 1.6 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
		1.87	—	1.93	V	IOVCC1 = 1.95 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 001b (with 1.9 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
		1.97	—	2.03	V	IOVCC1 = 2.05 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 010b (with 2.0 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
		2.07	—	2.13	V	IOVCC1 = 2.15 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 011b (with 2.1 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
		2.17	—	2.23	V	IOVCC1 = 2.25 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 100b (with 2.2 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
		2.27	—	2.33	V	IOVCC1 = 2.35 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 101b (with 2.3 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
		2.37	—	2.43	V	IOVCC1 = 2.45 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 110b (with 2.4 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)
Output voltage 1	VPM	2.47	—	2.53	V	IOVCC1 = 2.55 to 3.6 V VPM – VSS = 2 mA VPMCON.VPMAS[2:0] = 111b (with 2.5 V selected as the VPM pin output voltage) VPMCON.VPMENA = 1 (Forced voltage output from the VPM pin) VPMCON.VSYSSEL = 0 (VPM power supply drive)

Table 6.54 VPM Characteristics (2/2)

Conditions: $T_a = -20$ to $+60^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Temperature characteristics 1	Δ_{TVPM1}	-0.25	—	+0.75	mV/ $^\circ\text{C}$	IOVCC1 = 1.65 to 3.6 V VPMCON.VPMAS[2:0] = 000b (1.6 V is selected for the VPM pin output voltage.)
Temperature characteristics 2	Δ_{TVPM2}	-0.5	—	+1.0	mV/ $^\circ\text{C}$	IOVCC1 = (value set by the VPM pin output voltage select bit + 0.05 V) to 3.6 V

6.16 Flash Memory Characteristics

6.16.1 Code Flash Memory Characteristics

Table 6.55 Code Flash Memory Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Cycles of reprogramming and erasure*1		N _{PEC}	10000	—	—	Times	Tested in accord with the conditions defined by JEDEC
Data retention time		t _{DRP}	10	—	—	Year	

Note 1. The number of cycles of reprogramming and erasure defines the number of times a block can be erased. When the number of cycles of reprogramming and erasure is n, a block can be erased n times. For instance, if 8 bytes of data are written to the 256 different addresses on 8-byte boundaries within a 2-Kbyte block, erasing the whole block is counted as a single cycle of reprogramming and erasure. Note that programming of the same address is only allowed once; that is, overwriting is prohibited.

Table 6.56 Code Flash Memory Characteristics (2)

Item		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8 bytes	t _{P8}	—	5.0	6.0	—	5.0	6.0	ms
	256 bytes	t _{P256}	—	5.0	6.0	—	5.0	6.0	ms
Erase time	4 Kbytes	t _{E4K}	—	10.0	12.0	—	10.0	12.0	ms
Delay until first suspension during programming		t _{SPD1}	—	—	0.2	—	—	0.1	ms
Delay after second suspension during programming		t _{SPD2}	—	—	2.4	—	—	2.0	ms
Delay until first suspension during erasure		t _{SED1}	—	—	0.2	—	—	0.1	ms
Delay after second suspension during erasure		t _{SED2}	—	—	2.4	—	—	2.0	ms
Forced stop command		t _{FD}	—	—	0.2	—	—	0.1	ms

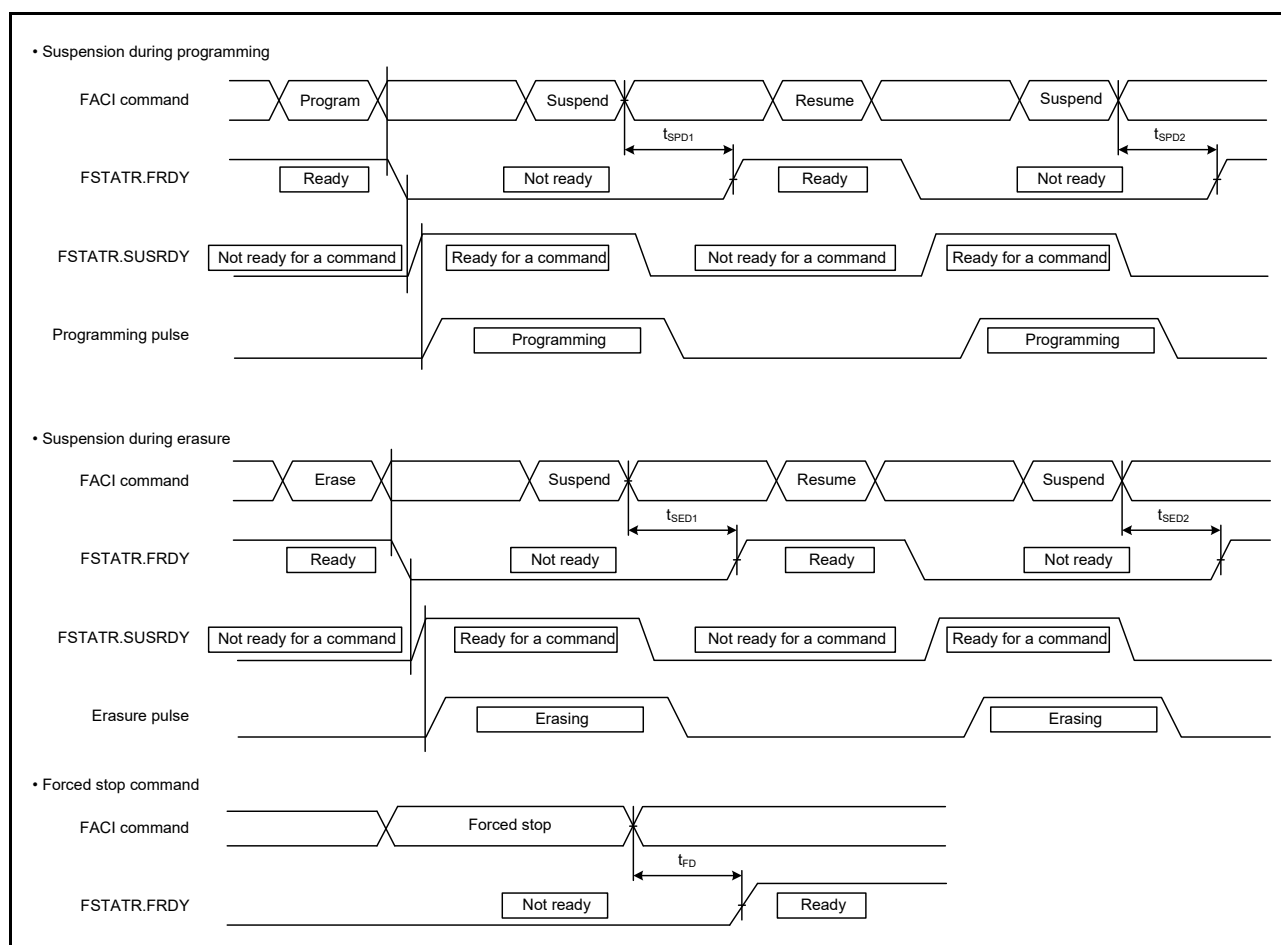


Figure 6.62 Timing of Suspension during Programming and Erasure and Timing of Forced Stop of the Flash Memory

6.17 Boundary Scan Characteristics

Table 6.57 Boundary Scan Characteristics

Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 6.63
TCK clock high pulse width	t_{TCKH}	43	—	—	ns	
TCK clock low pulse width	t_{TCKL}	43	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	7	ns	
TCK clock fall time	t_{TCKf}	—	—	7	ns	
TMS setup time	t_{TMSS}	15	—	—	ns	Figure 6.64
TMS hold time	t_{TMSh}	15	—	—	ns	
TDI setup time	t_{TDis}	15	—	—	ns	
TDI hold time	t_{TDIH}	15	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	100	ns	

Note: The values above apply when the LSI chip is in the normal (high-speed) mode.

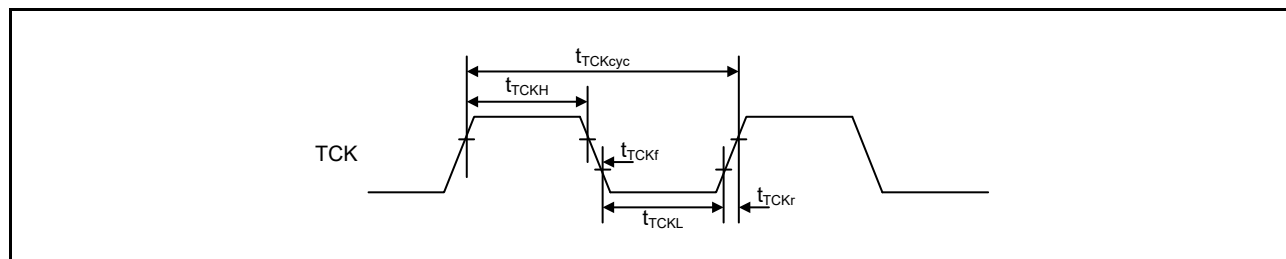


Figure 6.63 Boundary Scan TCK Timing

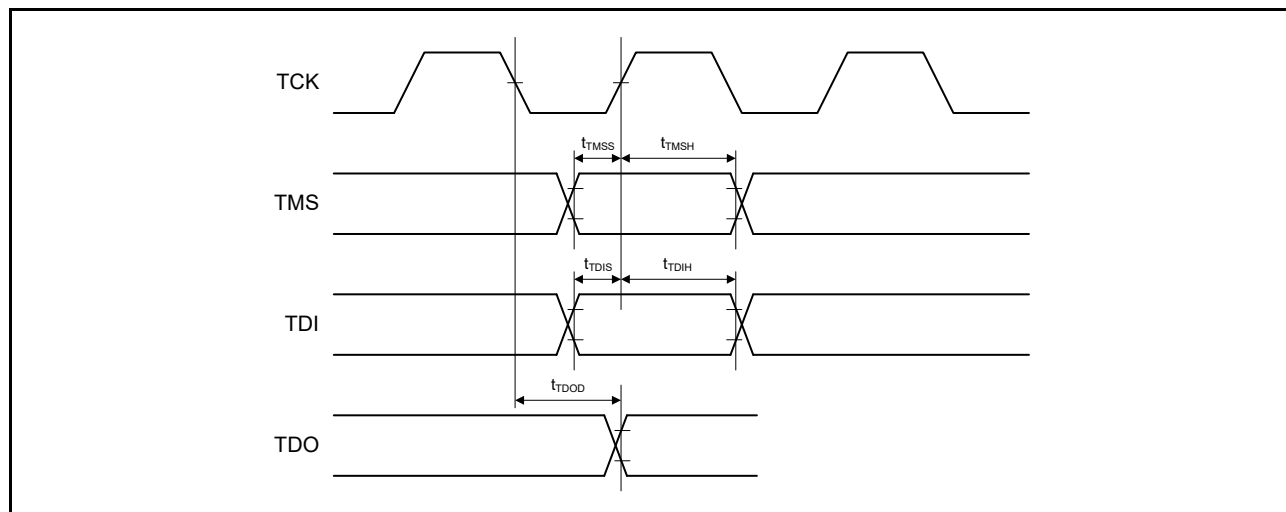


Figure 6.64 Boundary Scan Input and Output Timing

6.18 Serial Wire Debug (SWD) Characteristics

Table 6.58 SWD Characteristics
 Conditions: $V_{CC} = AV_{CC0} = 1.62$ to 3.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NORMAL	SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 6.65
	SWCLK clock high-level pulse width	t_{SWCKH}	$t_{SWCKcyc} \times 0.5 - t_{SWCKr}$	—	—	ns	
	SWCLK clock low-level pulse width	t_{SWCKL}	$t_{SWCKcyc} \times 0.5 - t_{SWCKf}$	—	—	ns	
	SWCLK clock rise time	t_{SWCKr}	—	—	7	ns	
	SWCLK clock fall time	t_{SWCKf}	—	—	7	ns	
	SWDIO setup time	t_{SWDS}	$t_{SWCKcyc} \times 0.2$	—	—	ns	Figure 6.66
	SWDIO hold time	t_{SWDH}	$t_{SWCKcyc} \times 0.2$	—	—	ns	
	SWDIO data delay time	t_{SWDD}	2	—	50	ns	
VBB	SWCLK clock cycle time	$t_{SWCKcyc}$	30000	—	—	ns	Figure 6.65
	SWCLK clock high-level pulse width	t_{SWCKH}	$t_{SWCKcyc} \times 0.5 - t_{SWCKr}$	—	—	ns	
	SWCLK clock low-level pulse width	t_{SWCKL}	$t_{SWCKcyc} \times 0.5 - t_{SWCKf}$	—	—	ns	
	SWCLK clock rise time	t_{SWCKr}	—	—	7	ns	
	SWCLK clock fall time	t_{SWCKf}	—	—	7	ns	
	SWDIO setup time	t_{SWDS}	1000	—	—	ns	Figure 6.66
	SWDIO hold time	t_{SWDH}	1000	—	—	ns	
	SWDIO data delay time	t_{SWDD}	2	—	1000	ns	

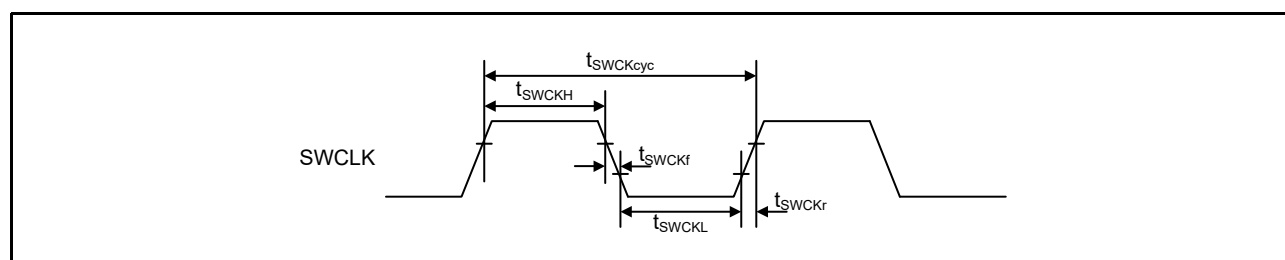


Figure 6.65 SWD SWCLK Timing

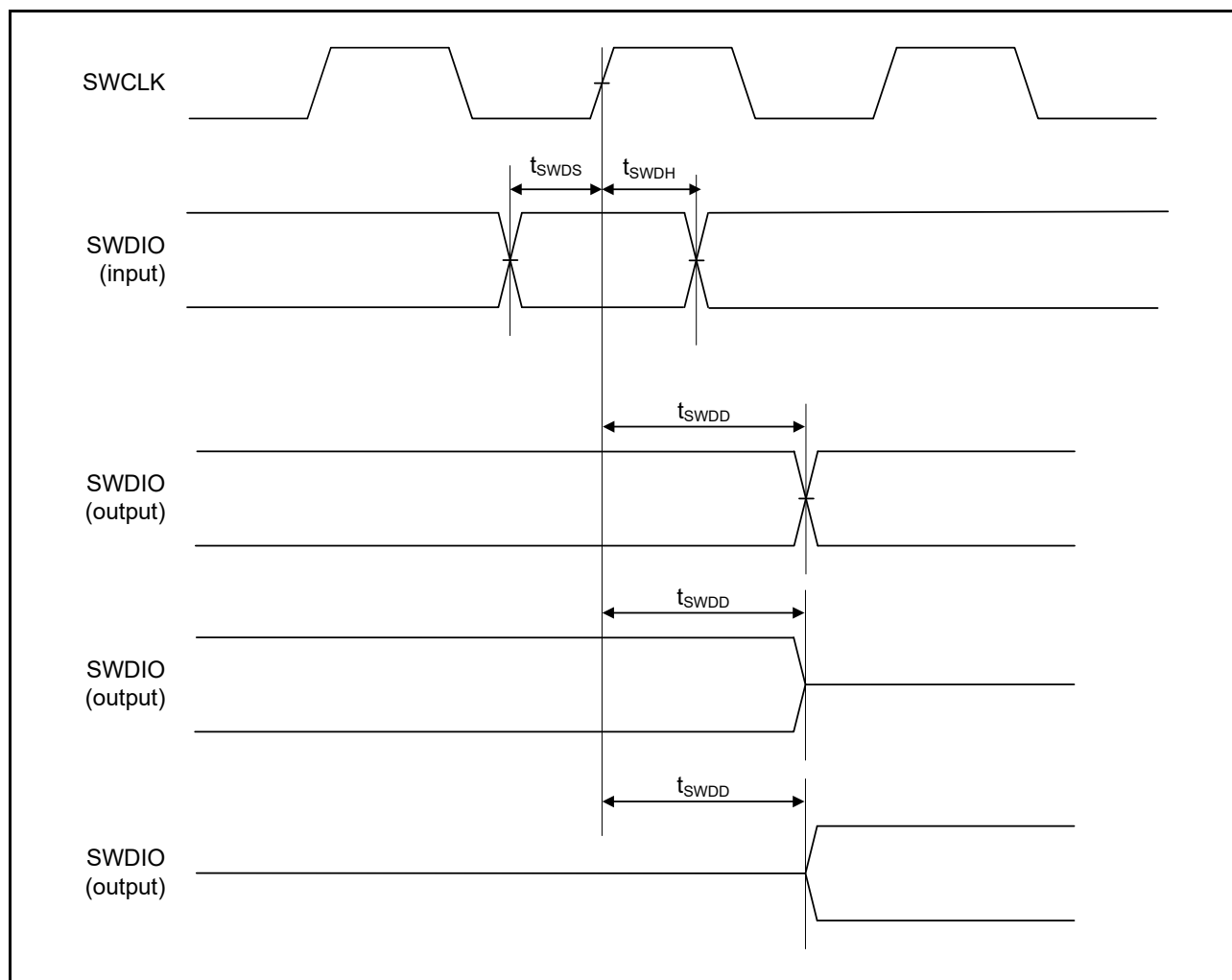


Figure 6.66 SWD Input and Output Timing

Appendix A. Package Dimensions

For the latest information on package dimensions and mounting, see “Packaging Information” on the Renesas website.

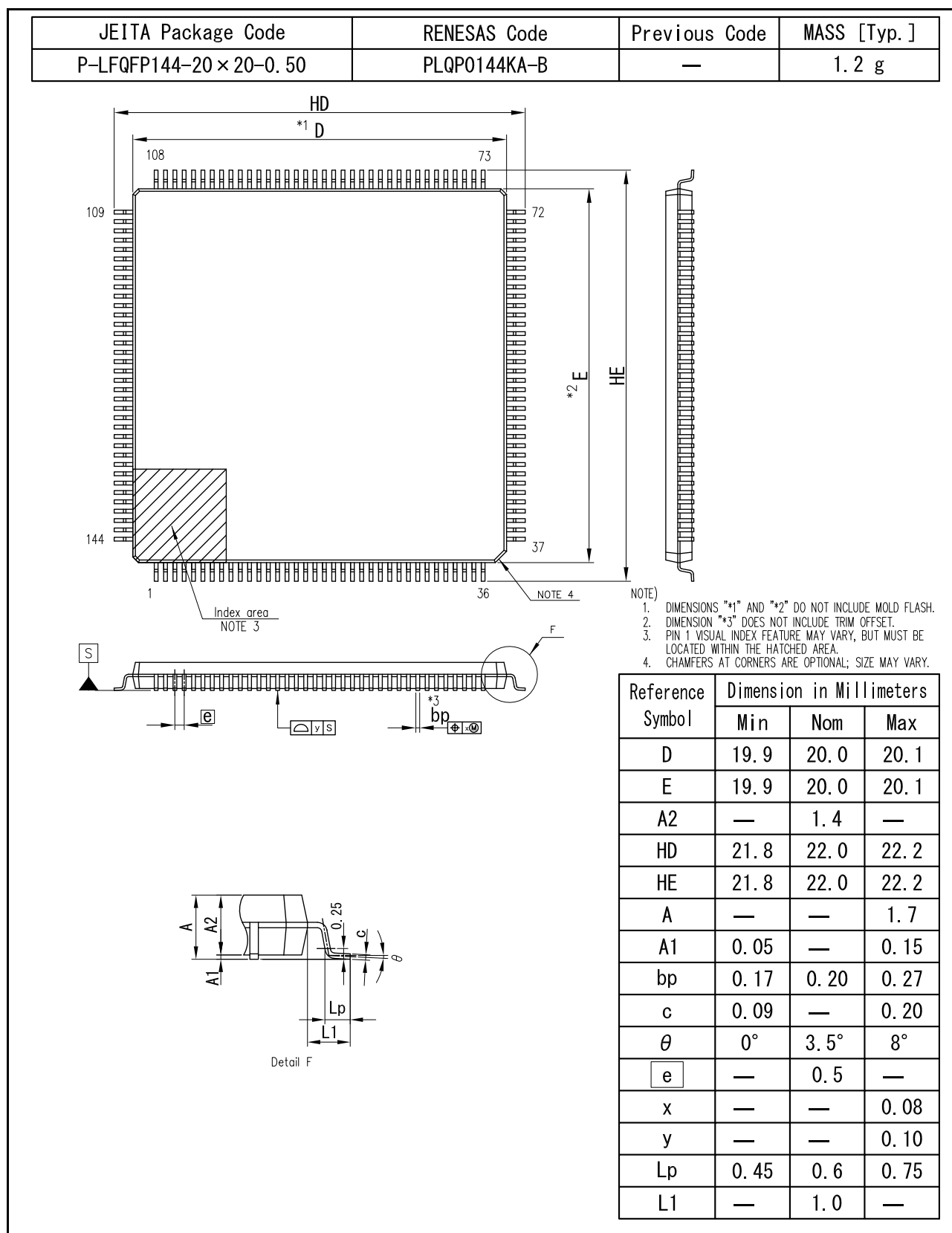


Figure A.1 144-Pin LFQFP (PLQP0144KA-B)

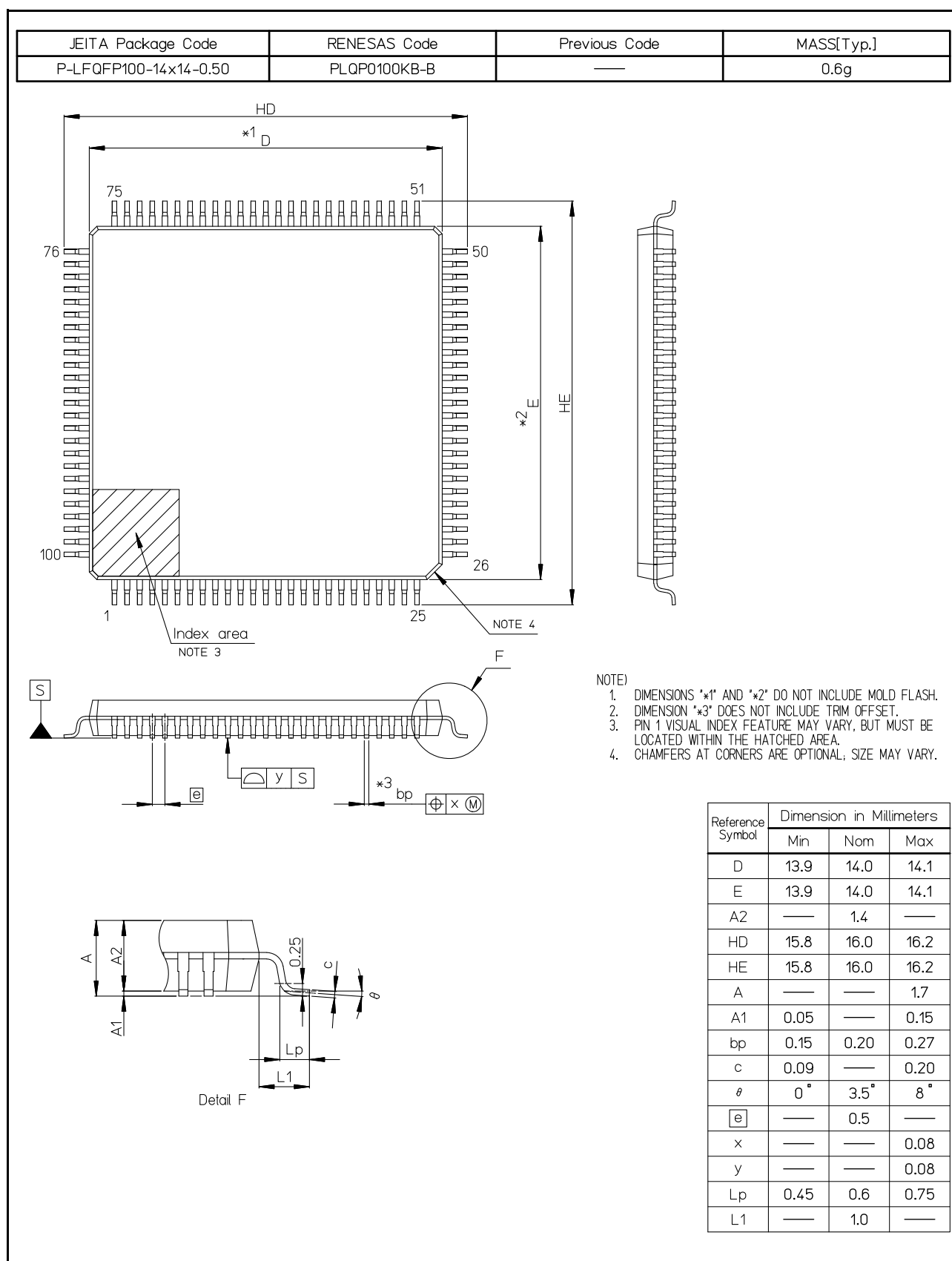


Figure A.2 100-Pin LFQFP (PLQP0100KB-B)

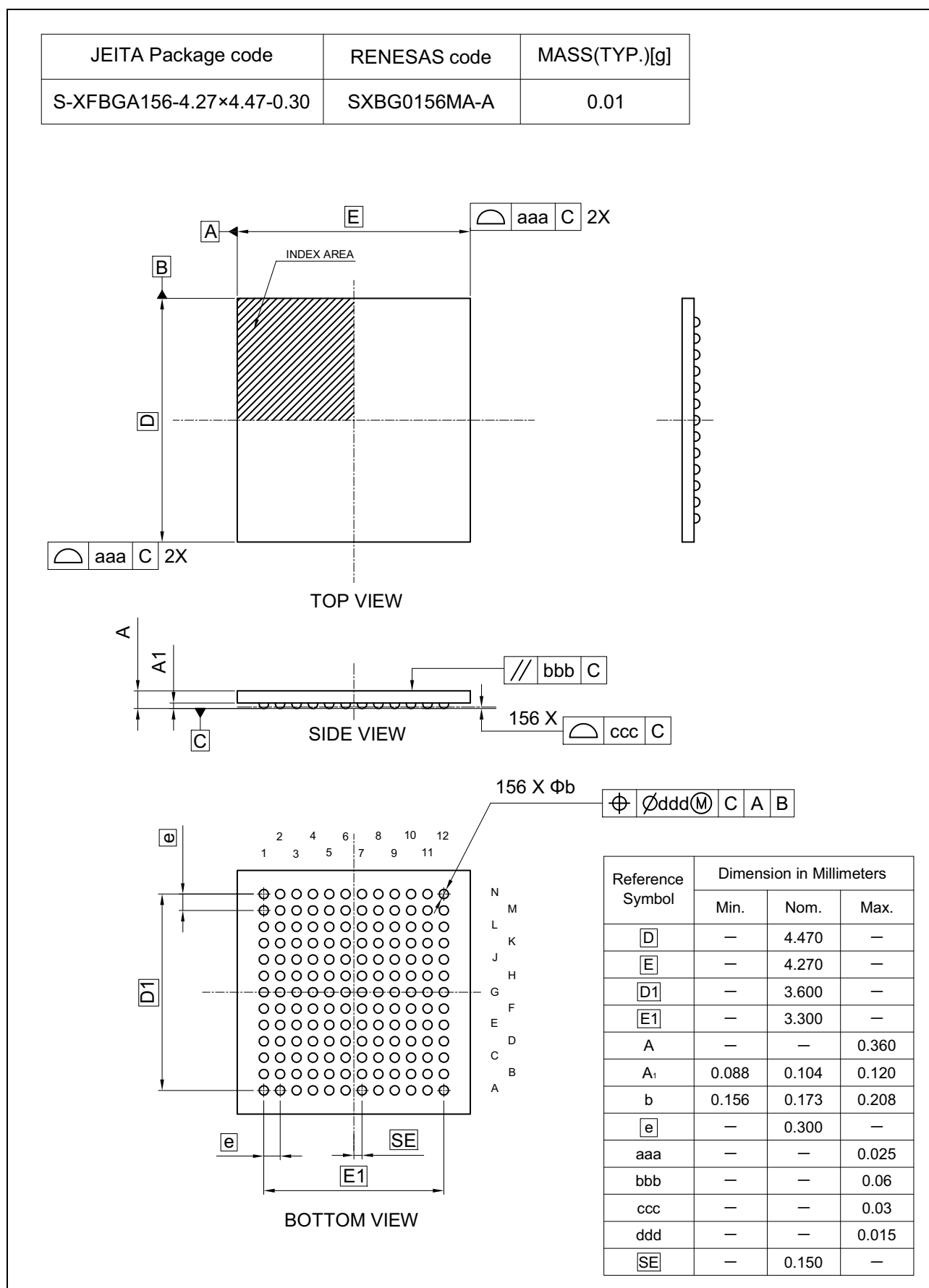


Figure A.3 156-Pin WLBGA (SXBG0156MA-A)

Appendix B. Connecting the Capacitors to the Power Supply Pins

The power supply pins must be connected to the ground via smoothing capacitors placed close to each of the power supply pins. This appendix shows representative examples of connections.

Setting the power supply open control register (VOCR) enables the external supply of power. In an environment where much external noise is present, place a 10- μ F capacitor close to each of the power supply pins as required, as well as the capacitors in the relevant example, to improve robustness against external noise and obtain stable operation of the circuit. For more details, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.

B.1 Example of Connections for Normal Startup Mode (1)

Figure B.1 shows an example of connections for normal startup mode with a single external power source and the EHC not in use.

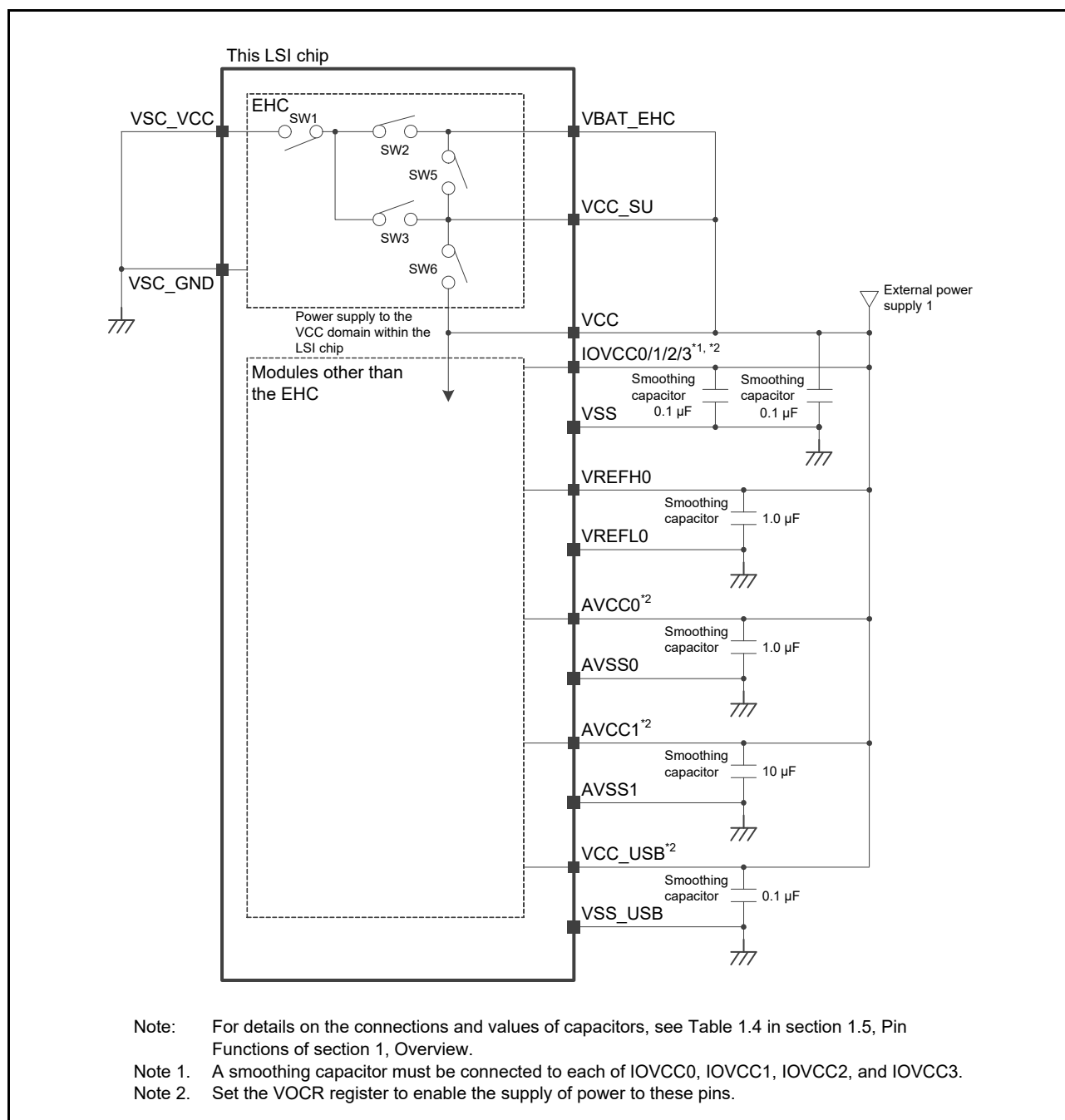


Figure B.1 Example 1 of Connections for Normal Startup Mode

B.2 Example of Connections for Normal Startup Mode (2)

Figure B.2 shows an example of connections for normal startup mode with the EHC not in use and each of the MLCD and USB connected to separate external power supplies.

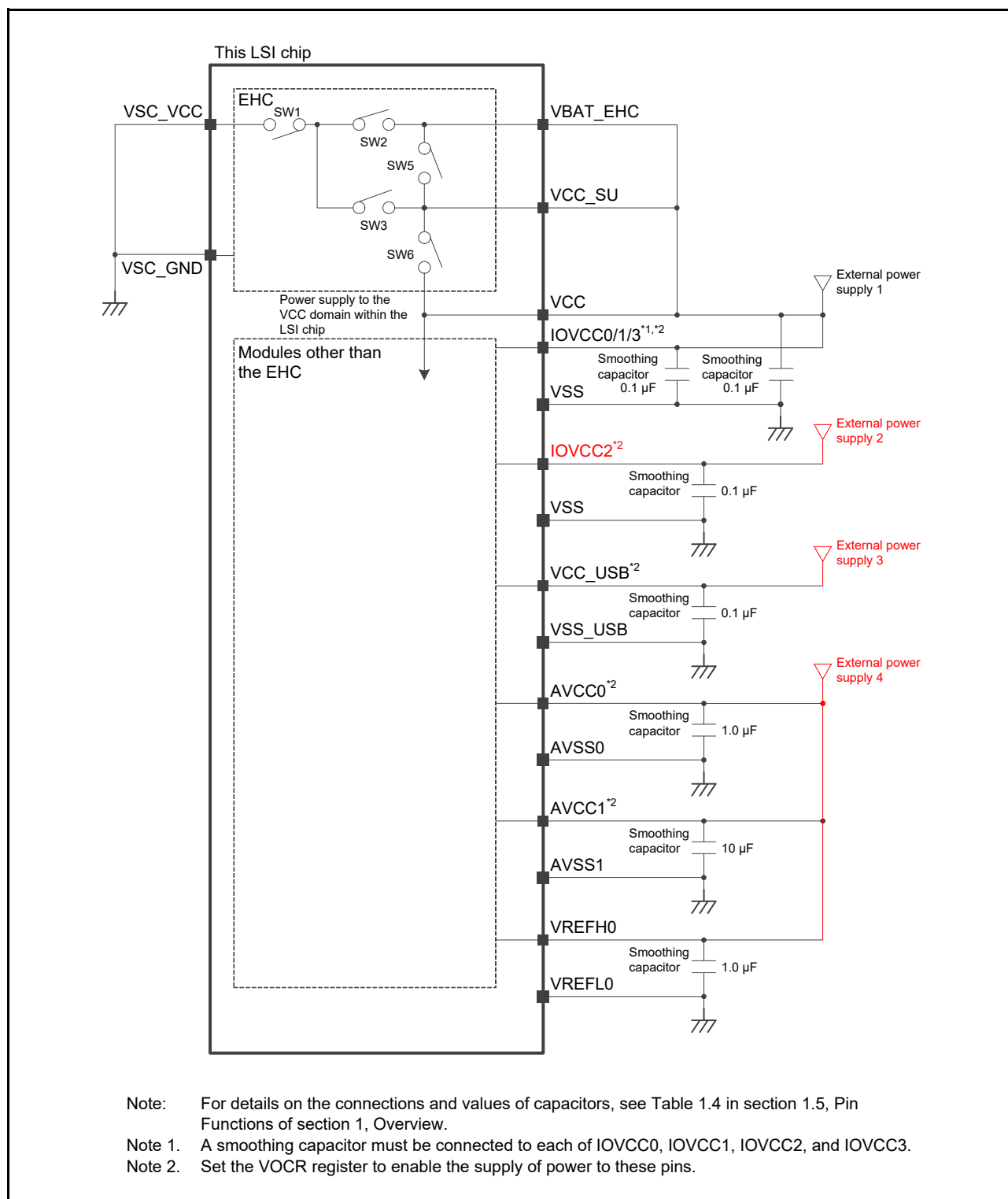


Figure B.2 Example 2 of Connections for Normal Startup Mode

B.3 Example of Connections in Energy Harvesting Startup Mode (1)

Figure B.3 shows an example of connections in energy harvesting startup mode with the EHC and VREF in use, and no external power supplies. Figure B.4 shows an example where AVCC0 is the reference voltage.

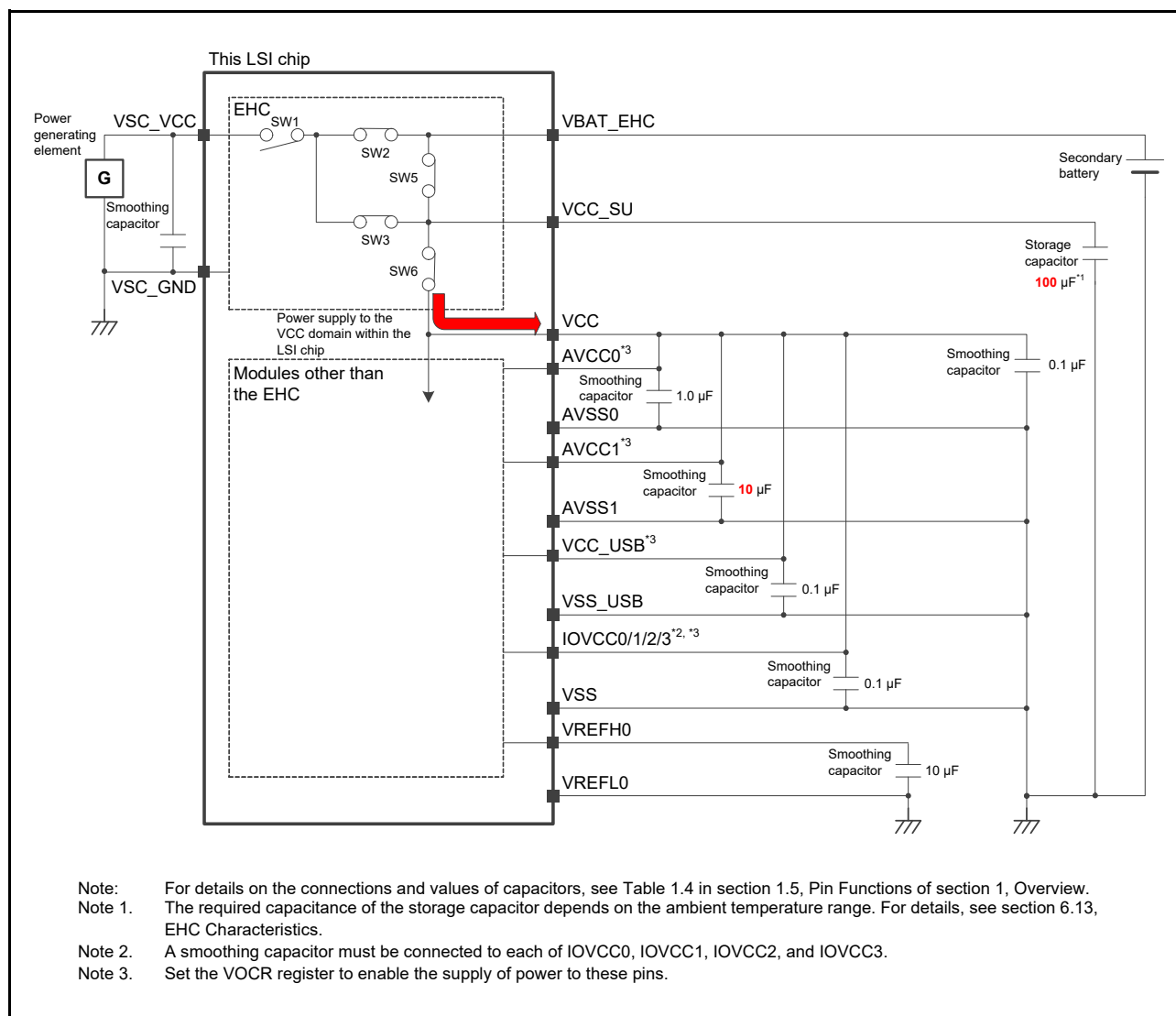


Figure B.3 Example of Connections in Energy Harvesting Startup Mode with the VREF in Use (1)

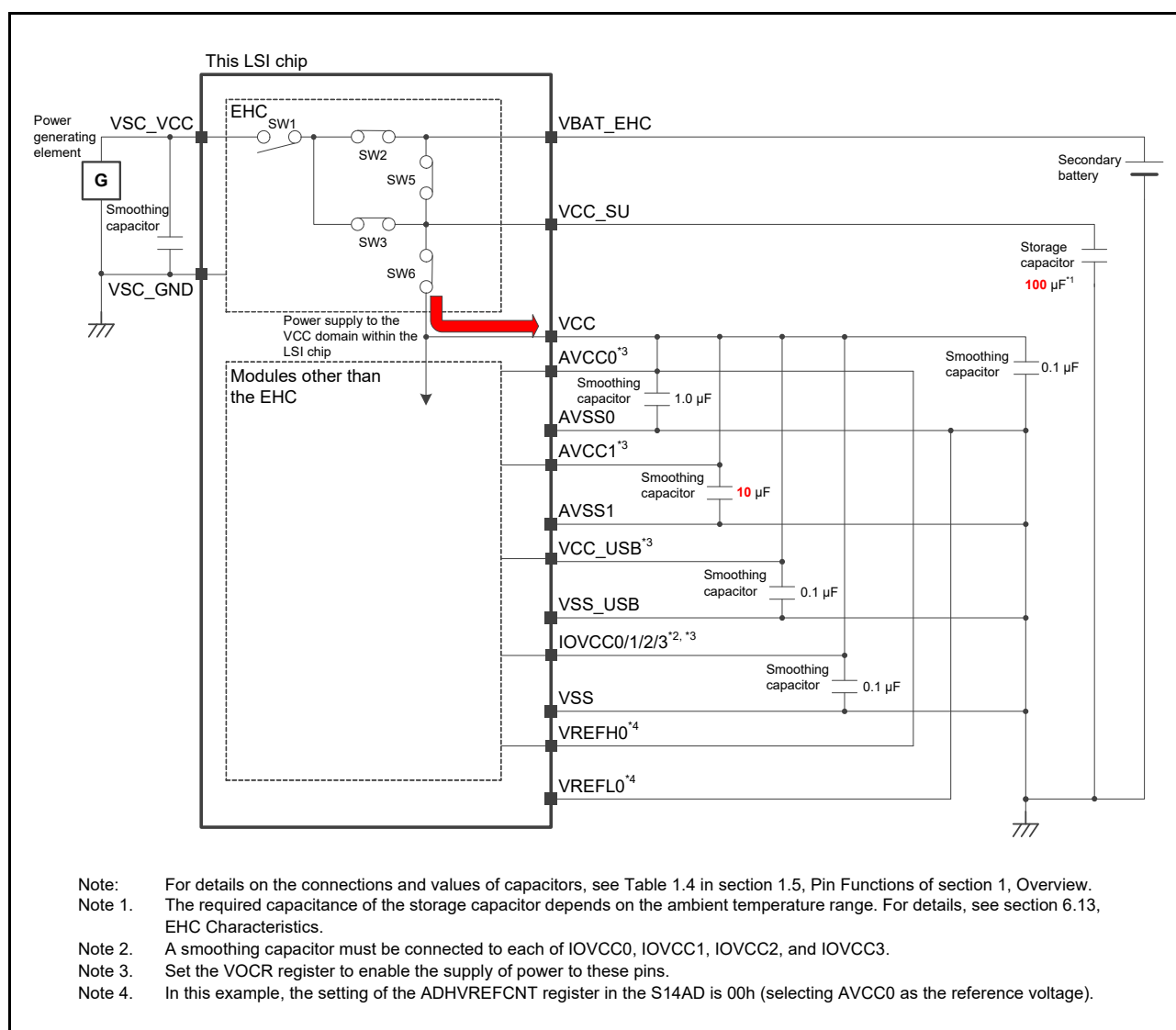


Figure B.4 Example of Connections in Energy Harvesting Startup Mode with AVCC0 as the Reference Voltage

B.4 Example of Connections in Energy Harvesting Startup Mode (2)

Figure B.5 shows an example of connections in energy harvesting startup mode with the EHC in use, no external power supplies, and neither the R12DA nor ACMP in use.

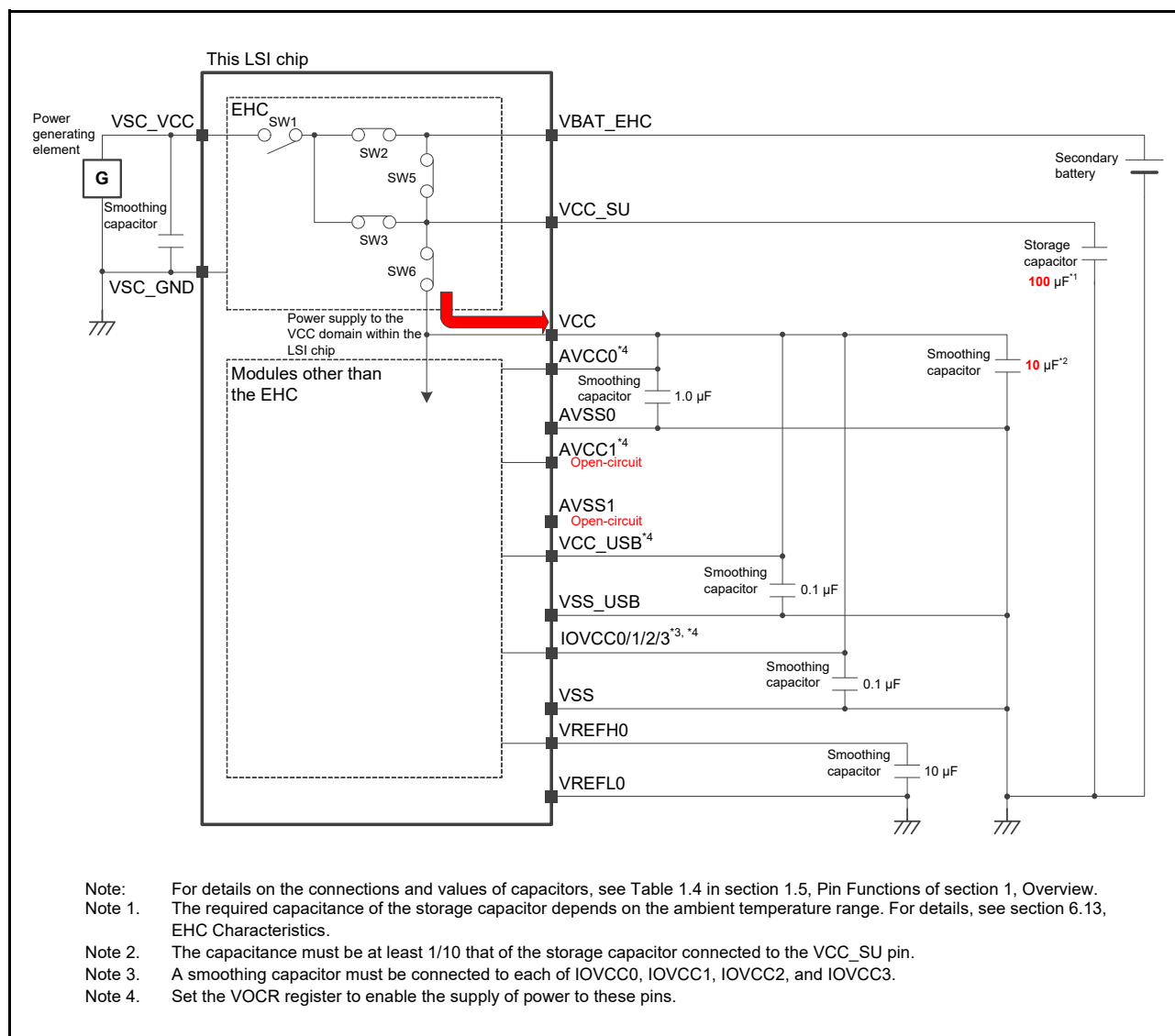


Figure B.5 Example of Connections in Energy Harvesting Startup Mode with the VREF in Use (2)

B.5 Example of Connections in Energy Harvesting Startup Mode (3)

Figure B.6 shows an example of connections in energy harvesting startup mode with the EHC in use and separate power sources for the analog circuits and USB. Figure B.7 shows an example with neither the analog circuits nor USB in use. Figure B.8 shows an example of minimum connections in energy harvesting startup mode.

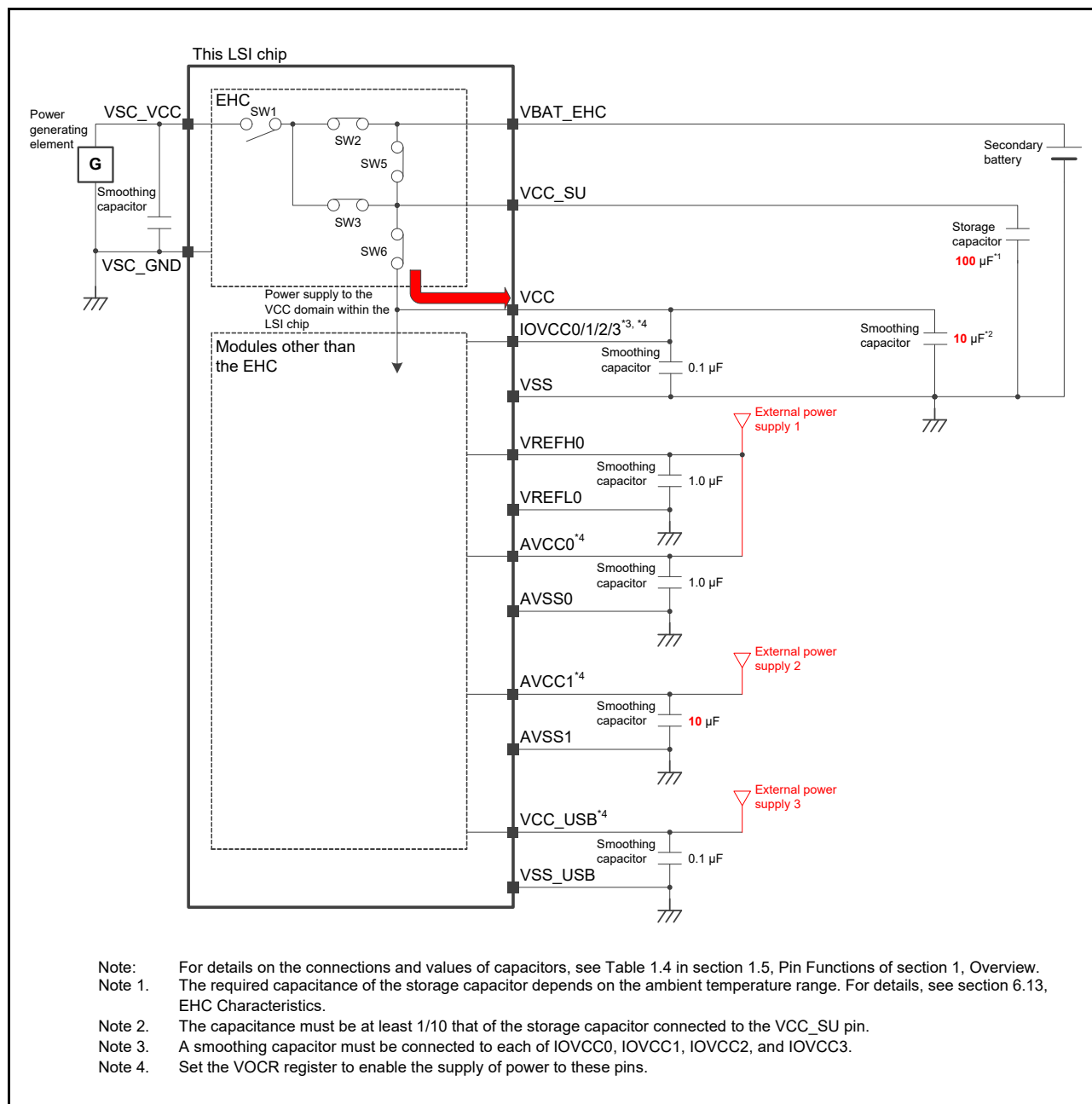


Figure B.6 Example of Connections in Energy Harvesting Startup Mode with Certain External Power Sources (1)

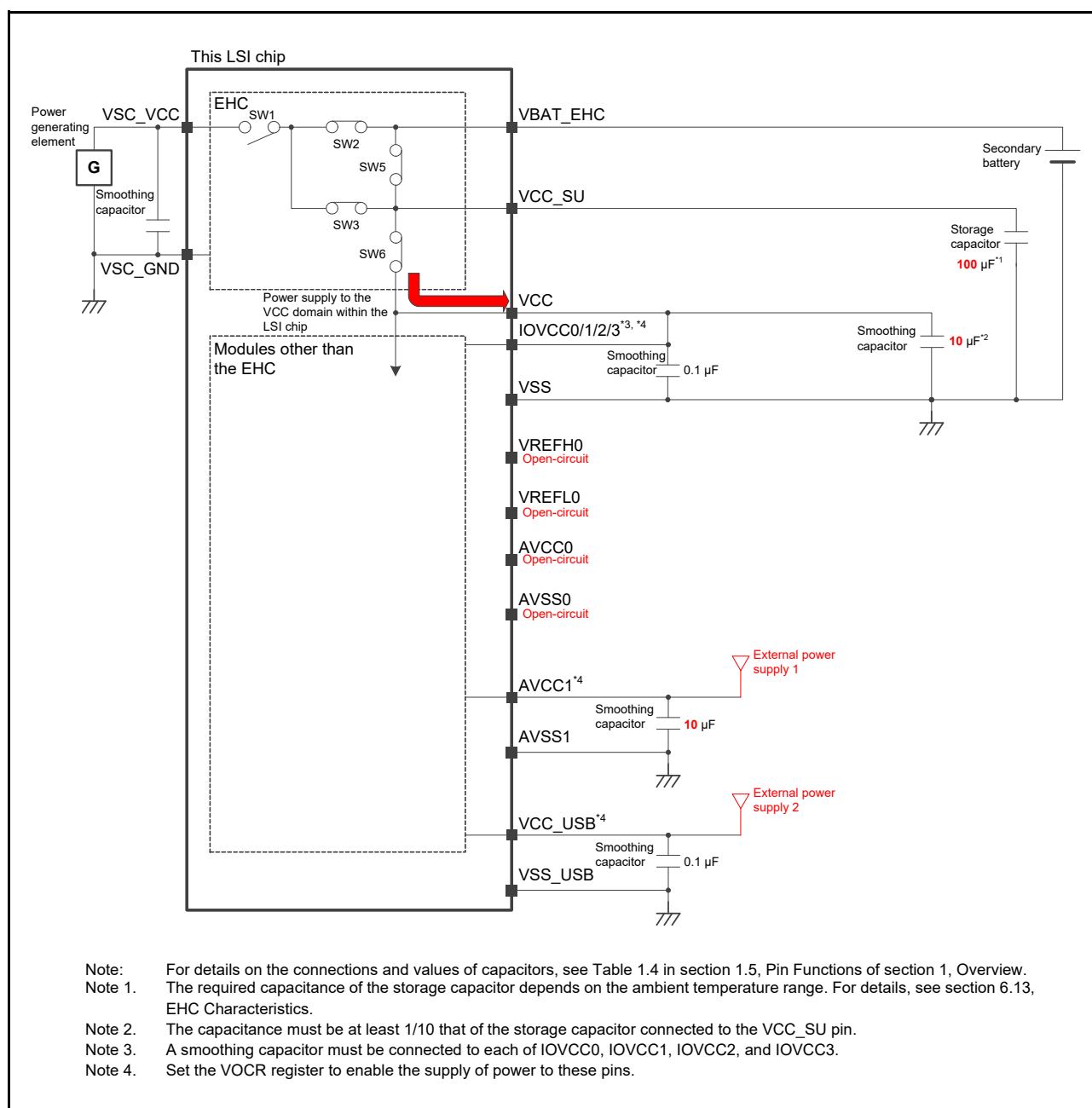


Figure B.7 Example of Connections in Energy Harvesting Startup Mode with Certain External Power Sources (2)

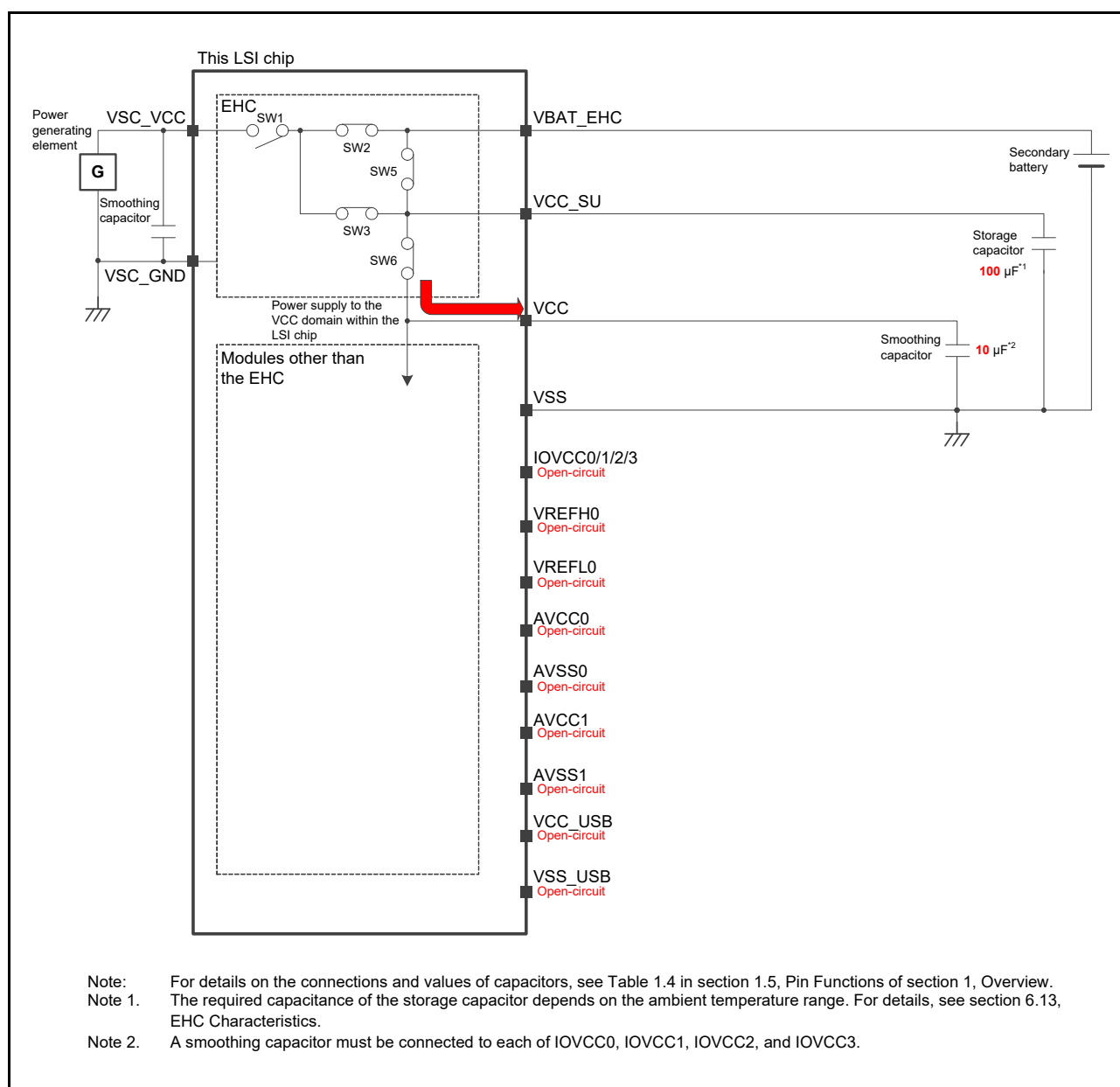


Figure B.8 Example of Minimum Connections in Energy Harvesting Startup Mode

REVISION HISTORY	RE01 Group Products with 1.5-Mbyte Flash Memory Datasheet
------------------	--

Rev.	Date	Description	
		Page	Summary
1.00	Oct 11, 2019	—	First edition, issued
1.10	May 29, 2020	Features	
		1	The following correction was made to Security functions (optional). • TSIP → TSIP-Lite
		1. Overview	
		2	The following correction was made to Table 1.1 Outline of Specifications (1/10). • The description of SysTick timer was corrected in the description of the CPU.
		4	The following corrections were made to Table 1.1 Outline of Specifications (3/10). • In the description of the CAC: CCC clock → CCC2K clock • In the description of the MPU: Arm® MPU: Eight MPU areas → Arm® MPU: Eight areas
		6	The following correction was made to Table 1.1 Outline of Specifications (5/10). • In the description of the CCC: 32.768-kHz sub-clock → sub-clock (32.768 kHz)
		7	The following correction was made to Table 1.1 Outline of Specifications (6/10). • Note was deleted from the description of the MTDV.
		13	The following correction was made to Table 1.2 List of Products. • The part numbers of the PLQP0100KB-B package products and the availability of the MLCD were changed.
		14	The following corrections were made to Table 1.3 Function Comparison (1/2). • The part numbers for the 100-pin products were changed. • Rows for number of general-purpose I/O port pins were added. • In a row for the MTDV: 3 channels → Yes (3 channels)
		15	The following correction was made to Table 1.3 Function Comparison (2/2). • The availability of the MLCD in the 100-pin products was corrected from No to Yes.
		16	The following correction was made to Table 1.4 Pin Functions (1/6). • A sentence was added to the end of the description of the VCC/IOVCC pin.
		18	The following description was made to Table 1.4 Pin Functions (3/6). • In the description of the AGTEE0 and AGTEE pins: signals → pins
		20	The following correction was made to Table 1.4 Pin Functions (5/6). • The description of the VREFH0/AVTRO pin was divided into the VREFH0 pin and the AVTRO pin.
		21	The following correction was made to Table 1.4 Pin Functions (6/6). • In the description of the PM_RES_DRV0 pin: Rotation detection pin → Back EMF detection pin
		26 to 41	The following corrections were made to Table 1.5 List of the Pins and Multiplexed Pin Functions (144-Pin LQFP) to Table 1.7 List of the Pins and Multiplexed Pin Functions (WLBGA). • The functions related to the SCI in the "Communications" column were corrected. - TXDn_m → TXDn_m/SSDAn_m/MOSIn_m - RXDn_m → RXDn_m/SSCLn_m/MISOn_m - CTSn_m → CTSn_m/RTSn_m/SSn_m
		32 to 35	The following corrections were made to Table 1.6 List of the Pins and Multiplexed Pin Functions (100-Pin LQFP). • The header was changed from Display to Display (MLCD). • The functions of the MLCD were added to the "Display (MLCD)" column.
		2. CPU	
		53	The title of section 2.5.5.3 DBGREG CoreSight Registers was corrected.
		56	The title of section 2.5.6.4 OCDREG CoreSight Registers was corrected.
		5. I/O Registers	
		67	The following correction was made to Table 5.2 I/O Register Access Cycle (1/2). • The end address of the flash memory: 4001 CFFFh → 4001 BFFFh
		6. Electrical Characteristics	
		69	At the beginning, the condition (description) was added at the end of the test conditions.
		71 to 75	The following corrections were made to section 6.2.2 Output Characteristics of I/O Pins (V_{OH} and V_{OL}) (1). • Table 6.5 Conditions for Testing I/O Characteristics was added. • Figure 6.1 V_{OL} vs. I_{OL} Characteristics (Low Driving Ability) to Figure 6.8 V_{OH} vs. I_{OH} Characteristics (High Driving Ability) were added.
		85	Section 6.2.9 Gradients of VCC Rising and Falling was newly added.
		85	Section 6.2.10 On-chip Linear Regulator Characteristics was newly added.

Rev.	Date	Description	
		Page	Summary
1.10	May 29, 2020	87	The following correction was made to Table 6.20 Timing of the Sub-clock Oscillator. • Note 1: SOSCCR.SOSTP flag → SOSCCR.SOSTP bit
		88	The following correction was made to Figure 6.14 PLL Clock Oscillation Start Timing. • A line irrelevant to the timing of the PLL circuit output was deleted.
		90	The following correction was made to Table 6.21 Reset Timing. • Rows for power-on (in the energy harvesting startup mode) and deep software standby mode (in the energy harvesting startup mode) were deleted.
		92	The following corrections were made to Table 6.22 Timing of Return from Low Power Consumption (Standby) Mode. • The descriptions in the "Item" column were corrected. • In the header: Power Control Mode → Power Control Mode before and after the Mode Transition • In the "Test Conditions" column, the references to the figure were deleted. • Note 1: (stopping the CAC) → (releasing the CAC from the module-stop state)
		94	The following correction was made to Table 6.24 I/O Ports, POE, GPT, AGT, and S14AD Trigger Timing. • ELC event pulse input width was added in a row for I/O ports.
		107	The following correction was made to Table 6.31 RIIC Timing. • The description of test conditions was corrected.
		125	The following correction was made to Table 6.50 EHC Characteristics. • Power generating element status flag → Threshold voltage for the power generating element status flag
		Appendix B. Connecting the Capacitors to the Power Supply Pins	
		140	The following correction was made to Figure B.1 Example 1 of Connections for Normal Startup Mode. • The value of the smoothing capacitor between the VREFH0 and VREFL0 pins was corrected from 0.1 μF to 1.0 μF.
		147	Note 3 was deleted from Figure B.8 Example of Minimum Connections in Energy Harvesting Startup Mode.
		140 to 147	The following changes were made to Figures B.1 to B.8. • On-chip peripheral modules other than the EHC → Modules other than the EHC

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
 4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
 5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
 6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
 7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
 8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
 9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
 10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
 11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics Corporation

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc. Milpitas Campus

1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.

Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics America Inc. San Jose Campus

6024 Silver Creek Valley Road, San Jose, CA 95138, USA

Tel: +1-408-284-8200, Fax: +1-408-284-2775

Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3

Tel: +1-905-237-2004

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany

Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China

Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China

Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong

Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan

Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, #06-02 Singapore 339949

Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia

Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India

Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.

17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea

Tel: +82-2-558-3737, Fax: +82-2-558-5338