



MP2696A

I²C-Controlled, Single-Cell Switching Charger with Power-Path Management and 3.6A Boost Output

DESCRIPTION

The MP2696A is a highly integrated, flexible, switch-mode battery-charging, power-path management device designed for a single-cell Li-ion and Li-polymer battery to be used in a wide range of portable applications.

The MP2696A integrates three battery-charging phases: pre-charge, constant-current, and constant-voltage charge. This device also manages the input power source through input current limit regulation and minimum input voltage regulation.

The MP2696A can switch to boost mode to generate the system power output from the battery.

The MP2696A has an integrated IN to SYS pass-through path to pass the input voltage to the system.

Using an I²C interface, the host can flexibly program the charge and boost parameters. The device operating status can also be read in the registers.

Safety features include SYS short-circuit protection, input over-voltage protection, battery under-voltage protection, thermal shutdown, and JEITA battery temperature monitoring.

The MP2696A is available in a QFN-21 (3mmx3mm) package.

FEATURES

- 4.0V to 11V Operation Voltage Range
- Up to 16V Sustainable Input Voltage
- 500mA to 3.6A Programmable Charge Current
- 3.6V to 4.45V Programmable Charge Regulation Voltage with $\pm 0.5\%$ Accuracy
- 100mA to 3A Programmable Input Current Limit with $\pm 10\%$ Accuracy
- Minimum Input Voltage Loop for Maximum Adapter Power Tracking
- Ultra-Low 25 μ A Battery Discharge Current in Idle Mode
- Boost Converter w/ Up to 3.6A Output Current:
 - Programmable Output Current Limit Loop
 - Programmable Boost Output Voltage
 - USB Output Cable Compensation
 - Programmable Inductor Peak Current Limiting
- Comprehensive Safety Features
 - Fully-Customizable JEITA Profile with Programmable Temperature Threshold
 - Charge Safety Timer
 - Input Over-Voltage Protection
 - Thermal Shutdown
 - SYS Over-Current and Short Protection
- Analog Voltage Output IB Pin for Battery Current Monitoring
- SYS Plug-In Detection
- SYS No Load Detection
- SYS DP/DM Interface for BC1.2 and Non-Standard Adapters
- Status and Fault Monitoring
- Available in a QFN-21 (3mmx3mm) Package

APPLICATIONS

- Sub-Battery Applications
- Power Bank Applications for Smartphone, Tablet, and Other Portable Devices

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION

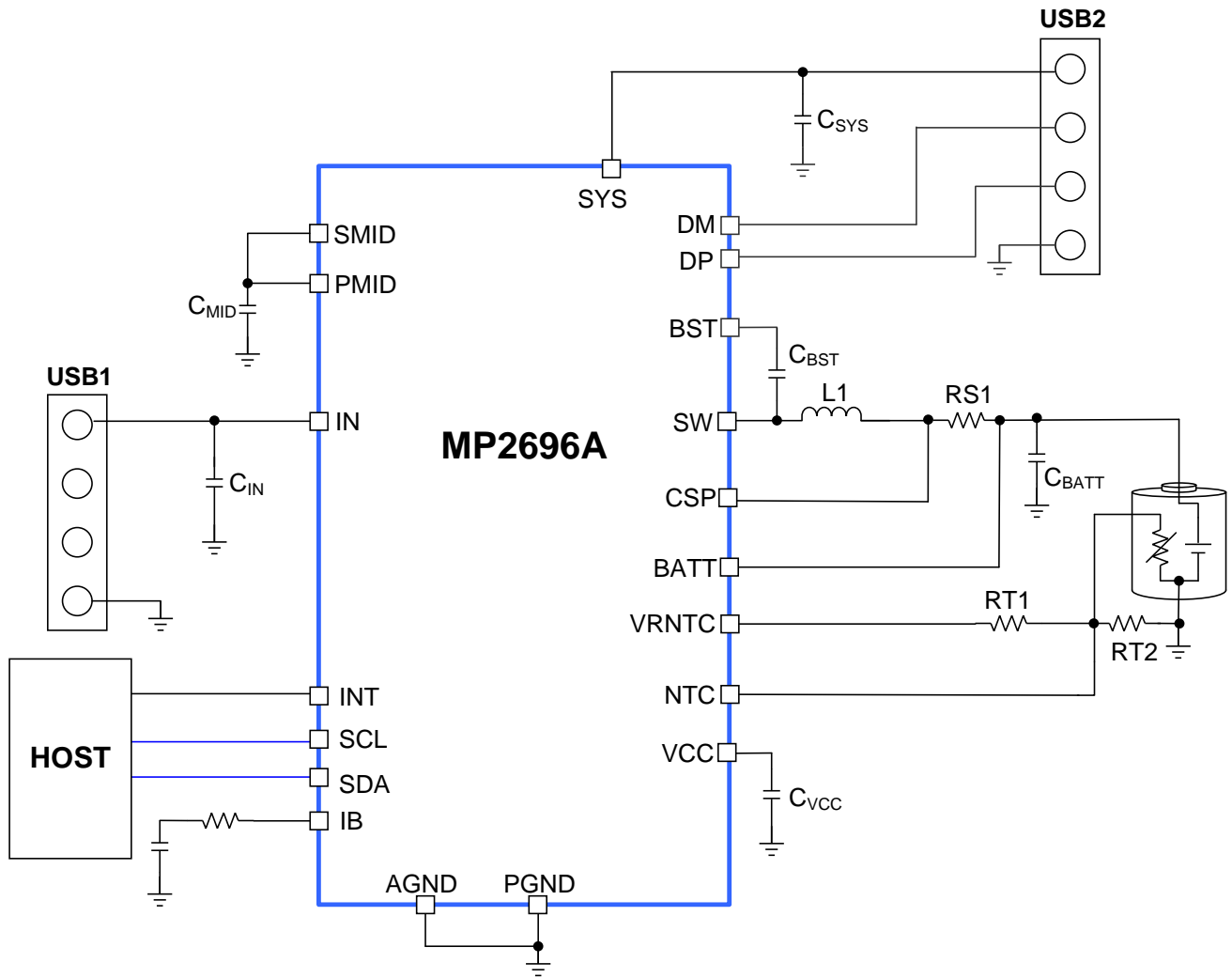


Figure 1: Typical Application

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2696AGQ-0000**	QFN-21 (3mmx3mm)	See Below
EVKT-MP2696A	Evaluation kit	

* For Tape & Reel, add suffix –Z (e.g. MP2696AGQ-xxxx–Z).

**“xxx” is the register setting option. The factory default is “0000.” This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an “xxx” value.

TOP MARKING

BKZY

LLL

BKZ: Product code of MP2696AGQ

Y: Year code

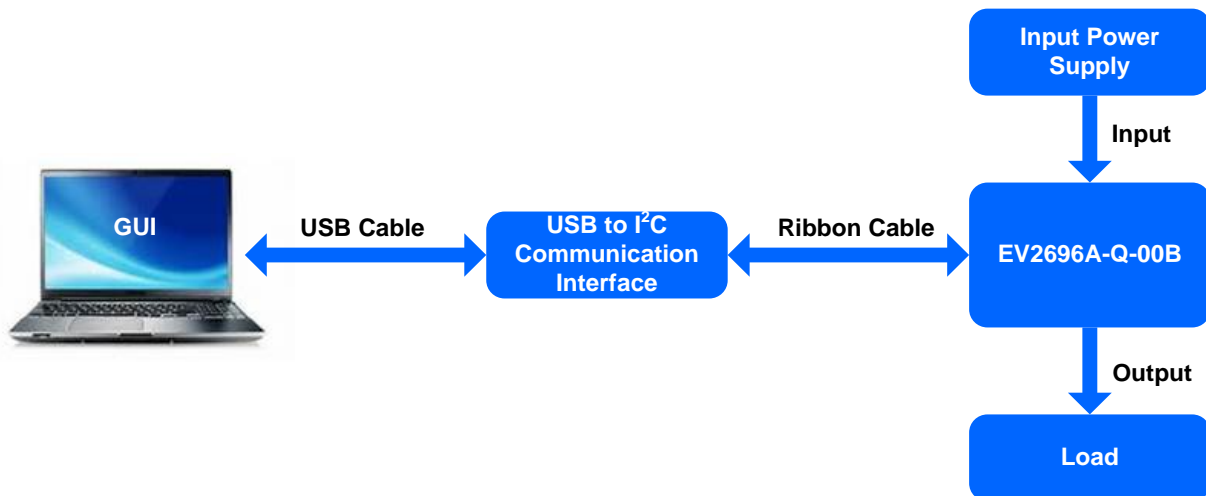
LLL: Lot number

EVALUATION KIT EVKT-MP2696A

EVKT-MP2696A kit contents (items below can be ordered separately):

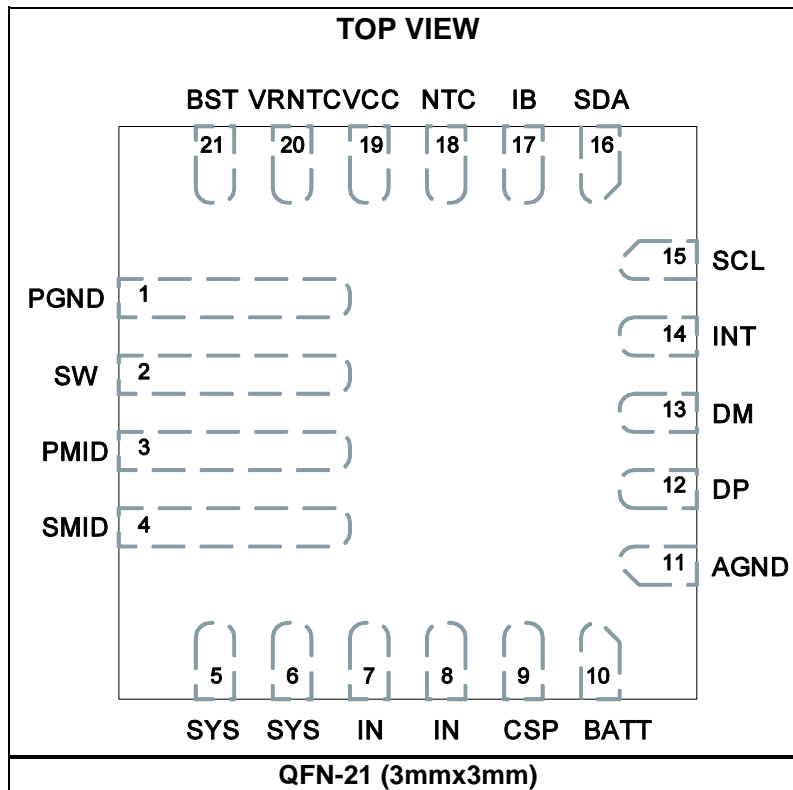
#	Part Number	Item	Quantity
1	EV2696A-Q-00B	MP2696A evaluation board	1
2	EVKT-USB I ² C-02-BAG	Includes one USB to I ² C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.



EVKT-MP2696A Evaluation Kit Set-Up

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	I/O	Description
1	PGND	Power	Power ground.
2	SW	Power	Switching output node. Connect SW to the inductor.
3	PMID	Power	Drain of the high-side switching MOSFET. Bypass PMID with ceramic capacitors from PMID to PGND, placed as close to the IC as possible. This pin cannot carry external load.
4	SMID	Power	Connected to the drain of Q1 and Q2. Short SMID to PMID on the PCB.
5,6	SYS	Power	System power output. Place ceramic capacitors from SYS to PGND.
7,8	IN	Power	Power input of the IC. Place ceramic capacitors from IN to PGND.
9	CSP	I	Battery current sense positive input.
10	BATT	I	Battery positive terminal.
11	AGND	Power	Analog ground. Short to PGND on the PCB.
12	DP	I/O	Positive port of the USB data for the output. High ESD rating.
13	DM	I/O	Negative port of the USB data for the output. High ESD rating.
14	INT	O	Open-drain interrupt output. Connect INT to the logic rail through a 10kΩ resistor.
15	SCL	I/O	I²C interface clock. Connect SCL to the logic rail through a 10kΩ resistor.
16	SDA	I/O	I²C interface data. Connect SDA to the logic rail through a 10kΩ resistor.
17	IB	O	Battery current indicator. The voltage at IB indicates the charge current to the battery in charge mode, and the discharge current of the battery in boost mode.
18	NTC	I	Temperature sense input. Connect NTC to a negative temperature coefficient thermistor. Program the temperature window with a resistor divider from VRNTC to NTC to GND. Programmable JEITA thresholds are supported.
19	VCC	I	Internal circuit and switch driver power supply. Bypass to AGND with a ceramic capacitor as close to the IC as possible. For the external load capacity, see the VCC Power Supply section on page 16.
20	VRNTC	O	Reference voltage output for powering up NTC.
21	BST	I	Bootstrap. Connect a 470nF bootstrap capacitor between BST and SW to form a floating supply across the high-side power switch driver.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN, PMID, SMID, SYS to PGND ...	-0.3V to +16V
SW to PGND	-0.3V (-2V for 20ns) to
.....	+14V (16V for 20ns)
BST to PGND.....	SW to SW + 5V
All other pins to AGND.....	-0.3V to +5.0V
Continuous power dissipation (T _A = 25°C) ⁽²⁾	2.5W
Junction temperature	150°C
Lead temperature (solder)	260°C
Storage temperature.....	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V _{IN})	4.5V to +11V
Input current (I _{IN})	Up to 3A
System current (I _{SYS}).....	Up to 3.6A
Charge current (I _{CC})	Up to 3.6A
Battery voltage (V _{BATT})	Up to 4.5V
Operating junction temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾ **θ_{JA}** **θ_{JC}**

QFN-21 (3mmx3mm)	50.....	12... °C/W
------------------------	---------	------------

ESD RATINGS

DP, DM pins:

 Human body model (HBM) ⁽⁵⁾ 8000V

 Charged device model (CDM) ⁽⁶⁾ 800V

All other pins:

 Human body model (HBM) ⁽⁵⁾ 2000V

 Charged device model (CDM) ⁽⁶⁾ 250V

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.
- 5) Per ANSI/ESDA/JEDEC JS-001.
- 6) Per JESD22-C101.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 5.0V$, $V_{BATT} = 3.5V$, $R_{S1} = 10m\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery discharge current in IDLE mode	I_{BATT_IDLE}	Idle mode		25	36	μA
Input quiescent current without switching	I_{IN_Q}	$V_{IN} > V_{IN_UVLO}$, $V_{IN} > V_{BATT} + V_{HDRM}$, charge disabled, float SYS		0.6	1	mA
Input quiescent current when switching	I_{IN_QSW}	$V_{IN} > V_{IN_UVLO}$, $V_{IN} > V_{BATT} + V_{HDRM}$, charge enabled, float BATT and SYS		1		mA
Battery discharge current in boost mode	I_{BOOST_Q}	$I_{SYS} = 0$, $V_{BOOST}[2:0] = 5.15V$, boost enabled, $V_{BATT} = 4.2V$		2		mA
Power On/Off						
IN operating range	V_{IN_OP}	Converter switching	4		11	V
Input under-voltage lockout	V_{IN_UV}	V_{IN} falling	2.95	3.10	3.25	V
Input under-voltage lockout hysteresis		V_{IN} rising		305		mV
Input vs. battery headroom	V_{HDRM}	V_{IN} rising		200	310	mV
		V_{IN} falling	10	80		mV
Battery under-voltage lockout	V_{BATT_UV}	During boost	2.4	2.5	2.6	V
		Before boost starts	2.8	2.9	3.0	V
VCC LDO output voltage	V_{VCC}	$V_{IN} = 5V$, $I_{VCC} = 30mA$	3.3	3.55	3.8	V
VCC under-voltage lockout	V_{CC_UV}	VCC rising	1.9	2.1	2.3	V
VCC under-voltage lockout hysteresis				80		mV
Power Path						
IN to PMID FET (Q1) on resistance	R_{ON_Q1}			25		$m\Omega$
PMID to SYS FET (Q2) on resistance	R_{ON_Q2}			15		$m\Omega$
High-side FET (Q3) on resistance	R_{ON_HS}			15		$m\Omega$
Low-side FET (Q4) on resistance	R_{ON_LS}			14		$m\Omega$
Peak current limit for high-side FET in buck mode	I_{HS_PK}	CC charge mode		6.5		A
		Pre-charge mode		1.3		A
Peak current limit for low-side FET in boost mode	I_{LS_PK}	$BST_IPK[1:0] = 6.5A$	5.9	6.6	7.3	A
		$BST_IPK[1:0] = 5A$	4.1	4.8	5.5	A
Switching frequency	f_{SW}	$SW_FREQ = 700kHz$		720		kHz
		$SW_FREQ = 1200kHz$		1200		kHz

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 5.0V$, $V_{BATT} = 3.5V$, $R_{S1} = 10m\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Charge Mode						
Charge voltage regulation	V_{BATT_REG}	BATT_REG range ⁽⁷⁾	3.6		4.45	V
		BATT_REG[2:0] = 3.6V	3.582	3.6	3.618	V
		BATT_REG[2:0] = 4.1V	4.080	4.1	4.120	V
		BATT_REG[2:0] = 4.2V	4.179	4.2	4.221	V
		BATT_REG[2:0] = 4.3V	4.279	4.3	4.321	V
		BATT_REG[2:0] = 4.35V	4.328	4.35	4.372	V
		BATT_REG[2:0] = 4.4V	4.378	4.40	4.422	V
		BATT_REG[2:0] = 4.45V	4.428	4.45	4.472	V
Fast charge current	I_{CC}	ICC[4:0] = 3A	2.7	3	3.4	A
		ICC[4:0] = 1.5A	1.35	1.5	1.7	A
		ICC[4:0] = 0.5A	0.41	0.5	0.6	A
Charge termination current	I_{TERM}	ITERM[1:0] = 100mA	40	100	160	mA
		ITERM[1:0] = 200mA	100	200	300	mA
Recharge threshold below V_{BATT_REG}	V_{RECH}	V_{BATT} falling	100	200	320	mV
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising	2.9	3.0	3.1	V
Pre-charge to fast charge hysteresis		V_{BATT} falling		290		mV
Pre-charge current	I_{PRE}	IPRE[1:0] = 150mA, $V_{BATT} = 1.8V$		150		mA
		IPRE[1:0] = 350mA, $V_{BATT} = 1.8V$		350		mA
Safety timer for charging cycle				20		hours
Input Regulation						
Input minimum voltage regulation	V_{IN_MIN}	VINMIN[2:0] = 4.5V	4.41	4.51	4.61	V
		VINMIN[2:0] = 4.65V	4.56	4.66	4.76	V
Input current limit	I_{IN_LIM}	IINLIM[2:0] = 3A	2.7	2.85	3	A
		IINLIM[2:0] = 1.5A	1.3	1.4	1.5	A
		IINLIM[2:0] = 0.5A	0.4	0.45	0.5	A
Boost Mode						
Boost output voltage at PMID	V_{PMID_BST}	VBOOST[2:0] = 5.15V, $I_{SYS} = 10mA$	5.05	5.13	5.21	V
		VBOOST[2:0] = 5.225V, $I_{SYS} = 10mA$	5.13	5.21	5.29	V
Boost output current limit	I_{BST_LMT}	IOLIM[3:0] = 3.6A	3.55	3.7	3.85	A
		IOLIM[3:0] = 2.8A	2.7	2.8	2.9	A
		IOLIM[3:0] = 2.1A	1.9	2.05	2.15	A

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 5.0V$, $V_{BATT} = 3.5V$, $R_{S1} = 10m\Omega$, $T_A = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Analog Control						
SYS no load current threshold	I_{BST_OFF}	NOLOAD_THR[1:0] = 30mA		30		mA
		NOLOAD_THR[1:0] = 50mA		50		mA
		NOLOAD_THR[1:0] = 75mA		75		mA
		NOLOAD_THR[1:0] = 100mA		100		mA
SYS plug-in detection threshold	V_{PLUG_IN}	SYS falling, percentage of V_{BATT}	70	75	80	%
Discharge dummy load at IN	R_{IN_DUM}			250		Ω
Discharge dummy load at SYS	R_{SYS_DUM}			30		Ω
Protection						
Battery over-voltage threshold	V_{BATT_OVP}		102	104	106	%
BATT over-voltage hysteresis				1.5		%
IN over-voltage protection	V_{IN_OV}	V_{IN} rising, $V_{IN_OVP} = 6V$	5.8	6	6.2	V
		V_{IN} rising, $V_{IN_OVP} = 11V$	10.6	11	11.4	V
IN over-voltage protection hysteresis		V_{IN} falling		300		mV
Thermal Shutdown and Temperature Control						
Thermal shutdown rising threshold ⁽⁷⁾	T_{J_SHDN}	T_J rising		150		$^{\circ}C$
Thermal shutdown hysteresis ⁽⁷⁾				20		$^{\circ}C$

ELECTRICAL CHARACTERISTICS (continued)
V_{IN} = 5.0V, V_{BATT} = 3.5V, R_{S1} = 10mΩ, T_A = 25°C, unless otherwise noted.

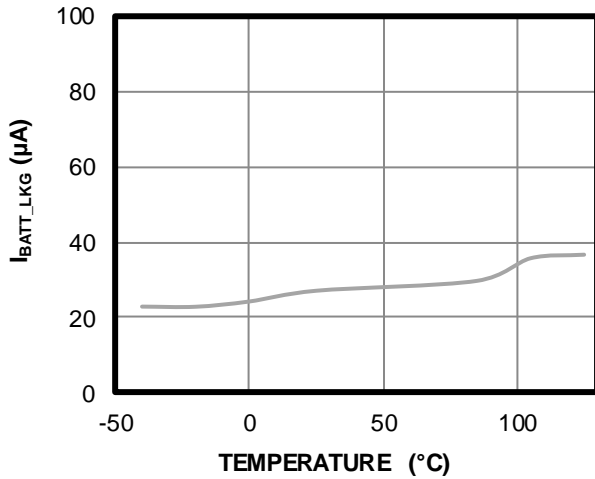
Parameters	Symbol	Condition	Min	Typ	Max	Units
VRNTC voltage	V _{VRNTC}	V _{IN} = 5V, I _{VRNTC} = 100μA		3.5		V
NTC low temp rising threshold	V _{COLD}	As percentage of V _{VRNTC} V _{COLD} [1:0] = 72%	72	73.1	74.3	%
NTC low temp rising threshold hysteresis		As percentage of V _{VRNTC}		1.6		%
NTC cool temp rising threshold	V _{COOL}	As percentage of V _{VRNTC} V _{COOL} [1:0] = 60%	59.7	61	62.2	%
NTC cool temp rising threshold hysteresis		As percentage of V _{VRNTC}		1.6		%
NTC warm temp falling threshold	V _{WARM}	As percentage of V _{VRNTC} V _{WARM} [1:0] = 40%	39.4	40.6	42	%
NTC warm temp falling threshold hysteresis		As percentage of V _{VRNTC}		1.6		%
NTC hot temp falling threshold	V _{HOT}	As percentage of V _{VRNTC} V _{HOT} [1:0] = 36%	35.3	36.6	37.9	%
NTC hot temp falling threshold hysteresis		As percentage of V _{VRNTC}		1.6		%
SYS DP/DM Signaling						
DP/DM source voltage 2V7	V _{SRC_2V7}		2.6	2.7	2.8	V
DP/DM source resistance	R _{SRC}		23	30	37	kΩ
DP/DM comparator threshold 2.9V	V _{TH_2V9}		2.75	2.9	3.1	V
DP/DM comparator threshold 2.1V	V _{TH_2V1}		1.95	2.1	2.25	V
Deglitch time for exiting non-standard adapter			8	10	12	ms
DP/DM short resistance	R _{SHORT}			100		Ω
Pull-down resistor on DP pin	R _{PULL_DWN}			300		kΩ
Timer for DCP to enter non-standard adapter				2		s
I²C Interface						
Input high threshold level		SDA and SCL	1.3			V
Input low threshold level		SDA and SCL			0.4	V
Output low threshold level		I _{SINK} = 5mA			0.3	V
I ² C clock frequency	f _{SCL}				400	kHz
Battery Current Indicator						
IB voltage output		I _{CC} = 1A in charge mode	0.33	0.35	0.37	V
		I _B = 1A in boost mode	0.15	0.16	0.17	V

Notes:

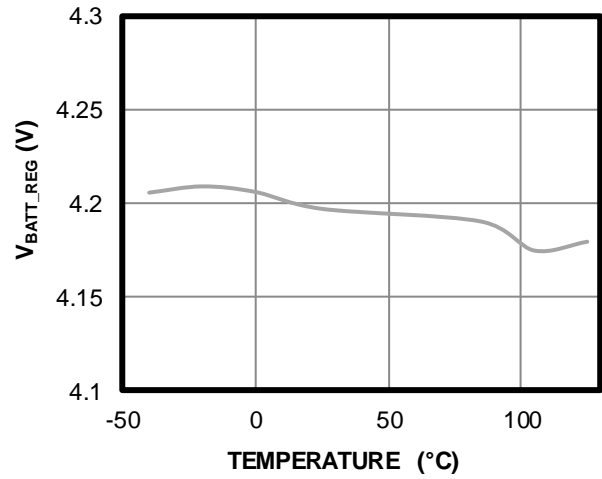
7) Guaranteed by design.

TYPICAL CHARACTERISTICS

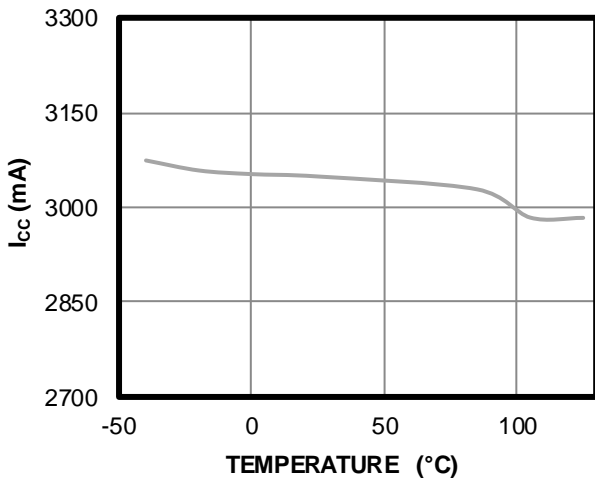
I_{BATT_LKG} @ BATT = 5V vs. Junction Temperature



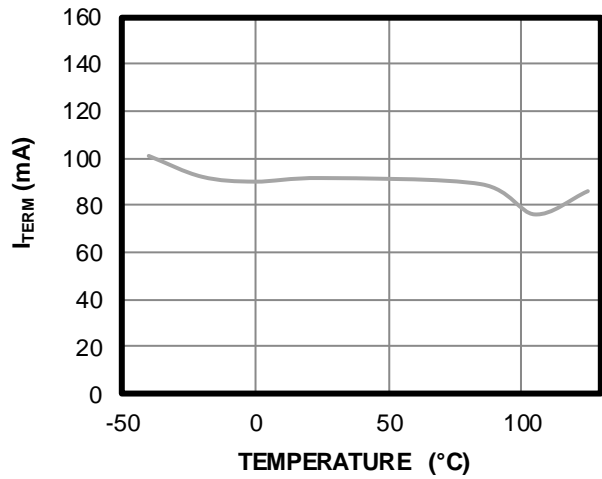
V_{BATT_REG} = 4.2V vs. Junction Temperature



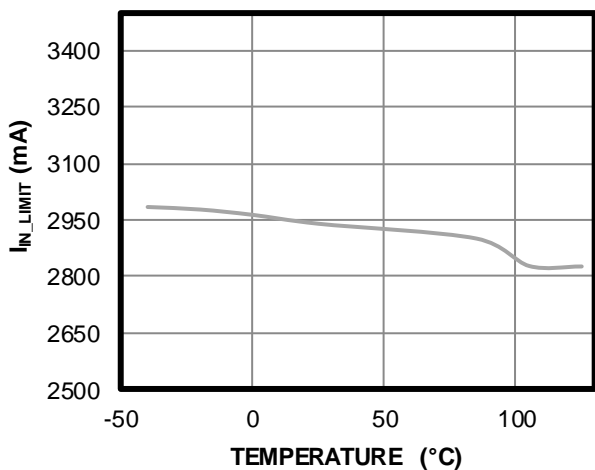
I_{CC} = 3A vs. Junction Temperature



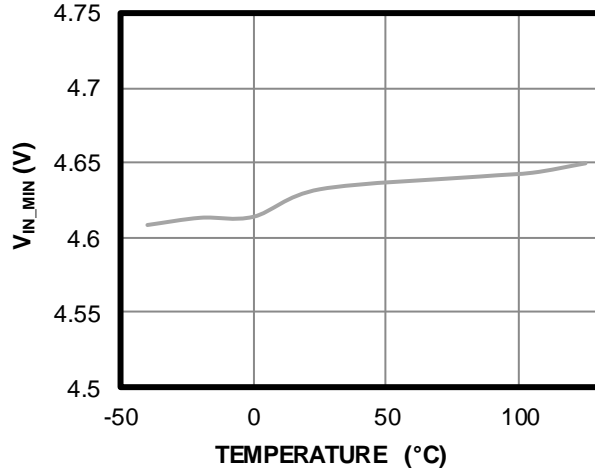
I_{TERM} = 100mA vs. Junction Temperature



I_{IN_LIMIT} = 3A vs. Junction Temperature

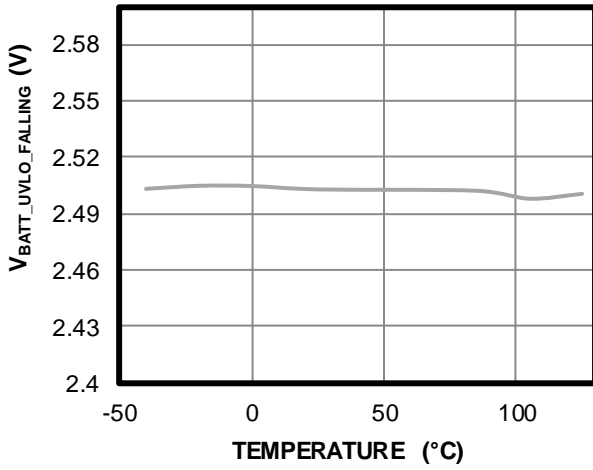


V_{IN_MIN} = 4.65V vs. Junction Temperature

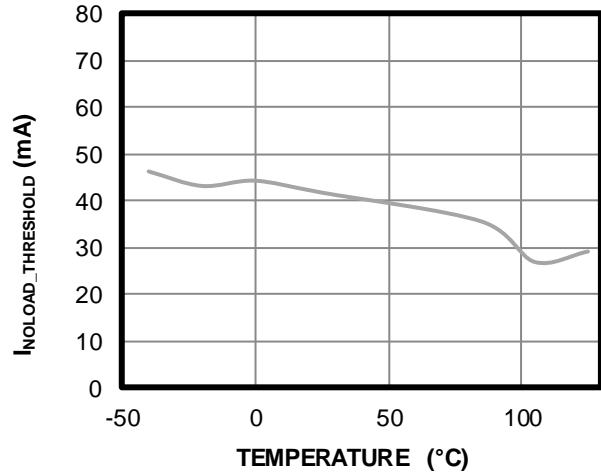


TYPICAL CHARACTERISTICS (continued)

V_{BATT_UVLO_Falling} vs. Junction Temperature



I_{NoLoad_Threshold = 30mA} vs. Junction Temperature

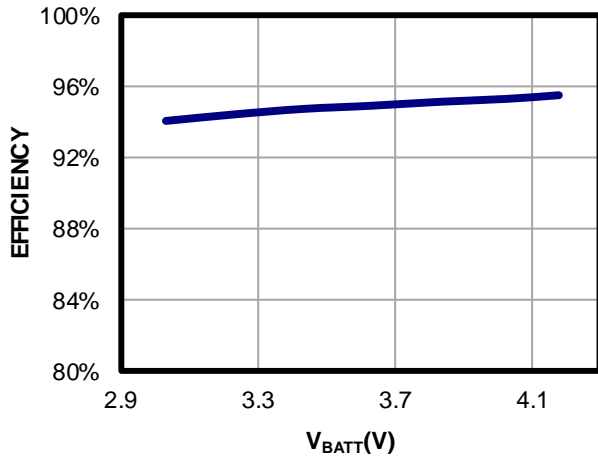


TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, battery simulator load, unless otherwise noted.

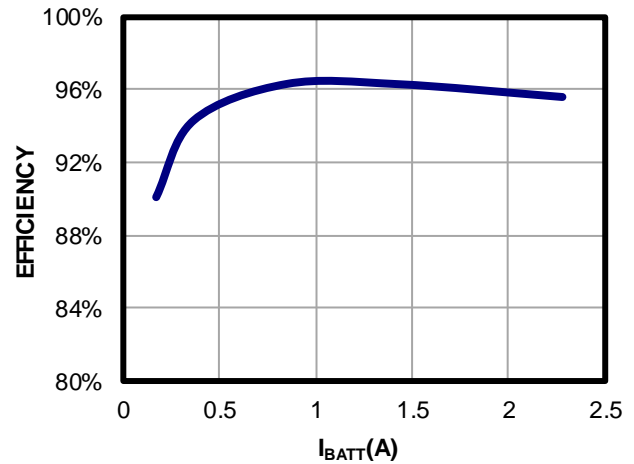
Constant Current Charge Efficiency

V_{IN} = 5V, I_{CHG} = 2.5A, DCR = 6.5mΩ



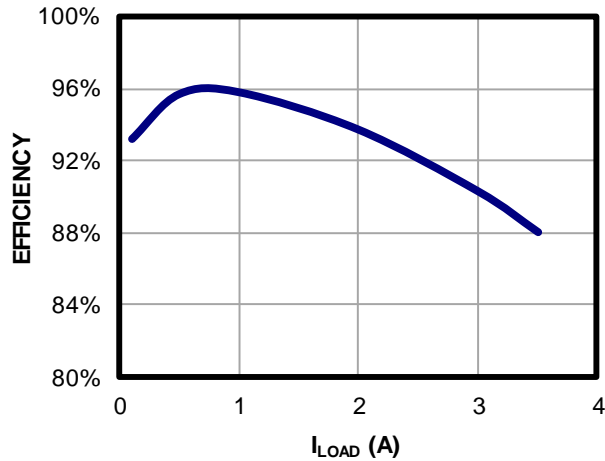
Constant Voltage Charge Efficiency

V_{IN} = 5V, V_{BATT} = 4.2V, DCR = 6.5mΩ



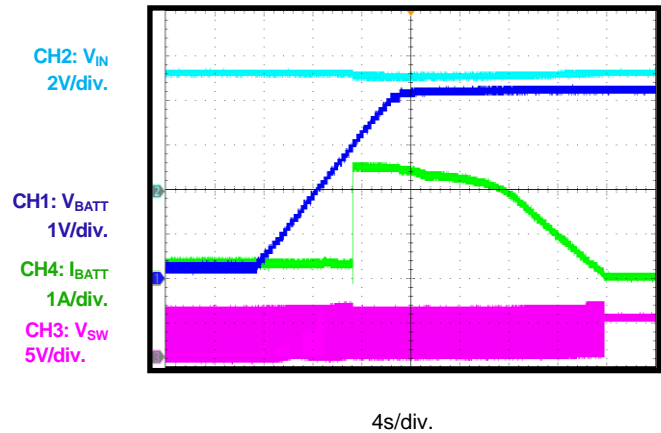
Boost Mode Efficiency

V_{BATT} = 3.5V, V_{sys} = 5.15V, DCR = 6.5mΩ



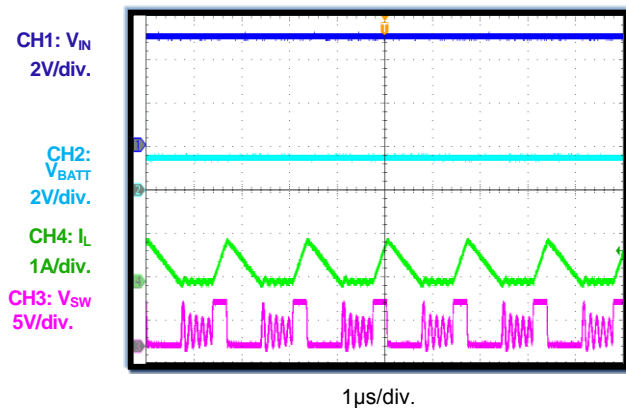
Battery Charge Curve

V_{IN} = 5V



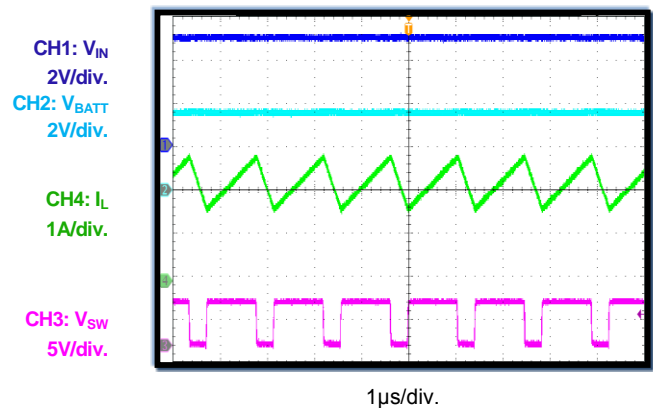
Pre-Charge Steady State

V_{IN} = 5V, V_{BATT} = 1.5V, I_{PRE} = 150mA



CC Charge Steady State

V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 2A

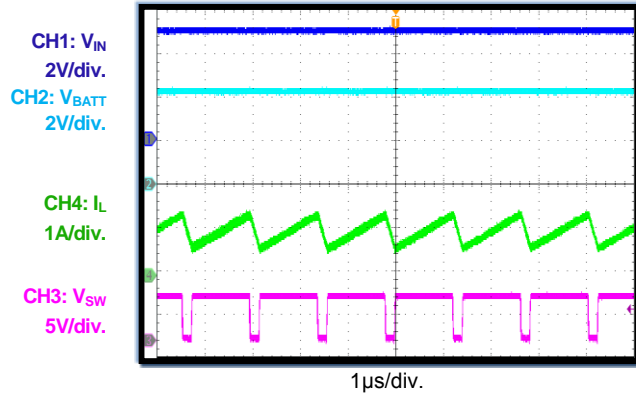


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = 25°C, battery simulator load, unless otherwise noted.

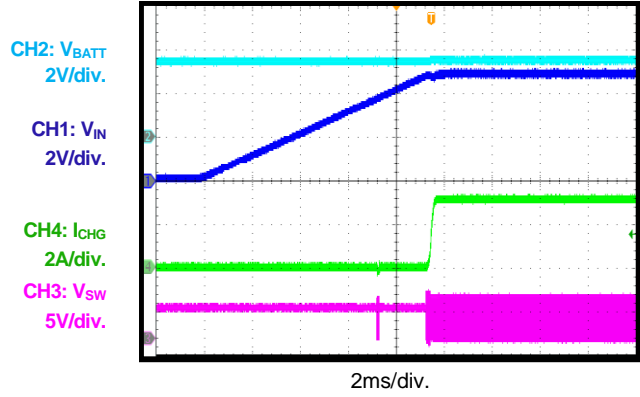
CV Charge Steady State

V_{IN} = 5V, V_{BATT} = 4.2V



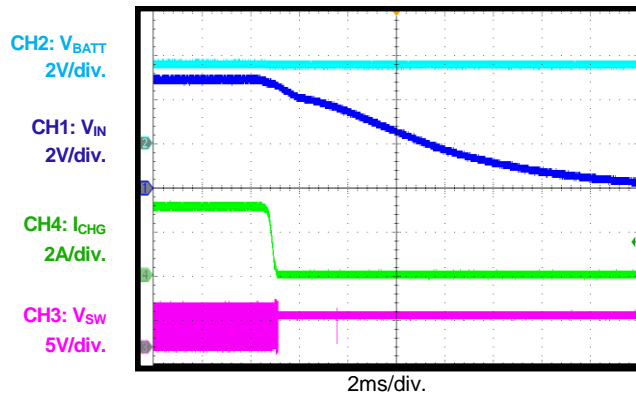
Power-On, CC Charge Mode

V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 3A



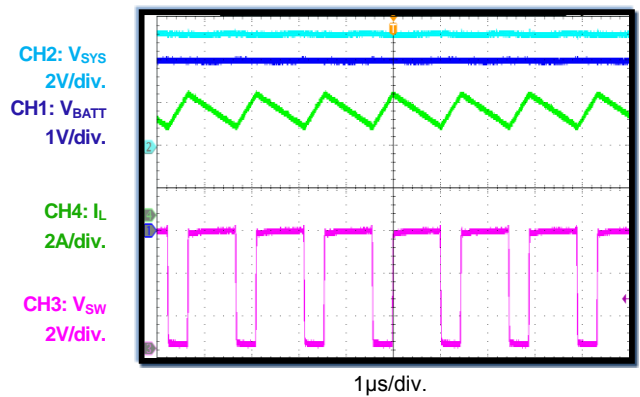
Power-Off, CC Charge Mode

V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 3A



Boost Steady State

V_{BATT} = 4V, I_{sys} = 3.5A



FUNCTIONAL BLOCK DIAGRAM

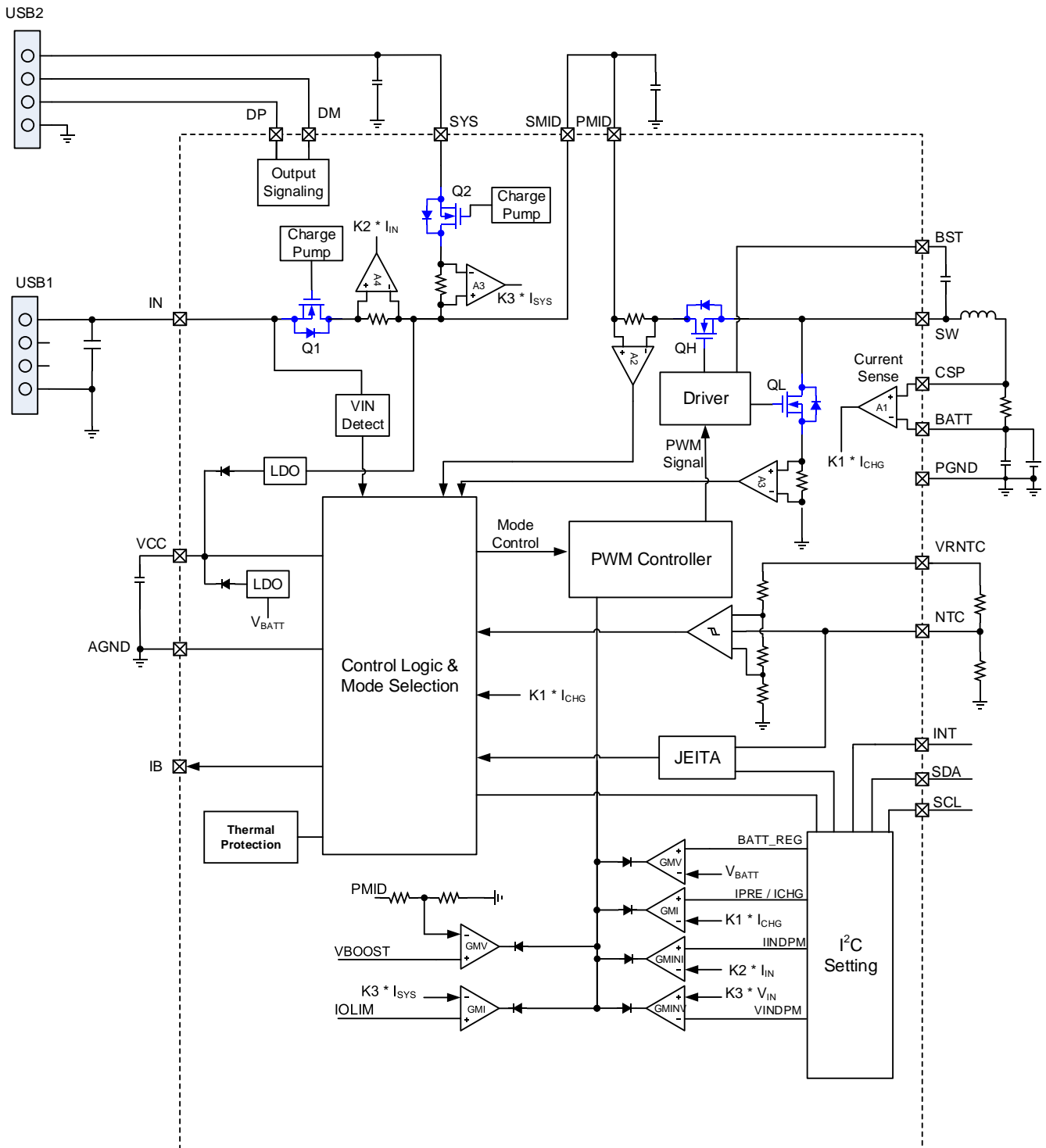


Figure 2: Functional Block Diagram

OPERATION

Introduction

The MP2696A is an I²C controlled switching charger with bidirectional operation that can step up the battery voltage to power the system. Depending on the input and output status, it operates in one of the three modes: charge mode, boost mode, or idle mode. In charge mode, the IC supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, the IC boosts the battery voltage to a regulated voltage at SYS for powering the load. In idle mode, the IC stops charging or boosting and operates at a low current from the input or the battery to reduce the power consumption when the IC is not operating.

VCC Power Supply

VCC provides power for the internal bias circuit, as well as the low-side switch driver. VCC is powered from whichever voltage is the highest between PMID and BATT. When the VCC voltage rises above the V_{VCC_UV} threshold, the I²C interface is ready for communication, and all the registers are reset to the default value. When the device is switching, VCC can provide up to 30mA for the external load.

CHARGER MODE OPERATION

Battery Charging Profile

The IC can run a charging cycle autonomously without host involvement. Also, the host can control the charge operations and parameters via the registers.

A new charge cycle can start when the following conditions are valid:

- V_{IN} is above V_{IN_UV}
- V_{IN} is below V_{IN_OV}
- V_{IN} is above V_{BATT} + V_{HDRM}
- The NTC voltage is in the proper range (if the NTC_STOP bit is set to 1)
- No charge timer fault
- Charging is enabled (CHG_EN=1)
- No battery over-voltage

After the charge is done, unplug and re-insert VIN or toggle the CHG_EN bit to start a new charge cycle.

Charge Cycle

The IC checks the battery voltage to provide three main charging phases: pre-charge, constant-current (CC) charge, and constant-voltage (CV) charge.

The IC regulates the voltage drop on the current-sensing resistor (RS1) for the battery pre-charge and constant-current charge current. Table 1 shows the default value for a 10mΩ resistor. The charge current can be scaled by implementing different current-sensing resistor values, calculated with Equation (1) and Equation (2):

$$I_{CC} = \frac{ICC[4:0] * 10m\Omega}{RS1} \quad (1)$$

$$I_{PRE} = \frac{IPRE[4:0] * 10m\Omega}{RS1} \quad (2)$$

Note that the soldering tin for the current-sensing resistor has resistance, which needs to be compensated.

Table 1: Charge Current vs. Battery Voltage (RS1 = 10mΩ)

Battery Voltage	Charge Current	Default Value	CHG_STAT
BATT < 3V	IPRE[1:0]	150mA	01
BATT > 3V	ICC[4:0]	3A	10

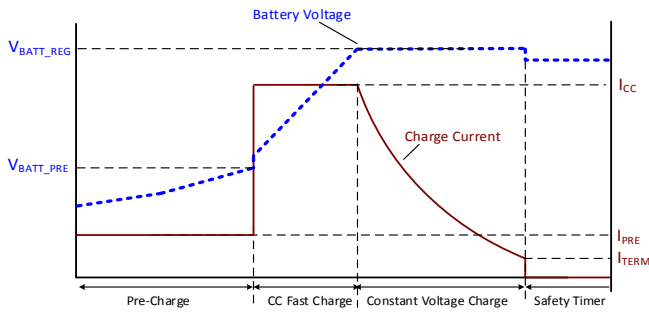
During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as the input current limit or the input voltage limit.

Charge Termination

Charging terminates if all the following conditions are met:

- The charge current is below the termination threshold for 20ms
- The IC works in a constant-voltage charge loop
- The IC is not in the input current loop or input voltage loop

After termination, the status register CHG_STAT is set to 11, and an INT pulse is generated.


Figure 3: Battery Charge Profile

Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged because of the system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold ($V_{BATT_REG} - 200mV$), the IC starts a new charging cycle automatically if the input power is valid. The timer resets when the auto-recharge cycle begins.

Safety Timer

The IC provides a safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer feature can be disabled via the I²C. The safety timer does not operate in boost mode.

The safety timer resets at the beginning of a new charging cycle. The following actions restart the safety timer:

- A new charge cycle starts
- The EN_TIMER bit is toggled
- Write 1 to the REG_RST bit

The IC can suspend the timer automatically when any fault occurs.

The timer is suspended if an NTC hot or cold fault is detected.

An INT pulse is generated if the safety timer expires before the charge is done, and the charge cycle stops.

Input Voltage Based and Input Current Based Power Management

The IC features both input current and input voltage based power management by monitoring the input current and input voltage continuously.

When the input current reaches the limit set by IINLIM[2:0], the charge current tapers off to keep the input current from increasing further.

If the preset input current limit is higher than the adapter rating, the backup input voltage based power management also works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation threshold set by VINMIN[2:0] due to the heavy load, the charge current is also reduced to keep the input voltage from dropping further.

An INT pulse is generated once the device enters a VINPPM or INPPM condition.

Thermistor Qualification

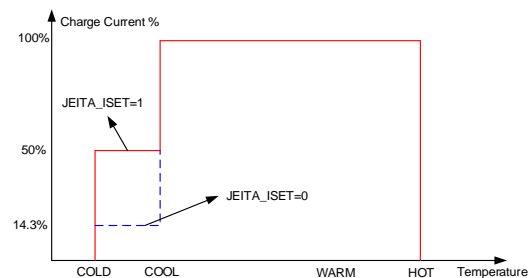
VRNTC is driven to be the same as the VCC voltage when the IC is in charge/boost mode. The IC monitors the battery's temperature continuously by measuring the voltage at the NTC pins. The NTC function can be disabled by setting EN_NTC=0.

When NTC_STOP is set to 1, the NTC voltage should be within the VHOT to VCOLD range for both charge and boost operation. The IC resumes switching when the NTC voltage returns to the VHOT to VCOLD range.

When NTC_STOP is set to 0, the IC only generates an interrupt signal and reports the NTC pin status if the NTC_FAULT[2:0] bits have any changes.

JEITA profile is supported when the JEITA_DIS bit is set to 0.

At a cool temperature (VCOLD to VCOOL) range, the charge current is reduced according to the JEITA_ISET[1:0] setting (see Figure 4).


Figure 4: JEITA Profile – Charge Current

At a warm temperature (V_{WARM} to V_{HOT}) range, the charge voltage is reduced according to the JEITA_VSET[1:0] setting (see Figure 5).

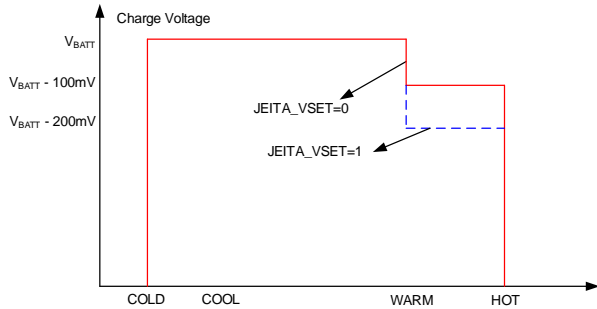


Figure 5: JEITA Profile – Charge Voltage

The HOT and COLD thresholds have two options in the register. The WARM and COOL thresholds have four options in the register, which offers accurate and flexible JEITA control.

Interrupt to Host (INT)

A 50µs interrupt pulse is generated on the open-drain INT pin when any of the events below occur:

- A good input source is detected
- A USB2 plug-in is detected
- Status register 05H changes
- Fault register 06H changes

Battery Over-Voltage Protection

When the battery voltage exceeds 104% of V_{BATT_REG}, the IC suspends charging immediately, the BATT_OVP bit is set to 1, and an INT is generated. An 800µA current source will discharge the battery until it returns to the normal range.

The battery over-voltage protection can be disabled by setting the BATT_OVP_DIS bit to 1.

Input Over-Voltage Protection

Once IN senses a voltage greater than the VIN_OVP threshold, the DC/DC converter stops immediately.

The input over-voltage protection threshold can be selected as 6V or 11V by the VIN_OVP bit.

BOOST MODE OPERATION

The IC is able to supply a regulated 5V output at SYS for powering the system. Boost will not start if BATT is below 2.9V to ensure that the battery is not drained. In order to enable boost mode, the IN voltage must be below 2.0V.

The boost output current limit can be programmed within a 2.1A to 3.6A range. Boost has an output current limit loop when V_{SYS} > V_{BATT}.

Once boost is enabled, the IC boosts PMID to the preset voltage first, and then the block FET Q2 turns on linearly. When V_{SYS} is charged higher than 4.2V within 3ms, Q2 turns fully on. Otherwise, Q2 turns off and tries to turn on again after 300ms.

Boost Power Limitation

During boost operation, the inductor peak current in each switching cycle is limited by the peak current limit of the low-side switch Q4 BST_IPK[1:0] bits. This helps limit the max battery discharge current.

Battery UVLO Protection

During boost operation, once the battery voltage drops below 2.5V, boost stops, and the BATT_UVLO bit is set to 1. Boost recovers when the battery voltage rises above 2.9V, but the BATT_UVLO bit is not reset until the input source plug-in and battery is charged again.

SYS Over-Current and Short Protection

In boost operation, the MP2696A always monitors the current flowing through Q2. When the SYS output current exceeds the preset boost output current limit, the output current loop takes control, and both the PMID and SYS voltages decrease. When V_{SYS} drops to V_{BATT} + 200mV, Q2 turns off. After 300ms, Q2 tries to restart.

The IC also features fast SYS over-current protection in both boost mode and pass-through mode. If the Q2 current exceeds 8A, Q2 turns off immediately. After 300ms, Q2 tries to restart.

Impedance Compensation for Boost Output

The IC allows the user to compensate the intrinsic resistance of Q2 and the USB2 output wire voltage drop by adjusting the boost output voltage according to the system load current, calculated with Equation (3):

$$V_{PMID} = V_{BOOST} + (I_{SYS} \times R_{SYS_CMP}) \quad (3)$$

Where V_{PMID} is the voltage at PMID, and V_{BOOST} is the boost regulation voltage set by VBOOST[2:0]. I_{SYS} is the real-time SYS load current during operation. R_{SYS_CMP} is the cable resistance compensation setting by R_{SYS_CMP}[2:0] in the register.

USB2 Plug-In Detection

In standby mode, if the USB2_EN_PLUG bit is enabled, SYS is pulled up to BATT. After the SYS voltage reaches 90% of the BATT voltage, detection starts. Once the system voltage drops to 75% of BATT, the USB2 plug-in is detected, the USB2_PLUG_IN bit is set to 1, and an INT pulse is generated.

The host needs to respond to the interrupt signal and enable boost/Q2.

The host needs to clear the USB2_PLUG_IN bit, and toggle the USB2_EN_PLUG bit for the next detection. Note that writing 1 to the USB2_PLUG_IN bit clears it to 0.

No Load Detection

During boost or pass-through operation, the Q2 current is monitored. If the Q2 current is smaller than NOLOAD_THR[1:0], the NO_LOAD bit is set to 1, and an INT pulse is generated. The host can monitor the NO_LOAD bit to decide whether boost/Q2 needs to be turned off.

Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and avoid overheating the chip. When the junction temperature reaches 150°C, the converter shuts down. When the junction temperature drops to 120°C, normal operation resumes.

Battery Current Analog Output

The IC has an IB pin to get the real-time battery current value in both charge and boost mode. The voltage at IB is a fraction of the battery current. It indicates the current flowing into and out of the battery during charge and boost mode.

Calculate for a 10mΩ current-sensing resistor using Equation (4) for charge mode, and Equation (5) for boost mode:

$$V_{IB} = I_{CHG} \times 0.35(V) \quad (4)$$

$$V_{IB} = I_{DSCHG} \times 0.16(V) \quad (5)$$

Note that scaling the current-sensing resistor also scales the gain of IB.

Idle Mode

When the input power source is not present and boost is disabled, the IC goes into idle mode. In idle mode, all the FETs and most of the internal

circuits are turned off to minimize leakage and extend the battery run time.

SYS DP/DM Signaling

Initially, the DP and DM pins are biased at 2.7V with an internal resistance of 30kΩ for non-standard adapter imitation.

In DCP mode, if the DP or DM pin is out of the 2.1V to 2.9V range for 10ms, the 2.7V reference is disconnected, and DP and DM are tied together with a 100Ω resistor.

If DP is less than 0.35V for 2 seconds in DCP mode, the IC returns to non-standard adapter mode with DP/DM biased at 2.7V.

Series Interface

The IC uses an I²C-compatible interface for flexible charging parameter setting and instantaneous device status reporting. I²C is a bidirectional, two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL).

The I²C interface supports both standard mode (up to 100kbs), and fast mode (up to 400kbs). Both SDA and SCL are bidirectional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. SDA and SCL are open-drain.

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred.

All transactions begin with a START (S) and can be terminated by a STOP (P). A high to low transition on the SDA line while SCL is high defines a START condition. A low to high transition on the SDA line when the SCL is high defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition. Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit

another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). The data transfer then continues when the slave is ready for another byte of data, and releases the clock line SCL.

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received; then another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low. It remains high during the ninth clock pulse; this is *not* the acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated start (S) to start a new transfer.

After the START, a slave address is sent. This address is 7 bits long followed by the eighth data direction bit (bit R/W). A 0 indicates a transmission (WRITE), and a 1 indicates a request for data (READ).

If the register address is not defined, the IC sends back a not acknowledge (NACK) signal, and returns to an idle state.

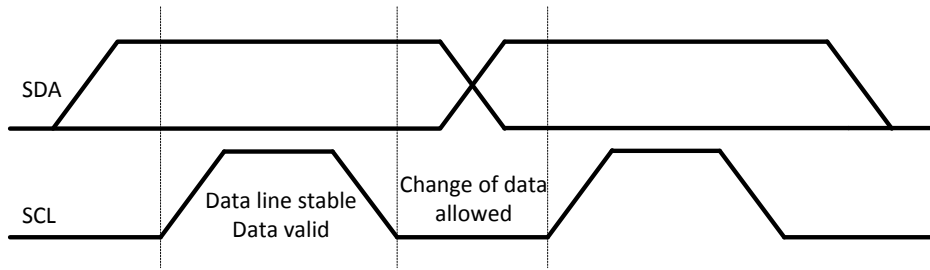


Figure 6: Bit Transfer on the I²C Bus

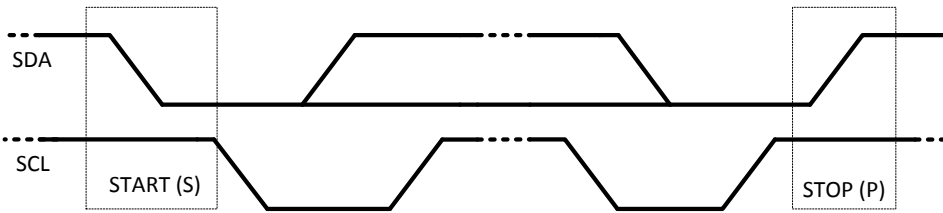


Figure 7: START and STOP Conditions

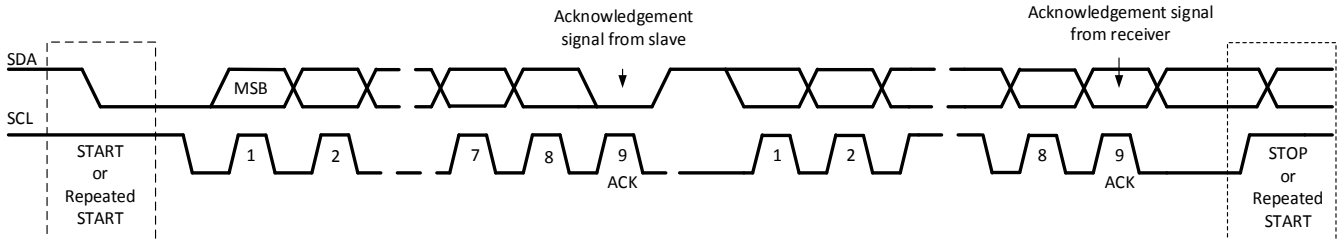


Figure 8: Data Transfer on the I²C BUS

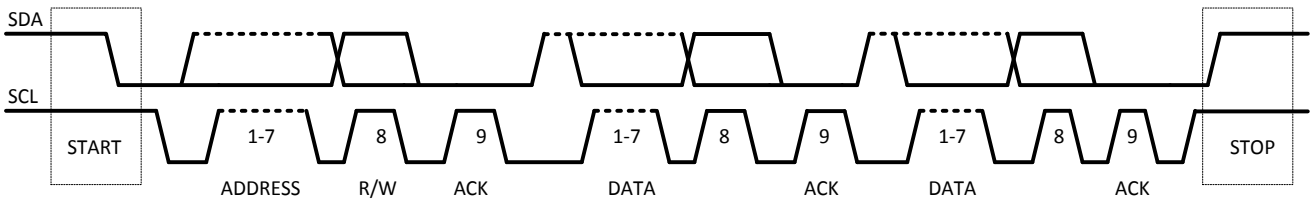


Figure 9: Complete Data Transfer

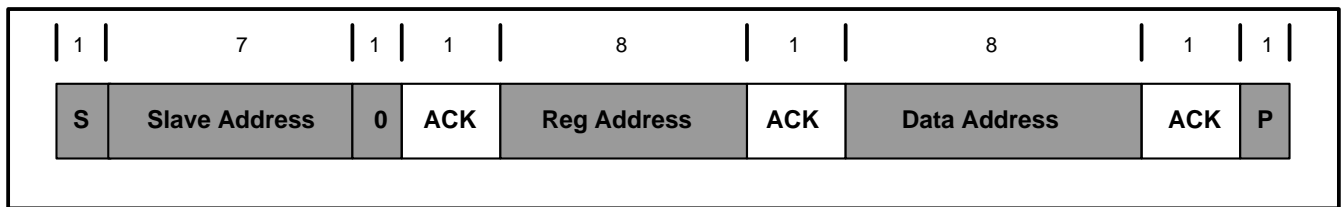


Figure 10: Single Write



Figure 11: Single Read

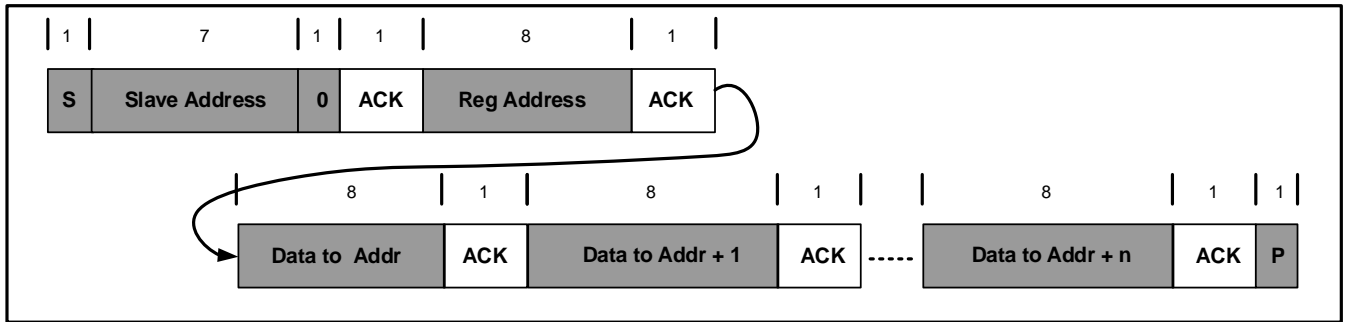


Figure 12: Multi-Write



Figure 13: Multi-Read

I²C REGISTER MAP

IC Address: 6BH

Register Name	Address	R/W	Description
REG00	0x00	R/W	Input voltage regulation setting and input current limit setting.
REG01	0x01	R/W	Charge current setting and pre-charge current setting.
REG02	0x02	R/W	Battery regulation voltage and termination current setting.
REG03	0x03	R/W	Boost output current limit setting and cable impedance compensation.
REG04	0x04	R/W	Boost output voltage setting and boost control.
REG05	0x05	R	Status register.
REG06	0x06	R	Fault register.
REG07	0x07	R/W	Boost no-load setting and miscellaneous control.
REG08	0x08	R/W	JEITA control.

REG 00H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	REG_RST	0	Y	R/W	0: Keep current setting 1: Reset	Reset all registers to default. After reset, this bit returns to 0 automatically.
6	EN_TIMER	1	Y	R/W	0: Disable 1: Enable	Charge safety timer control. Default: Enable
5	VINMIN[2]	1	Y	R/W	200mV	Input voltage dynamic regulation. Offset: 4.45V Range: 4.45V to 4.8V Default: 200mV (4.65V)
4	VINMIN[1]	0	Y	R/W	100mV	
3	VINMIN[0]	0	Y	R/W	50mV	
2	IINLIM[2]	0	Y	R/W	000: 100mA 001: 500mA 010: 1000mA	Input current limit. Default: 500mA
1	IINLIM[1]	0	Y	R/W	011: 1500mA 100: 1800mA 101: 2100mA	
0	IINLIM[0]	1	Y	R/W	110: 2400mA 111: 3000mA	

REG 01H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	ICC[4]	0	Y	R/W	1600mA	Charge current setting for a 10mΩ sensing resistor. Offset: 500mA Range: 500mA to 3.6A Default: 1A A scaling sensing resistor scales the setting as the same ratio.
6	ICC[3]	0	Y	R/W	800mA	
5	ICC[2]	1	Y	R/W	400mA	
4	ICC[1]	0	Y	R/W	200mA	
3	ICC[0]	1	Y	R/W	100mA	
2	EN_NTC	1	Y	R/W	0: Disable 1: Enable	Default: Enable
1	IPRE[1]	0	Y	R/W	01: 150mA 10: 250mA 11: 350mA	Pre-charge current setting for a 10mΩ sensing resistor. Range: 150mA to 350mA Default: 150mA
0	IPRE[0]	1	Y	R/W		

REG 02H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	BATT_OVP_DIS	0	Y	R/W	0: Enable battery OVP function 1: Disable battery OVP function	Default: Enable
6	BATT_REG[2]	0	Y	R/W	000: 3.6V 001: 4.1V 010: 4.2V 011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V	Charge voltage regulation. Default: 4.2V
5	BATT_REG[1]	1	Y	R/W		
4	BATT_REG[0]	0	Y	R/W		
3	JEITA_DIS	1	Y	R/W	0: JEITA enabled, NTC warm / cool decrease I _{CC} or V _{BATT_REG} 1: JEITA disabled, NTC warm / cool only report status and INT	Default: JEITA disabled
2	ITERM[1]	0	Y	R/W	200mA	Charge termination current for 10mΩ sensing resistor. Offset: 100mA Range: 100mA to 400mA Default: 100mA
1	ITERM[0]	0	Y	R/W	100mA	
0	CHG_EN	1	Y	R/W	0: Disable charge 1: Enable charge	Default: Enable charge

REG 03H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	IOLIM[1]	1	Y	R/W	800mA	SYS output current limit. Offset: 2.1A Range: 2.1A to 3.6A Default: 3.0A
6	IOLIM[0]	0	Y	R/W	400mA	
5	IOLIM[1]	0	Y	R/W	200mA	
4	IOLIM[0]	1	Y	R/W	100mA	
3	RSYS_CMP[2]	0	Y	R/W	80mΩ	SYS cable voltage drop compensation. Default: 60mΩ
2	RSYS_CMP[1]	1	Y	R/W	40mΩ	
1	RSYS_CMP[0]	1	Y	R/W	20mΩ	
0	NO_LOAD	0	Y	R	0: Q2 load normal 1: Q2 no load	

REG 04H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	VBOOST[2]	0	Y	R/W	-100mV	Boost regulation voltage at PMID pin. Offset: 5.2V Range: 5.05V to 5.225V Default: 5.15V
6	VBOOST[1]	1	Y	R/W	-50mV	
5	VBOOST[0]	0	Y	R/W	25mV	
4	BST_EN	0	Y	R/W	0: Disable boost 1: Enable boost	Default: Disable Boost can be enabled only when $V_{IN} < 2V$.
3	Q2_EN	0	Y	R/W	0: Q2 is off 1: Q2 is on	Default: Off
2	SYS_DSC	0	Y	R/W	0: Disable SYS discharge 1: Enable SYS discharge	SYS to GND discharge resistance 25Ω.
1	USB2_EN_PLUG	1	Y	R/W	0: Disable USB2 plug-in detection 1: Enable USB2 plug-in detection	Enables the USB2 plug-in detection circuit. Toggle this bit for new detection.
0	USB2_PLUG_IN	0	Y	R/W	0: USB2 is NOT plugged In 1: USB2 plug-in is detected	After SYS is pulled up to 90% of BATT, detection starts. Once SYS drops to 75% of BATT, the USB2 plug-in signal is asserted. Write 1 to reset this bit to 0. This bit should be cleared manually after read to enable the next detection.

REG 05H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	CHIP_STAT [1]	0	Y	R	00: Idle 01: Charge 10: Boost 11: Power path and charge	
6	CHIP_STAT [0]	0	Y	R		
5	CHG_STAT [1]	0	Y	R	00: Not charging 01: Pre-charge 10: CC or CV charge 11: Charge done	
4	CHG_STAT [0]	0	Y	R		
3	VPPM_STAT	0	Y	R	0: No VINPPM 1: VINPPM	
2	IPPM_STAT	0	Y	R	0: No IINPPM 1: IINPPM	
1	USB1_PLUG_IN	0	Y	R	0: USB1 is <i>not</i> plugged in 1: USB1 is plugged in	V _{IN} > 3.45V
0	Reserved	0	Y	R		

An interrupt is asserted when any bit of this REG changes.

REG 06H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	BATT_UVLO	0	Y	R	0: Battery <i>not</i> ULVO 1: Battery UVLO	If battery UVLO is touched, this bit is set to 1. Only when the battery is charged again, this bit will be reset to 0.
6	SYS_SHORT	0	Y	R	0: Normal 1: SYS short circuit	
5	BST_LMT	0	Y	R	0: Normal 1: Boost works in Q2 current limit	
4	CHG_FAULT [1]	0	Y	R	00: Normal 01: USB1 UV 10: USB1 OV 11: Safety timer expiration	
3	CHG_FAULT [0]	0	Y	R		
2	NTC_FAULT [2]	0	Y	R	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot	
1	NTC_FAULT [1]	0	Y	R		
0	NTC_FAULT [0]	0	Y	R		

An interrupt signal is asserted when any bit of this REG changes.

REG 07H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	NOLOAD_THR[1]	0	Y	R/W	00: 30mA 01: 50mA 10: 75mA 11: 100mA	SYS no load current threshold. Default: 30mA
6	NOLOAD_THR[0]	0	Y	R/W		
5	BATT_OVP	0	Y	R	0: Battery normal 1: Battery OVP	
4	NTC_STOP	1	Y	R/W	0: NTC out of window. Only report in register 1: NTC out of window. Suspend the charge and boost operation	
3	VIN_OVP	0	Y	R/W	0: VIN_OVP = 6V 1: VIN_OVP = 11V	
2	SW_FREQ	0	Y	R/W	0: 700kHz 1: 1200kHz	Default: 700kHz
1	BST_IPK[1]	1	Y	R/W	00: 5A 01: 5.5A 10: 6A 11: 6.5A	Low-side switch peak current limit in boost mode. Default: 6.5A
0	BST_IPK[0]	1	Y	R/W		

REG 08H

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	JEITA_VSET	1	Y	R/W	0: V _{BATT_REG} - 100mV 1: V _{BATT_REG} - 200mV	Default: V _{BATTFULL} - 200mV
6	JEITA_ISET	1	Y	R/W	0: 14.3% of I _{CC} 1: 50% of I _{CC}	Default: 50% of I _{CC}
5	VHOT	1	Y	R/W	0: 34% 1: 36%	Hot threshold setting. Default: 36%
4	VWARM[1]	0	Y	R/W	00: 44% 01: 40%	Warm threshold setting. Default: 40%
3	VWARM[0]	1	Y	R/W	10: 38% 11: 36%	
2	VCOOL[1]	1	Y	R/W	00: 72% 01: 68%	Cool threshold setting. Default: 60%
1	VCOOL[0]	1	Y	R/W	10: 64% 11: 60%	
0	VCOLD	0	Y	R/W	0: 72% 1: 68%	Cold threshold setting. Default: 72% (0)

REG 0AH ⁽⁸⁾

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	TMR	0	N/A	N/A	0: Charge timer is 20hrs 1: Charge timer is 10hrs	Default: 0
6	Reserved	N/A	N/A	N/A	N/A	
5	Reserved	N/A	N/A	N/A	N/A	
4	Reserved	N/A	N/A	N/A	N/A	
3	VPRE	0	N/A	N/A	0: Pre-charge threshold is 3V 1: Pre-charge threshold is 2.5V	Default: 0
2	Reserved	N/A	N/A	N/A	N/A	
1	Reserved	N/A	N/A	N/A	N/A	
0	Reserved	N/A	N/A	N/A	N/A	

Note:

8) Register 0AH is for OTP only and is not accessible to users.

OTP MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	N/A	BATT_REG: 3.6V to 4.45V			N/A	N/A	N/A	N/A
0x07	NOLOAD_THR		N/A	NTC_STOP	VIN_OVP	N/A	N/A	N/A
0x0A	TMR	N/A	N/A	N/A	VPRE	N/A	N/A	N/A

OTP DEFAULT

OTP Items	Default
BATT_REG[2:0]	4.2V
NOLOAD_THR[1:0]	30mA
NTC_STOP	1: NTC out of window. Suspend the charge and boost operation
VIN_OVP	0: VIN_OVP = 6V
TMR	0: Charge timer is 20hrs
VPRE	0: Pre-charge threshold is 3V

APPLICATION INFORMATION

NTC Function

JEITA profile is supported for battery temperature management. For a given NTC thermistor, select an appropriate R_{T1} and R_{T2} to set the NTC window, using Equation (6) and Equation (7):

$$R_{T1} = \frac{R_{NTC_HOT} \times R_{NTC_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC_COLD} - R_{NTC_HOT})} \quad (6)$$

$$R_{T2} = \frac{R_{NTC_HOT} \times R_{NTC_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC_HOT}} \quad (7)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the upper bound of its operating temperature range, and R_{NTC_COLD} is its lower bound. V_{HOT} is the hot temperature threshold percentage, which can be selected as 34% or 36%. V_{COLD} is the cold temperature threshold percentage, which can be selected as 72% or 68%.

The warm and cool temperature thresholds can be calculated with Equation (8) and Equation (9):

$$V_{WARM} = \frac{R_{T2} // R_{NTC_WARM}}{R_{T1} + R_{T2} // R_{NTC_WARM}} \quad (8)$$

$$V_{COOL} = \frac{R_{T2} // R_{NTC_COOL}}{R_{T1} + R_{T2} // R_{NTC_COOL}} \quad (9)$$

Choose the nearest warm/cool threshold in REG08H using the results from the calculations above.

If no external NTC is available, connect R_{T1} and R_{T2} to keep the voltage on NTC within the valid NTC window (e.g. $R_{T1} = R_{T2} = 10k\Omega$).

Selecting the Inductor

Inductor selection requires a tradeoff between cost, size, and efficiency. A lower inductance value means a smaller size, but results in greater current ripple, greater magnetic hysteretic losses, and greater output capacitance. A higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in greater inductor DC resistance (DCR) loss.

Table 2 shows recommended values with which to choose an inductor.

Table 2: Inductance Selection Guide

RS1 (mΩ)	Max I _{CC} (A)	L (μH)
10	3.6	1
20	1.8	2.2
30	1.2	3.3
50	0.72	4.7

Choose an inductor that does not saturate under the worst-case load condition.

Selecting the PMID Capacitor (C_{PMID})

Select C_{PMID} based on the demand of the PMID current ripple for the mode being used.

In charge mode, C_{PMID} acts as the input capacitor of the buck converter in charge mode. The input current ripple is calculated using Equation (10):

$$I_{RMS_MAX} = I_{CC_MAX} \times \frac{\sqrt{V_{BATT} \times (V_{IN} - V_{BATT})}}{V_{IN}} \quad (10)$$

In boost mode, C_{PMID} is the output capacitor of the boost converter. C_{PMID} keeps the system voltage ripple small and ensures feedback loop stability. The system current ripple is calculated using Equation (11):

$$I_{RMS_MAX} = I_{BATT} \times \frac{\sqrt{V_{BATT} \times (V_{SYS} - V_{BATT})}}{V_{SYS}} \quad (11)$$

Select the PMID capacitors based on the ripple current temperature rise, not exceeding 10°C. For best results, use ceramic capacitors with X5R dielectrics because of their low ESR and small temperature coefficients.

PCB Layout Guidelines

Efficient PCB layout is critical to meet specified noise, efficiency, and stability requirements. For the best results, follow the guidelines below:

1. Place the PMID capacitor as close as possible to PMID and PGND. The PMID capacitor should have a return to the IC's PMID and PGND pins that is as short as possible.
2. Connect AGND to the ground of the PMID capacitor.
3. Keep the switching node short.
4. The power pads for VIN, PMID, SYS, and PGND should be connected to as many coppers planes on the board as possible to improve thermal performance by conducting heat to the PCB.

Compensate the Current-Sensing Resistor

The soldering tin has resistance. For a 10mΩ resistor soldered on the PCB, the total resistance between resistor pads is about 11mΩ to 12mΩ.

One compensation method is to apply a resistor divider for the CSP/BATT pins (see Figure 14).

After the PCB is assembled, apply a 2A DC current source between SW and BATT, measure the voltage drop across the current-sensing resistor on its PCB pads, which is V_{CS} , and then R_1 can be calculated using Equation (12):

$$R_1 = \frac{V_{CS} - 2 \times RS1}{2 \times RS1} \times 10\Omega \quad (12)$$

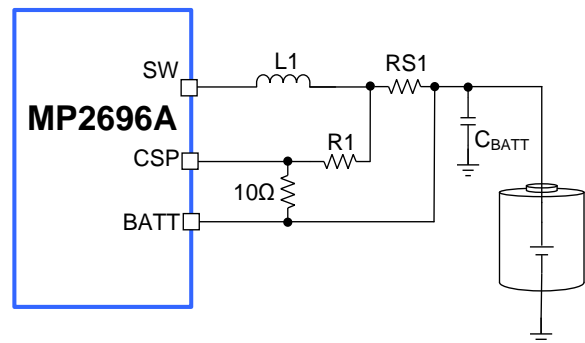


Figure 14: Current-Sensing Compensation

TYPICAL APPLICATION CIRCUITS

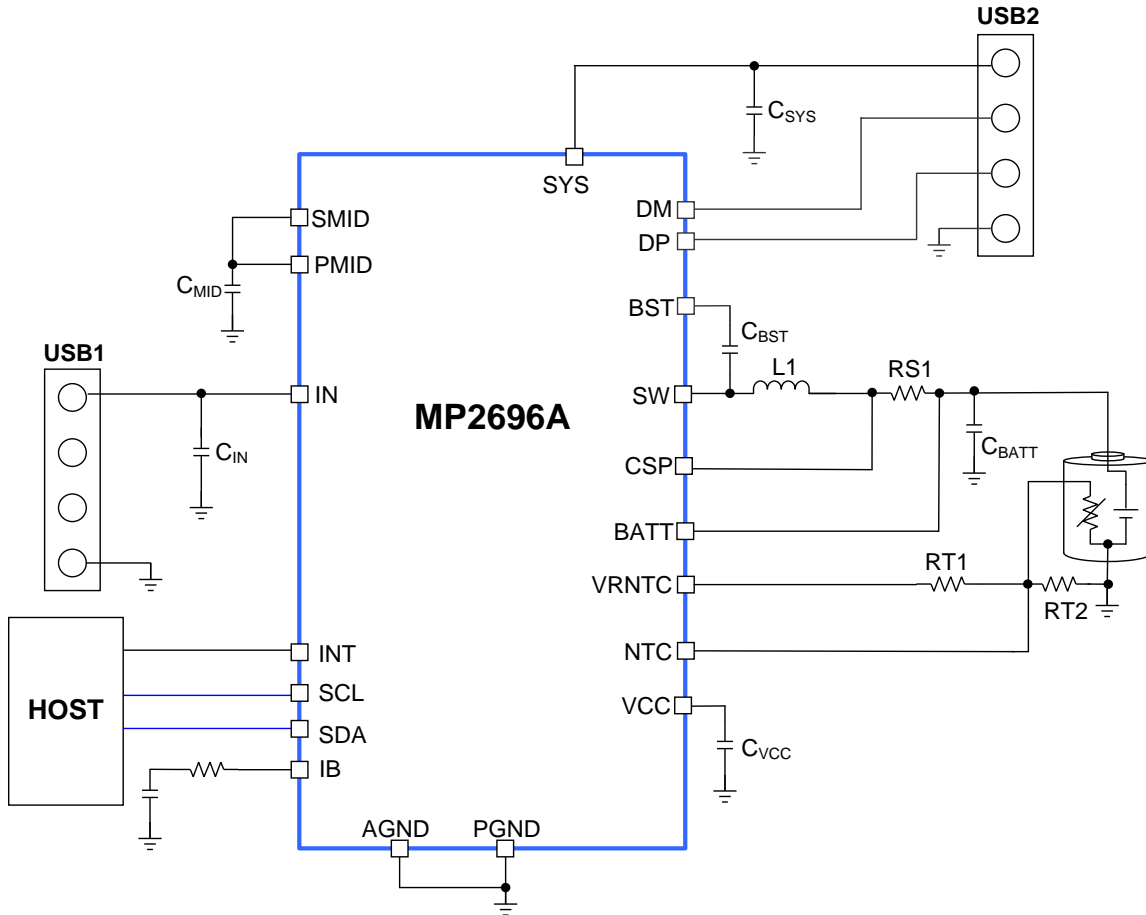


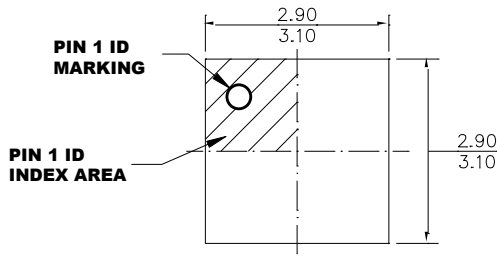
Figure 15: Typical Application Circuit for Power Bank

Table 3: Key BOM for Figure 15

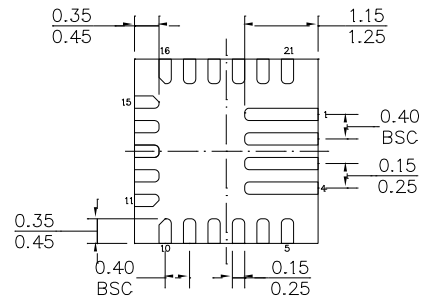
Qty	Ref	Value	Description	Package	Manufacture
1	C _{IN}	1µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C _{MID}	10µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
2	C _{SYS}	10µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C _{BATT}	22µF	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C _{VCC}	2.2µF	Ceramic capacitor, 6.3V, X5R or X7R	0603	Any
1	C _{BST}	470nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	1µH	Inductor, 1µH, low DCR	SMD	Any
1	RS1	10mΩ	Film resistor, 1%	1206	Any

PACKAGE INFORMATION

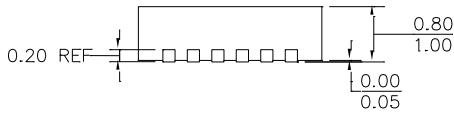
QFN-21 (3mmx3mm)



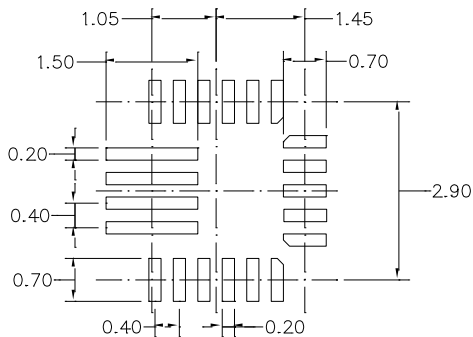
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.02	07/20/2020	Correct IB pin I/O description	P5
		Add comment in PMID pin description for not carrying current	

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.