Product Change Notification - SYST-12OVPV786

Date:

14 May 2020

Product Category:

32-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - SAM C20/C21 Family Silicon Errata Document Revision

Notification text:

SYST-12OVPV786
Microchip has released a new Product Documents for the SAM C20/C21 Family Silicon Errata of devices. If you are using one of these devices please read the document located at SAM C20/C21 Family Silicon Errata.

Notification Status: Final

Description of Change:
The following Data Sheet Clarifications were added in this revision:
1) Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics for SAM C20/C21 E/G/J at 85degC
2) Power Consumption for SAM C20/C21 N at 105degC - IDLE0
3) Analog-to-Digital Converter (ADC) Characteristics for SAM C20/C21 N at 105degC
4) Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics for SAM C20/C21 N at 105degC
5) Current Consumption - IDLE0 for SAM C20/C21 E/G/J AEC-Q100 Grade 1 at 125deg

Added the following silicon issues:
1) 1.8.13 Potential hard fault on standby entry
2) 1.17.14 Over consumption in standby

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 14 May 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

SAM C20/C21 Family Silicon Errata

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

ATSAMC21E16A-AZTVAO
ATSAMC21E16A-MNT
ATSAMC21E16A-MUT
ATSAMC21E16A-MUTDY
ATSAMC21E16A-MZ
ATSAMC21E16A-MZT
ATSAMC21E16A-MZTVAO
ATSAMC21E17A-ANT
ATSAMC21E17A-AUT
ATSAMC21E17A-AZ
ATSAMC21E17A-AZT
ATSAMC21E17A-MNT
ATSAMC21E17A-MUT
ATSAMC21E17A-MZ
ATSAMC21E17A-MZT
ATSAMC21E17A-MZTV07
ATSAMC21E17A-MZTVAO
ATSAMC21E18A-ANT
ATSAMC21E18A-AUT
ATSAMC21E18A-AZ
ATSAMC21E18A-AZT
ATSAMC21E18A-AZTVAO
ATSAMC21E18A-MNT
ATSAMC21E18A-MNTDY
ATSAMC21E18A-MUT
ATSAMC21E18A-MUTDY
ATSAMC21E18A-MZ
ATSAMC21E18A-MZT
ATSAMC21E18A-MZTV02
ATSAMC21E18A-MZTV05
ATSAMC21E18A-MZTVAO
ATSAMC21G15A-ANT
ATSAMC21G15A-AUT
ATSAMC21G15A-AZ
ATSAMC21G15A-AZT
ATSAMC21G15A-MNT
ATSAMC21G15A-MUT
ATSAMC21G15A-MZ
ATSAMC21G15A-MZT
ATSAMC21G16A-ANT
ATSAMC21G16A-AUT
ATSAMC21G16A-AZ
ATSAMC21G16A-AZT
ATSAMC21G16A-MNT
ATSAMC21G16A-MUT
ATSAMC21G16A-MZ

ATSAMC21G16A-MZT
ATSAMC21G16A-MZTVAO
ATSAMC21G17A-ANT
ATSAMC21G17A-AUT
ATSAMC21G17A-AZ
ATSAMC21G17A-AZT
ATSAMC21G17A-MNT
ATSAMC21G17A-MU
ATSAMC21G17A-MUT
ATSAMC21G17A-MZ
ATSAMC21G17A-MZT
ATSAMC21G17A-MZTV08
ATSAMC21G17A-MZTVAO
ATSAMC21G18A-ANT
ATSAMC21G18A-AUT
ATSAMC21G18A-AZ
ATSAMC21G18A-AZT
ATSAMC21G18A-MNT
ATSAMC21G18A-MUT
ATSAMC21G18A-MZ
ATSAMC21G18A-MZT
ATSAMC21G18A-MZTVAO
ATSAMC21J15A-ANT
ATSAMC21J15A-AUT
ATSAMC21J15A-AZ
ATSAMC21J15A-AZT
ATSAMC21J15A-MNT
ATSAMC21J15A-MUT
ATSAMC21J15A-MZ
ATSAMC21J15A-MZT
ATSAMC21J15A-MZTVAO
ATSAMC21J16A-ANT
ATSAMC21J16A-AUT
ATSAMC21J16A-AZ
ATSAMC21J16A-AZT
ATSAMC21J16A-AZTVAO
ATSAMC21J16A-AZVAO
ATSAMC21J16A-MNT
ATSAMC21J16A-MUT
ATSAMC21J16A-MZ
ATSAMC21J16A-MZT
ATSAMC21J16A-MZTV03
ATSAMC21J16A-MZTVAO
ATSAMC21J17A-ANT
ATSAMC21J17A-AUT
ATSAMC21J17A-AZ
ATSAMC21J17A-AZT
ATSAMC21J17A-AZTV06
ATSAMC21J17A-AZTVAO

ATSAMC21J17A-MNT
ATSAMC21J17A-MUT
ATSAMC21J17A-MUTB2
ATSAMC21J17A-MUTN02
ATSAMC21J17A-MZ
ATSAMC21J17A-MZT
ATSAMC21J17A-MZTV04
ATSAMC21J17A-MZTVAO
ATSAMC21J17A-UUT
ATSAMC21J18A-ANT
ATSAMC21J18A-AUT
ATSAMC21J18A-AZ
ATSAMC21J18A-AZT
ATSAMC21J18A-AZTVAO
ATSAMC21J18A-MNT
ATSAMC21J18A-MUT
ATSAMC21J18A-MZ
ATSAMC21J18A-MZT
ATSAMC21J18A-MZTVAO
ATSAMC21J18A-UUT
ATSAMC21N-XPRO
ATSAMC21N17A-AN
ATSAMC21N17A-ANT
ATSAMC21N18A-AN
ATSAMC21N18A-ANT
ATSAMC20E15A-ANT
ATSAMC20E15A-AUT
ATSAMC20E15A-AZ
ATSAMC20E15A-AZT
ATSAMC20E15A-MNT
ATSAMC20E15A-MUT
ATSAMC20E15A-MZ
ATSAMC20E15A-MZT
ATSAMC20E16A-ANT
ATSAMC20E16A-AUT
ATSAMC20E16A-AZ
ATSAMC20E16A-AZT
ATSAMC20E16A-MNT
ATSAMC20E16A-MUT
ATSAMC20E16A-MZ
ATSAMC20E16A-MZT
ATSAMC20E17A-ANT
ATSAMC20E17A-AUT
ATSAMC20E17A-AZ
ATSAMC20E17A-AZT
ATSAMC20E17A-MNT
ATSAMC20E17A-MUT
ATSAMC20E17A-MZ
ATSAMC20E17A-MZT

ATSAMC20E17A-MZTVAO
ATSAMC20E18A-ANT
ATSAMC20E18A-AUT
ATSAMC20E18A-AZ
ATSAMC20E18A-AZT
ATSAMC20E18A-MNT
ATSAMC20E18A-MUT
ATSAMC20E18A-MZ
ATSAMC20E18A-MZT
ATSAMC20G15A-ANT
ATSAMC20G15A-AUT
ATSAMC20G15A-AZ
ATSAMC20G15A-AZT
ATSAMC20G15A-MNT
ATSAMC20G15A-MUT
ATSAMC20G15A-MZ
ATSAMC20G15A-MZT
ATSAMC20G16A-ANT
ATSAMC20G16A-AUN01
ATSAMC20G16A-AUT
ATSAMC20G16A-AZ
ATSAMC20G16A-AZT
ATSAMC20G16A-MNT
ATSAMC20G16A-MUT
ATSAMC20G16A-MZ
ATSAMC20G16A-MZT
ATSAMC20G17A-ANT
ATSAMC20G17A-AUT
ATSAMC20G17A-AZ
ATSAMC20G17A-AZT
ATSAMC20G17A-MNT
ATSAMC20G17A-MUT
ATSAMC20G17A-MZ
ATSAMC20G17A-MZT
ATSAMC20G18A-ANT
ATSAMC20G18A-AUT
ATSAMC20G18A-AZ
ATSAMC20G18A-AZT
ATSAMC20G18A-MNT
ATSAMC20G18A-MUT
ATSAMC20G18A-MZ
ATSAMC20G18A-MZT
ATSAMC20J15A-ANT
ATSAMC20J15A-AUT
ATSAMC20J15A-AZ
ATSAMC20J15A-AZT
ATSAMC20J15A-MNT
ATSAMC20J15A-MUT
ATSAMC20J15A-MZ

ATSAMC20J15A-MZT
ATSAMC20J16A-ANT
ATSAMC20J16A-AUT
ATSAMC20J16A-AZ
ATSAMC20J16A-AZT
ATSAMC20J16A-AZTVAO
ATSAMC20J16A-MNT
ATSAMC20J16A-MUT
ATSAMC20J16A-MZ
ATSAMC20J16A-MZT
ATSAMC20J16A-MZTVAO
ATSAMC20J17A-ANT
ATSAMC20J17A-AUT
ATSAMC20J17A-AZ
ATSAMC20J17A-AZT
ATSAMC20J17A-MNT
ATSAMC20J17A-MUT
ATSAMC20J17A-MZ
ATSAMC20J17A-MZT
ATSAMC20J17A-UUT
ATSAMC20J18A-ANT
ATSAMC20J18A-AUT
ATSAMC20J18A-AZ
ATSAMC20J18A-AZT
ATSAMC20J18A-MNT
ATSAMC20J18A-MUT
ATSAMC20J18A-MZ
ATSAMC20J18A-MZT
ATSAMC20J18A-UUT
ATSAMC20N17A-ANT
ATSAMC20N18A-ANT
ATSAMC21E15A-ANT
ATSAMC21E15A-AUT
ATSAMC21E15A-AZ
ATSAMC21E15A-AZT
ATSAMC21E15A-AZTVAO
ATSAMC21E15A-MNT
ATSAMC21E15A-MUT
ATSAMC21E15A-MUTDY
ATSAMC21E15A-MZ
ATSAMC21E15A-MZT
ATSAMC21E15A-MZTVAO
ATSAMC21E15A-MZVAO
ATSAMC21E16A-ANT
ATSAMC21E16A-AUT
ATSAMC21E16A-AZ
ATSAMC21E16A-AZT

MICROCHIP

SAM C20/C21

SAM C20/C21 Family Silicon Errata and Data Sheet Clarification

SAM C20/C21 Family

The SAM C20/C21 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001479D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 and Table 2.

The errata described in this document will be addressed in future revisions of the SAM C20/C21 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 2. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM C20 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])				
		B	C	D	E	F
ATSAMC20E15A	0x1100xx0D	0x1	0x2	0x3	0x4	0x5
ATSAMC20E16A	0x1100xx0C					
ATSAMC20E17A	0x1100xx0B					
ATSAMC20E18A	0x1100xx0A					
ATSAMC20G15A	0x1100xx08					
ATSAMC20G16A	0x1100xx07					
ATSAMC20G17A	0x1100xx06					
ATSAMC20G18A	0x1100xx05					
ATSAMC20J15A	0x1100xx03					
ATSAMC20J16A	0x1100xx02					
ATSAMC20J17A	0x1100xx01					
ATSAMC20J18A	0x1100xx00					
ATSAMC20N17A	0x1100xx21	N/A	N/A	N/A	0x4	N/A
ATSAMC20N18A	0x1100xx20					

Table 2. SAM C21 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])				
		B	C	D	E	F
ATSAMC21E15A	0x1101xx0D	0x1	0x2	0x3	0x4	0x5
ATSAMC21E16A	0x1101xx0C					
ATSAMC21E17A	0x1101xx0B					
ATSAMC21E18A	0x1101xx0A					
ATSAMC21G15A	0x1101xx08					
ATSAMC21G16A	0x1101xx07					
ATSAMC21G17A	0x1101xx06					
ATSAMC21G18A	0x1101xx05					
ATSAMC21J15A	0x1101xx03					
ATSAMC21J16A	0x1101xx02					
ATSAMC21J17A	0x1101xx01					
ATSAMC21J18A	0x1101xx00					
ATSAMC21N17A	0x1101xx21	N/A	N/A	N/A	0x4	N/A
ATSAMC21N18A	0x1101xx20					

Note:

1. Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001479D) for detailed information on Device Identification and Revision IDs for your specific device.

Silicon Errata Summary

Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
OSC32KCTRL	Clock Failure Detection	1.1.1	At start-up and in case of clock failure detection (CFD), the auto switch by the CFD does not work if XOSC32K is requested by the GCLK.	E/G/J	X				
				N					
OSC48M	System Reset	1.2.1	When a System Reset is applied, the OSC48MDIV register is reset, but the value is not synchronized.	E/G/J	X				
				N					
OSC48M	Division Ratio	1.2.2	Changing the division ratio (OSC48MDIV) while the OSC48M is running but not requested by any generic clock generator (GCLK_GEN) makes the OSC48DIV bit in the OSC48MSYNCBUSY register to remain always set.	E/G/J	X	X	X	X	X
				N				X	

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Module	**Feature**	**Errata Number**	**Issue Summary**	**C20/C21 Device**	**Affected Revisions**				
					B	**C**	**D**	**E**	**F**
FDPLL	Standby Mode	1.3.1	When entering Standby mode, the FDPLL is still running even if not requested by any module causing extra consumption.	E/G/J	X				
				N					
FDPLL	Clocking Accuracy	1.3.2	The FDPLL96M exhibits high period jitter and is not suitable for accurate clocking.	E/G/J	X	X			
				N					
FDPLL	Ratio Value	1.3.3	When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.	E/G/J	X	X	X	X	X
				N				X	
FDPLL	FDPLL Loop Divider Ratio	1.3.4	Changing the FDPLL Loop Divider Ratio on-the-fly does not work if the GCLK_DPLL_32K is not available.	E/G/J	X	X	X	X	X
				N				X	
ADC	Software Trigger	1.4.1	Once set, the ADC.SWTRIG.START will not be cleared until the microcontroller is reset.	E/G/J	X				
				N					
ADC	Least Significant Byte Result	1.4.2	The LSB of ADC result is stuck at zero in unipolar mode for 8-bit and 10-bit resolution.	E/G/J	X				
				N					
ADC	Window Monitor	1.4.3	When the window monitor is enabled and its output is '0', the ADC GCLK is kept running.	E/G/J	X				
				N					
ADC	Synchronized Event	1.4.4	If a synchronized event is received during an ADC conversion, the ADC will not acknowledge the event,causing a stall of the event channel.	E/G/J	X	X	X	X	X
				N					
ADC	Software Trigger Sync Busy Status	1.4.5	ADC SYNCBUSY.SWTRIG becomes stuck to one after wake-up from Standby Sleep mode.	E/G/J	X	X	X	X	X
				N				X	
ADC	Reference Buffer Offset Compensation	1.4.6	TUE of the ADC conversion result is out of specification.	E/G/J	X	X	X	X	X
				N				X	
ADC	Differential and Single-Ended Mode	1.4.7	Electrical characteristics for differential mode and Single-Ended mode do not meet the published specification in the product data sheet.	E/G/J	X	X	X	X	
				N					
ADC	Power Consumption	1.4.8	Power consumption for the ADC does not meet the published specification in the product data sheet.	E/G/J	X	X	X	X	
				N				X	
AC	Hysteresis	1.5.1	Hysteresis is only present for a falling (1->0) transition of the comparator output.	E/G/J	X				
				N					

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
AC	Low-Power Mode with Hysteresis	1.5.2	Low-Power mode (COMPCTRLn.SPEED = 0x0) with hysteresis enabled (COMPCTRLn.HYSTEN = 0x1) may result in undesired behavior of the AC.	E/G/J	X	X	X	X	
				N				X	
AC	Analog Pins	1.5.3	Analog pins are shared between PTC and AC module.	E/G/J	X	X	X	X	X
				N				X	
AC	Hysteresis	1.5.4	Hysteresis specification for the AC does not meet the published specification in the product data sheet.	E/G/J	X	X	X	X	
				N					
AC	Power Consumption	1.5.5	Power consumption for the AC does not meet the published specification in the product data sheet.	E/G/J	X	X	X	X	
				N				X	
CAN	CAN 2.0 Frame Transmit	1.6.1	When a CAN 2.0 frame is transmitted while CAN FD operation is enabled, a recessive stuff bit following the first reserved bit will cause a shift in the DLC.	E/G/J	X				
				N					
CAN	CAN Operation Mode	1.6.2	When CCCR.CME ≠ ""00"" and a change of the CAN operation mode is requested by writing to CCCR.CMR while frame transmission/reception is ongoing, this request may be ignored.	E/G/J	X				
				N					
CAN	CAN FD Operation	1.6.3	M_CAN will internally overwrite the received arbitration bits with the pending transmission's arbitration bits.	E/G/J	X				
				N					
CAN	Classic CAN Operation	1.6.4	When BTP.TSEG2 and BTP.BRP are zero, and the M_CAN transmits a frame, the FDF bit in CAN FD format (reserved bit in Classic CAN format) in the control field may be falsified.	E/G/J	X				
				N					
CAN	FDF bit	1.6.5	When a CAN frame is received with bit FDF and the following res bit both recessive, the protocol controller correctly detects a Protocol Exception Event.	E/G/J	X				
				N					
CAN	CAN Mode Change	1.6.6	Erroneous transmission when CCCR.CMR is changed during start of transmission.	E/G/J	X				
				N					
CAN	Restricted Operation Mode	1.6.7	After detecting a Message RAM Access Failure during frame transmission, interrupt flag IR.MRAF is set and the M_CAN enters Restricted Operation Mode (CCCR.ASM = '1').	E/G/J	X				
				N					

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Module	**Feature**	**Errata Number**	**Issue Summary**	**C20/C21 Device**	**Affected Revisions**				
					B	**C**	**D**	**E**	**F**
CAN	CCCR.INIT	1.6.8	When CCCR.INIT is set while the M_CAN is receiving a frame, the next received frame after resetting CCCR.INIT will cause IR.MRAF to be set.	E/G/J	X				
				N					
CAN	Message Transmission in DAR Mode	1.6.9	When a message is transmitted while CCCR.DAR = '1' the Event Type of the corresponding Tx Event FIFO element is ET = ""01"" instead of ET = ""10"".	E/G/J	X				
				N					
CAN	Setting CCCR.CCE During a TX Scan	1.6.10	When CCCR.CCE is set while the M_CAN Tx Handler is scanning the Message RAM for Tx Buffers with pending transmission requests,register TXBRP is reset and the Tx Handler FSM is halted.	E/G/J	X				
				N					
CAN	CAN FD Network Compatibility	1.6.11	The CAN FD frame format implements Bosch CAN FD Specification V1.0 and is not compatible with ISO11898-1.	E/G/J	X				
				N					
CAN	On-demand Clock Source	1.6.12	The CAN is not compatible with an on-demand clock source.	E/G/J	X				
				N					
CAN	Edge Filtering	1.6.13	When edge filtering is activated, the CAN synchronizes itself wrongly and does not correctly receive the first bit of the frame.	E/G/J		X	X	X	X
				N				X	
CAN	Erroneous Transmission	1.6.14	When NBTP.NTSEG2 is configured to zero, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive.	E/G/J	X	X	X	X	X
				N				X	
CAN	DAR Mode	1.6.15	Retransmission in DAR mode due to lost arbitration.	E/G/J	X	X	X	X	X
				N				X	
CAN	TxFIFO	1.6.16	Tx FIFO message sequence inversion.	E/G/J	X	X	X	X	X
				N				X	
CAN	High Priority Message (HPM) interrupt	1.6.17	Unexpected High Priority Message (HPM) interrupt	E/G/J	X	X	X	X	X
				N				X	
CAN	INTFLAG Status	1.6.18	Message transmitted with wrong arbitration and control fields.	E/G/J	X	X	X	X	X
				N				X	
CCL	RS Latch Reset	1.7.1	The reset of the RS latch is not functional.	E/G/J	X				
				N					
CCL	Sequential Logic	1.7.2	LUT Output is corrupted after enabling the CCL when sequential logic is used.	E/G/J	X	X	X	X	X
				N				X	

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
CCL	Enable Protected Registers	1.7.3	The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they should be enable-protected by the LUTCTRLx.ENABLE bits.	E/G/J	X	X	X	X	X
				N				X	
CCL	PAC Protection Error	1.7.4	Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.	E/G/J	X	X	X	X	X
				N				X	
Device	Idle Sleep Mode	1.8.1	In Idle Sleep mode, the APB and AHB clocks are not stopped if the FDPLL is running as a GCLK clock source.	E/G/J	X				
				N					
Device	Clock Configuration	1.8.2	The Analog Comparators and ADC1 use the same generic clock configuration.	E/G/J	X				
				N					
Device	TC Selection	1.8.3	The default TC selection as CCL input is not TC0, but TC4.	E/G/J	X				
				N					
Device	CTRLB Register Writes	1.8.4	In I^2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY Interrupt Service Routines can cause the state machine to reset.	E/G/J	X				
				N					
Device	Increased Power Consumption	1.8.5	Increased power consumption in Standby Sleep mode.	E/G/J	X				
				N					
Device	SYSTICK Calibration Value	1.8.6	The SYSTICK calibration value is incorrect.	E/G/J	X				
				N					
Device	DMA Write Access	1.8.7	DMA write access in Standby mode (i.e., during SleepWalking) may not work on some registers.	E/G/J	X	X	X	X	X
				N				X	
Device	PC10 Pin	1.8.8	Driving PC10 to logic HIGH affects VDDCORE.	E/G/J					
				N				X	
Device	DAC Output	1.8.9	When using DAC Output as Positive MUX Input Selection for the ADC, starting an ADC conversion results in noise on the DAC Output voltage and noisy ADC reading.	E/G/J	X	X	X	X	X
				N				X	
Device	DAC Output Reference Selection	1.8.10	When using DAC Output as the Reference Selection for the SDADC, starting a SDADC conversion results in noise on the DAC Output voltage.	E/G/J	X	X	X	X	X
				N				X	
Device	VREGSMOD bits	1.8.11	VREGSMOD bits have no effect in the PM.STDBYCFG register.	E/G/J	X				
				N					

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
Device	OSC48M Accuracy	1.8.12	The OSC48M accuracy cannot be reached for the whole VDD range.	E/G/J	X	X	X	X	
				N					
Device	Standby entry	1.8.13	Potential hard fault upon standby entry when systick interrupt is enabled	E/G/J	X	X	X	X	X
				N				X	
DAC	Dithering Mode	1.9.1	DAC in Dithering mode with right-adjust data leads to INL of 16 LSBs.	E/G/J	X				
				N					
DAC	Standby Sleep Mode	1.9.2	When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written, DAC.INTFLAG.EMPTY will be set after exit from Sleep mode.	E/G/J	X	X	X	X	X
				N				X	
DMAC	CRCDATAIN Writes	1.10.1	If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.	E/G/J	X				
				N					
DMAC	Fetch Error	1.10.2	When using more than one DMA channel a fetch error can appear on this channel.	E/G/J	X	X	X		
				N				X	
DMAC	Enabling Channels	1.10.3	When at least one channel using linked descriptors is already active, enabling another DMA channel can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.	E/G/J	X	X	X		
				N				X	
DMAC	Linked Descriptors	1.10.4	When using concurrent channels triggers, the DMAC write-back descriptors may get corrupted.	E/G/J				X	X
				N					
EIC	NMI Exception	1.11.1	If the NMI pin PORT config is INPUT+PULL-UP enabled and the NMI is configured to trigger on rising edge (or both edges), the NMI exception is triggered as soon as the NMI config is written.	E/G/J	X				
				N					
EIC	Write-protection	1.11.2	The EIC ASYNCH register is not write-protected.	E/G/J	X				
				N					
EIC	Spurious Flag	1.11.3	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges with the filter enabled, a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register	E/G/J	X	X	X	X	
				N					
EIC	False NMI Interrupt	1.11.4	Changing the NMI configuration (CONFIGn.SENSEx) on-the-fly may lead to a false NMI interrupt.	E/G/J	X	X	X	X	
				N					
EIC	Edge Detection	1.11.5	When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled.	E/G/J					
				N				X	

...........continued									
Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
EIC	Edge Detection in Standby Mode	1.11.6	When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will be detected.	E/G/J	X	X	X	X	X
				N				X	
EVSYS	Generic Clock	1.12.1	Using synchronous, spurious overrun can appear with generic clock for the channel always on.	E/G/J	X	X	X	X	X
				N				X	
EVSYS	Overrun Flag Trigger	1.12.2	The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later.	E/G/J	X	X	X	X	
				N					
EVSYS	Software Event	1.12.3	When using a software event on a channel with resynchronized path, CHSTATUS.CHBUSYn bit will not be set immediately.	E/G/J	X	X	X	X	X
				N				X	
EVSYS	Event Channel Configuration	1.12.4	Right after an Event channel configuration is done and enabled, the channel is busy for 1 generic clock (GCLK_EVSYS_Channelx) tick, however the EVSYS.CHSTATUS.CHBUSYn corresponding bit is not set during that time.	E/G/J	X	X	X	X	X
				N					
PORT	Overrun Events	1.13.1	When the PORT is defined as EVSYS.USER in a synch/resynch path, the first event is transmitted to the PORT but the acknowledgment coming from the PORT is not released.	E/G/J	X				
				N					
PORT	PORT Read and Write	1.13.2	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...) do not generate a PAC protection error.	E/G/J	X	X	X	X	X
				N				X	
PORT	Write-Protect	1.13.3	The non-debugger IOBUS writes to the PAC Write-protected registers are not prevented when the PORT is PAC Write-protected.	E/G/J	X	X	X	X	X
				N				X	
NVMCTRL	EEPROM Cache	1.14.1	The RWW EEPROM cache is not invalidated when performing write or erase operations.	E/G/J	X	X	X	X	X
				N				X	
PTC	Excess Power Consumption	1.15.1	The PTC generic clock is always requested during Standby mode when RUNSTDBY is set to one.	E/G/J	X				
				N					
RTC	Read Synchronization	1.16.1	The COUNTSYNC/CLOCKSYNC bit of the RTC.CTRLA register has no effect.	E/G/J	X				
				N					

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
RTC	COUNTSYNC	1.16.2	When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and generates an incorrect value.	E/G/J	X	X	X	X	
				N				X	
RTC	Write Corruption	1.16.3	An 8-bit or 16-bit write access for a 32-bit register, or an 8-bit write access for a 16-bit register can fail.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	SPI Mode	1.17.1	If the SERCOM is enabled in SPI mode with SSL detection enabled (CTRLB.SSDE) and CTRLB.RXEN =1, an erroneous slave select low interrupt (INTFLAG.SSL) can be generated.	E/G/J	X				
				N					
SERCOM	Auto-baud Mode	1.17.2	In USART Auto-baud mode, missing Stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	E/G/J	X	X	X	X	
				N				X	
SERCOM	SPI	1.17.3	In SPI Slave mode with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select pin low until the end of transmission.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	USART	1.17.4	In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	I^2C	1.17.5	In I^2C slave transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push data to the DATA register.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	Repeated Start	1.17.6	For Master Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	Repeated Start I^2C	1.17.7	For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	CLKHOLD Bit Status in I^2C	1.17.8	The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	NACK and Repeated Start in I^2C Master Mode	1.17.9	For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.	E/G/J	X	X	X	X	X
				N				X	

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
SERCOM	10-bit Addressing Mode	1.17.10	10-bit addressing in I^2C Slave mode is not functional.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	I^2C in Slave Mode	1.17.11	In I^2C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	Collision Detection	1.17.12	In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	Quick Command	1.17.13	Message transmitted with wrong arbitration and control fields.	E/G/J	X	X	X	X	X
				N				X	
SERCOM	USART	1.17.14	Unexpected over consumption in Standby mode	E/G/J	X	X	X	X	X
				N				X	
SDADC	Input Conversion	1.18.1	If the APB clock is not 2x or higher than the Generic Clock frequency, the first input conversion in a sequence will be invalid.	E/G/J	X				
				N					
SDADC	INL	1.18.2	Poor INL is observed when the SDADC input signal is close to VREF.	E/G/J	X	X	X	X	
				N					
SDADC	Conversions	1.18.3	The default value of zero in GAINCORR causes RESULT to be zero.	E/G/J	X				
				N					
SDADC	Power Consumption	1.18.4	Power consumption for the SDADC does not meet the published specification in the product data sheet.	E/G/J	X	X	X	X	
				N				X	
TSENS	PAC Write-protection	1.19.1	When PAC Write-Protection is enabled for TSENS, writes to TSENS.CTRLB are not functional.	E/G/J	X	X	X	X	X
				N				X	
TC	Capture Overflow	1.20.1	A capture overflow can occur without INTFLAG.ERR being set if a new capture occurs within 3 APB clock periods + 3 generic clock periods after a previous capture.	E/G/J	X				
				N					
TC	I/O Pins	1.20.2	The input capture on I/O pins does not work.	E/G/J	X				
				N					
TC	SYNCBUSY Flag	1.20.3	When clearing the STATUS.PERBUFV/ STATUS.CCBUFx flag, SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.	E/G/J	X	X	X	X	X
				N				X	

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
TCC	Circular Buffer	1.21.1	When the circular buffer is enabled, an APB clock is requested to update the corresponding APB register.	E/G/J	X				
				N					
TCC	RAMP 2 Mode	1.21.2	In RAMP 2 mode with Fault keep, qualified and restart, if a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.	E/G/J	X				
				N					
TCC	CAPTMARK	1.21.3	FCTRLX.CAPTURE[CAPTMARK] does not work as described in the data sheet.	E/G/J	X				
				N					
TCC	Capture Overflow	1.21.4	A capture overflow can occur without INTFLAG.ERR being set if a new capture occurs within 3 APB clocks + 3 generic Clock periods from a previous capture.	E/G/J	X				
				N					
TCC	Advance Capture Mode	1.21.5	Advance Capture mode does not work if an upper channel is not in one of these mode.	E/G/J	X	X	X	X	X
				N					
TCC	SYNCBUSY	1.21.6	When clearing STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.	E/G/J	X	X	X	X	X
				N					
TCC	Dithering Mode	1.21.7	Using TCC in Dithering mode with external retrigger events can lead to unexpected stretch of right-aligned pulses, or shrink of left-aligned pulses.	E/G/J	X	X	X	X	X
				N				X	
TCC	PERBUF	1.21.8	In down counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.	E/G/J	X	X	X	X	X
				N				X	
TCC	TCC with EVSYS in SYNC/ RESYNC Mode	1.21.9	TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.	E/G/J	X	X	X	X	X
				N				X	
TCC	ALOCK Feature	1.21.10	ALOCK feature is not functional .	E/G/J	X	X	X	X	X
				N				X	
XOSC32K	CFD and Clock Switching	1.22.1	When the CFD is enabled for XOSC/ XOSC32K and the oscillator input signal is stuck at 1 (i.e., logic high), the clock failure detection works correctly but the switch to the safe clock will fail.	E/G/J					
				N				X	
MCLK	PAC Protection	1.23.1	Writes to the MCLK Control A register (MCLK.CTRLA) do not generate a PAC protection error even if this register has been write-protected using the PAC.	E/G/J	X	X	X	X	X
				N				X	

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Module	Feature	Errata Number	Issue Summary	C20/C21 Device	Affected Revisions				
					B	C	D	E	F
FRQM	PAC Protection Error	1.24.1	FREQM reads on the Control B register (FREQM.CTRLB) and generates a PAC protection error.	E/G/J	X	X	X	X	X
				N				X	

Table of Contents

1. SAM C20/C21 Errata Issues

The following issues apply to the SAM C20/C21 Family devices.

1.1 32 kHz Oscillators Controller (OSC32KCTRL)

1.1.1 Clock Failure Detection

At start-up and in case of clock failure detection (CFD), the auto switch by the CFD does not work if XOSC32K is requested by the GCLK.

Workaround
Manually change the clock from XOSC32K to another 32K source.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.2 48 MHz High-Accuracy Internal Oscillator (OSC48M)

1.2.1 System Reset

When a System Reset is applied, the OSC48MDIV register is reset, but the value is not synchronized. This may result in the system clock running too fast.

Workaround
Do not write the OSC48MDIV register to lower than 0xB.

Do not run the device faster than 4 MHz when running from internal oscillators

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.2.2 Division Ratio

Changing the division ratio (OSC48MDIV) while the OSC48M is running but not requested by any generic clock generator (GCLK_GEN), makes the OSC48DIV bit in the OSC48MSYNCBUSY register to remain always set.

Workaround
If the OSC48M clock is not requested by any Generic Clock Generator (GCLK_GEN), clear the ONDEMAND bit in the OSC48MCTRL register before changing the division ratio in the OSC48MDIV register.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X

...........continued

C20/C21 Device	B	C	D	E	F
N				X	

1.3 96 MHz Fractional Digital Phase-Locked Loop (FDPLL)

1.3.1 Standby Mode

When entering Standby mode, the FDPLL is still running even if not requested by any module causing extra consumption.

Workaround

The FDPLL must be disabled before entering in Standby mode and re-enabled after wake-up

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.3.2 Clocking Accuracy

The FDPLL96M exhibits high period jitter and is not suitable for accurate clocking. Accurate clocking is limited to 32 MHz and below through XOSC.

Workaround

Connect a XTAL of up to 32 MHz to XOSC for a high-speed accurate clock source. OSC48M may be used for frequencies up to 48 MHz when less accuracy is required.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X			
N					

1.3.3 Ratio Value

When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround

Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for the DPLLRATIO register update.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.3.4 FDPLL Loop Divider Ratio

Changing the FDPLL Loop Divider Ratio on-the-fly does not work if the GCLK_DPLL_32K is not available.

Workaround
Ensure GCLK_DPLL_32K is available and enabled for the FDPLL internal lock timer before changing the FDPLL Loop Divider Ratio on-the-fly.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.4 Analog-to-Digital Converter (ADC)

1.4.1 Software Trigger

Once set, the ADC.SWTRIG.START will not be cleared until the microcontroller is reset.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.4.2 Least Significant Byte Result

The LSB of ADC result is stuck at zero in unipolar mode for 8-bit and 10-bit resolution.

Workaround
Use 12-bit resolution and take only least 8 bits or 10 bits, if necessary.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.4.3 Window Monitor

When the window monitor is enabled and its output is '0', the ADC GCLK is kept running. Power consumption will be higher than expected in Sleep mode.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.4.4 Synchronized Event

If a synchronized event is received during an ADC conversion, the ADC will not acknowledge the event, causing a stall of the event channel.

Workaround

When using events with the ADC, only the asynchronous path from the Event System must be used.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N					

1.4.5 Software Trigger Sync Busy Status

ADC SYNCBUSY.SWTRIG becomes stuck to one after wake-up from Standby Sleep mode.

Workaround

Ignore ADC SYNCBUSY.SWTRIG status when waking up from Standby Sleep mode. The ADC result can be read after INTFLAG.RESRDY is set. To start the next conversion, write a ‘1’ to SWTRIG.START.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.4.6 Reference Buffer Offset Compensation

TUE of the ADC conversion result is out of specification when,

- Using the reference source as REFCTRL.REFSEL ≠ VDDANA
  and
- Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1)

Workaround

The first five conversions after enabling ADC must be ignored. All further ADC conversions are within the specification.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.4.7 Differential and Single-Ended Mode

Electrical characteristics for Differential mode and Single-Ended mode do not meet the published specification in the product data sheet.

Workaround

None. Consider the following electrical characteristics for the affected silicon revisions.

Table 1-1. Differential Mode(1)

Symbol	Parameter	Conditions		Measurement			Unit
				Min.	Typ.	Max.	
ENOB	Effective Number of bits	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	10.0	10.7	11	bits
			Vddana = 2.7V Vref = 2.0V	10.3	10.5	10.9	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	10.5	10.8	11.1	
			Vddana = 2.7V Vref = 2.0V	9.9	10.0	10.6	
TUE	Total Unadjusted Error	Fadc = 500 ksps	VDDANA = 5.0V Vref = VDDANA	-	7.8	17.0	LSB
			Vddana = 2.7V Vref = 2.0V	-	8.0	32.0	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	-	9.0	20.0	
			Vddana = 2.7V Vref = 2.0V	-	10.5	32.0	
INL	Integral Non Linearity	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	-	+/-1.6	+/-3	LSB
			Vddana = 2.7V Vref = 2.0V	-	+/-1.9	+/-3	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	-	+/-1.5	+/-3	
			Vddana = 2.7V Vref = 2.0V	-	+/-3.2	+/-5	
DNL	Differential Non Linearity	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	-	-0.8/+1	-1/+2	LSB
			Vddana = 2.7V Vref = 2.0V	-	-0.7/+1.3	-1/+2.1	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	-	-0.8/+1.1	-1/+3.3	
			Vddana = 2.7V Vref = 2.0V	-	-0.9/+1.3	-1/+3.2	
Gain	Gain Error	Fadc = 1 Msps	Vddana = 2.7V Vref = 2.0V	-	+/-18	+/-57	mV
			Vddana = 5.0V Vref = 4.096V	-	+/-41	+/-100	
			Vddana = 3.0V Vref = Vddana	-	+/-17	+/-66	
			Vddana = 5.0V Vref = Vddana		+/-39	+/-81	
TCg	Gain Drift	Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	-250	-210	-170	μV/°C

...........continued							
Symbol	Parameter	Conditions		Measurement			Unit
				Min.	Typ.	Max.	
Offset	Offset Error	Fadc = 1 Msps	Vddana = 2.7V Vref = 2.0V	-	+/-1.4	+/-11	mV
			Vddana = 5.0V Vref = 4.096V	-	+/-6	+/-18	
			Vddana = 3.0V Vref = Vddana	-	+/-2	+/-9	
			Vddana = 5.0V Vref = Vddana		+/-0.2	+/-23	
Tco	Offset Drift	Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	20	80	120	μV/°C
SFDR		Spurious Free Dynamic Range	Fs = 1Msps / Fin = 14 kHz / Full range Input signal Vddana = 5.0V Vref = Vddana	71	75	81	dB
SINAD		Signal-to- Noise and Distortion ratio		65	67	68	
SNR		Signal-to- Noise ratio		67	68	69	
THD				-77	-74	-70	
		Noise RMS	External Reference voltage	-	0.5	2.0	mV

Note:
1. These values are based on characterization and not covered by test limits in production.

Table 1-2. Single-Ended Mode(1)

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
ENOB	Effective Number of bits	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	9.1	9.7	10.0	bits
			Vddana = 2.7V Vref = 2.0V	9.1	9.4	9.8	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	9.1	9.7	9.9	
			Vddana = 2.7V Vref = 2.0V	9.0	9.2	9.6	
TUE	Total Unadjusted Error	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	-	18.0	65.0	LSB
			Vddana = 2.7V Vref = 2.0V	-	30.2	62.0	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	-	18.4	60.0	
			Vddana = 2.7V Vref = 2.0V	-	30.4	61.0	

...........continued

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
INL	Integral Non Linearity	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	-	+/-2.4	+/-4	LSB
			Vddana = 2.7V Vref = 2.0V	-	+/-3.7	+/-6	
		Fadc = 1 Msps	Vddana = 5.0V Vref = Vddana	-	+/-2.2	+/-4	
			Vddana = 2.7V Vref=2.0V	-	+/-4.1	+/-6	
DNL	Differential Non Linearity	Fadc = 500 ksps	Vddana = 5.0V Vref = Vddana	-	-0.8/+1.1	-1/+3.8	LSB
			Vddana=2.7V Vref=2.0V	-	-0.8/+1.1	-1/+1.7	
		Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-	-0.8/+1	-1/+2	
			Vddana=2.7V Vref=2.0V	-	-1/+1.1	-1/+2.4	
Gain	Gain Error	Fadc = 1 Msps	Vddana=2.7V Vref=2.0V	-	+/-13	+/-28	mV
			Vddana=5.0V Vref=4.096V	-	+/-26	+/-52	
			Vddana=3.0V Vref=Vddana	-	+/-14	+/-24	
			Vddana=5.0V Vref=Vddana		+/-22	+/-42	
TCg	Gain Drift	Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	-170	-140	-80	uV/°C
Offset	Offset Error	Fadc = 1 Msps	Vddana=2.7V Vref=2.0V	-	+/-2.2	+/-21	mV
			Vddana=5.0V Vref=4.096V	-	+/-2.3	+/-61	
			Vddana=3.0V Vref=Vddana	-	+/-15	+/-42	
			Vddana=5.0V Vref=Vddana		+/-31	+/-80	
Tco	Offset Drift	Fadc = 1 Msps	Vddana=5.0V Vref=Vddana	160	180	210	μV/°C

...........continued							
Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
SFDR		Spurious Free Dynamic Range	Fs = 1Msps / Fin = 14 kHz / Full range Input signal Vddana=5.0V Vref=Vddana	69	71	73	dB
SINAD		Signal-to- Noise and Distortion ratio		57	60	61	
SNR		Signal-to-Noise ratio		57	61	61	
THD				-72	-70	-66	
		Noise RMS	External Reference voltage	-	0.7	2.0	mV

Note:

1. These values are based on characterization and not covered by test limits in production.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.4.8 Power Consumption

Power consumption for the ADC does not meet the specifications in the published product data sheet.

Workaround

None. Consider the following power consumption specifications for the affected silicon revisions.

Table 1-3. Power Consumption (1)

Symbol	Parameters	Conditions	Ta	Typ.	Max.	Units
IDD VDDANA	Differential mode	fs = 1Msps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V	Max. 85°C Typ. 25°C	905	1021	uA
		fs = 1Msps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		1062	1184	
		fs = 10 ksps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		381	460	
		fs = 10 ksps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		525	643	
	Single- Ended mode	fs = 1Msps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref=5.5V	Max. 85°C Typ. 25°C	984	1077	uA
		fs = 1Msps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref=5.5V		1103	1237	
		fs = 10 ksps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		437	528	
		fs = 10 ksps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		553	675	

...........continued

Symbol	Parameters	Conditions	Ta	Typ.	Max.	Units
IDD VDDANA	Differential mode	fs = 1 Msps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V	Max. 105°C Typ 25°C	905	1034	uA
		fs = 1 Msps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		1062	1199	
		fs = 10 ksps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		381	466	
		fs = 10 ksps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		525	654	
	Single- Ended mode	fs = 1 Msps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref=5.5V	Max. 105°C Typ. 25°C	984	1090	uA
		fs = 1 Msps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA = Vref = 5.5V		1103	1249	
		fs = 10 ksps / Reference buffer disabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA = Vref = 5.5V		437	536	
		fs = 10 ksps / Reference buffer enabled / BIASREFBUF = '111', BIASREFCOMP = '111' VDDANA=Vref= 5.5V		553	688	

Note:
1. These values are based on characterization.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N				X	

1.5 Analog Comparators (AC)

1.5.1 Hysteresis

Hysteresis is only present for a falling (1->0) transition of the comparator output.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				

...........continued

C20/C21 Device	B	C	D	E	F
N					

1.5.2 Low-Power Mode with Hysteresis

Low-Power mode (COMPCTRLn.SPEED = 0x0) with hysteresis enabled (COMPCTRLn.HYSTEN = 0x1) may result in undesired behavior of the AC.

Workaround

Do not use AC Low-Power mode (COMPCTRLn.SPEED = 0x0) and hysteresis (COMPCTRLn.HYSTEN = 0x1) together. Use only one of these features to avoid incorrect AC behavior.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N				X	

1.5.3 Analog Pins

Analog pins are shared between PTC and AC module. This may result in PTC accuracy issues.

Workaround

To guarantee the accuracy of the PTC measurement when using these shared pins, configure the AC input to anything different from default configuration, that is, VDD scaler, DAC or Bandgap.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.5.4 Hysteresis

Hysteresis specification for AC does not meet the published specification in the product data sheet.

Workaround

None. Consider the following hysteresis specifications for the affected silicon revisions.

Table 1-4. Analog Comparator Hysteresis Specifications

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
VHYS(1)(2)	Hysteresis	High speed COMPCTRLn.SPEED = 0x3	58	106	140	mV

Note:

1. These values are based on characterization.
2. Hysteresis enabled

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.5.5 Power Consumption

Power consumption for AC does not meet the specification in the published product data sheet.

Workaround

None. Consider the following power consumption specifications for the affected silicon revisions.

Table 1-5. AC Power Consumption (1)

Symbol	Parameters	Conditions	Ta	Typ.	Max.	Units
IDD ANA	Current consumption - Vcm=Vddana/2, +-100 mV overdrive from Vcm, Voltage scaler disabled	COMPCTRLn.SPEED = 0x0, VDDANA =5.0V	Max. 85°C Typ. 25°C	10	13	µA
		COMPCTRLn.SPEED = 0x3, VDDANA =5.0V		39	50	
	Current consumption Voltage scaler only	VDDANA =5.0V		43	54	
	Current consumption - Vcm=Vddana/2, +-100 mV overdrive from Vcm, Voltage scaler disabled	COMPCTRLn.SPEED = 0x0, VDDANA =5.0V	Max. 105°C Typ. 25°C	10	13	
		COMPCTRLn.SPEED = 0x3, VDDANA =5.0V		39	51	
	Current consumption Voltage scaler only	VDDANA =5.0V		43	57	

Note:

1. These values are based on characterization.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N				X	

1.6 Controller Area Network (CAN)

1.6.1 CAN 2.0 Frame Transmit

When a CAN 2.0 frame is transmitted while CAN FD operation is enabled, a recessive stuff bit following the first reserved bit will cause a shift in the DLC for specific identifiers with the result, that a frame with faulty DLC and faulty number of data bytes is transmitted.

Scope:

The erratum is limited to the case when a CAN 2.0 frame is transmitted while CAN FD operation is enabled (CCCR.CME ≠ ""00""). The problem does not occur when CAN FD frames are transmitted or when CAN FD operation is disabled.

Effects:

If the identifier of a transmit message ends with two dominant bits (11-bit ID) or three dominant bits (29-bit ID), bit stuffing causes the DLC to be shifted by one bit to the right. This results in transmission of a message with faulty DLC and therefore faulty number of data bytes.

Workaround
No workaround needed in CAN 2.0 networks, CAN Conformance Test passed. No workaround needed when only CAN FD messages are transmitted. For mixed operation (CAN 2.0 and CAN FD frames) the problematic identifiers may not be used for the transmission of CAN 2.0 frames.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.2 CAN Operation Mode

When CCCR.CME ≠ ""00"" and a change of the CAN operation mode is requested by writing to CCCR.CMR while frame transmission/reception is ongoing, this request may be ignored and the M_CAN remains in its previous operation mode.

Scope:

The errata is limited to the case when a change of the CAN operation mode from/to CAN FD operation is requested while frame transmission/reception is ongoing.

Effects:

If one of the affected CAN operation mode changes is requested by writing CCCR.CMR while a frame transmission/reception is ongoing, the request is acknowledged by resetting CCCR.CMR to ""00"" but the M_CAN remains in its previous operation mode.

Workaround
No workaround needed in CAN 2.0 networks, CAN Conformance Test passed. No workaround needed for switching between CAN operation according to ISO11898-1 and CAN FD operation with bit rate switching. In all other cases check whether the requested CAN operation mode change has been executed by reading CCCR.FDO and CCCR.FDBS. If not, repeat the command until requested mode change is signaled by CCCR.FDO and CCCR.FDBS.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.3 CAN FD Operation

When a CAN 2.0 frame with a recessive stuff bit following the first reserved bit is received while CAN FD operation is enabled and a transmission is pending, the M_CAN will internally overwrites the received arbitration bits with the pending transmission's arbitration bits.

Scope:

The erratum is limited to the case when CAN 2.0 frames with specific identifiers causing the described stuff bit are received while CAN FD operation is enabled (CCCR.CME ≠ ""00""). The problem does not occur when CAN FD operation is disabled.

Effects:

If the identifier of a received data frame ends with two dominant bits (11-bit ID) or three dominant bits (29-bit ID), there will be a recessive stuff bit after the first reserved bit. This causes the falsification of the received arbitration bits if a transmission is pending. If the pending transmission is a remote frame, the received data frame is treated as a received remote frame which will cause a format or CRC error resulting in an error frame. If the pending transmission is a data frame, the incoming frame is received and is presented to the receive message handler with the identifier of the pending transmit message. Depending on the configuration of the acceptance filtering, the frame may be stored in an Rx Buffer or Rx FIFO.

Workaround
No workaround needed in CAN 2.0 networks, CAN Conformance Test passed. No workaround needed when only CAN FD frames are received. For mixed operation (CAN 2.0 and CAN FD frames) the problematic identifiers may not be used.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.4 Classic CAN Operation

When BTP.TSEG2 and BTP.BRP are zero, and the M_CAN transmits a frame, the FDF bit in CAN FD format (reserved bit in Classic CAN format) in the control field may be falsified. The effect is different for frames to be transmitted in Classic CAN format and for frames to be transmitted in CAN FD format. Transmission of Classic CAN Frame => When BTP.TSEG2 and BTP.BRP are zero and the M_CAN transmits a Classic CAN frame (CCCR.CME = ""00"") with a 29-bit identifier where the MSB (ID28) is '1', the reserved bit following the RTR bit will be transmitted recessive instead of dominant while the rest of the frame is transmitted in Classic CAN format. Transmission of CAN FD Frame => When BTP.TSEG2 and BTP.BRP are zero, and the M_CAN transmits a CAN FD frame with a 29-bit identifier where the MSB (ID28) is ’0’ or a CAN FD frame with 11-bit identifier, the FDF bit of the frame is transmitted dominant instead of recessive, the rest of the frame is transmitted in Classic CAN format with a falsified DLC.

Scope:

The erratum is limited to the case when in the bit time configuration for Classic CAN operation and the Arbitration Phase in CAN FD operation BTP.TSEG2 and BTP.BRP are both zero. This configures the time segment after the sample point to the length of one time quantum and the length of the time quantum to one clock period. This is an unusual configuration.

Effects:

Transmission of Classic CAN Frame => When a Classic CAN frame is received by a CAN FD enabled receiving node it will interpret the falsified reserved bit as FDF bit. If this bit is recessive instead of dominant, the frame will be interpreted as CAN FD frame. In this case the receiving node will respond with an error frame when it detects that the rest of the frame is not in CAN FD format. A strictly Classic CAN receiving node will interpret the recessive FDF bit as reserved bit, ignore its actual value and will receive this frame correctly without detecting an error. Transmission of CAN FD Frame => When the M_CAN wants to transmit a CAN FD frame, it transmits the FDF bit dominant instead of recessive and the rest of the frame in Classic CAN format with a falsified DLC.

Workaround
Do not use bit timing configurations where BTP.TSEG2 and BTP.BRP are both zero for CAN FD communication.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.5 FDF bit

When a CAN frame is received with bit FDF and the following res bit both recessive, the protocol controller correctly detects a Protocol Exception Event. Reception of the disturbed message is not finished, the message is discarded. If this happened, two cases have to be distinguished:

- Message reception directly after Protocol Exception Event => When the next frame is received interrupt flag IR.MRAF is set to ’1’ although the frame has been received correctly.

- Message transmission directly after Protocol Exception Event => When a frame is transmitted directly after a Protocol Exception Event, that frame is transmitted with faulty frame format. In this case interrupt flag IR.MRAF is not set. The frame will cause an error frame. Only the first message after a Protocol Exception Event is affected, all following messages (received or transmitted) have no problem.

Scope:

The errata is limited to the case when the reserved bit res after the FDF bit in CAN FD frames is received recessive.

Effects:

Reception directly after Protocol Exception Event => Interrupt flag IR.MRAF is set although there was no problem in accessing the Message RAM. The Message is received correctly. Transmission directly after Protocol Exception Event => Transmission of a frame with faulty frame format.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.6 CAN Mode Change

When CCCR.CMR is changed during start of transmission, the following may happen:

- Case 1: Classic CAN -> CAN FD with bit rate switching => When the Tx Event FIFO is used, bits EDL and BRS of the related Tx Event FIFO element do not match with the transmitted frame type. They signal a CAN FD frame with bit rate switching (both set to one) while a Classic CAN frame was transmitted.
- Case 2: Classic CAN -> CAN FD without bit rate switching => When the Tx Event FIFO is used, bit EDL of the related Tx Event FIFO element does not match with the transmitted frame type. It signals a CAN FD frame while a Classic CAN frame was transmitted.
- Case 3: CAN FD with bit rate switching -> CAN FD without bit rate switching => When the Tx Event FIFO is used, bit BRS of the related Tx Event FIFO element does not match with the transmitted frame type. It signals a CAN FD frame without bit rate switching while a CAN FD frame with bit rate switching was transmitted.
- Case 4: CAN FD without bit rate switching -> CAN FD with bit rate switching => When the Tx Event FIFO is used, bit BRS of the related Tx Event FIFO element does not match with the transmitted frame type. It signals a CAN FD frame with bit rate switching while a CAN FD frame without bit rate switching was transmitted.
- Case 5: CAN FD with/without bit rate switching -> Classic CAN => IR.MRAF is set, the M_CAN switches to Restricted Operation Mode, and the transmission is aborted.

Scope:

The errata is limited to the case when the CAN operation mode is changed during start of transmission.

Effects:

Tx Event FIFO element faulty (Cases 1, 2, 3, 4) or interrupt flag IR.MRAF set, Restricted Operation Mode entered, and transmission aborted (Case 5).

Workaround
Do not change the CAN operation mode by writing to CCCR.CMR as long as there are pending transmission requests (TXBRP.TRPnn = '1').

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.7 Restricted Operation Mode

After detecting a Message RAM Access Failure during frame transmission, interrupt flag IR.MRAF is set and the M_CAN enters Restricted Operation Mode (CCCR.ASM = ’1’). When the Restricted Operation Mode is left by writing CCCR.ASM = '0', it may happen, that the first frame transmitted is send out with unexpected identifier and control field. If this is a valid frame, it may happen that it is accepted and acknowledged by a receiver.

Scope:

The errata is limited to the case when the M_CAN has entered Restricted Operation Mode due to a Message RAM Access Failure, signaled by interrupt flag IR.MRAF.

Effects:

With the next transmission after leaving Restricted Operation Mode by resetting CCCR.ASM, a frame with unexpected identifier and control field is transmitted which accidentally might be accepted and acknowledged by a receiver.

Workaround

To recover from Restricted Operation Mode proceed as follows:

1. Cancel all pending transmission requests by writing 0hFFFF FFFF to register TXBCR.
2. Issue a clock stop request by setting bit CCCR.CSR.
3. Wait until the M_CAN sets CCCR.INIT and CCCR.CSA to one.
4. First reset CCCR.CSR.
5. Then reset CCCR.INIT.
6. Wait until CCCR.INIT is read as zero.
7. Issue a second clock stop request by setting bit CCCR.CSR.
8. Wait until the M_CAN sets CCCR.INIT and CCCR.CSA to one.
9. Set CCCR.CCE, reset CCCR.CSR, and reset CCCR.ASM.
10. Restart M_CAN by writing CCCR.INIT = '0'.
11. Configure the CAN operation mode by writing to CCCR.CMR.
12. Request the transmissions canceled by step one.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.8 CCCR.INIT

When CCCR.INIT is set while the M_CAN is receiving a frame, the next received frame after resetting CCCR.INIT will cause IR.MRAF to be set.

Scope:

The errata is limited to the case when CCCR.INIT is set/reset while the M_CAN is receiving a frame.

Effects:

IR.MRAF is set when the first frame after resetting CCCR.INIT is received although that frame is received correctly.

Workaround

If CCCR.INIT shall be set during operation proceed as follows:

1. Issue a clock stop request by setting the CCCR.CSR bit.
2. Wait until the M_CAN sets CCCR.INIT and CCCR.CSA to one.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.9 Message Transmission in DAR Mode

When a message is transmitted while CCCR.DAR = ’1’ (automatic re-transmission disabled for messages not transmitted successfully), the Event Type of the corresponding Tx Event FIFO element is ET = ""01"" instead of ET = ""10"".

When multiple messages are transmitted sequentially using the same Tx Buffer while CCCR.DAR = ’1’, it may happen that a newly requested transmission is not started when it is requested in the time window starting at the successful completion of the previous message and ending at the end of the intermission phase before the bus is idle again. This message is then treated as if it had lost arbitration.

Scope:

The errata is limited to message transmission when DAR mode is configured. Normal CAN/CAN FD operation is not affected

Effects:

1. The Event Type of the associated Tx Event FIFO element is not correct.
2. When a message was transmitted successfully from a specific Tx Buffer, a following transmission using the same Tx Buffer and requested in the described time window will not be started.

Workaround
Do not use the same Tx Buffer for consecutive DAR transmissions or wait at least for 4 CAN bit times after successful transmission before requesting the next transmission from the same Tx Buffer.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.10 Setting CCCR.CCE During a TX Scan

When CCCR.CCE is set while the M_CAN Tx Handler is scanning the Message RAM for Tx Buffers with pending transmission requests (bits TXBRP.TRPnn set), register TXBRP is reset and the Tx Handler FSM is halted. After CCCR.INIT and CCCR.CCE have been reset by the Host, the M_CAN is unable to transmit messages. When the Host requests a transmission by writing to register TXBAR, the respective Tx Buffer Request Pending bit in register TXBRP is set, but the Tx Handler will not start the requested transmission.

Scope:

The errata is limited to the case when CCCR.CCE is set while the M_CAN Tx Handler is scanning the Message RAM.

Effects:

When CCCR.CCE is set while a Tx scan is in progress, the Tx Handler FSM stops. After CCCR.INIT and CCCR.CCE are reset, the Tx Handler FSM does not execute transmission requests.

Workaround
Perform the following steps to workaround the issue:

1. Cancel all pending transmission requests by writing 0hFFFF FFFF to register TXBCR.
2. Issue a clock stop request by setting bit CCCR.CSR.
3. Wait until the M_CAN sets CCCR.INIT and CCCR.CSA to one.

4. First reset CCCR.CSR.
5. Then reset CCCR.INIT.
6. Wait until CCCR.INIT is read as zero.
7. Issue a second clock stop request by setting bit CCCR.CSR.
8. Wait until the M_CAN sets CCCR.INIT and CCCR.CSA to one.
9. Set CCCR.CCE and reset CCCR.CSR.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.11 CAN FD Network Compatibility

The CAN FD frame format implements Bosch CAN FD Specification V1.0 and is not compatible with ISO11898-1. The CCR.NISO bit has no effect.

Workaround

Connect only to CAN-FD networks that support Bosch CAN FD Specification V1.0

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.12 On-demand Clock Source

The CAN is not compatible with an on-demand clock source.

Workaround

Clear the ONDEMAND bit to zero for the oscillator source that provides the GCLK to the CAN.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.6.13 Edge Filtering

When edge filtering is activated (CCCR.EFBI='1') and when the end of the integration phase coincides with a falling edge at the Rx input pin it may happen, that the CAN synchronizes itself wrongly and does not correctly receive the first bit of the frame. In this case the CRC will detect that the first bit was received incorrectly, it will rate the received FD frame as faulty and an error frame will be sent.

The issue only occurs, when there is a falling edge at the Rx input pin (CAN_RX) within the last time quantum (tq) before the end of the integration phase. The last time quantum of the integration phase is at the sample point of the 11th recessive bit of the integration phase. When the edge filtering is enabled, the bit timing logic of the CAN sees the Rx input signal delayed by the edge filtering. When the integration phase ends, the edge filtering is automatically disabled. This affects the reset of the FD CRC registers at the beginning of the frame. The Classical CRC register is not affected, hence this issue does not affect the reception of Classical frames.

In CAN communication, the CAN may enter integrating state (either by resetting the CCCR.INIT or by protocol exception event) while a frame is active on the bus. In this case the 11 recessive bits are counted between the acknowledge bit and the following start of frame. All nodes have synchronized at the beginning of the dominant acknowledge bit. This means that the edge of the following start of frame bit cannot fall on the sample point, so the issue does not occur. The issue occurs only when the CAN is, by local errors, mis-synchronized with regard to the other nodes.

Glitch filtering as specified in ISO 11898-1:2015 is fully functional.

Edge filtering was introduced for applications where the data bit time is at least two tq (of nominal bit time) long. In that case, edge filtering requires at least two consecutive dominant time quanta before the counter counting the 11 recessive bits for idle detection is restarted. This means edge filtering covers the theoretical case of occasional 1-tq-long dominant spikes on the CAN bus that would delay idle detection. Repeated dominant spikes on the CAN bus would disturb all CAN communication, so the filtering to speed up idle detection would not help network performance.

When this rare event occurs, the CAN sends an error frame and the sender of the affected frame retransmits the frame. When the retransmitted frame is received, the CAN has left integration phase and the frame will be received correctly. Edge filtering is only applied during integration phase, it is never used during normal operation. As integration phase is very short with respect to ""active communication time"", the impact on total error frame rate is negligible. The issue has no impact on data integrity.

The CAN enters integration phase under the following conditions:

- When CCCR.INIT is set to ’0’ after start-up
- After a protocol exception event (only when CCCR.PXHD = ’0’)

Scope:

The erratum is limited to FD frame reception when edge filtering is active (CCCR.EFBI=’1’) and when the end of the integration phase coincides with a falling edge at the Rx input pin.

Effects:

The calculated CRC value does not match the CRC value of the received FD frame and the CAN sends an error frame. After retransmission the frame is received correctly.

Workaround
Disable edge filtering or wait on retransmission if this rare event happens.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J		X	X	X	X
N				X	

1.6.14 Erroneous Transmission

When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as ’1’ in the CAN’s Tx Buffer Element.

A phase buffer segment 2 of length ’1’ (Phase_Seg2(N) = 1) is not sufficient to switch to the first identifier bit after the sample point in Intermission where the dominant bit was detected.

The CAN protocol according to ISO 11898-1 defines that a dominant third bit of Intermission causes a pending transmission to be started immediately. The received dominant bit is handled as if the CAN has transmitted a Start-of-Frame (SoF) bit.

The ISO 11898-1 specifies the minimum configuration range for Phase_Seg2(N) to be 2..8 tq. Therefore, excluding a Phase_Seg2(N) of ’1’ will not affect CAN conformance.

Effects:

If NBTP.NTSEG2 = ’0’, it may happen that the CAN transmits the first identifier bit dominant instead of recessive.

Workaround
Update configuration range of NBTP.NTSEG2 from 0..127 tq to 1..127 tq in the CAN documentation.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.6.15 DAR Mode

When CAN is configured in DAR mode (CCCR.DAR = 1), the automatic retransmission for transmitted messages that are disturbed by an error or have lost arbitration is disabled. When the transmission attempt is not successful, the Tx Buffer's Transmission Request bit (TXBRP.TRPn) will be cleared and the Tx Buffer's Cancellation Finished bit (TXBCF.CFn) will be set.

When the transmitted message loses arbitration at any one of the first two identifier bits, chances are that instead of the bits of the actually transmitted Tx Buffer, the TXBRP.TRPn and TXBCF.CFn bits of the previously started Tx Buffer (or Tx Buffer 0, if there is no previous transmission attempt) are written (TXBRP.TRPn = 0, TXBCF.CFn = 1).

If, in this case the TXBRP.TRPn bit of the Tx Buffer that lost arbitration at the first two identifier bits are not cleared, retransmission is attempted. When CAN loses arbitration again at the immediately following retransmission, then actually and previously transmitted Tx Buffer are the same and this Tx Buffer's TXBRP.TRPn bit is cleared and its TXBCF.CFn bit is set.

Scope:

The erratum is limited to the case when CAN loses arbitration at one of the first two transmitted identifier bits while in DAR mode. This problem does not occur when the transmitted message is disturbed by an error.

Effects:

In this case, it might happen that the TXBRP.TRPn bit is cleared after the second transmission attempt instead of the first. Additionally it may happen that the TXBRP.TRPn bit of the previously started Tx Buffer is cleared, if it has been set again. As in this case the previously started Tx Buffer has lost CAN internal arbitration against the active Tx Buffer, its message has a lower identifier priority. It would also have lost arbitration on the CAN bus at the same position.

Workaround
Update the configuration range of the NBTP.NTSEG2 from 0..127 tq to 1..127 tq in the CAN documentation.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.6.16 TxFIFO

Assuming that there are two Tx FIFO messages in the output pipeline of the Tx Message Handler.

Transmission of Tx FIFO message 1 is started:

Position 1: Tx FIFO message 1 (transmission ongoing).

Position 2: Tx FIFO message 2.

Position 3: Free FIFO bugger.

During the transmission of Tx FIFO message 1, a non Tx FIFO message with a higher CAN priority is requested. Due to its priority it will be inserted into the output pipeline. The TxMH performs "message scans" to keep the output pipeline up to date with the highest priority messages from the message RAM.

After the following two message scans, the output pipeline has the following content:

Position 1: Tx FIFO message 1 (transmission ongoing).

Position 2: non Tx FIFO message with higher CAN priority.

Position 3: Tx FIFO message 2.

If the transmission of Tx FIFO message 1 is not successful (lost arbitration or CAN bus error), it is pushed from the output pipeline by the non Tx FIFO message with higher CAN priority. The following scan again inserts Tx FIFO message 1 into the output pipeline at position 3:

Position 1: non Tx FIFO message with higher CAN priority (transmission ongoing).

Position 2: Tx FIFO message 2.

Position 3: Tx FIFO message 1.

This results in Tx FIFO message 2 being in the output pipeline in front of Tx FIFO message 1 and they are transmitted in that order, resulting in a message sequence inversion.

Scope:

The erratum describes the case when CAN uses both, dedicated Tx Buffers and a Tx FIFO (TXBC.TFQM = 0) and the messages in the Tx FIFO do not have the highest internal CAN priority. The described sequence inversion may also happen between two non Tx FIFO messages (Tx Queue or dedicated Tx Buffers) that have the same CAN identifier and that should be transmitted in the order of their buffer numbers (not the intended use).

Effects:

In the above described case, it may happen that two consecutive messages from the Tx FIFO exchange their positions in the transmit sequence.

Workaround
When transmitting messages from a dedicated Tx Buffer with higher priority than the messages in the Tx FIFO, choose one of the following workarounds:

Workaround 1

Use two dedicated Tx Buffers, for example, use Tx Buffers 4 and 5 instead of the Tx FIFO.

The Transmit Loop below replaces the function that fills the Tx FIFO.

Write the message to Tx Buffer 4.

Transmit Loop:

- Request Tx Buffer 4 - write TXBAR.A4
- Write message to Tx Buffer 5
- Wait until transmission of Tx Buffer 4 completed - IR.TC, read TXBTO.TO4
- Request Tx Buffer 5 - write TXBAR.A5
- Write message to Tx Buffer 4
- Wait until transmission of Tx Buffer 5 completed - IR.TC, read TXBTO.TO5

Workaround 2

Ensure that only one Tx FIFO element is pending for transmission at any time.

The Tx FIFO elements may be filled at any time with messages to be transmitted, but their transmission requests are handled separately. Each time a Tx FIFO transmission has completed and the Tx FIFO becomes empty (IR.TFE = 1), the next Tx FIFO element is requested.

Workaround 3

Use only a Tx FIFO. Send the message with the higher priority also from Tx FIFO.

Drawback: The higher priority message has to wait until the preceding messages in the Tx FIFO are sent.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.6.17 High-Priority Message (HPM) Interrupt

There are two configurations where the issue occurs:

Configuration A:

- At least one Standard Message ID Filter Element is configured with priority flag set (S0.SFEC = 0b100/0b101/0b110)
- No Extended Message ID Filter Element configured
- Non-matching extended frames are accepted (GFC.ANFE = 0b00/0b01)

The HPM interrupt flag IR.HPM is set erroneously on reception of a non high-priority extended message under the following conditions:

1. A standard HPM frame is received and accepted by a filter with priority flag set (that is, Interrupt flag IR.HPM is set as expected).
2. An extended frame is received and accepted because of the GFC.ANFE configuration (that is, Interrupt flag IR.HPM is set erroneously).

Configuration B:

- At least one Extended Message ID filter element is configured with priority flag set (F0.EFEC = 0b100/0b101/0b110)
- No Standard Message ID filter element is configured
- Non matching standard frames are accepted (GFC.ANFS = 0b00/0b01)

The HPM interrupt flag IR.HPM is set erroneously on reception of a non high-priority standard message under the following conditions:

1. An extended HPM frame is received and accepted by a filter with priority flag set (that is, Interrupt flag IR.HPM is set as expected).
2. A standard frame is received and accepted because of the GFC.ANFS configuration (that is, Interrupt flag IR.HPM is set erroneously).

Scope:

The erratum is limited to the following configurations:

Configuration A:

No Extended Message ID filter element is configured and non matching extended frames are accepted due to Global Filter Configuration (GFC.ANFE = 0b00/0b01).

Configuration B:

No Standard Message ID Filter Element configured and non-matching standard frames are accepted due to Global Filter Configuration (GFC.ANFS = 0b00/0b01).

Effects:

Interrupt flag IR.HPM is set erroneously at the reception of a frame with:

- Configuration A: Extended Message ID
- Configuration B: Standard Message ID

Workaround
Configuration A:

Setup an Extended Message ID filter element with the following configuration:

- F0.EFEC = 001/010: Select Rx FIFO for storage of extended frames
- F0.EFID1 = any value: The value is not relevant as all ID bits are masked out by F1.EFID2
- F1.EFT = 10: Classic filter, F0.EFID1 = filter, F1.EFID2 = mask
- F1.EFID2 = 0: All bits of the received extended ID are masked out

Now all extended frames are stored in Rx FIFO ‘0’ or Rx FIFO ‘1’ depending on the configuration of F0.EFEC.

Configuration B:

Setup an Standard Message ID filter element with the following configuration:

- S0.SFEC = 001/010: Select Rx FIFO for storage of standard frames
- S0.SFID1 = any value: The value is not relevant as all ID bits are masked out by S0.SFID2
- S0.SFT = 10: Classic filter, S0.SFID1 = filter, S0.SFID2 = mask
- S0.SFID2 = 0: All bits of the received standard ID are masked out

Now all standard frames are stored in Rx FIFO ‘0’ or Rx FIFO ‘1’ depending on the configuration of S0.SFEC.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.6.18 INTFLAG Status

Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- CAN is in the Receiver state (PSR.ACT ≠0b10), therefore there is no pending transmission
- A new transmission is requested before the third bit of intermission is reached
- The CAN bus is sampled dominant at the third bit of intermission which is treated as SoF (See ISO11898-1:2015, “Section 10.4.2.2”)

Under the conditions above, the following might happen:

- The shift register is not loaded with ID, format, and DLC of the requested message
- CAN will start arbitration with wrong ID, format, and DLC on the next bit
- If the ID wins arbitration, a CAN message with a valid CRC is transmitted
- If this message is acknowledged, the ID stored in the Tx event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, hence no error is detected by the transmitting CAN

The erratum is limited when CAN is in the Receiver state (PSR.ACT = 0b10) with no pending transmission (register TXBRP == 0) and a new transmission is requested before the third bit of intermission is reached and this third bit of intermission is seen dominant.

When a transmission is requested by the CPU by writing to TXBAR, the Tx message handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated in the critical time window between the sample points of the second and third bit of intermission and if that third bit of intermission is seen dominant.

This dominant level at the third bit of intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

Effects:

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

Workaround
Workaround 1:

Request a new transmission only if another transmission is already pending (that is, register TXBRP ≠ 0) or when CAN is not in the Receiver state (when PSR.ACT ≠ 0b10). To avoid activating the transmission request in the critical time window between the sample points of the second and third bit of intermission, the application software can evaluate the Rx interrupt flags, such as IR.DRX, IR.RF0N, and IR.RF1N, which are set at the last bit of EoF when a received and accepted message becomes valid. The last bit of EoF is followed by third bits of intermission.

Therefore the critical time window has safely terminated three bit times after the Rx interrupt. Now a transmission may be requested by writing to TXBAR. After the interrupt, the application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

Workaround 2:

If a transmission is to be requested while no other transmission request is already pending and the CAN bus is not idle, set the CCCR.INIT bit (which stops the CAN protocol controller), set the transmission request and clear the CCCR.INIT bit. The message currently being received when the CCCR.INIT bit is set will be lost, but no errors (or error frames) will be generated and the CAN protocol controller will re-integrate into the CAN communication immediately at the 11 recessive bits of the next End-of-Frame including intermission.

Workaround 3:

It is also possible to keep the number of pending transmissions always at > 0 by frequently requesting a message, then the condition 'No pending transmission' is never met. The frequently requested message may be given a low priority, losing arbitration to all other messages.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.7 Configurable Custom Logic (CCL)

1.7.1 RS Latch Reset

The reset of the RS latch is not functional. The latch can only be cleared by disabling the LUT.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.7.2 Sequential Logic

The LUT output is corrupted after enabling the CCL when sequential logic is used.

Workaround

Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.7.3 Enable Protected Registers

The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they must be enable-protected by the LUTCTRLx.ENABLE bits.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.7.4 PAC Protection Error

Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.8 Device

1.8.1 Idle Sleep Mode

In Idle Sleep mode, the APB and AHB clocks are not stopped if the FDPLL is running as a GCLK clock source.

Workaround
Disable the FDPLL before entering Idle Sleep mode.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.2 Clock Configuration

The Analog Comparators and ADC1 use the same generic clock configuration. GCLK_ADC1 must be used to configure the clock for AC as GCLK_AC is not functional.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.3 TC Selection

The default TC selection as CCL input is not TC0, but TC4. Thus the TC selection for the CCL is TC4/TC0/TC1/TC2 instead of TC0/TC1/TC2/TC3. The TC alternate selection is TC0/TC1/TC2/TC3 instead of TC1/TC2/TC3/TC4.

Workaround
Use the TC input mapping described above.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.4 CTRLB Register Writes

In I²C Slave mode, writing the CTRLB register when in the AMATCH or DRDY Interrupt Service Routines can cause the state machine to reset.

Workaround
Write CTRLB.ACKACT to 0 using the following sequence:

```
 // If higher priority interrupts exist, then disable so that the following two writes are
atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
 // Re-enable interrupts if applicable.
```

Write CTRLB.ACKACT to 1 using the following sequence:

```
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
```

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a 1 to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a 1 to its bit position.

Code replacements examples:

Current:

```
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;
```

Change to:

```
SERCOM - STATUS.reg = 0;
 SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;
 SERCOM - CTRLB.reg = 0;
 /* ACK or NACK address */
 SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);
 // CMD=0x3 clears all interrupts, so to keep the result similar,
 // PREC is cleared if it was set.
 if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_AMATCH;
```

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.5 Increased Power Consumption

Increased power consumption in Standby Sleep mode.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.6 SYSTICK Calibration Value

The SYSTICK calibration value is incorrect.

Workaround

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.7 DMA Write Access

DMA write access in Standby mode (i.e., during SleepWalking) may not work on some registers. The impacted peripheral registers for SAM C20/C21 "E/G/J" devices are:

- ADC: SWTRIG
- RTC: COUNT
- TC: CTRLB, STATUS, COUNTH, COUNTL, PER, PERBUF, CC, CCBUF
- TCC: CTRLB, STATUS, COUNT, PATT, WAVE, PER, PERBUF, CC, CCBUF
- SDADC: SWTRIG

The impacted peripheral registers for SAM C20/C21 "N" devices are:

- RTC: COUNT
- SDADC: SWTRIG

Workaround

Use Idle Sleep mode when using DMA write access (SleepWalking) to the impacted registers.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.8.8 PC10 Pin

Driving PC10 to logic HIGH affects VDDCORE.

Workaround
Do not use the pin PC10. Keep the default configuration for the pin. Connect externally the PC10 pin to GND.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J					
N				X	

1.8.9 DAC Output

When using DAC Output as Positive MUX Input Selection for the ADC, starting an ADC conversion results in noise on the DAC Output voltage and noisy ADC reading.

Workaround
Wire the DAC VOUT pin externally to a ADC AINx pin input. Select the corresponding ADC AINx pin as Positive MUX Input Selection.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.8.10 DAC Output Reference Selection

When using DAC Output as the Reference Selection for the SDADC, starting a SDADC conversion results in noise on the DAC Output voltage.

Workaround
Set the SDADC Reference Buffer On by writing REFCTRL.ONREFBUF = 1.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.8.11 VREGSMOD bits

VREGSMOD bits have no effect in the PM.STDBYCFG register. The power domain controller always operates in Automatic Regulator mode.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.8.12 OSC48M Accuracy

The OSC48M accuracy cannot be reached for the whole VDD range.

Workaround

SAM C20/C21 "E/G/J" - Revision B Silicon: None.

SAM C20/C21 "E/G/J" - Revision C Silicon: Limited VDD range, according to the Electrical Characteristics chapter

SAM C20/C21 "E/G/J" - Revision D and E Silicon: Write OSCCTRL.CAL48M register, depending on the VDD range used.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.8.13 Potential hard fault on standby entry

When the systick interrupt is enabled and the standby back-bias option is set (STDBYCFG.BBIAS = 1), an hard fault can occur upon standby entry in the rare occasion when the systick interrupt coincides exactly with the standby entry.

Workaround

Disable the systick interrupt before entering standby and re-enable it after.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.9 Digital-to-Analog Converter (DAC)

1.9.1 Dithering Mode

DAC in Dithering mode with right-adjust data leads to INL of 16 LSBs.

Workaround

Use dithering with left-adjusted data only.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.9.2 Standby Sleep Mode

When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written (not empty), if the device goes to Standby Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exit from Sleep mode.

Workaround

After waking from Standby mode, ignore and clear the flag DAC.INTFLAG.EMPTY.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.10 Direct Memory Access Controller (DMAC)

1.10.1 CRCDATAIN Writes

If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.

Workaround
Add a `NOP` instruction between each write to CRCDATAIN register.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.10.2 Fetch Error

When using more than one DMA channel and if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.

Workaround
Do not use linked descriptors, make a software link instead:

Replace the channel which used linked descriptor by two channels DMA (with linked descriptor disabled) handled by two channels event system:

- DMA channel 0 transfer completion is able to send a conditional event for DMA channel 1 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 0 and configuration CHCTRLB.EVACT=CBLOCK for channel 1)
- On the transfer complete reception of the DMA channel 0, immediately re-enable the channel 0
- Then DMA channel 1 transfer completion is able to send a conditional event for DMA channel 0 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 1 and configuration CHCTRLB.EVACT=CBLOCK for channel 0)
- On the transfer complete reception of the DMA channel 1, immediately re-enable the channel 1
- The mechanism can be launched by sending a software event on the DMA channel 0

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X		
N				X	

1.10.3 Enabling Channels

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.

This happens if the channel number of the channel being enabled is lower than the channel already active.

Workaround
When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X		
N				X	

1.10.4 Concurrent channels triggers

When using concurrent channels triggers, the DMAC write-back descriptors may get corrupted.

Workaround
Multiple transfers must only be sequenced using linked descriptors on a single channel.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J				X	X
N					

1.11 External Interrupt Controller (EIC)

1.11.1 NMI Exception

If the NMI pin PORT config is INPUT+PULL-UP enabled and the NMI is configured to trigger on rising edge (or both edges), the NMI exception is triggered as soon as the NMI config is written.

Workaround
Set the NMI pin PORT config, enable EIC in

- Edge Detection

mode, and then disable the EIC. Clear INTFLAG, and then write the NMI configuration.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.11.2 Write-protection

The EIC ASYNCH register is not write-protected.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.11.3 Spurious Flag

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using CTRLA ENABLE bit.

Workaround

Clear the INTFLAG bit after the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.11.4 False NMI Interrupt

Changing the NMI configuration (CONFIGn.SENSEx) on-the-fly may lead to a false NMI interrupt.

Workaround

Clear the NMIFLAG bit once the NMI is modified.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.11.5 Edge Detection

When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J					
N				X	

1.11.6 Edge Detection in Standby Mode

When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

Workaround for SAM C20/C21 "E/G/J" Devices
Asynchronous edge detection doesn't work, instead use the synchronous edge detection (ASYNCH.ASYNCH[x]=0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL=1).

Workaround for SAM C20/C21 "N" Devices
Use the asynchronous edge detection with debouncer enabled. It is recommended to have the DPRESCALER.PRESCALER and DPRESCALER.TICKON settings such as to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.12 Event System (EVSYS)

1.12.1 Generic Clock

Using synchronous, spurious overrun can appear with generic clock for the channel always on.

Workaround
Request the generic clock on demand by setting the CHANNEL.ONDEMAND bit to one.

No penalty is introduced.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.12.2 Overrun Flag Trigger

The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later. As a consequence, any generator event occurring on that channel before that extra GCLK_EVSYS_CHANNEL_n clock cycle will trigger the overrun flag.

Workaround
For applications using event generators other than the software event, monitor the OVR flag.

For applications using the software event generator, wait one GCLK_EVSYS_CHANNEL_n clock cycle after the CHSTATUS.CHBUSYn bit is cleared before issuing a software event.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.12.3 Software Event

When using a software event on a channel with resynchronized path, CHSTATUS.CHBUSYn bit will not be set immediately. If another event occurs during this time the event is lost and the overrun flag is not generated.

Workaround

Wait three GCLK_EVSYS_CHANNEL_n clock cycles for the CHSTATUS.CHBUSYn bit to be set, before issuing a new software event.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.12.4 Event Channel Configuration

Right after an Event channel configuration is done and enabled, the channel is busy for 1 generic clock (GCLK_EVSYS_Channelx)tick, however the EVSYS.CHSTATUS.CHBUSYn corresponding bit is not set during that time. This is noticeable when the EVSYS input GCLK frequency is less than the CPU frequency.

Workaround

Wait for at least 1 generic clock(GCLK_EVSYS_Channelx) tick before triggering the channel for the first time after it has been configured and enabled.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N					

1.13 I/O Pin Controller (PORT)

1.13.1 Overrun Events

When the PORT is defined as EVSYS.USER in a synch/resynch path, the first event is transmitted to the PORT but the acknowledgment coming from the PORT is not released. So next coming events are treated as overrun by EVSYS.

Workaround

None.

Do not use the synch/resynch path, only use asynchronous path.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.13.2 PORT Read and Write

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...) do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.13.3 Write Protect

The non-debugger IOBUS writes to the PAC Write-protected registers are not prevented when the PORT is PAC Write-protected.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.14 Non-Volatile Memory Controller (NVMCTRL)

1.14.1 EEPROM Cache

The RWW EEPROM cache is not invalidated when performing write or erase operations. Reading RWWEE cached data can result in outdated data.

Workaround
When the RWW EEPROM Cache is on CTRLB.CACHEDIS=0x2 or CTRLB.CACHEDIS=0x3, invalidate the cache by issuing the INVALL NVMCTRL command immediately after issuing a RWW EEPROM write or erase operation.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.15 Peripheral Touch Controller (PTC)

1.15.1 Excess Power Consumption

The PTC generic clock is always requested during Standby mode when RUNSTDBY is set to one. Power consumption will be higher if the PTC is enabled during Standby Sleep mode even if no conversion is ongoing.

Workaround
Disable PTC in Standby mode to reduce power consumption.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.16 Real-Time Clock (RTC)

1.16.1 Read Synchronization

The COUNTSYNC/CLOCKSYNC bit of the RTC.CTRLA register has no effect. Read synchronization of the COUNT/CLOCK register is always enabled.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.16.2 COUNTSYNC

When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized, hence it is a wrong value.

Workaround
After enabling COUNTSYNC, read the COUNT register until its value is changed when compared to its first value read. After this, all consequent value read from the COUNT register is valid.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N				X	

1.16.3 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround
Write the registers with:

- A 32-bit write access for the COUNT register in COUNT32 mode, the CLOCK register in CLOCK mode
- A 16-bit write access for the COUNT register in COUNT16 mode

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17 Serial Communication Interface (SERCOM)

1.17.1 SPI Mode

If the SERCOM is enabled in SPI mode with SSL detection enabled (CTRLB.SSDE) and CTRLB.RXEN = 1, an erroneous slave select low interrupt (INTFLAG.SSL) can be generated.

Workaround
Enable the SERCOM first with CTRLB.RXEN = 0. In a subsequent write, set CTRLB.RXEN = 1.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.17.2 Auto-baud Mode

In USART Auto-baud mode, missing Stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N				X	

1.17.3 SPI

In SPI Slave mode with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select pin low until the end of transmission.

Workaround
In SPI Slave mode, the Slave Select (SS) pin must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.4 USART

In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.5 I^{2}C

In I^{2}C slave transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push data to the DATA register. Because a NACK was received, the transfer on the I^{2}C bus will not happen causing the loss of this data.

Workaround

Configure the DMA transfer size to the number of data to be received by the I^{2}C master. DMA can not be used if the number of data to be received by the master is not known.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.6 Repeated Start

For Master Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to properly generate a Repeated Start.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.7 Repeated Start I^{2}C

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.8 CLKHOLD Bit Status in I^2C

The STATUS.CLKHOLD bit in master and slave modes can be written, whereas it is a read-only status bit.

Workaround
Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.9 NACK and Repeated Start in I^2C Master Mode

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.10 10-bit Addressing Mode

10-bit addressing in I^2C Slave mode is not functional.

Workaround
None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.11 I^2C in Slave Mode

In I^2C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

Workaround
Manually clear status bits LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to 1 when set.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.12 Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Workaround
The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.13 Quick Command

When Quick command is enabled (CTRLB.QCEN=1), the software can issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, SCL Stretch Mode is CTRLA.SCLSM=1, a bus error will be generated.

Workaround
Use Quick Command mode (CTRLB.QCEN=1) only if SCL Stretch Mode is CTRLA.SCLSM=0.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.17.14 Over Consumption in standby

When SERCOM USART CTRLA.RUNSTDBY = 0 and the Receiver is disabled (CTRLB.RXEN = 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected over consumption.

Workaround
Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX, or add an external pull-up on the RX pin.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.18 Sigma-Delta Analog-to-Digital Converter (SDADC)

1.18.1 Input Conversion

If the APB clock is not 2x or higher than the Generic Clock frequency, the first input conversion in a sequence will be invalid.

Workaround
The APB clock must be twice the generic clock frequency or higher, or the prescaler must be configured to provide a similar ratio.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.18.2 INL

Poor INL is observed when the SDADC input signal is close to VREF.

Workaround
SDADC Differential Input Voltage Range should be limited to ± 0.7.VREF (and not ± VREF).

SDADC Single-Ended Input Voltage Range should be limited to 0 to 0.7.VREF (and not 0 to VREF).

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N					

1.18.3 Conversions

The default value of zero in GAINCORR causes RESULT to be zero. The default value of zero in CTRLB.SKPCNT generates invalid data on the first two conversions

Workaround
Write GAINCORR to '1' before running any conversions. Write CTRLB.SKPCNT to 2 before running single conversions.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.18.4 Power Consumption

Power consumption for the SDADC does not meet the specification in the published product data sheet.

Workaround
None. Consider the following power consumption specifications for the affected silicon revisions.

Table 1-6. SDADC Power Consumption (1)

Symbol	Parameters	Conditions	Ta	Typ.	Max.	Units
IDD VDDANA	Power consumption	CTLSDADC=0x0 External Reference - VDDANA = 5.5V Vref = 2V Reference buffer on SCLK_SDADC = 6 MHz	Max. 85°C Typ. 25°C	588	658	uA
		CTLSDADC=0x0 Internal Reference - VDDANA = Vref = 5.5V Reference buffer off SCLK_SDADC = 6 MHz		552	608	uA
		CTLSDADC=0x0 External Reference - VDDANA = 5.5V Vref = 2V Reference buffer on SCLK_SDADC = 6 MHz	Max. 105°C Typ. 25°C	588	667	uA
		CTLSDADC=0x0 Internal Reference - VDDANA=Vref= 5.5V Reference buffer off SCLK_SDADC = 6 MHz		552	617	uA

Note:
1. These values are based on characterization.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	
N				X	

1.19 Temperature Sensor (TSENS)

1.19.1 PAC Write-protection

When PAC Write-Protection is enabled for TSENS, writes to TSENS.CTRLB are not functional.

Workaround
Do not enable the PAC Write-Protection for TSENS.CTRLB or use the TSENS in free-running mode.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.20 Timer/Counter (TC)

1.20.1 Capture Overflow

A capture overflow can occur without INTFLAG.ERR being set if a new capture occurs within 3 APB clock periods + 3 generic clock periods after a previous capture.

Workaround
The delay between two capture events must be longer than 3 APB clock periods + 3 generic clock periods.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.20.2 I/O Pins

The input capture on I/O pins does not work.

Workaround
Use the input capture through TC event and use the EIC or CCL as event generators.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.20.3 SYNCBUSY Flag

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

Workaround
Clear successively twice the STATUS.PERBUFV/STATUS.CCBUFx flag to ensure that the PERBUF/CCBUFx register value is properly restored before updating it.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.21 Timer/Counter for Control Applications (TCC)

1.21.1 Circular Buffer

When the circular buffer is enabled, an APB clock is requested to update the corresponding APB register. If all masters in the system (CPU, DMA) are disabled, the APB clock is never provided to the TCC, making the circular buffer feature not functional in standby Sleep mode.

Workaround
Keep a master enabled in the system (enable DMA or do not enable standby Sleep mode when circular buffer is enabled).

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.21.2 RAMP 2 Mode

In RAMP 2 mode with Fault keep, qualified and restart, if a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.

Workaround

Avoid faults few cycles before the end or the beginning of a ramp.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.21.3 CAPTMARK

FCTRLX.CAPTURE[CAPTMARK] does not work as described in the data sheet. CAPTMARK cannot be used to identify captured values triggered by fault inputs source A or B on the same channel.

Workaround

Use two different channels to timestamp FaultA and FaultB.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.21.4 Capture Overflow

A capture overflow can occur without INTFLAG.ERR being set if a new capture occurs within 3 APB clocks + 3 generic Clock periods from a previous capture.

Workaround

The delay between two capture events must be longer than 3 APB clock periods + 3 generic clock periods.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X				
N					

1.21.5 Advance Capture Mode

Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn’t work if an upper channel is not in one of these mode. Example: when CC[0] = CAPTMIN, CC[1] = CAPTMAX, CC[2] = CAPTEN, and CC[3] = CAPTEN, CAPTMIN and CAPTMAX will not work.

Workaround

Basic capture mode must be set in lower channel and advance capture mode in upper channel.

Example: CC[0] = CAPTEN , CC[1] = CAPTEN , CC[2] = CAPTMIN, CC[3] = CAPTMAX.

All capture will be done as expected.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N					

1.21.6 SYNCBUSY

When clearing STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.

Workaround

To ensure that the register value is properly restored before updating this same register through xx or xxBUF with a new value, the STATUS.xxBUFV flag must be cleared successively two times.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N					

1.21.7 Dithering Mode

Using TCC in Dithering mode with external retrigger events can lead to unexpected stretch of right-aligned pulses, or shrink of left-aligned pulses.

Workaround

Do not use retrigger events or actions when TCC is configured in Dithering mode.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.21.8 PERBUF

In Down-Counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.21.9 TCC with EVSYS in SYNC/RESYNC Mode

The TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Workaround

Use TCC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.21.10 ALOCK Feature

ALOCK feature is not functional.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.22 XOSC/XOSC32K Oscillator

1.22.1 CFD and Clock Switching

When the CFD is enabled for XOSC/XOSC32K and the oscillator input signal is stuck at 1 (i.e., logic high), the clock failure detection works correctly but the switch to the safe clock will fail.

Workaround

Two possible workarounds are:

1. If the main clock source comes from the XOSC/XOSC32K oscillator, then use the WDT in firmware and switch to the safe clock source in firmware at the WDT Reset.
2. Else since the clock failure detection is functional, once the STATUS.CLKFAIL is set and if the STATUS.CLKSW is not set, manually switch to safe clock from firmware to use another source clock instead.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J					
N				X	

1.23 Master Clock (MCLK)

1.23.1 PAC Protection

Writes to the MCLK Control A register (MCLK.CTRLA) do not generate a PAC protection error even if this register has been write-protected using the PAC.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

1.24 Frequency Meter (FRQM)

1.24.1 PAC Protection Error

FREQM reads on the Control B register (FREQM.CTRLB) and generates a PAC protection error.

Workaround

None.

Affected Silicon Revisions

C20/C21 Device	B	C	D	E	F
E/G/J	X	X	X	X	X
N				X	

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001479D):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics for SAM C20/C21 E/G/J at 85°C

Table 45-23 Operating Conditions was updated with a new data for the Res row and Maximum values for Vref and Vcom. The Conditions were updated for Vin.

Table 45-23 Operating Conditions (1)

<table>
<tr><th>Symbol</th><th>Parameters</th><th colspan="2">Conditions</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td rowspan="2">Res</td><td rowspan="2">Resolution</td><td colspan="2">Differential mode</td><td>-</td><td>16</td><td>-</td><td rowspan="2">bits</td></tr>
<tr><td colspan="2">Single-Ended mode (3)</td><td>-</td><td>15</td><td>-</td></tr>
<tr><td>CLK_SDADC</td><td>Sampling Clock Speed</td><td colspan="2">-</td><td>1</td><td>-</td><td>6</td><td rowspan="4">MHz</td></tr>
<tr><td>CLK_SDADC_FS</td><td>Conversion rate</td><td colspan="2">-</td><td colspan="3">CLK_SDADC/4</td></tr>
<tr><td rowspan="2">fs</td><td rowspan="2">Output Data Rate</td><td colspan="2">Free Running mode</td><td colspan="3">CLK_SDADC_FS / OSR</td></tr>
<tr><td colspan="2">Single Conversion mode SKPCNT = N</td><td colspan="3">(CLK_SDADC_FS / OSR) x (N +1)</td></tr>
<tr><td>OSR</td><td>Oversampling ratio</td><td colspan="2">Differential mode</td><td>64</td><td>256</td><td>1024</td><td>Cycles</td></tr>
<tr><td rowspan="4">Vin</td><td rowspan="4">Input Conversion range</td><td rowspan="2">VREF<VDDANA-0.3V</td><td>Differential mode Gaincorr = 0x1</td><td>- VREF</td><td>-</td><td>VREF</td><td rowspan="2">V</td></tr>
<tr><td>Single-Ended mode Gaincorr = 0x1(3)</td><td>0</td><td>-</td><td>VREF</td></tr>
<tr><td rowspan="2">VREF> = VDDANA-0.3V</td><td>Differential mode Gaincorr = 0x1</td><td>-0.7xVREF</td><td>-</td><td>0.7xVREF</td><td rowspan="2">V</td></tr>
<tr><td>Single-Ended mode Gaincorr = 0x1(3)</td><td>0</td><td>-</td><td>0.7xVREF</td></tr>
<tr><td>Vref</td><td>Reference Voltage range</td><td colspan="2"></td><td>1</td><td>-</td><td>VDDANA</td><td>V</td></tr>
<tr><td>Vcom</td><td>Common mode voltage</td><td colspan="2">Differential mode</td><td>0</td><td>-</td><td>VDDANA</td><td>V</td></tr>
</table>

...........continued

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
Cin	Input capacitance		0.425	0.5	0.575	pF
Zin	Input impedance	Differential mode	1/(Cin x CLK_SDADC_FS)			kΩ
		Single-Ended mode (3)	1/(Cin x CLK_SDADC_FS x 2)			
	Input anti-alias filter recommendation (2)	Rext	-	1.0	-	kΩ
		Cext	3.3	-	10	nF

Note:

1. These values are based on simulation and are not covered by test or characterization.
2. External anti-alias filter must be placed in front of each SDADC input to ensure high-frequency signals to not alias into measurement bandwidth. Use capacitors of X5R type for DC measurement, or capacitors of COG or NPO type for AC measurement.
3. This mode corresponds to a Differential mode where the selected AINNx pin is externally grounded.

2.2 Power Consumption for SAM C20/C21 N at 105°C - IDLE0

Table 47-2 Power Consumption was updated with the following information for IDLE0:

- Typical was updated from 1.9 to 2.0
- Maximum was updated from 2.5 to 3.2

Table 47-2. Power Consumption (1)

Mode	Conditions	Ta	Vcc	Typ.	Max.	Units
ACTIVE	CPU running a While 1 algorithm	25°C	5.0V	3.8	4.2	mA
		105°C	5.0V	4.0	5.0	
	CPU running a While 1 algorithm	25°C	3.0V	3.7	4.1	mA
		105°C	3.0V	4.0	5.0	
	CPU running a While 1 algorithm. with GCLKIN as reference	25°C	5.0V	71*Freq+160	78*Freq+162	µA (with freq in MHz)
		105°C	5.0V	71*Freq+374	68*Freq+1564	
	CPU running a Fibonacci algorithm	25°C	5.0V	4.7	5.2	mA
		105°C	5.0V	5.0	6.1	
	CPU running a Fibonacci algorithm	25°C	3.0V	4.7	5.1	mA
		105°C	3.0V	5.0	6.0	
	CPU running a Fibonacci algorithm. with GCLKIN as reference	25°C	5.0V	90*Freq+163	99*Freq+168	µA (with freq in MHz)
		105°C	5.0V	90*Freq+379	90*Freq+1568	
	CPU running a CoreMark algorithm	25°C	5.0V	5.9	6.4	mA
		105°C	5.0V	6.3	7.1	
	CPU running a CoreMark algorithm	25°C	3.0V	5.2	5.7	mA
		105°C	3.0V	5.5	6.6	
	CPU running a CoreMark algorithm. with GCLKIN as reference	25°C	5.0V	115*Freq+167	126*Freq+167	µA (with freq in MHz)
		105°C	5.0V	118*Freq+383	110*Freq+1583	
IDLE0		25°C	5.0V	1.8	2.4	mA
		105°C	5.0V	**2.0**	**3.2**	
IDLE2		25°C	5.0V	1.2	1.7	mA
		105°C	5.0V	1.5	2.6	
STANDBY	XOSC32K running RTC running at 1.024 kHz	25°C	5.0V	15.9	37.0	µA
		105°C	5.0V	187.0	602.0	
	XOSC32K and RTC stopped	25°C	5.0V	14.6	35.0	
		105°C	5.0V	185.0	600.0	

Note:

1. These values are based on characterization.

2.3 Analog-to-Digital Converter (ADC) Characteristics for SAM C20/C21 N at 105°C

Table 47-5 Operating Conditions was updated with the new information for the Rs Sampling Rate. New values were implemented for fadc, Ts, Vcnv, and Vref.

Table 47-5 Operating Conditions (1)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
Res	Resolution	-	-	-	12	bits

...........continued

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
Rs	**Sampling rate**[(2)]	**SAMPLEN = 3 resolution 12 bit (CTRLC.RESSEL = 0)**	10	-	1000	ksps
Nb_cycles	Differential mode Number of ADC clock cycles SAMPCTRL.OFFCOMP = 1	resolution 12 bit (CTRLC.RESSEL= 0)	-	16	-	cycles
		resolution 10 bit (CTRLC.RESSEL = 2)		14		
		resolution 8 bit (CTRLC.RESSEL = 3)		12		
	Differential mode Number of ADC clock cycles SAMPCTRL.OFFCOMP = 0 SAMPLEN corresponds to the decimal value of SAMPCTRL.SAMPLEN[5:0] register	resolution 12 bit (CTRLC.RESSEL = 0)	-	SAMPLEN+13	-	cycles
		resolution 10 bit (CTRLC.RESSEL = 2)		SAMPLEN+11		
		resolution 8 bit (CTRLC.RESSEL = 3)		SAMPLEN+9		
	Single-ended mode Number of ADC clock cycles SAMPCTRL.OFFCOMP = 1	resolution 12 bit (CTRLC.RESSEL = 0)	-	16	-	cycles
		resolution 10 bit (CTRLC.RESSEL = 2)		15		
		resolution 8 bit (CTRLC.RESSEL = 3)		13		
	Single-ended mode Number of ADC clock cycles SAMPCTRL.OFFCOMP = 0 SAMPLEN corresponds to the decimal value of SAMPCTRL.SAMPLEN[5:0] register	resolution 12 bit (CTRLC.RESSEL = 0)	-	SAMPLEN+13	-	cycles
		resolution 10 bit (CTRLC.RESSEL = 2)		SAMPLEN+12		
		resolution 8 bit (CTRLC.RESSEL = 3)		SAMPLEN+10		
fadc	**ADC Clock frequency**		**160**	**-**	**16000**	**kHz**
Ts	**Sampling time**	**SAMPCTRL.OFFCOMP = 1**	**250**	**-**	**25000**	**ns**
		SAMPCTRL.OFFCOMP = 0	**(SAMPLEN+1)/ fadc**	**-**	**-**	**s**
	Sampling time with DAC as input		**3**	**-**	**-**	**µs**
	Sampling time with Bandgap as input		**10**	**-**	**-**	**µs**
Vcnv	**Conversion range**	**Differential mode**	**-VREF**	**-**	**+VREF**	**V**
		Single-ended mode	**0**	**-**	**VREF**	
Vref	**Reference input**		**2**	**-**	**VDDANA-0.6**	**V**
Vin	Input channel range	-	0	-	VDDANA	V
Vcmin	Input common mode voltage	CTRLC.R2R = 1	0.2	-	VREF-0.2	V
		CTRLC.R2R = 0	VREF/2-0.2	-	VREF/2+0.2	V
CSAMPLE	Input sampling capacitance		-	1.6	4.5	pF
RSAMPLE	Input sampling on-resistance	For a sampling rate at 1 Msps	-	1000	1715	Ω

...........continued

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
Rref	Reference input source resistance		0	-	1000	kΩ

Note:

1. These values are based on simulation, and are not covered by test limits in production or characterization.
2. Sampling rate (in samples per second) is equal to Nb_cycles/fadc.

2.4 Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics for SAM C20/C21 N at 105°C

Table 47-8 Operating Conditions was updated with new values for Res, CLK_SDADC, CLK_SDADC_FS, Vin, Vref, and Vcom.

Table 47-8 Operating Conditions (1)

Symbol	Parameters	Conditions		Min.	Typ.	Max.	Unit
Res	Resolution	Differential mode		-	16	-	bits
		Single-Ended mode(3)		**-**	**15**	**-**	
CLK_SDADC	**Sampling Clock Speed**			**1**	**-**	**6**	MHz
CLK_SDADC_FS	**Conversion rate**			**CLK_SDADC/4**			
fs	Output Data Rate	Free-Running mode		CLK_SDADC_FS / OSR			
		Single-Conversion mode , SKPCNT = N		(CLK_SDADC_FS / OSR) x (N+1)			
OSR	Oversampling ratio	Differential mode		64	256	1024	Cycles
Vin	**Input Conversion range**	**VREF<VDDANA-0.3V**	**Differential mode** **Gaincorr = 0x1**	**- VREF**	**-**	**VREF**	**V**
			Single-Ended mode(3) **Gaincorr = 0x1**	**0**	**-**	**VREF**	
		VREF>=VDDANA-0.3V	**Differential mode** **Gaincorr = 0x1**	**-0.7xVREF**	**-**	**0.7xVREF**	**V**
			Single-Ended mode(3) **Gaincorr = 0x1**	**0**	**-**	**0.7xVREF**	
Vref	Reference Voltage range			1	-	**VDDANA**	V
Vcom	Common mode voltage	Differential mode		0	-	**VDDANA**	V
Cin	Input capacitance			0.425	0.5	0.575	pF
Zin	Input impedance	Differential mode		1/(Cin x CLK_SDADC_FS)			kΩ
		Single-Ended mode(3)		1/(Cin x CLK_SDADC_FS x 2)			
	Input anti-alias filter recommendation(2)	Rext		-	1.0	-	kΩ
		Cext		3.3	-	10	nF

Note:
1. These values are based on simulation, and are not covered by test or characterization.
2. External Anti-alias filter must be placed in front of each SDADC input to ensure high-frequency signals to not alias into measurement bandwidth. Use capacitors of X5R type for DC measurement or capacitors of COG or NPO type for AC measurement.
3. This mode corresponds to a differential mode where the selected AINNx pin is externally grounded.

2.5 Current Consumption for SAM C20/C21 E/G/J AEC-Q100 Grade 1 at 125℃ - IDLE0

Table 48-3 Current Consumption was updated with the following information for IDLE0:
- Typical was updated from 1.7 to 1.8

Table 48-3. Current Consumption (1)

Mode	conditions	Ta	Vcc	Typ.	Max.	Units
ACTIVE	CPU running a While 1 algorithm	25°C	5.0V	3.8	4.2	mA
		125°C	5.0V	4.4	5.4	
	CPU running a While 1 algorithm	25°C	3.0V	3.7	4.2	mA
		125°C	3.0V	4.4	5.4	
	CPU running a While 1 algorithm, with GCLKIN as reference	25°C	5.0V	71*Freq+160	79*Freq+166	µA (with freq in MHz)
		125°C	5.0V	72*Freq+659	68*Freq +1866	
	CPU running a Fibonacci algorithm	25°C	5.0V	4.7	5.2	mA
		125°C	5.0V	5.3	6.4	
	CPU running a Fibonacci algorithm	25°C	3.0V	4.7	5.2	mA
		125°C	3.0V	5.3	6.3	
	CPU running a Fibonacci algorithm, with GCLKIN as reference	25°C	5.0V	90*Freq+163	100*Freq +173	µA (with freq in MHz)
		125°C	5.0V	91*Freq+664	88*Freq +1863	
	CPU running a CoreMark algorithm	25°C	5.0V	5.9	6.5	mA
		125°C	5.0V	6.7	8.0	
	CPU running a CoreMark algorithm	25°C	3.0V	5.2	5.7	mA
		125°C	3.0V	5.9	6.9	
	CPU running a CoreMark algorithm, with GCLKIN as reference	25°C	5.0V	115*Freq +167	127*Freq +169	µA (with freq in MHz)
		125°C	5.0V	119*Freq +668	122*Freq +1849	
IDLE0		25°C	5.0V	**1.8**	1.9	mA
		125°C	5.0V	2.3	3.4	
IDLE2		25°C	5.0V	1.2	1.3	mA
		125°C	5.0V	1.8	3.1	

...........continued

Mode	conditions	Ta	Vcc	Typ.	Max.	Units
STANDBY	XOSC32K running RTC running at 1.024 kHz	25°C	5.0V	15.9	37	µA
		125°C	5.0V	363.4	950	
	XOSC32K and RTC stopped	25°C	5.0V	14.6	35	
		125°C	5.0V	361.4	953	

Note:

1. These values are based on characterization.

3. Appendix A: Revision History

Rev E Document (05/2020)
The following Data Sheet Clarifications were added in this revision:

- Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics for SAM C20/C21 E/G/J at 85°C
- Power Consumption for SAM C20/C21 N at 105°C - IDLE0
- Analog-to-Digital Converter (ADC) Characteristics for SAM C20/C21 N at 105°C
- Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics for SAM C20/C21 N at 105°C
- Current Consumption - IDLE0 for SAM C20/C21 E/G/J AEC-Q100 Grade 1 at 125℃

Added the following silicon issues:

- 1.8.13 Potential hard fault on standby entry
- 1.17.14 Over consumption in standby

Rev D Document (01/2019)
The following updates were included in this revision:

- New silicon revision F for SAM C20/21 E/G/J product family is introduced in this document.
- Added the following silicon issues:
  - OSC48M: 1.2.2 Division Ratio
  - FDPLL: 1.3.4 FDPLL Loop Divider Ratio
  - AC: 1.5.4 Hysteresis
  - AC: 1.5.5 Power Consumption
  - ADC: 1.4.7 Differential and Single Ended Mode
  - ADC: 1.4.8 Power Consumption
  - CAN: 1.6.15 DAR Mode
  - CAN: 1.6.16 TxFIFO
  - CAN: 1.6.17 High Priority Message Interrupt
  - CAN: 1.6.18 INTFLAG Status
  - CCL: 1.7.2 Sequential Logic
  - CCL: 1.7.3 Enable Protected Registers
  - CCL: 1.7.4 PAC Protection Error
  - DMAC: 1.10.4 Linked Descriptors
  - MCLK: 1.23.1 PAC Protection
  - PORT: 1.13.3 Write-Protect
  - RTC: 1.16.2 COUNTSYNC
  - RTC: 1.16.3 Write Corruption
  - SERCOM: 1.17.3 SPI
  - SERCOM: 1.17.4 USART
  - SERCOM: 1.17.5 I2C
  - SERCOM: 1.17.6 Repeated Start
  - SERCOM: 1.17.7 Repeated Start I2C
  - SERCOM: 1.17.8 CLKHOLD Bit Status in I2C
  - SERCOM: 1.17.9 NACK and Repeated Start in I2C Master Mode
  - SERCOM: 1.17.10 10-bit Addressing Mode
  - SERCOM: 1.17.11 I2C in Slave Mode
  - SERCOM: 1.17.12 Collision Detection
  - SERCOM: 1.17.13 Quick Command
  - SDADC: 1.18.4 Power Consumption

  - TCC: 1.21.8 PERBUF
  - TCC: 1.21.9 TCC with EVSYS in SYNC/RESYNC Mode
  - TCC: 1.21.10 ALOCK Feature
  - FRQM: 1.24.1 PAC Protection Error
- The following silicon issues have been fixed in the SAM C20/21 E/G/J device silicon revision F:
  - USART: 1.17.2 Auto-baud Mode
  - RTC: 1.16.2 COUNTSYNC
  - EVSYS: 1.12.2 Overrun Flag Trigger
  - EIC: 1.11.3 Spurious Flag
  - EIC: 1.11.4 False NMI Interrupt
  - AC: 1.5.2 Low-Power Mode with Hysteresis

Rev C Document (9/2018)

- Added silicon issues for EVSYS: Software Event, Event Channel Configuration
- Added silicon issues for ADC (Reference Buffer Offset)
- Added silicon issues for XOSC/XOSC32K Oscillator (CFD and Clock Switching)

Rev B Document (6/2017)

This revision includes the following updates:

- Updated SAM C20 Family Silicon Device Identification (see Table 1. SAM C20 Family Silicon Device Identification)
- Updated SAM C21 Family Silicon Device Identification (see Table 2. SAM C21 Family Silicon Device Identification)
- Updated silicon issues Device (DMA Write Access), Device (OSC48M Accuracy), and EIC (Edge Detection)

Rev A Document (5/2017)

Initial release of this document.

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