RFD16N05, RFD16N05SM

HARRIS SEMICONDUCTOR

16A, 50V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- **16A, 50V**
- **$r_{DS(ON)} = 0.047\Omega$**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**
- **+175^{o}C Operating Temperature**

Description

The RFD16N05 and RFD16N05SM N-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

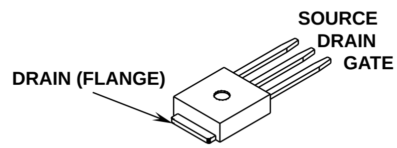
PART NUMBER	PACKAGE	BRAND
RFD16N05	TO-251AA	F16N05
RFD16N05SM	TO-252AA	F16N05

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD16N05SM9A.

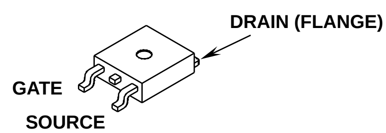
Formerly developmental type TA09771.

Packaging

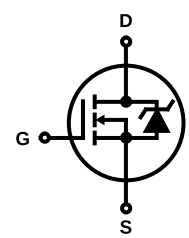
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD16N05, RFD16N05SM	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage	V_{DGR}	50	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	72	W
Derate above +25^{o}C		0.48	W/^{o}C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^{o}C
Soldering Temperature of Leads for 10s	T_L	260	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **2267.3**

Electrical Specifications

$T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	μA
			$T_C = +150^oC$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 16A$, $V_{GS} = 10V$		-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 25V$, $I_D = 8A$, $R_L = 3.125\Omega$, $V_{GS} = 10V$, $R_{GS} = 25\Omega$		-	-	65	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	55	-	ns
Fall Time	t_F			-	30	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 40V$, $I_D = 16A$, $R_L = 2.5\Omega$	-	-	80	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	-	2.2	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	900	-	pF
Output Capacitance	C_{OSS}			-	325	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	2.083	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 16A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

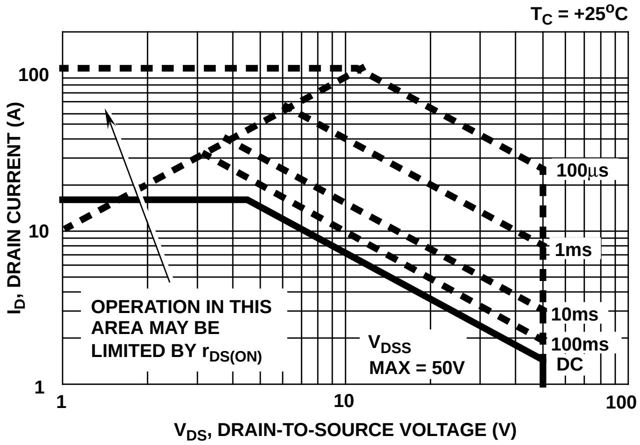


FIGURE 1. SAFE OPERATING AREA CURVE

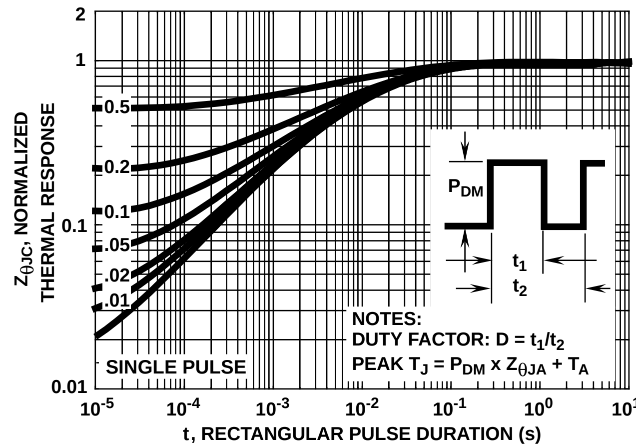


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

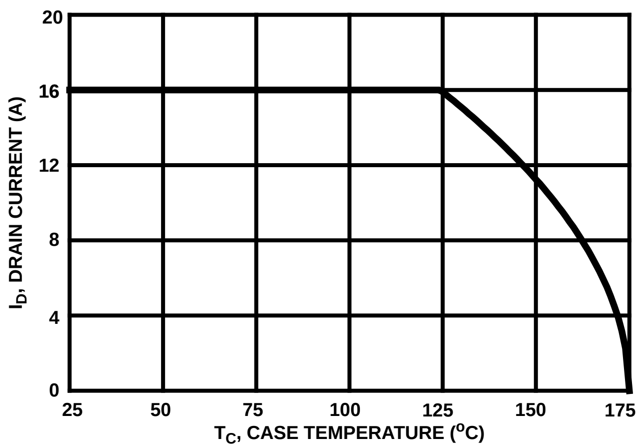


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

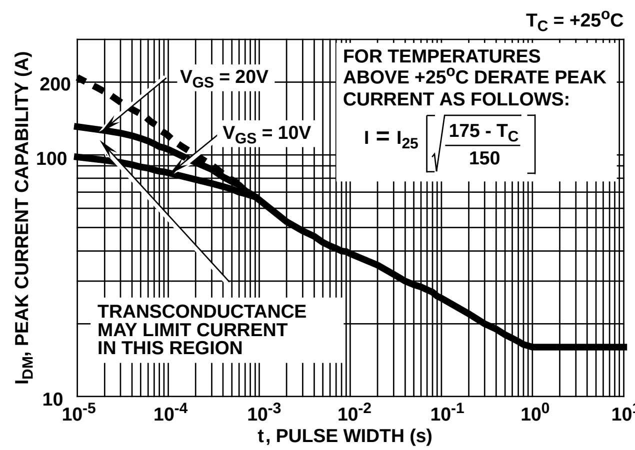


FIGURE 4. PEAK CURRENT CAPABILITY

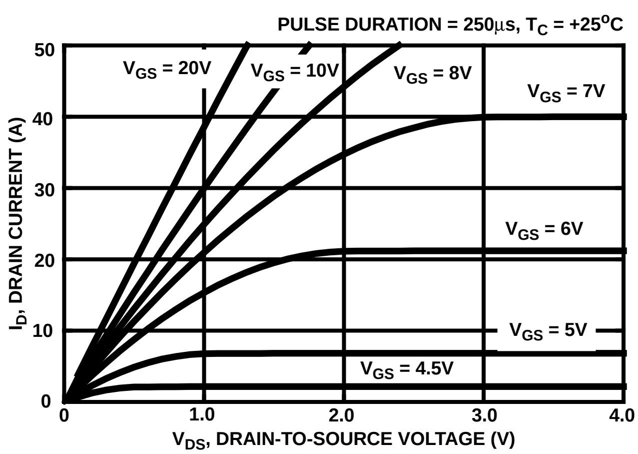


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

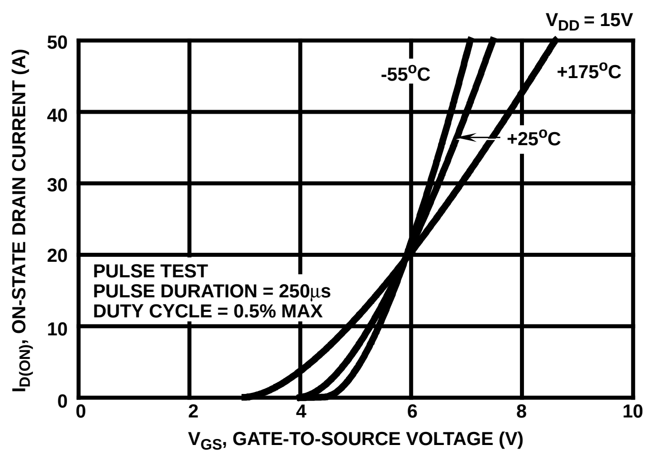


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

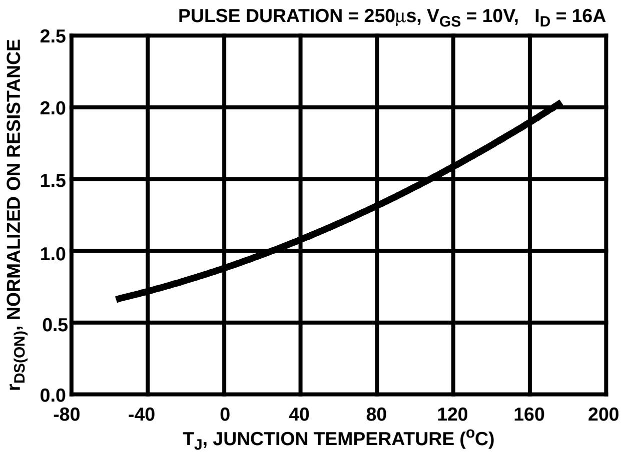


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

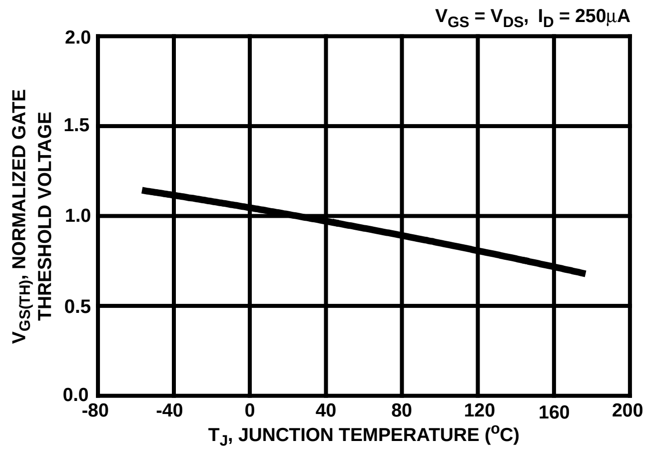


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

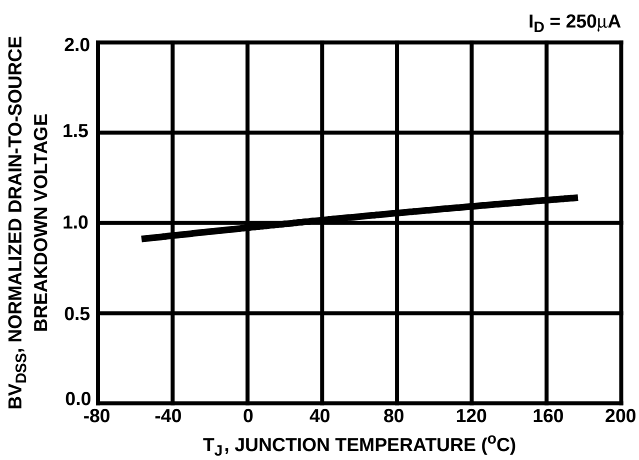


FIGURE 9. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

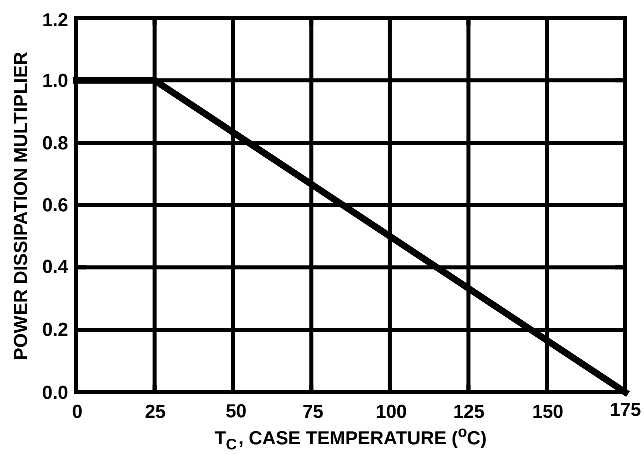


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

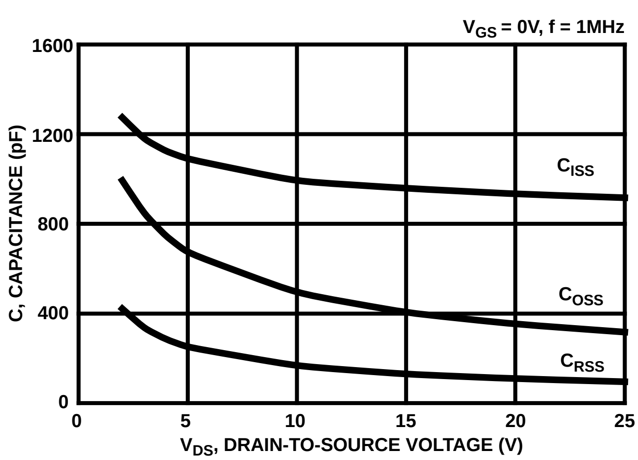


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

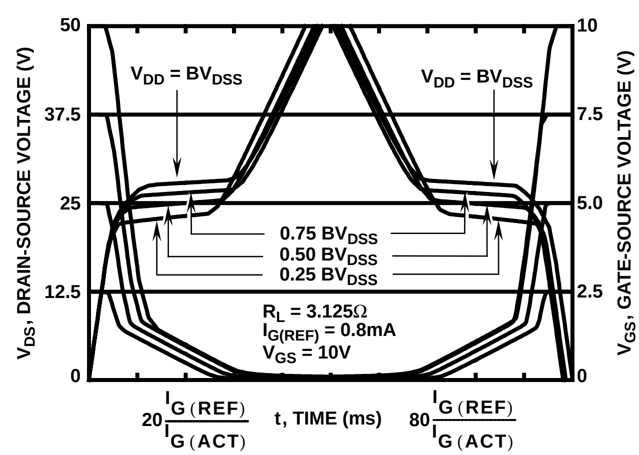


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

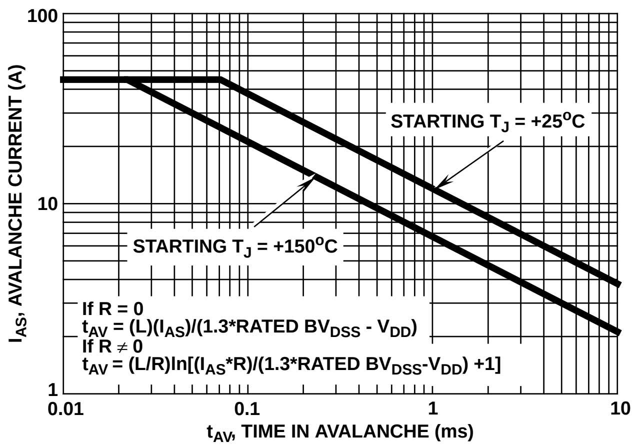


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.
REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

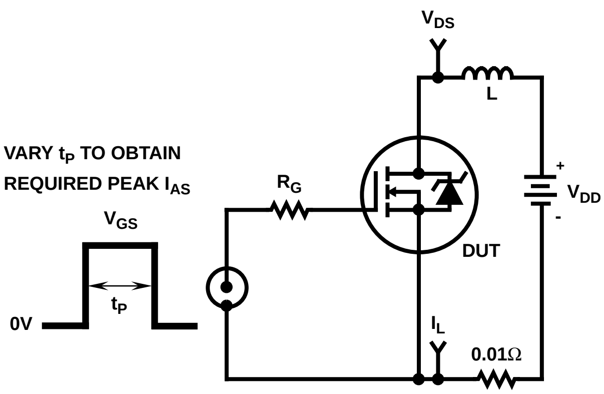


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

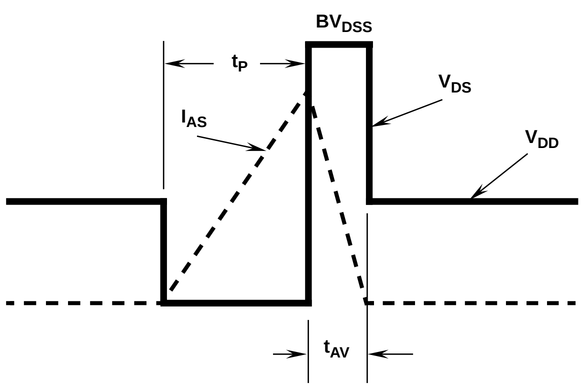


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

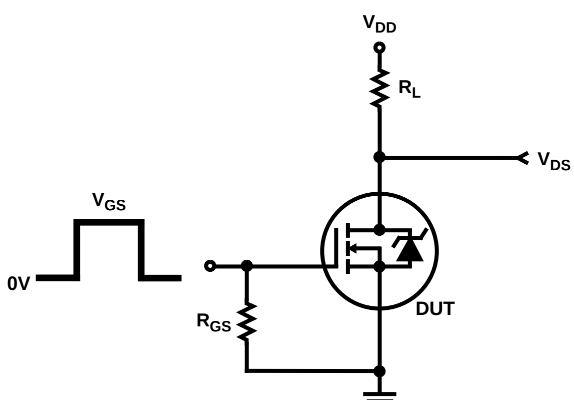


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

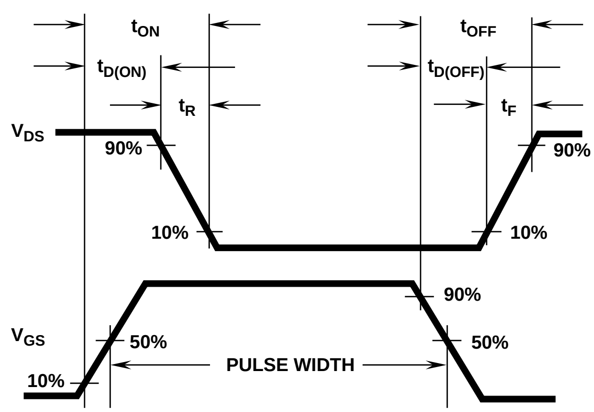
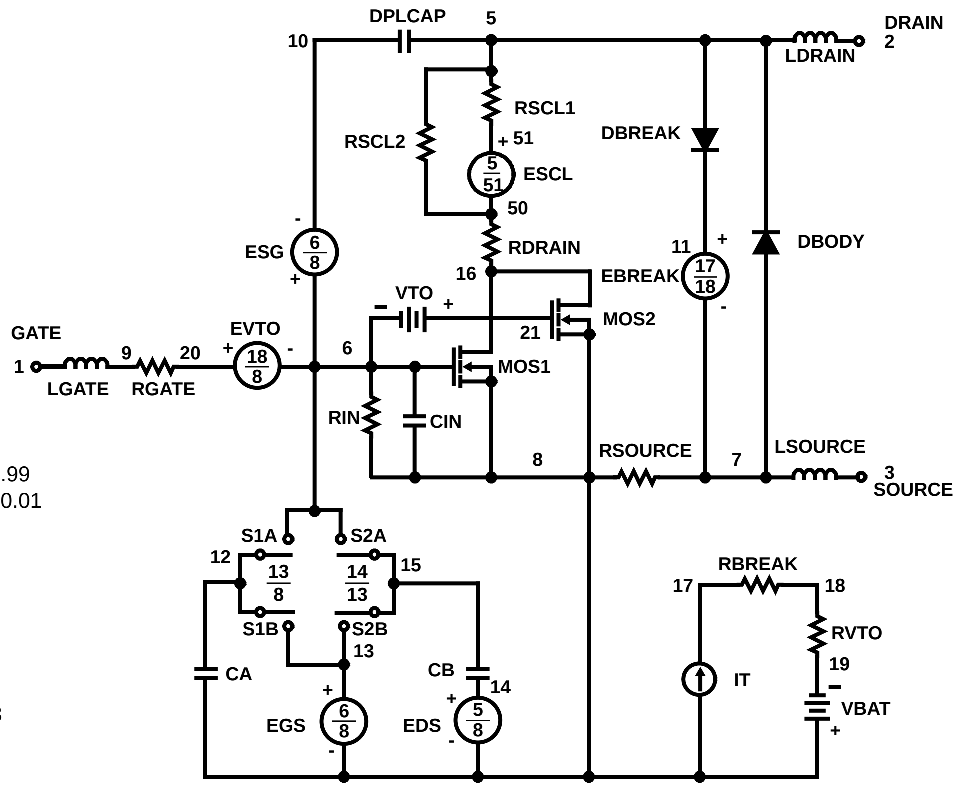


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD16N05, RFD16N05SM

.SUBCKT RFD16N05 2 1 3 ; rev 10/31/94

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CA 12 8 1.788e-10
CB 15 14 1.875e-10
CIN 6 8 8.33e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.56e-9
LSOURCE 3 7 4.13e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.4e-3
RGATE 9 20 3.0
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 21.5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.82

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/94,7))}

.MODEL DBDMOD D (IS = 2.5e-13 RS = 7.1e-3 TRS1 = 3.04e-3 TRS2 = -10e-6 CJO = 1.12e-9 TT = 5.6e-8)
.MODEL DBKMOD D (RS = 2.51e-1 TRS1 = -6.57e-4 TRS2 = 1.66e-6)
.MODEL DPLCAPMOD D (CJO = 6.1e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.96 KP = 16.68 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3 TC2 = -7.19e-7)
.MODEL RDSMOD RES (TC1 = 5.45e-3 TC2 = 1.66e-5)
.MODEL RSCLMOD RES (TC1 = 1.25e-3 TC2 = 17e-6)
.MODEL RVTOMOD RES (TC1 = -5.15e-3 TC2 = -4.83e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.25 VOFF= -3.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.25 VOFF= -5.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.56 VOFF= 5.56)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 5.56 VOFF= 0.56)

.ENDS
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NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.