RE01 Group (256-KB Flash Memory)

Renesas Microcontrollers

R01DS0369EJ0100
Rev.1.00
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64 MHz, 32-bit Arm® Cortex®-M0+, 256-KB flash memory, 128-KB SRAM, energy harvesting control circuit, MIP LCD controller, 2D graphic engine, 14-bit ultra-low power consumption A/D converter, VREF circuit, RTC, sub-clock correction circuit (theoretical regulation), security function (optional), SPI, quad SPI

Features

■ Arm Cortex-M0+ core incorporated
- Maximum operating frequency: 64 MHz
- Arm® Memory Protection Unit (Arm MPU) with 8 regions
- CoreSight™ Debug Port: SW-DP

■ Power-aving functions
- Back-bias control function based on silicon-on-thin-buried-oxide (SOTB™) process technology
- Operation at ultra-low power-supply voltages (from 1.62 V to 3.6 V)
- Three power control modes based on the operating frequency
- Four low power consumption modes
- Three power supply modes

■ On-chip Code flash memory
- 256-Kbyte code flash memory
- No cycles of waiting for access in operation at or below 32 MHz; one cycle of waiting at frequencies above 32 MHz
- Function for area protection prevents erroneous overwriting or tampering

■ On-chip SRAM
- 128-Kbyte SRAM with no access wait cycles

■ Data transfer
- Four DMA controllers
- Single data transfer controller (DTC)

■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) can be set.

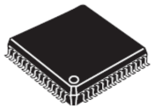
■ Multiple clock sources
- External crystal oscillator (main clock): 8 to 32 MHz
- External crystal oscillator (sub-clock): 32.768 kHz
- High-speed on-chip oscillator (HOCO): 24, 32, 48, or 64 MHz
- Middle-speed on-chip oscillator (MOCO): 2 MHz
- Low-speed on-chip oscillator (LOCO): 32 kHz
- Independent watchdog timer on-chip oscillator: 16 kHz

■ Energy harvesting control
- A power generation element is directly connectable.
- High-speed startup is possible without having to wait for the charging of a secondary battery.
- Function to prevent a secondary battery from overcharging

■ Independent watchdog timer
- 14-bit counter, 16-kHz (1/2 LOCO clock frequency) operation

■ Sub-clock correction circuit (CCC)
- The CCC corrects the accuracy of oscillation every 16 seconds (theoretical regulation).
- Events can be generated per second in deep software standby mode.

■ Communication functions
- Two serial peripheral interfaces
  Single 128-bit buffer for which up to eight commands can be specified
  Single 32-bit buffer for which one command can be specified
- Single quad serial peripheral interface connectable to an external flash memory
- Two I^{2}C bus interfaces
- • Five serial communications interfaces (SCIg)
  Asynchronous, clock-synchronous, simple I^{2}C, simple SPI, and smart card interfaces, and IrDA interface version 1.0 (the latter is only applicable to SCI0)
- Two serial communication interfaces (SCIi) each having a 16-byte FIFO



PLQP0100KB-B
14 × 14mm, 0.5-mm pitch

PLQP0064KB-A
10 × 10mm, 0.5-mm pitch

■ Various analog circuits
- Single 14-bit successive approximation A/D converter
  High precision: 8 channels, standard precision: 4 channels
- Single temperature sensor for measuring the internal temperature of the chip
- VREF circuit for the 14-bit A/D converter reference voltage

■ Various timer circuits
- Six general PWM timers (GPT)
  Two 32-bit counters
  Four 16-bit counters
- Four asynchronous general-purpose timers (AGT) that can be used in standby mode
  Two 32-bit counters
  Two 16-bit counters
- Two 8-bit timers (TMR)
- Single realtime clock (RTC)
- Single watchdog timer (WDT)
- Single low-speed timer (LST) that operates at 1 kHz
  A circuit for converting hexadecimal numbers to decimal numbers for use as a stopwatch

■ Human machine interfaces
- Single memory-in-pixel (MIP) LCD controller (MLCD) Parallel interface is supported.
- Single 2D graphics data conversion circuit (GDT)

■ Security functions (optional)
- Single Trusted Secure IP Lite (TSIP)
  - AES (128- or 256-bit key length, supporting ECB, CBC, CMAC, GCM, and others)
  - Key wrapping protects against the leakage of the encryption keys of users.
  - An access management circuit disables illicit access to the encryption engine.
  - Using the other security functions together with area protection enables secure booting and secure over-the-air (OTA) software updates.

■ Operating voltage and temperature range
- VCC = IOVCC = IOVCCn= AVCC0 = 1.62 V to 3.6 V
  IOVCCn and AVCC0 can each be independently set to a voltage within the range between 1.62 V and 3.6 V.
- Ta: –40 to +85°C

1. Overview

1.1 Function Outline

Table 1.1 to Table 1.11 show the outline of maximun specifications. Tthe number of peripheral channels differs depending on the number of pins of the package. For details, see Table 1.13.

Table 1.1 Arm core

Feature	Functional description
Arm® Cortex®-M0+ core	• Maximum operating frequency: up to 64 MHz • Arm Cortex-M0+ core: – Revision: r0p1-00rel0 – Armv6-M architecture profile – Single-cycle integer multiplier • Arm Memory Protection Unit (MPU): – Armv6 Protected Memory System Architecture – Eight protect regions • SysTick timer: – Driven by SYSTICCLK (LOCO or ICLK)

Table 1.2 Memory

Feature	Functional description
Code flash memory	• Maximum 256 KB of code flash memory. • No cycles of waiting for access in operation at or below 32 MHz; one cycle of waiting at frequencies above 32 MHz • Prefetch function • On-board programming (three types): – Programming in serial programming mode (SCI boot mode) – Programming in on-chip debug mode – Programming by a routine for code flash memory rewriting within a user program
SRAM	• Maximum 128 KB of SRAM SRAM0: 0x2000_0000 to 0x2000_7FFF SRAM1: 0x2000_8000 to 0x2001_FFFF Both areas are available during low leakage current mode. • 64 MHz, No cycles of waiting for access

Table 1.3 System (1 of 2)

Feature	Functional description
Startup modes	Three startup modes: • Normal startup mode • Energy harvesting startup mode • SCI boot mode
Resets	The MCU provides 13 resets. The resets are classified into two types: System resets that initialize the MCU and power shutdown reset that does not initialize the MCU.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin and VBAT_EHC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVDBAT). LVD0 and LVD1 measure the voltage level input to the VCC pin, and LVDBAT measures the voltage level input to the VBAT_EHC pin. LVD registers allow your application to configure detection of VCC and VBAT_EHC changes at various voltage thresholds.
Clocks	• The MCU has the following clock generation circuits. – Main clock oscillator (MOSC) – Sub-clock oscillator (SOSC) – High-speed on-chip oscillator (HOCO) – Middle-speed on-chip oscillator (MOCO) – Low-speed on-chip oscillator (LOCO) – IWDT-dedicated on-chip oscillator (IWDTLOCO) • Clock output support – CLKOUT pin (capable of outputting all types of clock signals) – CLKOUT32K pin (capable of outputting SOSC clock signals)

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Power-saving functions	The MCU has several functions for power saving, such as setting clock dividers, stopping modules, selecting power control mode in operating mode, transitioning to low power consumption mode, and power supply mode per domain. ● Three power control modes based on the operating frequency – Boost mode (up to 64 MHz) – Normal mode • High-speed mode (up to 32 MHz) • Low-speed mode (up to 2 MHz) – Low leakage current mode (32.768 kHz) ● Five low-power consumption modes – Operating mode – Sleep mode – Software standby mode – Snooze mode – Deep software standby mode ● Three power supply modes – All-power supply mode (ALLPWON) – Flash-excluded power supply mode (EXFPWON) – Minimum power supply mode (MINPWON)
Back-bias voltage control[*1] (VBBC) function	Program control of the back bias voltage enables low leakage current operation in the low leakage current mode.
Energy harvesting control circuit (EHC)	Starting up of the MCU in the power-saving mode is possible by controlling the power generating element, storage capacitor, and secondary battery.
Register write protection (RWP)	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided.
Key Interrupt Function (KINT)	The key interrupt function (KINT) is generated a key interrupt by detecting a valid edge on the key interrupt input pin.

Note 1. Voltage for charging the VBP and VBN pins

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to interconnect (link) modules, allowing direct link between modules without CPU intervention. Event signals can be output regardless of the setting of the associated interrupt request enable bit.

Table 1.5 Direct memory access

Feature	Functional description
DMA Controller (DMAC)	This MCU incorporates an 4-channel direct memory access controller (DMAC). The DMAC is a module to transfer data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 4 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter.
Port Output Enable for GPT (POE)	The Port Output Enable (POE) function can place the General PWM Timer (GPT) output pins in the output disable state
Low power Asynchronous General Purpose Timer (AGT, AGTW)	The low power Asynchronous General Purpose Timer (AGT, AGTW) is a 16-bit, 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
8-bit timers (TMR)	8-bit timer (TMR) can count external events and provide multiple functions such as clearing counters, and outputting interrupt requests and pulses of required duty cycles, using the compare match signals with two registers.
Wake Up Timer (WUPT)	The wake up timer based on 32-bit counter provides multiple functions such as resetting count, and outputting interrupt requests and pulses to external pins when an overflow occurs.
Realtime Clock (RTC)	The realtime clock (RTC) has three counting modes, calendar count mode, binary count mode, and 32-kHz count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.
Clock Correction Circuit (CCC)	The CCC corrects the oscillation accuracy every 16 seconds for the 32.768-kHz subclock. ● Clock output after correction: 2.048 kHz/512 Hz ● Signal output (CCCOUT): Selectable from 512 Hz/1 Hz, or RTC output (1 Hz/64 Hz) ● Support of function for event linking by the ELC
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.
Low-Speed Clock Timer (LST)	The low-speed clock timer (LST) contains a 1-kHz timer-counter and a circuit for converting hexadecimal numbers to decimal numbers. This is a 13-bit timer that can be used to indicate a count that needs to be displayed in decimal. ● Capable of counting from 0.000 to 1.999 seconds (in units of 0.001 seconds) ● A value in decimal notation can be directly stored in a register

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 7 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 1) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
IrDA Interface (IrDA)	The IrDA (Infrared Data Association) interface sends and receives IrDA data communication waveforms in association with SCI1 based on the IrDA standard 1.0.

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 2 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
Serial Peripheral Interface (SPI)	The SPI provides high-speed full-duplex and transmit-only synchronous serial communications with multiple processors and peripheral devices.
Quad Serial PeripheralInterface (QSPI)	The QSPI is connectable to a serial ROM that has an SPI-compatible interface. ● 1 channel ● Support for extended SPI, dual SPI, and quad SPI protocols ● Configurable to SPI mode 0 and SPI mode 3 ● Address width selectable from 8, 16, 24, or 32 bits
External bus	QSPI area: Connectable to the QSPI (external device interface)

Table 1.8 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter incorporated Up to 12 analog input channels are selectable. The analog input channels and the temperature sensor output are selectable for conversion. The A/D conversion accuracy is selectable between 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. ● 14 bits × 12 channels (maximum value) (high accuracy: 8 channels, standard accuracy: 4 channels) ● Resolution: 14 bits (14-bit or 12-bit conversion selectable) ● Operating mode: Scan mode (single-scan mode, continuous-scan mode, or group-scan mode) ● Group A priority control (only for group-scan mode) ● Variable sampling state count ● A/D-converted value addition mode or average mode selectable ● Disconnection detection assist function ● Double-trigger mode (duplication of A/D conversion data) ● Support of function for event linking by the ELC ● Automatic clear function of A/D data registers ● Compare function for window A and window B ● Digital compare function Comparison of values in the comparison register and the data register, and comparison between values in the data registers
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application.
Reference voltage generation circuit (VREF)	The circuit generates two types (1.25 V/2.5 V) of reference voltage. The generated voltage can be used as the reference voltage for the ADC.

Table 1.9 Human machine interfaces (1 of 2)

Feature	Functional description
MIP LCD controller (MLCD)*1	MIP-method liquid crystal panel driver circuit incorporated

Table 1.9 Human machine interfaces (2 of 2)

Feature	Functional description
2D graphics data conversion circuit (GDT)	A graphic accelerator circuit that handles 2D image processing incorporated ● Handling of up to 32-byte image data. Up to 63 × 64 bits for conversion of glyph data into image data. ● Rotations of 90-degree clockwise, 90-degree counterclockwise, vertical flip, and horizontal flip ● Scaling down to 1/8, 2/8, 3/8, 4/8, 5/8, 6/8, or 7/8 by pixel averaging and to 1/2 by pixel skipping ● Inversion allows bit-wise inversion of images; 1 is inverted to 0, and vice versa. ● Monochrome compositing of a foreground image, background image, and trimming image ● Color compositing of a foreground image and background image, and setting of priority color and transparent color ● Scrolling of an image in 1-bit units ● Conversion of glyph data into image data ● Colorization of monochrome images by RGB values ● Color data sorting allows separate R, G, and B images in memory to be sorted into a single area in order of R, G, and B ● Endian conversion

Note 1. General three-wire MIP can be supported by combining SPI0 and GDT.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows monitoring of reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.
Divider (DIV)	A circuit for handling high-speed division for signed 32-bit fixed point data ● Dividend: Signed 32-bit data ● Divisor: Signed 32-bit data
Data inversion and Logical operation (DIL)	● Data inversion – The bit inversion value of input data is output ● AND, OR, and XOR operations of two input data – Data inversion enables NAND, NOR, and XNOR operations ● Conversion of data alignment per byte width (byte swap) ● Bit order inversion of MSB and LSB every 8 bits

Table 1.11 Security

Feature	Functional description
Trusted Secure IP Lite (TSIP-Lite)	● Access management circuit available ● Security algorithms: – Common key cryptosystem (symmetrical cryptography): AES key length: 128 bits/256 bits – Encryption usage modes: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR, CCM

1.2 Block Diagram

Figure 1.1 shows a block diagram of the superset. Some individual devices within the group have a subset of the features.

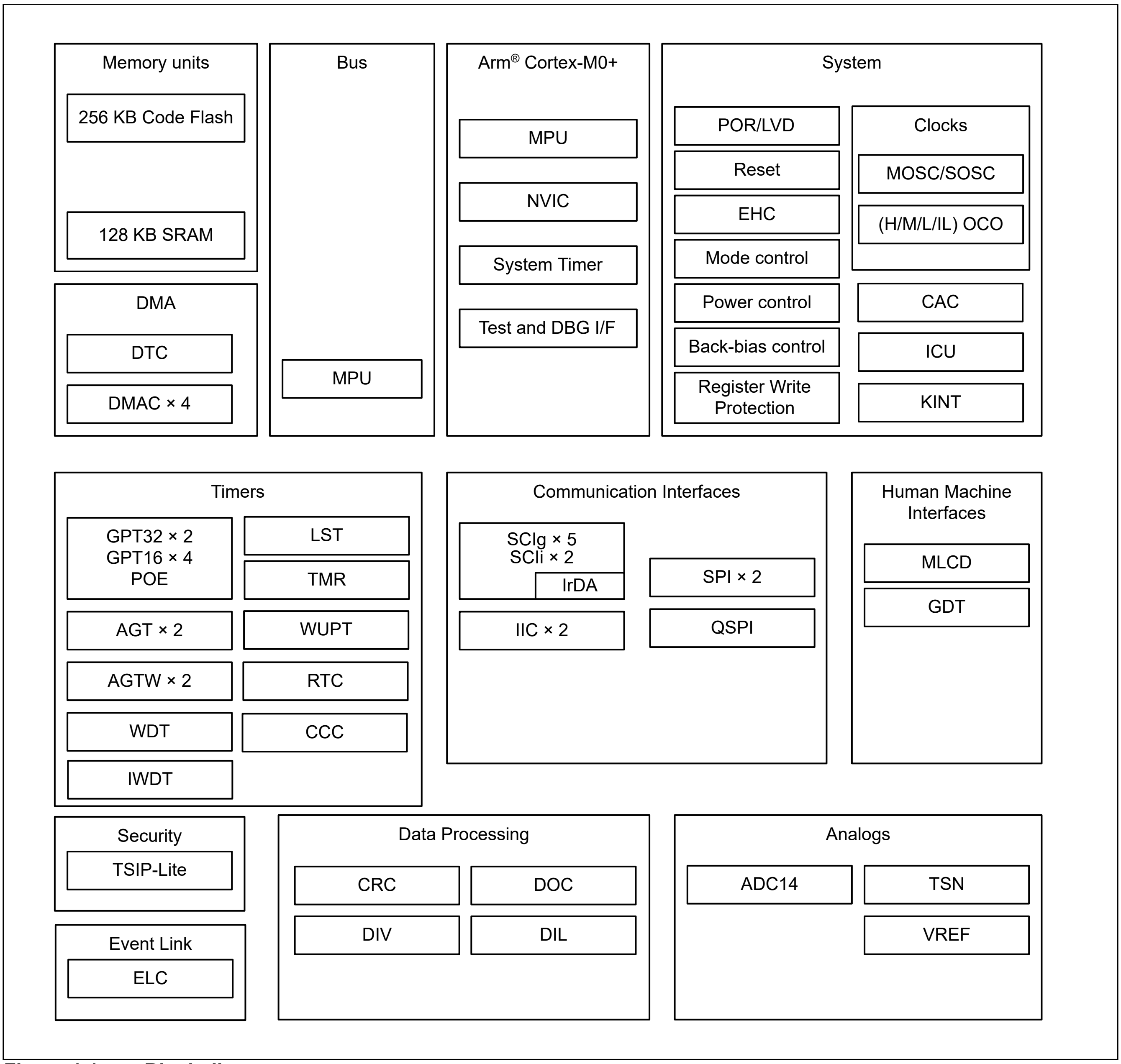


Figure 1.1 Block diagram

1.3 Part Numbering

Table 1.12 shows a list of products.

Table 1.12 Product list

Product part number	Package code	Code flash	SRAM	TSIP-Lite
R7F0E01182CFP	PLQP0100KB-B	256 KB	128 KB	Supported
R7F0E01082CFP	PLQP0100KB-B			Not supported
R7F0E01182CFM	PLQP0064KB-A			Supported
R7F0E01082CFM	PLQP0064KB-A			Not supported
R7F0E01182DBH	TBD (BGA100pin)			Supported
R7F0E01082DBH	TBD (BGA100pin)			Not supported
R7F0E01182DBR	SXBG0072MA-A			Supported
R7F0E01082DBR	SXBG0072MA-A			Not supported
R7F0E01182DNG	PVQN0056LA-A			Supported
R7F0E01082DNG	PVQN0056LA-A			Not supported

1.4 Function Comparison

Table 1.13 Function Comparison (1 of 4)

Part Number		R7F0E01182CFP	R7F0E01082CFP	R7F0E01182CFM	R7F0E01082CFM	R7F0E01182DBH	R7F0E01082DBH
Pin count		100		64		100	
GPIO	I/O pins	73		37		73	
	Input pins	1		1		1	
Package		LFQFP				BGA	
Code flash memory		256 KB					
SRAM		128 KB					
CPU operating freqency		32 MHz maximum (Normal mode) 64 MHz maximum (Boost mode) 32.768 kHz maximum (Low leakage current mode)					
Interrupt control	ICU	Yes					
	IRQ	Channels 0 to 9		Channels 0 to 5, 7, and 8		Channels 0 to 9	
Key interrupt	KINT	8 channels					
DMA	DTC	Yes					
	DMAC	Channels 0 to 3					
Event control	ELC	Yes					
Energy harvesting	EHC	Yes					
Back-bias voltage control	VBBC	Yes					

Table 1.13 Function Comparison (2 of 4)

<table>
<tr><th colspan="3">Part Number</th><th>R7F0E01182CFP</th><th>R7F0E01082CFP</th><th>R7F0E01182CFM</th><th>R7F0E01082CFM</th><th>R7F0E01182DBH</th><th>R7F0E01082DBH</th></tr>
<tr><td rowspan="12">Timers</td><td colspan="2">GPT32</td><td colspan="6">Channels 0 and 1</td></tr>
<tr><td colspan="2">GPT16</td><td colspan="6">Channels 2 to 5</td></tr>
<tr><td></td><td>POE</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">AGT</td><td colspan="6">Channels 0 and 1</td></tr>
<tr><td colspan="2">AGTW</td><td colspan="6">Channels 0 and 1</td></tr>
<tr><td colspan="2">TMR</td><td colspan="6">Channels 0 and 1</td></tr>
<tr><td colspan="2">WUPT</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">RTC</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">CCC</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">WDT</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">IWDT</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">LST</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="7">Communications</td><td>SCIg</td><td>w/o FIFO</td><td colspan="6">Channels 2 to 5, and 9</td></tr>
<tr><td rowspan="2">SCIi</td><td>w/ FIFO</td><td colspan="6">Channels 0 and 1</td></tr>
<tr><td>IrDA</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">IIC</td><td colspan="2">Channels 0 and 1</td><td colspan="2">Channel 1</td><td colspan="2">Channels 0 and 1</td></tr>
<tr><td rowspan="2">SPI</td><td>128 bit buffer</td><td colspan="6">Channel 0</td></tr>
<tr><td>32 bit buffer</td><td colspan="6">Channel 1</td></tr>
<tr><td colspan="2">QSPI</td><td colspan="6">Yes</td></tr>
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<tr><td>Standard precision</td><td colspan="2">4 channels</td><td colspan="2">No</td><td colspan="2">4 channels</td></tr>
<tr><td colspan="2">TSN</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">VREF</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="2">HMI graphics</td><td colspan="2">MLCD</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">GDT</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="4">Data Processing</td><td colspan="2">CRC</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">DOC</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">DIV</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">DIL</td><td colspan="6">Yes</td></tr>
<tr><td>Security</td><td colspan="2">TSIP-Lite</td><td>Yes</td><td>No</td><td>Yes</td><td>No</td><td>Yes</td><td>No</td></tr>
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Table 1.13 Function Comparison (3 of 4)

<table>
<tr><th colspan="2">Function</th><th>R7F0E01182DBR</th><th>R7F0E01082DBR</th><th>R7F0E01182DNG</th><th>R7F0E01082DNG</th></tr>
<tr><td colspan="2">Pin count</td><td colspan="2">72</td><td colspan="2">56</td></tr>
<tr><td rowspan="2">GPIO</td><td>I/O pins</td><td colspan="2">43</td><td colspan="2">33</td></tr>
<tr><td>Input pins</td><td colspan="2">1</td><td colspan="2">1</td></tr>
<tr><td colspan="2">Package</td><td colspan="2">WLBGA</td><td colspan="2">QFN</td></tr>
<tr><td colspan="2">Code flash memory</td><td colspan="4">256 KB</td></tr>
<tr><td colspan="2">SRAM</td><td colspan="4">128 KB</td></tr>
<tr><td colspan="2">CPU operating freqency</td><td colspan="4">32 MHz maximum (Normal mode)
64 MHz maximum (Boost mode)
32.768 kHz maximum (Low leakage current mode)</td></tr>
</table>

Table 1.13 Function Comparison (4 of 4)

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<tr><th colspan="3">Function</th><th>R7F0E01182DBR</th><th>R7F0E01082DBR</th><th>R7F0E01182DNG</th><th>R7F0E01082DNG</th></tr>
<tr><td rowspan="2">Interrupt control</td><td colspan="2">ICU</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">IRQ</td><td colspan="2">Channels 0 to 9</td><td colspan="2">Channels 0 to 5, Channels 7 to 8</td></tr>
<tr><td>Key interrupt</td><td colspan="2">KINT</td><td colspan="4">8 channels</td></tr>
<tr><td rowspan="2">DMA</td><td colspan="2">DTC</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">DMAC</td><td colspan="4">Channels 0 to 3</td></tr>
<tr><td>Event control</td><td colspan="2">ELC</td><td colspan="4">Yes</td></tr>
<tr><td>Energy harvesting</td><td colspan="2">EHC</td><td colspan="4">Yes</td></tr>
<tr><td>Back-bias voltage control</td><td colspan="2">VBBC</td><td colspan="4">Yes</td></tr>
<tr><td rowspan="13">Timers</td><td colspan="2">GPT32</td><td colspan="4">Channels 0 and 1</td></tr>
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<tr><td colspan="2">CCC</td><td colspan="4">Yes</td></tr>
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<tr><td colspan="2">IWDT</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">LST</td><td colspan="4">Yes</td></tr>
<tr><td rowspan="7">Communications</td><td>SCIg</td><td>w/o FIFO</td><td colspan="4">Channels 2 to 5, and 9</td></tr>
<tr><td rowspan="2">SCIi</td><td>w/ FIFO</td><td colspan="4">Channels 0 and 1</td></tr>
<tr><td>IrDA</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">IIC</td><td colspan="2">Channels 0 and 1</td><td colspan="2">Channel 1</td></tr>
<tr><td rowspan="2">SPI</td><td>128 bit buffer</td><td colspan="4">Channel 0</td></tr>
<tr><td>32 bit buffer</td><td colspan="4">Channel 1</td></tr>
<tr><td colspan="2">QSPI</td><td colspan="4">Yes</td></tr>
<tr><td rowspan="4">Analogs</td><td rowspan="2">ADC14</td><td>High precision</td><td colspan="4">8 channels</td></tr>
<tr><td>Standard precision</td><td colspan="2">4 channels</td><td colspan="2">No</td></tr>
<tr><td colspan="2">TSN</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">VREF</td><td colspan="4">Yes</td></tr>
<tr><td rowspan="2">HMI graphics</td><td colspan="2">MLCD</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">GDT</td><td colspan="4">Yes</td></tr>
<tr><td rowspan="4">Data Processing</td><td colspan="2">CRC</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">DOC</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">DIV</td><td colspan="4">Yes</td></tr>
<tr><td colspan="2">DIL</td><td colspan="4">Yes</td></tr>
<tr><td>Security</td><td colspan="2">TSIP-Lite</td><td>Yes</td><td>No</td><td>Yes</td><td>No</td></tr>
</table>

1.5 Pin Functions

Table 1.14 shows a list of pin functions.

Table 1.14 Pin functions (1 of 6)

Function	Signal	I/O	Description
Power supply	VCC/ IOVCC	Input	**Normal startup mode** Power supply pin. Connect it to the system power supply. Connect to VSS through a 0.1-μF smoothing capacitor. Place the smoothing capacitor close to the pin.*2 Apply voltage prior to the IOVCCn pins. **Energy harvesting startup mode** Power supply pin. Connect it to the system power supply. Connect to VSS through 0.1-μF smoothing capacitor (1). Place the smoothing capacitor close to the pin. In addition, connect to VSS through smoothing capacitor (2) having capacity of 1/10 of capacity of a storage capacitor connected to the VCC_SU pin to improve robustness against external noise and obtain stable operation of the circuit. For instance, connect a 4.7-μF smoothing capacitor in the case where a 47-μF storage capacitor is connected to the VCC_SU pin. If placing the smoothing capacitor (2) close to this pin is possible, the smoothing capacitor (1) is not required.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VCL	Input	Internal power supply stabilization pin. Connect the pin to VSS through a 4.7-μF smoothing capacitor. Place the smoothing capacitor close to the pin.
	VCLH	Input	Internal power supply stabilization pin. Separately from the VCL pin, connect the VCLH pin to VSS through a 4.7-μF smoothing capacitor. Place the smoothing capacitor close to the pin.
	VBN	—	Back-bias voltage stabilization pin. Connect the pin to VSS through a 0.56-μF smoothing capacitor. Place the smoothing capacitor close to the pin.
	VBP	—	
	VSC_VCC	Input	**Normal startup mode** Power supply pin supplied from a power generation element. Connect it to the system power supply (0 V) in normal startup mode. **Energy harvesting startup mode** Power supply pin supplied from a power generation element. Connect this pin to VSC_GND through a smoothing capacitor in parallel with the power generation element. Place the smoothing capacitor close to the pin. While a 4.7-nF to 47-nF smoothing capacitor is recommended, select a capacity value suitably in accordance with stability of a power generating element or the like.

Table 1.14 Pin functions (2 of 6)

Function	Signal	I/O	Description
Power supply	VCC_SU	I/O	**Normal startup mode** Power supply pin supplied from a storage capacitor. Short it to VCC/ IOVCC in normal startup mode. **Energy harvesting startup mode** Power supply pin supplied from a storage capacitor. When using a photovoltaic cell as a power generating element, connect a storage capacitor with a capacitance value in accordance with an operating temperature, and with a value of at least 10 times VCC. A capacitance value of 47 μF is required at 25°C. As a temperature becomes higher, a larger capacitance value is required. Connect this pin to a 100-μF storage capacitor in the case where other power generating elements are used.
	VSC_GND	Input	VSC_VCC ground pin. Connect it to the system power supply (0 V).
	VBAT_EHC	Input	**Normal startup mode** Power supply pin supplied from a secondary battery. Connected it to VCC/IOVCC in normal startup mode. **Energy harvesting startup mode** Power supply pin supplied from a secondary battery. Connect a 2.4-, 2.5-, 2.6-, 2.7-, 2.8-, 2.9-, 3.0-, or 3.1-V secondary battery or a super capacitor in energy harvesting startup mode.
	IOVCC0, IOVCC1	Input	Power supply pin for input/output. Connect the pin to VSS through a 0.1-μF smoothing capacitor. Place the smoothing capacitor close to the pin.[*2 *3]
Clock	XTAL	Input	MOSC resonator connect pin. EXTAL is an external clock input pin.
	EXTAL	Output	
	XCIN	Input	SOSC resonator connect pin
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
	CLKOUT32K	Output	SOSC clock output pin
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Startup mode control	MD	Input	Pin for setting the startup mode. The signal level on this pin must not be changed during startup mode transition on release from the reset state.
	EHMD	Input	Pin for setting the energy harvesting mode
System control	RES#	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
	BSCANP	Input	IOVCCn pin power supply forced input pin When the boundary scan function is in use, setting this pin to the high level while IOVCCn power is being supplied enables the supply of power to all I/O ports.
Interrupts	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ9,IRQ0_A_DS to IRQ3_A_DS	Input	Maskable interrupt request pins Pins that have "_DS" appended to their names can be used as triggers for release from deep software standby mode.
KINT	KRM00 to KRM07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
On-chip debugger	SWDIO	I/O	SWD data input/output pin
	SWCLK	Input	SWD clock input pin

Table 1.14 Pin functions (3 of 6)

Function	Signal	I/O	Description
Boundary scan	TMS	Input	Boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
GPT, POE	GTIOC0A to GTIOC5A, GTIOC0B to GTIOC5B	I/O	Input capture, output compare, or PWM output pin
	GTETRGA, GTETRGB	Input	External trigger input pin
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)
AGT	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Compare match A output pins
	AGTOB0, AGTOB1	Output	Compare match B output pins
AGTW	AGTWIO0, AGTWIO1	I/O	External event input and pulse output pins
	AGTWEE0, AGTWEE1	Input	External event input enable signals
	AGTWO0, AGTWO1	Output	Pulse output pins
	AGTWOA0, AGTWOA1	Output	Compare match A output pins
	AGTWOB0, AGTWOB1	Output	Compare match B output pins
TMR	TMCI0, TMCI1	Input	Input pins for external clocks to be input to the counter
	TMRI0, TMRI1	Input	Input pins for the counter reset
	TMO0, TMO1	Output	Compare match output pins
WUPT	TMWO	Output	Pulse output pin
RTC	RTCIC0 to RTCIC2	Input	Time capture event input pins
	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
CCC	CCCOUT	Output	CCC clock output pin

Table 1.14 Pin functions (4 of 6)

Function	Signal	I/O	Description
SCIi	[Asynchronous mode/clock synchronous mode]		
	SCK0, SCK1	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0, CTS1	Input	Input pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	RTS0, RTS1	Output	Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	[Simple I^2C mode]*1		
	SSCL0, SSCL1	I/O	Input/output pins for the I^2C clock (simple I^2C mode)
	SSDA0, SSDA1	I/O	Input/output pins for the I^2C data (simple I^2C mode)
	[Simple SPI mode]*1		
	SCK0, SCK1	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0, MISO1	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0, MOSI1	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0, SS1	Input	Chip-select input pins (simple SPI mode)
SCIg	[Asynchronous mode/clock synchronous mode]		
	SCK2 to SCK5, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD2 to RXD5, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD2 to TXD5, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS2 to CTS5, CTS9	Input	Input pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	RTS2 to RTS5, RTS9	Output	Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	[Simple I^2C mode]*1		
	SSCL2 to SSCL5, SSCL9	I/O	Input/output pins for the I^2C clock (simple I^2C mode)
	SSDA2 to SSDA5, SSDA9	I/O	Input/output pins for the I^2C data (simple I^2C mode)
	[Simple SPI mode]*1		
	SCK2 to SCK5, SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO2 to MISO5, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI2 to MOSI5, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS2 to SS5, SS9	Input	Chip-select input pins (simple SPI mode)
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pins
	MOSIA, MOSIB	I/O	Input/output pins for data output from the master
	MISOA, MISOB	I/O	Input/output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input/output pins for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection

Table 1.14 Pin functions (5 of 6)

Function	Signal	I/O	Description
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data 0 to data 3
Analog power supply	AVCC0	Input	Analog power supply pin for a 14-bit A/D converter, a reference voltage generation circuit, and a temperature sensor. Connect the pin to AVSS0 through a 1.0-μF smoothing capacitor. Place the smoothing capacitor close to the pin.*4 This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR).
	AVSS0	Input	Analog ground pin for the 14-bit A/D converter, reference voltage generation circuit, and temperature sensor. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR).
	VREFH0	Input	Analog reference voltage pin for the 14-bit A/D converter. Connect the pin to VREFL0 through a 1.0-μF smoothing capacitor. Place the smoothing capacitor close to the pin.*5 Connect this pin to AVCC0 when not using the A/D converter. Leave this pin open-circuit if AVCC0 is not to be supplied.
	AVTRO	Output	Reference voltage output terminal of reference voltage generation circuit (VREF). Connect the pin to VREFL0 through a 10-μF smoothing capacitor.
	VREFL0	Input	Analog reference ground pin for the 14-bit A/D converter. Connect this pin to AVSS0 when not using the A/D converter. Leave open if AVCC0 is not supplied.
ADC14	AN000 to AN007, AN016, AN017, AN020, AN021	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion
MLCD	MLCD_VCOM	Output	Polar signal pin for common electrode
	MLCD_XRST	Output	Output pin for LCD control
	MLCD_SCLK	Output	Communication serial output clock pin
	MLCD_DEN	Output	Data identification signal pin
	MLCD_ENBS	Output	Horizontal directional data enable pin
	MLCD_ENBG	Output	Vertical directional data enable pin
	MLCD_SI0 to MLCD_SI7	Output	Graphics data signal pin

Table 1.14 Pin functions (6 of 6)

Function	Signal	I/O	Description
I/O ports	P000 to P007, P010 to P015	I/O	14-bit input/output pins
	P100 to P113	I/O	14-bit input/output pins
	P200	Input	1-bit input dedicated pin. Multiplexed with the NMI pin function.
	P201 to P205, P207 to P210	I/O	8-bit input/output pins
	P300 to P302, P314 to P315	I/O	5-bit input/output pins
	P409 to P411	I/O	3-bit input/output pins
	P412, P413	I/O	2-bit input/output pin. Multiplexed with the EXTAL and XTAL pin functions.
	P500, P501, P508 to P511	I/O	6-bit input/output pins
	P600 to P604	I/O	5-bit input/output pins
	P700 to P704	I/O	5-bit input/output pins
	P806 to P815	I/O	10-bit input/output pins

Note: Use a laminated ceramic capacitor as a smoothing capacitor.
Note 1. For the SCIi and SCIg interfaces, each communications pin has multiple functions that work differently depending on the mode as follows: RXDn/SCLn/MISOn, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
Note 2. In an environment where there is much external noise, optionally connect these pins to VSS through a 10-μF smoothing capacitor close to the respective current sources to improve robustness against external noise and obtain stable operation of the circuit.
Note 3. When some of the IOVCC0 and IOVCC1 pins are connected at the same voltage, a 10-μF smoothing capacitor can be shared. In the case where the pin is connected to VCC/IOVCC, a 10-μF smoothing capacitor is not necessary.
Note 4. In an environment where there is much external noise, optionally connect this pin to AVSS0 through a 10-μF smoothing capacitor close to the current source to improve robustness against external noise and obtain stable operation of the circuit.
Note 5. In an environment where there is much external noise, optionally connect this pin to VREFL0 through a 10-μF smoothing capacitor close to the current source to improve robustness against external noise and obtain stable operation of the circuit.

1.6 Pin Assignments

Figure 1.2, Figure 1.3 and Figure 1.4 show the pin assignments from the top view. The pin arrangement diagram indicates the positions of power supply pins and I/O ports.

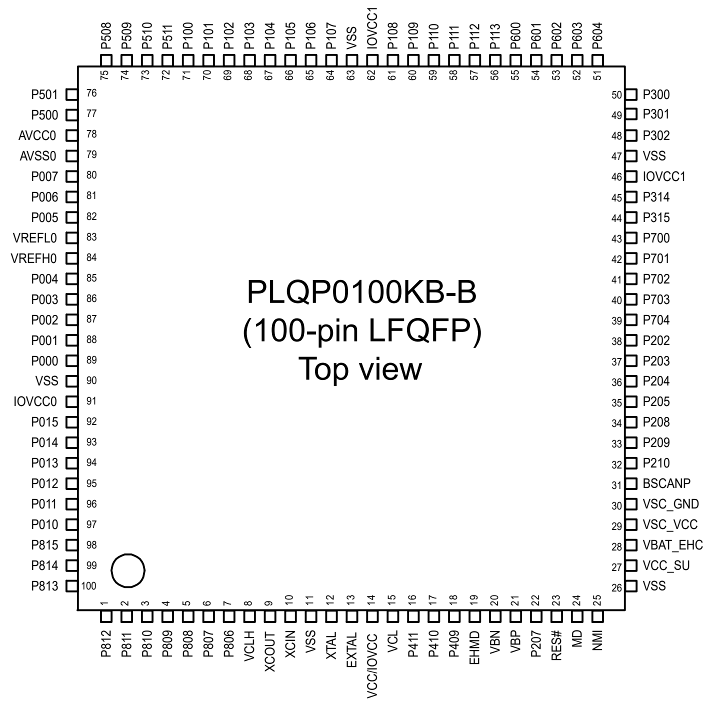


Figure 1.2 Pin assignment for LFQFP 100-pin

SXBG0072MA-A (72-pin WLBGA)

Top view transparent figure (Top view)

	A	B	C	D	E	F	G	H
9	VSS	VBAT_ EHC	VSC_ VCC	VSC_ GND	P204	P701	P700	VSS
8	VBP	NMI	VCC_SU	BSCANP	P208	P202	IOVCC1	VSS
7	P410	VBN	MD	VSS	P209	P203	P113	P112
6	EXTAL	EHMD	RES#	P210	P111	P110	P109	P108
5	XTAL	VCL	P207	P807	P107	P106	IOVCC1	VSS
4	VSS	VCC	P411	P012	P103	P102	P104	P105
3	XCIN	VCLH	P015	IOVCC0	VSS	AVSS0	AVCC0	P101
2	XCOUT	P013	P001	P003	P004	P005	P007	P100
1	P807	P014	P000	P002	VREFH0	VREFL0	P006	AVCC0

Ball surface (Bottom view)

	A	B	C	D	E	F	G	H
1	P807	P014	P000	P002	VREFH0	VREFL0	P006	AVCC0
2	XCOUT	P013	P001	P003	P004	P005	P007	P100
3	XCIN	VCLH	P015	IOVCC0	VSS	AVSS0	AVCC0	P101
4	VSS	VCC	P411	P012	P103	P102	P104	P105
5	XTAL	VCL	P207	P807	P107	P106	IOVCC1	VSS
6	EXTAL	EHMD	RES#	P210	P111	P110	P109	P108
7	P410	VBN	MD	VSS	P209	P203	P113	P112
8	VBP	NMI	VCC_SU	BSCANP	P208	P202	IOVCC1	VSS
9	VSS	VBAT_ EHC	VSC_ VCC	VSC_ GND	P204	P701	P700	VSS

Figure 1.3 Pin assignment for BGA 72-pin

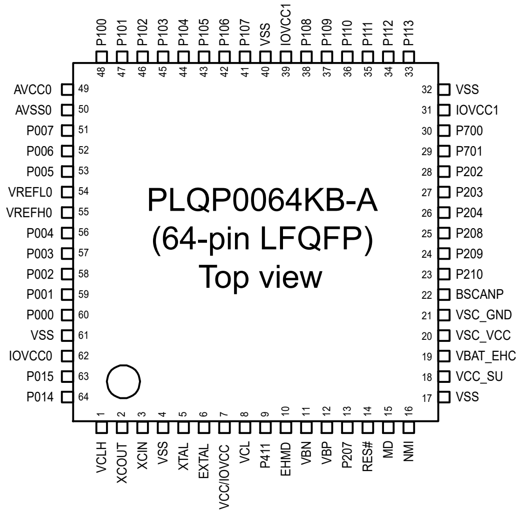


Figure 1.4 Pin assignment for LFQFP 64-pin

TBD
（100-pin BGA）
Ball surface（bottom view）

	1	2	3	4	5	6	7	8	9	10	11	12
M	P812	P814	P811	XCOUT	XCIN	VSS	VCC	P411	EHMD	RES#	P201	VSS
L	IOVCC0	P813	P810	VCLH	XTAL	EXTAL	VCL	VBP	VBN	P207	P200	VCC_SU
K	P010	P011	P809	P807	P806			P409	P410	P209	VBAT_EHC	VSS
J	IOVSS0	P013	P808							P210	BSCANP	VSC_VCC
H	P815	P012	P014							P208	P205	P204
G	P002	P015									P203	P703
F	VREFL	P001									P704	P701
E	VREFH	P007	P003							P202	P702	P314
D	AVSS0	P004	P006							P109	P700	IOVCC1
C	AVCC0	P000	P005	P501	P104			P110	P111	P302	P315	IOVSS1
B	P500	P100	P101	P102	P103	P106	P107	P108	P112	P600	P300	P301
A	P509	P508	P510	P511	P105	IOVSS1	IOVCC1	P113	P602	P601	P603	P604

Figure 1.5 Pin assignment for BGA 100-pin (Bottom view)

TBD
（100-pin BGA）
Top view transparent figure （Top view）

	1	2	3	4	5	6	7	8	9	10	11	12
A	P509	P508	P510	P511	P105	IOVSS1	IOVCC1	P113	P602	P601	P603	P604
B	P500	P100	P101	P102	P103	P106	P107	P108	P112	P600	P300	P301
C	AVCC0	P000	P005	P501	P104			P110	P111	P302	P315	IOVSS1
D	AVSS0	P004	P006							P109	P700	IOVCC1
E	VREFH	P007	P003							P202	P702	P314
F	VREFL	P001									P704	P701
G	P002	P015									P203	P703
H	P815	P012	P014							P208	P205	P204
J	IOVSS0	P013	P808							P210	BSCANP	VSC_VCC
K	P010	P011	P809	P807	P806			P409	P410	P209	VBAT_EHC	VSS
L	IOVCC0	P813	P810	VCLH	XTAL	EXTAL	VCL	VBP	VBN	P207	P200	VCC_SU
M	P812	P814	P811	XCOUT	XCIN	VSS	VCC	P411	EHMD	RES#	P201	VSS

Figure 1.6 Pin assignment for BGA 100-pin (Top view)

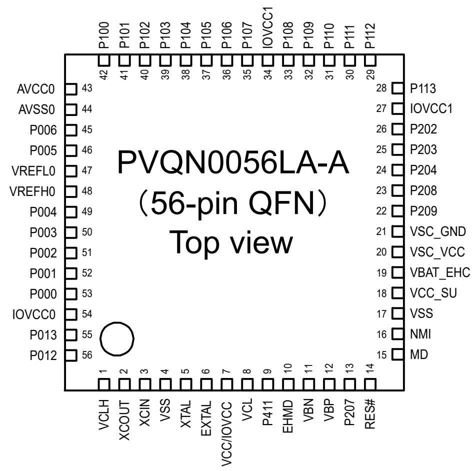


Figure 1.7 Pin assignment for QFN 56-pin

1.7 Pin Lists

Table 1.15 Pin list (1 of 3)

100-pin LFQFP	100-pin BGA	72-pin WLBGA	64-pin LFQFP	56-pin QFN	Power, System, Clock	I/O ports	Timers (CAC, CCC, GPT, AGT, AGTW, TMR, WUPT, RTC)	Communications (SCI, SPI, IIC, QSPI)	Display (MLCD)	External Int. (IRQn, KINT)	Analog (ADC14)	Power
1	M1	—	—	—		P812	AGTWEE1_B	TXD4_C/QSPCLK_A				IOVCC0
2	M3	—	—	—		P811	AGTWIO1_B	QIO0_A				IOVCC0
3	L3	—	—	—		P810	AGTIO1_B/GTIOC3A_B	QIO1_A		IRQ5_B		IOVCC0
4	K3	—	—	—		P809	AGTEE1_B/GTIOC3B_B	QIO2_A		IRQ6_B		IOVCC0
5	J3	F5	—	—		P808	AGTO1_B	RXD3_B/QIO3_A		IRQ2_B		IOVCC0
6	K4	E4	—	—		P807	AGTOA1_B	CTS3_B/QSSL_A		IRQ6_A		IOVCC0
7	K5	—	—	—		P806	AGTOB1_B					IOVCC0
8	L4	G2	1	1	VCLH							
9	M4	H1	2	2	XCOUT							IOVCC
10	M5	G1	3	3	XCIN							IOVCC
11	M6	F1	4	4	VSS							
12	L5	E1	5	5	XTAL	P413	GTIOC0A_A	TXD3_A				IOVCC
13	L6	D1	6	6	EXTAL	P412	GTIOC0B_A	RXD3_A				IOVCC
14	M7	F2	7	7	VCC/IOVCC							
15	L7	E2	8	8	VCL							
16	M8	F3	9	9	CLKOUT32K_A	P411	AGTWEE1_A/GTIOC0B_B	TXD9_A/SCK3_A		IRQ0_A_DS		IOVCC
17	K9	C1	—	—		P410				IRQ9_A		IOVCC
18	K8	—	—	—	CLKOUT32K_B	P409				IRQ9_B		IOVCC
19	M9	D2	10	10	EHMD							IOVCC
20	L9	C2	11	11	VBN							
21	L8	B1	12	12	VBP							
22	L10	E3	13	13		P207	AGTWO1_A/GTIOC0A_B	RXD9_A/CTS3_A		IRQ1_A_DS		IOVCC
23	M10	D3	14	14	RES#							IOVCC
24	M11	C3	15	15	MD	P201						IOVCC
25	L11	B2	16	16		P200				NMI		IOVCC
26	M12	A1	17	17	VSS							
27	L12	B3	18	18	VCC_SU							
28	K11	A2	19	19	VBAT_EHC							
29	J12	A3	20	20	VSC_VCC							
30	K12	A4	21	21	VSC_GND							
31 *1	J11	B4	22 *1	—	BSCANP							IOVCC
32	J10	D4	23	—		P210	AGTWOA1_A					IOVCC
33	K10	C4	24	22		P209	AGTWOB1_A					IOVCC
34	H10	B5	25	23		P208	AGTWIO1_A/TMWO					IOVCC
35	H11	E5	—	—		P205	AGTWO0_B	CTS4_B		IRQ8_C		IOVCC1
36	H12	A5	26	24		P204	ADTRG0_A/AGTO0_A/ GTIU_A/TMCI0_A/RTCIC0_A	SCK4_B		IRQ7_B		IOVCC1
37	G11	D5	27	25		P203	AGTOA0_A/GTIV_A/ TMRI0_A/RTCIC1_A	RXD4_B				IOVCC1
38	E10	C5	28	26		P202	CACREF_A/AGTOB0_A/ GTIW_A/TMO0_A/ CCCOUT_A/RTCOUT_A	TXD4_B		IRQ4_A		IOVCC1
39	F11	—	—	—		P704	AGTWOA0_B	CTS0_C				IOVCC1
40	G12	—	—	—		P703	AGTWOB0_B	TXD0_C				IOVCC1
41	E11	—	—	—		P702	AGTWEE0_B	RXD0_C				IOVCC1
42	F12	A6	29	—		P701	TMRI1/RTCIC2_A	SCL1				IOVCC1
43	D11	A7	30	—		P700	TMO1	SCK0_C/SDA1				IOVCC1

Table 1.15 Pin list (2 of 3)

100-pin LFQFP	100-pin BGA	72-pin WLBGA	64-pin LFQFP	56-pin QFN	Power, System, Clock	I/O ports	Timers (CAC, CCC, GPT, AGT, AGTW, TMR, WUPT, RTC)	Communications (SCI, SPI, IIC, QSPI)	Display (MLCD)	External Int. (IRQn, KINT)	Analog (ADC14)	Power
44	C11	—	—	—		P315	AGTWIO0_B/GTIOC4A_B	TXD5_B				IOVCC1
45	E12	—	—	—		P314	GTIOC4B_B	RXD5_B				IOVCC1
46	D12	B7	31	27	IOVCC1							
47	C12	A8	32	—	VSS							
48	C10	—	—	—		P302	GTIU_B/GTIOC2A_B/ TMCI0_B/	CTS5_B				IOVCC1
49	B12	—	—	—		P301	GTIV_B/GTIOC2B_B/ TMRI0_B/CCCOUT_B/ RTCOUT_B	SCK5_B				IOVCC1
50	B11	—	—	—		P300	GTIW_B/TMO0_B					IOVCC1
51	A12	—	—	—		P604	GTOWLO_B/GTIOC5B_B/ RTCIC0_B	TXD9_B		IRQ3_C		IOVCC1
52	A11	—	—	—		P603	GTETRGB_B/GTIOC5A_B/ RTCIC1_B	RXD9_B				IOVCC1
53	A9	—	—	—		P602	GTOUUP_B/RTCIC2_B	SCK9_B				IOVCC1
54	A10	—	—	—		P601	GTOULO_B	CTS9_B				IOVCC1
55	B10	—	—	—		P600	GTETRGA_B					IOVCC1
56	A8	B8	33	28		P113	AGTEE0_A/GTOWUP_A/ TMCI1	TXD4_A/SSLB2_A/QIO0_B	MLCD_VCOM	IRQ3_A_DS		IOVCC1
57	B9	B6	34	29		P112	AGTEE0_B/AGTWEE0_A/ GTOWLO_A	RXD4_A/SSLB3_A/QIO1_B	MLCD_XRST	IRQ8_B		IOVCC1
58	C9	C8	35	30		P111	AGTO0_B/AGTWO0_A/ GTOUUP_A/GTIOC2A_A	CTS4_A/RXD5_A/SSLB1_A/ QIO2_B	MLCD_SCLK			IOVCC1
59	C8	C7	36	31		P110	AGTOA0_B/AGTWOA0_A/ GTOULO_A/GTIOC2B_A	SCK9_A/SCK5_A/MOSIB_A/ QIO3_B	MLCD_DEN			IOVCC1
60	D10	C6	37	32		P109	AGTOB0_B/AGTWOB0_A/ GTOVUP_A	CTS9_A/CTS5_A/MISOB_A/ QSPCLK_B	MLCD_ENBS			IOVCC1
61	B8	D8	38	33		P108	AGTIO0_B/AGTWIO0_A/ GTOVLO_A	SCK4_A/TXD5_A/RSPCKB_A/ QSSL_B	MLCD_ENBG			IOVCC1
62	A7	E7	39	34	IOVCC1							
63	A6	E8	40	—	VSS							
64	B7	D7	41	35	TMS	P107	AGTOB1_A/GTETRGA_A/ GTIOC1A_A	CTS0_A/RSPCKA_A	MLCD_SI0	IRQ7_A/ KRM07_A		IOVCC1
65	B6	D6	42	36	TDO	P106	AGTOA1_A/GTETRGB_A/ GTIOC1B_A	TXD0_A/SSLB0_A	MLCD_SI1	IRQ3_B/ KRM06_A		IOVCC1
66	A5	E6	43	37	TDI	P105	AGTO1_A/GTIOC4A_A	RXD0_A/MISOA_A	MLCD_SI2	IRQ8_A/ KRM05_A		IOVCC1
67	C5	F8	44	38	TCK	P104	AGTIO1_A/GTIOC4B_A	SCK0_A/MOSIA_A	MLCD_SI3	IRQ4_B/ KRM04_A		IOVCC1
68	B5	F7	45	39		P103	AGTEE1_A/GTIOC5A_A	CTS2_A/CTS1_A/SSLA0_A	MLCD_SI4	KRM03_A		IOVCC1
69	B4	F6	46	40		P102	AGTIO0_A/GTIOC5B_A	TXD2_A/TXD1_A/IRTXD1_A/ SSLA1_A	MLCD_SI5	KRM02_A		IOVCC1
70	B3	G8	47	41		P101	ADTRG0_B/GTIOC0A_C	RXD2_A/RXD1_A/IRRXD1_A/ SSLA2_A	MLCD_SI6	KRM01_A		IOVCC1
71	B2	H8	48	42		P100	CACREF_B/GTIOC0B_C	SCK2_A/SCK1_A/SSLA3_A	MLCD_SI7	KRM00_A		IOVCC1
72	A4	—	—	—		P511	GTOVUP_B/GTIOC1B_B	SCK0_B		KRM03_B		IOVCC1
73	A3	—	—	—		P510	GTOVLO_B/GTIOC1A_B	RXD0_B		KRM02_B	AN021	IOVCC1
74	A1	—	—	—		P509		TXD0_B		KRM01_B	AN020	IOVCC1
75	A2	—	—	—		P508				IRQ4_C	AN017	IOVCC1
76	C4	—	—	—		P501					AN016	IOVCC1
77	B1	—	—	—		P500	GTOWUP_B	CTS0_B				IOVCC1
78	C1	G7	49	43	AVCC0							
79	D1	G6	50	44	AVSS0							
80	E2	H7	51	—		P007					AN007	AVCC0
81	D3	J7	52	45		P006					AN006	AVCC0

Table 1.15 Pin list (3 of 3)

100-pin LFQFP	100-pin BGA	72-pin WLBGA	64-pin LFQFP	56-pin QFN	Power, System, Clock	I/O ports	Timers (CAC, CCC, GPT, AGT, AGTW, TMR, WUPT, RTC)	Communications (SCI, SPI, IIC, QSPI)	Display (MLCD)	External Int. (IRQn, KINT)	Analog (ADC14)	Power
82	C3	H6	53	46		P005					AN005	AVCC0
83	F1	J6	54	47	VREFL0							
84	E1	J5	55	48	VREFH0/AVTRO							
85	D2	H5	56	49		P004					AN004	AVCC0
86	E3	H4	57	50		P003					AN003	AVCC0
87	G1	J4	58	51		P002					AN002	AVCC0
88	F2	H3	59	52		P001					AN001	AVCC0
89	C2	J3	60	53		P000					AN000	AVCC0
90	J1	G5	61	—	VSS							
91	L1	G4	62	54	IOVCC0							
92	G2	G3	63	—	CLKOUT	P015	GTIOC3A_A	SSLA1_B		IRQ5_A		IOVCC0
93	H3	F4	64	—		P014	GTIOC3B_A	SSLA0_B		IRQ2_A_DS		IOVCC0
94	J2	J2	—	55		P013		SCK3_B/SCL0				IOVCC0
95	H2	H2	—	56		P012		TXD3_B/SDA0				IOVCC0
96	K2	—	—	—		P011		RSPCKA_B				IOVCC0
97	K1	—	—	—		P010		MOSIA_B				IOVCC0
98	H1	—	—	—		P815	AGTWOB1_B	CTS4_C/MISOA_B				IOVCC0
99	M2	—	—	—		P814	AGTWOA1_B	SCK4_C/SSLA2_B				IOVCC0
100	L2	—	—	—		P813	AGTWO1_B	RXD4_C/SSLA3_B				IOVCC0

Note: Note the following regarding pin names:

- For the SCIi and SCIg interfaces, each communication pin has multiple functions that work differently depending on the mode as follows: RXDn/SCLn/MISOn, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
- Renesas recommends using the sets of pins that have the same letter (“_A”,“_B”,“_C” to indicate group membership) appended to their names. For the SPI, QSPI, and SCI interfaces, the AC portion of the electrical characteristics is measured per group.
- Pins that have "_DS" appended to their names can be used as triggers for release from deep software standby.

Note 1. LFQFP package does not have BSCANP function, so connect to GND.

2. Electrical Characteristics

The electrical characteristics are defined under the following conditions unless otherwise specified:

- VCC = AVCC0 = IOVCC0 = IOVCC1 = 1.62 to 3.6 V
- 1.62 V ≤ VREFH0 ≤ AVCC0
- VSS = AVSS0 = VREFL0 = 0V
- Ta = Topr
- The load capacitance of each I/O pin is 30 pF.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Item		Symbol	Value	Unit
Power-supply voltage	Power-supply voltage	VCC	-0.3 to 4.6	V
	Input voltage for EHC	VSC_VCC	-0.3 to 4.6	V
	Input voltage of secondary battery for EHC	VBAT_EHC	-0.3 to 4.6	V
	Power-supply voltage for I/O	IOVCC, IOVCC0, IOVCC1	-0.3 to 4.6	V
Input voltage		V_{in}	-0.3 to VCC + 0.3 (max. 4.6 V)	V
Reference power supply voltage		VREFH0	-0.3 to AVCC0 + 0.3 (max. 4.6 V)	V
		VREFL0	-0.3 to AVSS0 + 0.3	V
Analog power supply voltage		AVCC0	-0.3 to 4.6	V
Junction temperature		T_j	-40 to +95	°C
Storage Temperature		T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power-supply voltage	VCC	1.62	—	3.6	V
	VSS	—	0	—	V
Input voltage for EHC	VSC_VCC	1.62	—	3.6	V
Input voltage of secondary battery for EHC	VBAT_EHC*1	1.62	—	3.6	V
Analog power supply voltage	AVCC0	1.62	—	3.6	V
	AVSS0	—	0	—	V
	VREFH0	1.62	—	AVCC0	V
	VREFL0	—	0	—	V
Power-supply for I/O	IOVCC, IOVCC0, IOVCC1	1.62	—	3.6	V
Power-supply voltage	T_{opr}	-40	—	85	°C

Note 1. The voltage of the secondary battery to be connected to VBAT_EHC is 2.4 V, 2.5 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, or 3.1 V.

2.2 DC Characteristics

2.2.1 I/O input characteristics (V_{IH}, V_{IL})

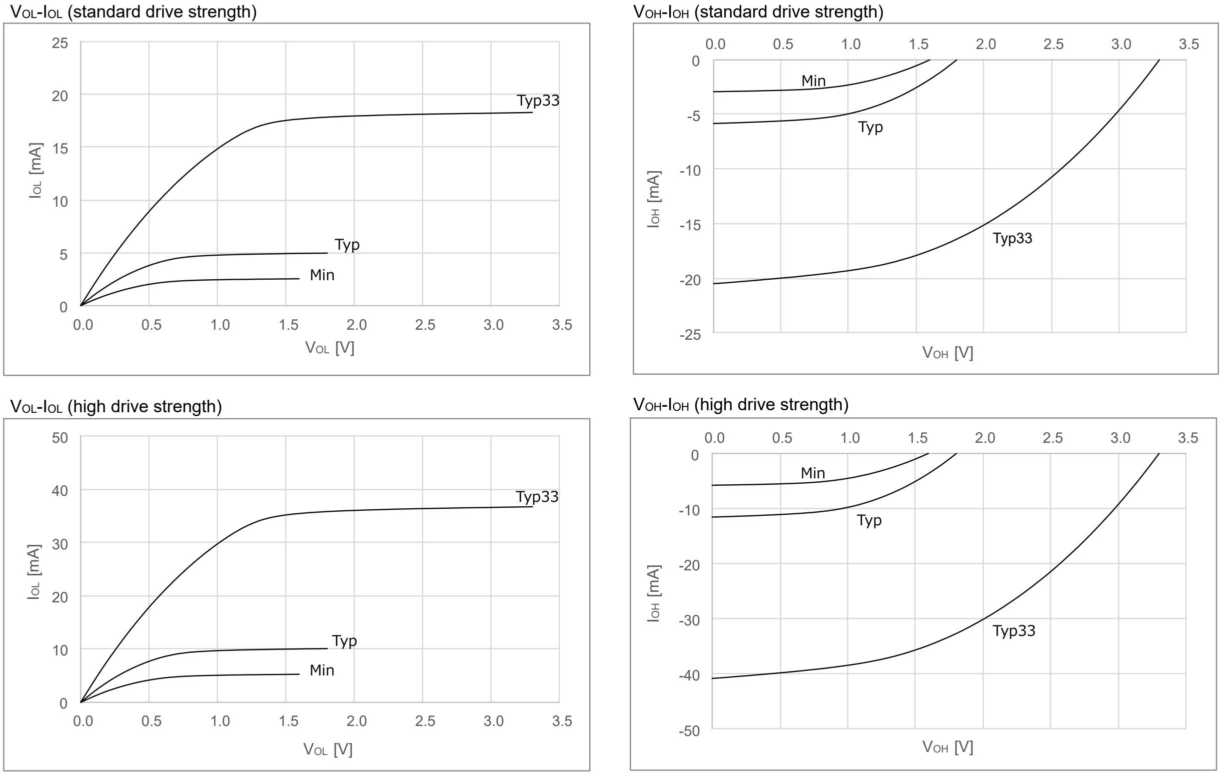
Table 2.3 I/O input characteristics (V_{IH}, V_{IL})

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Schmitt trigger input voltage	Input pins of RES#, NMI, IRQn, and peripheral functions (except for IIC)	V_{IH}	VCC × 0.8	—	—	V	—
		V_{IL}	—	—	VCC × 0.2		
		ΔV_T	0.3	—	—		
	IIC	V_{IH}	VCC × 0.7	—	—		VCC = 3.0 to 3.6 V
		V_{IL}	—	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
Input voltage (except for Schmitt trigger input pin)	EXTAL, MD, EHMD, General-Purpose I/O Ports	V_{IH}	VCC × 0.8	—	—		—
		V_{IL}	—	—	VCC × 0.2		

2.2.2 I/O output characteristics (V_{OH}, V_{OL}) (1)

Table 2.4 I/O output characteristics (V_{OH}, V_{OL}) (1)

Item	Register settings	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Output high level voltage	Standard drive (PmnPFS.DSCR[1:0] = 10b)	V_{OH}	VCC - 0.6	—	—	V	I_{OH} = 2 mA
	High drive (PmnPFS.DSCR[1:0] = 11b)		VCC - 0.5	—	—		I_{OH} = 2 mA
Output low level voltage	Standard drive (PmnPFS.DSCR[1:0] = 10b)	V_{OL}	—	—	0.6		I_{OL} = 2 mA
	High drive (PmnPFS.DSCR[1:0] = 11b)		—	—	0.5		I_{OL} = 2 mA



Measurement conditions

Parameter	Typ33	Typ	Min	Unit
VCC	3.3	1.8	1.6	V
Ta	25	25	125	°C

Figure 2.1 V_{OH}-I_{OH} and V_{OL}-I_{OL} characteristics

2.2.3 I/O output characteristics (V_{OL}) (2)

Table 2.5 I/O output characteristics (V_{OL}) (2)

Condition: VCC = 3.0 to 3.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Output low level voltage	IIC	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA

2.2.4 Pull-up Resistors

Table 2.6 Pull-up resistors

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Pull-up resistor	I_P	120	200	—	kΩ	VCC = 2.5 V

2.2.5 Pin Capacitance

Table 2.7 Pin capacitance

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Pin Related to IIC	P012, P013, P700, P701	C_{in}	—	—	8	pF	—
EXTAL, XTAL	P412, P413						
All of pins other than above			—	—	16		

2.2.6 Operating and Standby Current

Table 2.8 Operating and Standby Current (1 of 6)

Measurement condition of maximum values: VCC = AVCC0 = AVCC1 = VREFH0 = 3.6 V, $T_a = T_{opr}$ = 85°C
Typical measurement conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, $T_a = T_{opr}$ = 25°C

Power supply mode	Power control mode/low power mode		Setting value of operating frequency	Clock source	Typ.	Max.	Unit
The mode code of all the power supply (ALLPWON) is executed from the flash memory.	BOOST	Maximum operation*1	ICLK/PCLKB = 64/32 MHz	HOCO	—	14	mA
			ICLK/PCLKB = 32/16 MHz		—	9.1*3	
		while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32/32 MHz	MOSC	3.6	—	
			ICLK/PCLKB = 16/16 MHz		1.9	—	
			ICLK/PCLKB = 32/16 MHz		3.0	—	
			ICLK/PCLKB = 64/32 MHz	HOCO	5.7	—	
			ICLK/PCLKB = 32/16 MHz		2.9	—	
		CoreMark (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 64/1 MHz	HOCO	2.3	—	
			ICLK/PCLKB = 32/0.5 MHz		1.2	—	
		while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 64/32 MHz	HOCO	2.0	—	
			ICLK/PCLKB = 32/16 MHz		1.1	—	
			ICLK/PCLKB = 32/32 MHz	MOSC	1.2	—	
			ICLK/PCLKB = 16/16 MHz		0.7	—	
			ICLK/PCLKB = 64/1 MHz	HOCO	1.8	—	
			ICLK/PCLKB = 32/0.5 MHz		1.0	—	
		Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 64/32 MHz	HOCO	0.9	—	
			ICLK/PCLKB = 32/16 MHz		0.5	—	
			ICLK/PCLKB = 64/1 MHz		0.7	—	
			ICLK/PCLKB = 32/0.5 MHz		0.5	—	
	Normal	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	8.3	mA
			ICLK/PCLKB = 16/16 MHz		—	6.1*3	
		while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32/32 MHz	MOSC	2.9	7.6	
			ICLK/PCLKB = 16/16 MHz		1.5	5.7*3	
			ICLK/PCLKB = 32/32 MHz	HOCO	2.8	7.5	
			ICLK/PCLKB = 16/16 MHz		1.6	5.8*3	
		CoreMark (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/0.50 MHz	MOSC	1.1	—	
			ICLK/PCLKB = 16/0.25 MHz		0.61	—	
		while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/32 MHz	MOSC	0.97	—	
			ICLK/PCLKB = 16/16 MHz		0.56	—	
			ICLK/PCLKB = 32/0.50 MHz		0.84	5.7	
			ICLK/PCLKB = 16/0.25 MHz		0.49	—	
		Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/32 MHz	MOSC	0.56	—	
			ICLK/PCLKB = 16/16 MHz		0.35	—	
			ICLK/PCLKB = 32/0.50 MHz		0.45	—	
			ICLK/PCLKB = 16/0.25 MHz		0.3	—	

Table 2.8 Operating and Standby Current (2 of 6)

Measurement condition of maximum values: VCC = AVCC0 = AVCC1 = VREFH0 = 3.6 V, $T_a = T_{opr}$ = 85°C
Typical measurement conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, $T_a = T_{opr}$ = 25°C

Power supply mode	Power control mode/low power mode		Setting value of operating frequency	Clock source	Typ.	Max.	Unit
The mode code of all the power supply (ALLPWON) is executed from the flash memory.	VBB	Maximum operation*1	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	—	120*3	μA
		while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32.7/32.7 kHz		44	—	
			ICLK/PCLKB = 32.7/0.51 kHz		43	—	
		Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32.7/0.51 kHz		40	—	
		while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32.768/32.768 kHz	SOSC (standard CL)	44	—	
		Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32.768/0.512 kHz		40	—	
		while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32.768/32.768 kHz	SOSC (low CL)	43	—	
		while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32.768/32.768 kHz		43	—	
			ICLK/PCLKB = 32.768/0.512 kHz		43	—	
		Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32.768/32.768 kHz		39	—	
			ICLK/PCLKB = 32.768/0.512 kHz		39	—	

Table 2.8 Operating and Standby Current (3 of 6)

Measurement condition of maximum values: VCC = AVCC0 = AVCC1 = VREFH0 = 3.6 V, T_a = T_{opr} = 85°C
Typical measurement conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, T_a = T_{opr} = 25°C

Power supply mode	Power control mode/low power mode			Setting value of operating frequency	Clock source	Typ.	Max.	Unit
The mode code of power supply other than flash (EXFPWON) is executed from the SRAM.	BOOST	Software standby mode*4	When VCC = 3.3 V	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	39	—	μA
			When VCC = 1.8 V	ICLK/PCLKB = 32.7/32.7 kHz		38	—	
	BOOST_VBB	Software standby mode*4	When VCC = 3.3 V	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	14	—	μA
			When VCC = 1.8 V	ICLK/PCLKB = 32.7/32.7 kHz		13	—	
	Normal	High-speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	7.3*3	mA
				ICLK/PCLKB = 16/16 MHz		—	5.8*3	
			while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32/32 MHz		2.8	—	
				ICLK/PCLKB = 16/16 MHz		1.5	—	
				ICLK/PCLKB = 32/32 MHz	HOCO	2.8	—	
				ICLK/PCLKB = 16/16 MHz		1.5	—	
			while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/32 MHz	MOSC	0.93	—	
				ICLK/PCLKB = 16/16 MHz		0.52	—	
				ICLK/PCLKB = 32/0.50 MHz		0.8	—	
				ICLK/PCLKB = 16/0.25 MHz		0.45	—	
			Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/32 MHz	MOSC	0.52	—	
				ICLK/PCLKB = 16/16 MHz		0.32	—	
				ICLK/PCLKB = 32/0.50 MHz		0.41	—	
				ICLK/PCLKB = 16/0.25 MHz		0.26	—	
		Low-speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	4.4*3	mA
				ICLK/PCLKB = 1/1 MHz		—	4.3*3	
			while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 2/2 MHz	MOSC	0.22	—	
				ICLK/PCLKB = 1/1 MHz		0.13	—	
				ICLK/PCLKB = 2/2 MHz	MOCO	0.2	—	
				ICLK/PCLKB = 1/1 MHz		0.12	—	
			while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 2/2 MHz	MOSC	0.10	—	
				ICLK/PCLKB = 1/1 MHz		0.07	—	
				ICLK/PCLKB = 2000/31.25 kHz		0.09	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.07	—	
			Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 2/2 MHz	MOSC	0.07	—	
				ICLK/PCLKB = 1/1 MHz		0.06	—	
				ICLK/PCLKB = 2000/31.25 kHz		0.07	—	
				ICLK/PCLKB = 1000/31.25 kHz		0.05	—	
		Software standby mode*4	When VCC = 3.3 V		LOCO	24	—	μA
			When VCC = 1.8 V			24	—	
			When VCC = 3.3 V		SOSC (standard CL)	24	—	
			When VCC = 1.8 V			24	—	
			When VCC = 3.3 V		SOSC (low CL)	23	—	
			When VCC = 1.8 V			23	—	

Table 2.8 Operating and Standby Current (4 of 6)

Measurement condition of maximum values: VCC = AVCC0 = AVCC1 = VREFH0 = 3.6 V, T_a = T_{opr} = 85°C
Typical measurement conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, T_a = T_{opr} = 25°C

Power supply mode	Power control mode/low power mode			Setting value of operating frequency	Clock source	Typ.	Max.	Unit
The mode code of power supply other than flash (EXFPWON) is executed from the SRAM.	VBB	Maximum operation*1		ICLK/PCLKB = 32.7/32.7 kHz	LOCO	—	26*3	μA
		while(1) operation (peripheral clock is supplied.)		ICLK/PCLKB = 32.7/32.7 kHz		4.1	—	
		Sleep mode (stopping clock supply to peripheral functions*2)		ICLK/PCLKB = 32.7/0.51 kHz		1.6	—	
		Software standby mode*4	When VCC = 3.3/3.6 V			1.4	22*3	
			When VCC = 1.8 V			1.3	—	
		while(1) operation (peripheral clock is supplied.)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (standard CL)	4.7	—	
		Sleep mode (stopping clock supply to peripheral functions*2)		ICLK/PCLKB = 32.768/0.512 kHz		2.2	—	
		Software standby mode*4	When VCC = 3.3 V			2.0	—	
			When VCC = 1.8 V			1.9	—	
		while(1) operation (peripheral clock is supplied.)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (low CL)	4.0	—	
		while(1) operation (stopping clock supply to peripheral functions*2)		ICLK/PCLKB = 32.768/32.768 kHz		4.0	—	
		Sleep mode (stopping clock supply to peripheral functions*2)		ICLK/PCLKB = 32.768/0.512 kHz		1.5	—	
		Software standby mode*4	When VCC = 3.3 V			1.3	—	
			When VCC = 1.8 V			1.2	—	

Table 2.8 Operating and Standby Current (5 of 6)

Measurement condition of maximum values: VCC = AVCC0 = AVCC1 = VREFH0 = 3.6 V, T_a = T_{opr} = 85°C
Typical measurement conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, T_a = T_{opr} = 25°C

Power supply mode	Power control mode/low power mode			Setting value of operating frequency	Clock source	Typ.	Max.	Unit
The mode code of the minimum power supply (MINPWON) is executed from the SRAM.	BOOST	Software standby mode*4	When VCC = 3.3 V	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	29	—	μA
			When VCC = 1.8 V	ICLK/PCLKB = 32.7/32.7 kHz		28	—	
	BOOST_VBB	Software standby mode*4	When VCC = 3.3 V	ICLK/PCLKB = 32.7/32.7 kHz	LOCO	14	—	μA
			When VCC = 1.8 V	ICLK/PCLKB = 32.7/32.7 kHz		13	—	
	Normal	High-speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	4.6*3	mA
				ICLK/PCLKB = 16/16 MHz		—	3.8*3	
			while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 32/32 MHz	MOSC	1.3	—	
				ICLK/PCLKB = 16/16 MHz		0.72	—	
			while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/32 MHz	MOSC	0.9	—	
				ICLK/PCLKB = 16/16 MHz		0.5	—	
				ICLK/PCLKB = 32/0.5 MHz		0.78	3.7*3	
				ICLK/PCLKB = 16/0.5 MHz		0.44	—	
			Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 32/32 MHz	MOSC	0.5	—	
				ICLK/PCLKB = 16/16 MHz		0.3	—	
				ICLK/PCLKB = 32/0.5 MHz		0.39	—	
				ICLK/PCLKB = 16/0.5 MHz		0.25	—	
		Low-speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	3000*3	μA
				ICLK/PCLKB = 1/1 MHz		—	2900*3	
			while(1) operation (peripheral clock is supplied.)	ICLK/PCLKB = 2/2 MHz	MOCO	108	—	
				ICLK/PCLKB = 1/1 MHz		60	—	
			while(1) operation (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 2000/31.25 kHz	MOSC	78	—	
				ICLK/PCLKB = 1000/31.25 kHz		52	—	
				ICLK/PCLKB = 2/2 MHz	MOCO	68	—	
				ICLK/PCLKB = 1/1 MHz		46	—	
				ICLK/PCLKB = 2000/31.25 kHz		60	—	
				ICLK/PCLKB = 1000/31.25 kHz		42	—	
			Sleep mode (stopping clock supply to peripheral functions*2)	ICLK/PCLKB = 2/2 MHz	MOCO	43	—	
				ICLK/PCLKB = 1/1 MHz		34	—	
				ICLK/PCLKB = 2000/31.25 kHz		36	—	
				ICLK/PCLKB = 1000/31.25 kHz		30	—	
		Software standby mode*4	When VCC = 3.3 V		LOCO	14	—	μA
			When VCC = 1.8 V			14	—	
			When VCC = 3.3 V		SOSC (standard CL)	14	—	
			When VCC = 1.8 V			14	—	
			When VCC = 3.3 V		SOSC (low CL)	14	—	
			When VCC = 1.8 V			13	—	

Table 2.8 Operating and Standby Current (6 of 6)

Measurement condition of maximum values: VCC = AVCC0 = AVCC1 = VREFH0 = 3.6 V, T_a = T_{opr} = 85°C
Typical measurement conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, T_a = T_{opr} = 25°C

Power supply mode	Power control mode/low power mode			Setting value of operating frequency	Clock source	Typ.	Max.	Unit
The mode code of the minimum power supply (MINPWON) is executed from the SRAM.	VBB	while(1) operation (peripheral clock is supplied.)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (standard CL)	2.4	10[*3]	μA
		Sleep mode (stopping clock supply to peripheral functions[*2])		ICLK/PCLKB = 32.768/0.512 kHz		1.4	—	
		Software standby mode[*4]	When VCC = 3.3 V			1.2	—	
			When VCC = 1.8 V			1.1	—	
		while(1) operation (peripheral clock is supplied.)		ICLK/PCLKB = 32.7/32.7 kHz	LOCO	2	10[*3]	μA
		Sleep mode (stopping clock supply to peripheral functions[*2])		ICLK/PCLKB = 32.7/0.51 kHz		0.9	8.5[*3]	
		Software standby mode	VCC = 3.3 V (Typ.)/ 3.6 V (Max.)		LOCO	0.6	8.4	μA
			When VCC = 1.8 V			0.5	7.3[*3]	
		while(1) operation (peripheral clock is supplied.)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (low CL)	1.7	—	μA
		while(1) operation (stopping clock supply to peripheral functions[*2])		ICLK/PCLKB = 32.768/32.768 kHz		1.7	—	
		Sleep mode (stopping clock supply to peripheral functions[*2])		ICLK/PCLKB = 32.768/0.512 kHz		0.7	—	
		Software standby mode[*4]	When VCC = 3.3 V			0.5	7[*3]	
			When VCC = 1.8 V			0.4	5.8[*3]	
		Software standby mode[*4]	Increment when IWDT is used (OFS0.IWDTSTRT = 0)			81	—	nA
		Increase when peripheral modules are in use	Increase for using AGT and AGTW (AGTCR.TSTART = 1)			38	—	
		(No dependency on VCC)	Increase for each 32 KB of SRAM in use (set by the RAMSDCR register)			12	—	
Deep software standby			VCC = 3.3 V (Typ.)/ 3.6 V (Max.)	—	—	120	1600[*3]	nA
			When VCC = 1.8 V	—	—	100	1200[*3]	
			Increment when SOSC is used (VCC = 3.3 V)		SOSC (low CL)	160	—	
			Increment when SOSC is used (VCC = 1.8 V)			100	—	
Increment on peripheral function during the standby mode			Increase for using LVD0 (OFS1.LVDAS = 0)			48	—	nA
			Increase for using LVD1 (LVCMPCR.LVD1E = 1)			66	—	
			Increase for using LVDBAT (LVCMPCR.LVDBATR = 1)			66	—	
			Increase for using CCC (CADJUSCEN = 1 and ADUSTEN = 1) (3.3 V)			35	—	
			Increase for using CCC (CADJUSCEN = 1 and ADUSTEN = 1) (1.8 V)			12	—	
			Increase for using WUPT (TCR.TCST = 1 and TCR.TCCE = 1) (3.3 V)			65	—	
			Increase for using WUPT (TCR.TCST = 1 and TCR.TCCE = 1) (1.8 V)			30	—	
			Increase for using RTC (RCR4.R32KMD = 0 and RCR2.CNTMD = 1) (3.3 V)			200	—	
			Increase for using RTC (RCR4.R32KMD = 0 and RCR2.CNTMD = 1) (1.8 V)			100	—	
			Increase for using RTC (RCR4.R32KMD = 1 and RCR2.CNTMD = 1) (3.3 V)			280	—	
			Increase for using RTC (RCR4.R32KMD = 1 and RCR2.CNTMD = 1) (1.8 V)			150	—	

Note 1. The value for current in a “Maximum operation” row is for a case where the DMAC is handling transfer in every cycle and the CPU is repeatedly executing a multiply instruction while all modules are released from the module-stop state. The value does not include the supply of current for the pins.

Note 2. The value for current in a row with a label that includes “stopping clock supply to peripheral functions” is for a case where the peripheral circuits have been placed in the module-stop state following the settings for frequency-division of ICLK and PCLKB.

Note 3. We do not inspect this value before shipment. The values presented in this manual are only for reference.

Note 4. The supply of the clock signals is stopped in this mode regardless of the operating frequency settings.

Table 2.9 Analog operating current (AVCC0) and standby current

Maximum measurement conditions: VCC = AVCC0 = VREFH0 = 3.6 V, T_a = T_{opr} = 85°C
Typical measurement conditions: VCC = AVCC0 = VREFH0 = 3.3 V, T_a = T_{opr} = 25°C (when VREF circuit is not used.)
Typical measurement conditions: VCC = AVCC0 = 3.3 V, AVTRO = 1.25 V, T_a = T_{opr} = 25°C (when VREF circuit is used.)

Item	Operation state of circuit			Symbol	Typ.	Max.	Unit	Measurement conditions
	A/D	Temperature sensor	VREF					
AVCC0 power supply current	Under conversion	Under operation	Under operation	I_{AVCC0}	81	—	μA	PCLKB = 16 MHz Sampling time is 1 μs. (ADSSTRn.SST[7:0] = 0x10)
		Stopped	Under operation		77	—		
		Under operation	Stopped		69	—		
		Stopped	Stopped		53	—		
		Stopped	Stopped		0.19	—		PCLKB = 32.768 kHz Sampling time is 61 μs. (ADSSTRn.SST[7:0] = 0x02)
	Waiting for conversion	Stopped	Stopped		22	—	nA	PCLKB = 16 MHz[*1]
	Standby mode				22	1900		Clock supply is stopped.
Reference power supply current	Under conversion	Stopped	Stopped	I_{REFH0}	18	—	μA	PCLKB = 16 MHz
					0.08	—		PCLKB = 32.768 kHz
	Waiting for conversion	Stopped	Stopped		22	—	nA	PCLKB = 16 MHz[*1]
	Standby mode				22	—		Clock supply is stopped.

Note 1. This indicates that the clock is supplied to the A/D converter, but the A/D conversion is not performed.

Table 2.10 IOVCC wait current

Maximum measurement conditions: VCC = IOVCCn = 3.6 V, T_a = T_{opr} = 85°C
Typical measurement conditions: VCC = IOVCCn = 3.3 V, T_a = T_{opr} = 25°C

Item	Symbol	Typ.	Max.	Unit	Measurement conditions
IOVCC0 wait current	$I_{IOVCC0ST}$	10	—	nA	—
IOVCC1 wait current	$I_{IOVCC1ST}$	18	—		—
IOVCC0 and IOVCC1 wait current (total value)	—	—	1500		—

2.2.7 VCC Rise and Fall Gradient

Table 2.11 Rise and fall gradient characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	—
Allowable voltage change rising and falling gradient	dt/dVCC	2	—	20	ms/V	—

2.2.8 Internal Liner Regulator Characteristics

Table 2.12 Internal Liner Regulator Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
LDO startup time	t_{LDO}	220	—	—	μs	Figure 2.2
LDO stabilizaition time	t_{LDOWT}	60	—	—	μs	Figure 2.2

Note: The device should not be consume large currents during the LDO stabilization time to ensure stable operation.

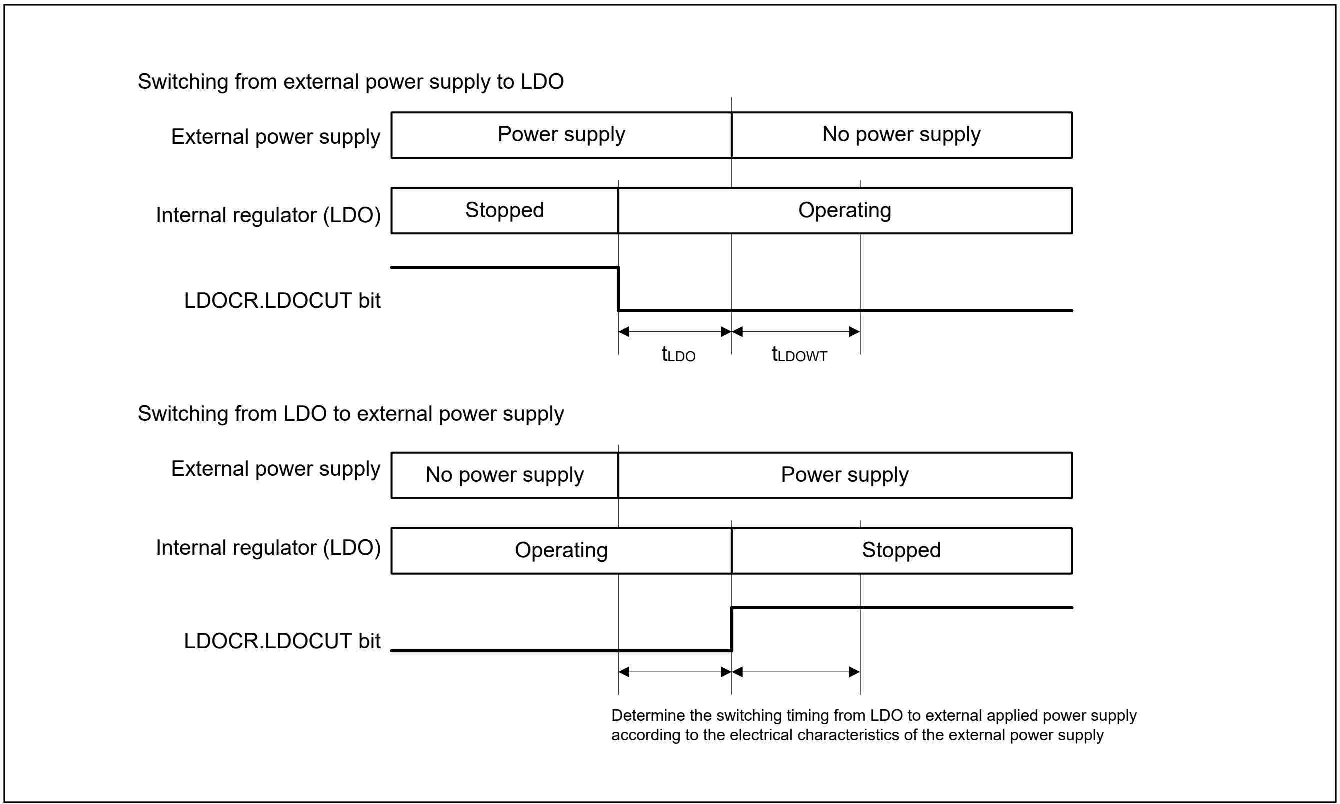


Figure 2.2 Switching timing between external power supply and LDO

2.3 AC Characteristics

2.3.1 Operating Frequency

Table 2.13 Operating frequency in each mode

Power control mode		Clock source	Symbol	Min.	Typ.	Max.	Unit
BOOST		System clock (ICLK)	f	—	—	64	MHz
		Peripheral module clock A (PCLKA)		—	—	64	
		Peripheral module clock B (PCLKB)		—	—	32	
NORMAL	High-speed	System clock (ICLK)		—	—	32	
		Peripheral module clock A (PCLKA)		—	—	32	
		Peripheral module clock B (PCLKB)		—	—	32	
	Low-speed	System clock (ICLK)		—	*1	2.3	
		Peripheral module clock A (PCLKA)		—	*1	2.3	
		Peripheral module clock B (PCLKB)		—	*1	2.3	
VBB		System clock (ICLK)		—	*2	37.6	kHz
		Peripheral module clock A (PCLKA)		—	*2	37.6	
		Peripheral module clock B (PCLKB)		—	*2	37.6	

Note: The minimum ICLK frequency is 1 MHz during programming or erasure of flash memory.
Note: Restriction on the clock frequency settings: ICLK/PCLKA ≥ PCLKB
Restriction on the clock frequency ratio (N: integer, and up to 64): ICLK/PCLKA:PCLKB = N:1
PCLKA and ICLK are at the same speed.
Note 1. The value is 2.0 MHz when the MOCO is selected as the clock source and the frequency is not being divided.
Note 2. The value is 32.768 kHz when the sub-clock oscillator is selected as the clock source and the frequency is not being divided.

2.3.2 Clock Timing

Table 2.14 Clock timing except for sub-clock oscillator (1 of 2)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
EXTAL external clock input cycle time	t_{EXcyc}	39	—	—	ns	Figure 2.3
EXTAL external clock input high-level pulse width	t_{EXH}	15	—	—	ns	
EXTAL external clock input low-level pulse width	t_{EXL}	15	—	—	ns	
EXTAL external clock input rise time	t_{EXr}	—	—	4.5	ns	
EXTAL external clock input fall time	t_{EXf}	—	—	4.5	ns	
Main clock oscillator frequency	f_{MAIN}	8	—	32	MHz	—
Main clock oscillation stabilization wait time (crystal)*1	$t_{MAINOSCWT}$	—	—	—	ms	Figure 2.4
LOCO clock oscillation frequency	f_{LOCO}	27.8	32.7	37.6	kHz	—
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	130	μs	Figure 2.5
IWDT-dedicated clock oscillation frequency	$f_{IWDTLOCO}$	13.9	16.35	18.8	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	1.4	2	2.3	MHz	—
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	—	—	16	μs	—

Table 2.14 Clock timing except for sub-clock oscillator (2 of 2)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
HOCO clock oscillation frequency*3	FLL correction function is disabled.	f_{HOCO24}	23.64	24	24.36	MHz	$0 \le T_a \le +85°C$
		f_{HOCO32}	31.52	32	32.48		
		f_{HOCO48}	47.28	48	48.72		
		f_{HOCO64}	63.04	64	64.96		
		f_{HOCO24}	23.64	24	24.36		$-40 \le T_a \le 0°C$
		f_{HOCO32}	31.52	32	32.48		
		f_{HOCO48}	47.28	48	48.72		
		f_{HOCO64}	63.04	64	64.96		
	FLL correction function is enabled.	f_{HOCO24}	23.88	24	24.12		$-40 \le T_a \le +85°C$
		f_{HOCO32}	31.84	32	32.16		
		f_{HOCO48}	47.76	48	48.24		
		f_{HOCO64}	63.68	64	64.32		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	320	µs	—
FLL correction function stabilization wait time		f_{FLLWT}	—	—	1800	µs	—

Note 1. For setting up the main clock oscillator, we recommend consulting the oscillator manufacturer regarding the results of oscillation evaluation and use the results for the oscillation stabilization time. The value of the MOSCWTCR register should correspond to at least that value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
Note 2. This is the time period between when HOCOCR.HCSTP is changed to 0 and when OSCSF.HOCOSF is changed to 1.
Note 3. The guaranteed values stated for this item apply to products in packages. If you are using WLBGA samples, note that the characteristics deteriorate once the device has been mounted on your system due to fluctuations in stress.

Table 2.15 Clock timing for sub-clock oscillator

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 2.6

Note 1. For setting up the sub-clock oscillator, we recommend consulting the oscillator manufacturer regarding the results of oscillation evaluation and use the results for the oscillation stabilization time. After changing the setting in the SOSCCR.SOSTP flag to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. We recommend using two times the value of the results of oscillation evaluation by the oscillator manufacturer.

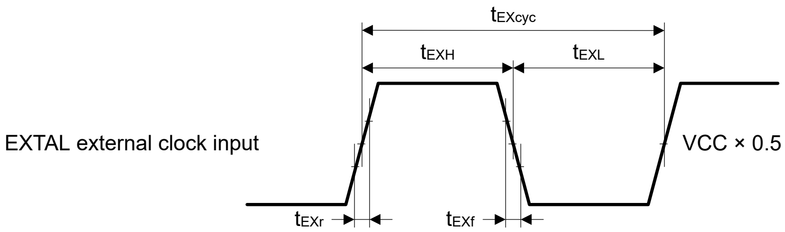


Figure 2.3 EXTAL external clock input timing

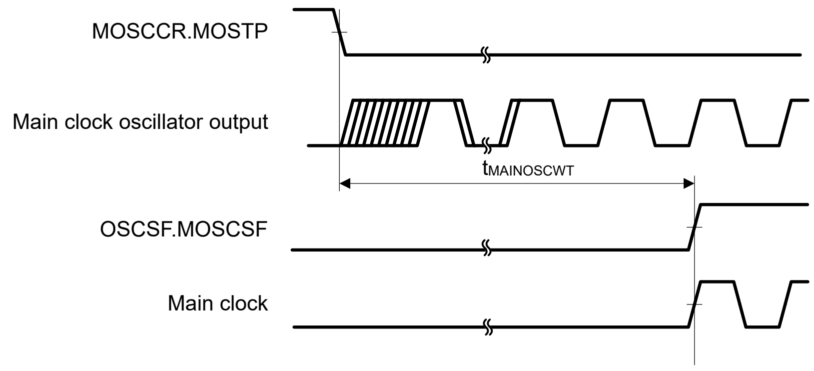


Figure 2.4 Main clock oscillation start timing

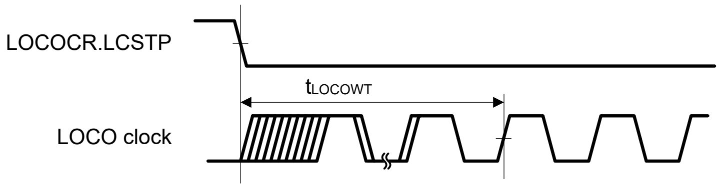


Figure 2.5 LOCO clock oscillation start timing

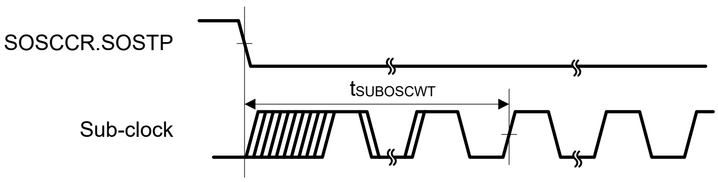


Figure 2.6 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.16 Reset timing

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
RES# pulse width	Power-on (in the normal start-up mode)		t_{RESWP}	44	—	—	ms	Figure 2.7
	Deep software standby mode		t_{RESWD}	7.7	—	—	ms	Figure 2.8
	Software standby mode		t_{RESWS}	1.2	—	—	ms	
	ALLPWON	Operation in boost mode	t_{RESW}	0.15	—	—	ms	
		Operation in normal mode	t_{RESW}	0.14	—	—	ms	
		Operation in low leakage current mode	t_{RESW}	0.62	—	—	ms	
		Transition between boost mode and normal mode	t_{RESW}	0.99	—	—	ms	
		Transition between normal mode and low leakage current mode	t_{RESW}	0.84	—	—	ms	
	EXFPWON	Operation in normal mode	t_{RESW}	0.46	—	—	ms	
		Operation in low leakage current mode	t_{RESW}	0.58	—	—	ms	
		Transition between normal mode and low leakage current mode	t_{RESW}	0.87	—	—	ms	
	MINPWON	Operation in normal mode	t_{RESW}	0.46	—	—	ms	
		Operation in low leakage current mode	t_{RESW}	0.58	—	—	ms	
		Transition between normal mode and low leakage current mode	t_{RESW}	0.87	—	—	ms	
	Transition between ALLPWON and EXFPWON in normal mode		t_{RESW}	0.78	—	—	ms	
	Transition between EXFPWON and MINPWON in normal mode		t_{RESW}	0.44	—	—	ms	
	Transition between ALLPWON and MINPWON in normal mode		t_{RESW}	0.78	—	—	ms	
	Transition between ALLPWON and EXFPWON in low leakage current mode		t_{RESW}	0.80	—	—	ms	
	Transition between EXFPWON and MINPWON in low leakage current mode		t_{RESW}	1.04	—	—	ms	
	Transition between ALLPWON and MINPWON in low leakage current mode		t_{RESW}	1.01	—	—	ms	
Wait time after release from the RES# pin reset			t_{RESWT}	—	19	22	ms	Figure 2.7, Figure 2.8

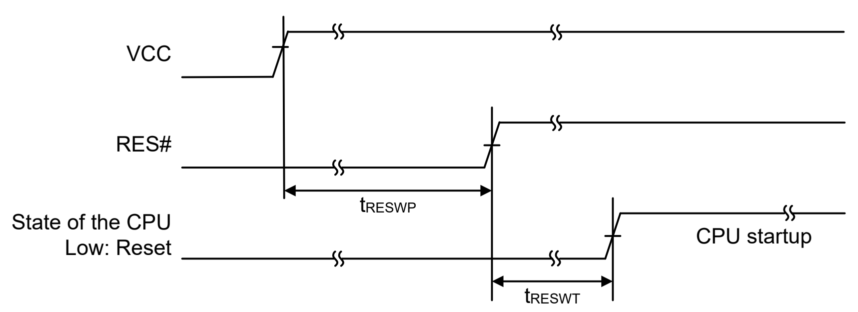


Figure 2.7 Timing of input through the reset pin when power is supplied

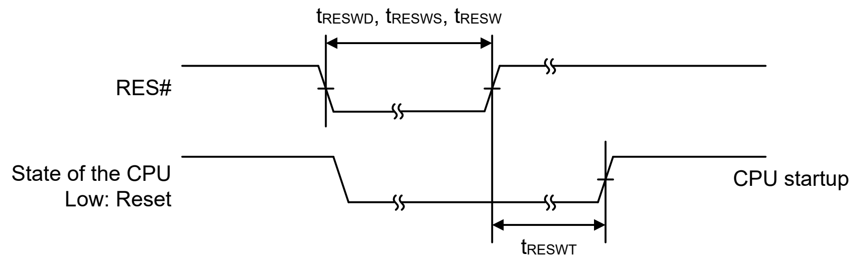


Figure 2.8 Reset input timing

2.3.4 Wakeup Timing

Table 2.17 Wakeup time from low power modes (standby modes) (1 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time from Software Standby mode (EXFPWON) to Operating mode (ALLPWON) *1*3	Normal	MOSC	t_{SBYMC}	—	—	3.1	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.8		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		SOSC	t_{SBYSC}	—	—	3.0		
		LOCO	t_{SBYLO}	—	—	3.5		
	BOOST	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
	VBB	SOSC	t_{SBYSC}	—	—	3.0	ms	
		LOCO	t_{SBYLO}	—	—	3.5		
Wakeup time from Software Standby mode (EXFPWON) to Operating mode (EXFPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.7	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.6		
		MOCO	t_{SBYMO}	—	—	0.4		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.05	ms	
		SOSC	t_{SBYSC}	—	—	0.4		
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		

Table 2.17 Wakeup time from low power modes (standby modes) (2 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time from Software Standby mode (MINPWON) to Operating mode (MINPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.7	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		MOCO	t_{SBYMO}	—	—	0.4		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.05	ms	
		SOSC	t_{SBYSC}	—	—	0.4		
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5	ms	
Wakeup time from Software Standby mode (MINPWON) to Operating mode (ALLPWON) *1*3	Normal	MOSC	t_{SBYMC}	—	—	3.1	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
		HOCO[*2]	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.8		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
		SOSC	t_{SBYSC}	—	—	3.0		
		LOCO	t_{SBYLO}	—	—	3.5		
	BOOST	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
		HOCO[*2]	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
	VBB	SOSC	t_{SBYSC}	—	—	3.2	ms	
		LOCO	t_{SBYLO}	—	—	3.7		
Wakeup time from Software Standby mode (MINPWON) to Operating mode (EXFPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.8	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
		HOCO[*2]	t_{SBYHO}	—	—	0.6		
		MOCO	t_{SBYMO}	—	—	0.5		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.2	ms	
		SOSC	t_{SBYSC}	—	—	0.5		
		LOCO	t_{SBYLO}	—	—	0.6		
	VBB	SOSC	t_{SBYSC}	—	—	1.0	ms	
		LOCO	t_{SBYLO}	—	—	1.1		

Table 2.17 Wakeup time from low power modes (standby modes) (3 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time from Software Standby mode (MINPWON) to Operating mode (MINPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.7	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
		MOCO	t_{SBYMO}	—	—	0.4		Figure 2.9 The division ratio of all oscillators is 1. SSBYPWG = 1, SSBYVBB = 0, SSBYACC = 0
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.05	ms	
		SOSC	t_{SBYSC}	—	—	0.4		
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		
Wakeup time from Software Standby mode (VBB MINPWON) to Operating mode (ALLPWON) *1*3	Normal	MOSC	t_{SBYMC}	—	—	3.2	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	1.0		
		MOCO	t_{SBYMO}	—	—	0.8		Figure 2.9 The division ratio of all oscillators is 1. Minimum current condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
		SOSC	t_{SBYSC}	—	—	3.1		
		LOCO	t_{SBYLO}	—	—	3.6		
	BOOST	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. Minimum current condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
	VBB	SOSC	t_{SBYSC}	—	—	3.2	ms	
		LOCO	t_{SBYLO}	—	—	3.7		

Table 2.17 Wakeup time from low power modes (standby modes) (4 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time from Software Standby mode (VBB MINPWON) to Operating mode (EXFPWON) [*1*3]	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.9	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
		HOCO[*2]	t_{SBYHO}	—	—	0.7		
		MOCO	t_{SBYMO}	—	—	0.6		Figure 2.9 The division ratio of all oscillators is 1. Minimum current condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.7	ms	
		SOSC	t_{SBYSC}	—	—	1.0		
		LOCO	t_{SBYLO}	—	—	1.1		
	VBB	SOSC	t_{SBYSC}	—	—	1.0	ms	
		LOCO	t_{SBYLO}	—	—	1.1		
Wakeup time from Software Standby mode (VBB MINPWON) to Operating mode (MINPWON) [*1*3]	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.8	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
		MOCO	t_{SBYMO}	—	—	0.5		Figure 2.9 The division ratio of all oscillators is 1. Minimum current condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 0
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.6	ms	
		SOSC	t_{SBYSC}	—	—	0.9		
		LOCO	t_{SBYLO}	—	—	1.1		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		

Table 2.17 Wakeup time from low power modes (standby modes) (5 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time in fast transition from Software Standby mode (EXFPWON) to Operating mode (ALLPWON) *1*3	Normal	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
		SOSC	t_{SBYSC}	—	—	3.0		
		LOCO	t_{SBYLO}	—	—	3.5		
	BOOST	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
	VBB	SOSC	t_{SBYSC}	—	—	3.0	ms	
		LOCO	t_{SBYLO}	—	—	3.5		
Wakeup time in fast transition from Software Standby mode (EXFPWON) to Operating mode (EXFPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.4	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
		HOCO*2	t_{SBYHO}	—	—	0.3		
		MOCO	t_{SBYMO}	—	—	0.05		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.05	ms	
		SOSC	t_{SBYSC}	—	—	0.4		
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		

Table 2.17 Wakeup time from low power modes (standby modes) (6 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time in fast transition from Software Standby mode (MINPWON) to Operating mode (MINPWON) [*1*3]	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.4	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
		MOCO	t_{SBYMO}	—	—	0.05		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 1
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.05	ms	
		SOSC	t_{SBYSC}	—	—	0.4		
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		
Wakeup time in fast transition from Software Standby mode (VBB MINWON) to Operating mode (ALLPWON) [*1*3]	Normal	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
		HOCO[*2]	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
		SOSC	t_{SBYSC}	—	—	3.0		
		LOCO	t_{SBYLO}	—	—	3.5		
	BOOST	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
		HOCO[*2]	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
	VBB	SOSC	t_{SBYSC}	—	—	3.0	ms	
		LOCO	t_{SBYLO}	—	—	3.5		

Table 2.17 Wakeup time from low power modes (standby modes) (7 of 7)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time in fast transition from Software Standby mode (VBB MINPWON) to Operating mode (EXFPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.6	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
		HOCO*2	t_{SBYHO}	—	—	0.4		
		MOCO	t_{SBYMO}	—	—	0.3		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.3	ms	
		SOSC	t_{SBYSC}	—	—	0.6		
		LOCO	t_{SBYLO}	—	—	0.7		
	VBB	SOSC	t_{SBYSC}	—	—	0.5	ms	
		LOCO	t_{SBYLO}	—	—	0.7		
Wakeup time in fast transition from Software Standby mode (VBB MINPWON) to Operating mode (MINPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.5	ms	Figure 2.9 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
		MOCO	t_{SBYMO}	—	—	0.2		Figure 2.9 The division ratio of all oscillators is 1. Minimum transition time condition: SSBYPWG = 1, SSBYVBB = 1, SSBYACC = 1
	Normal, Low-speed	MOCO	t_{SBYMO}	—	—	0.2	ms	
		SOSC	t_{SBYSC}	—	—	0.5		
		LOCO	t_{SBYLO}	—	—	0.6		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		
Wait time after cancellation of Software Standby mode			t_{SBYWT}	—	—	*4	ms	Figure 2.9
Wakeup time from Deep Software Standby mode (on normal start-up mode)			t_{DSBY}	—	—	6.8	ms	Figure 2.10
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	—	—	22.0	ms	

Note 1. The wakeup time is determined by the system clock source. When multiple oscillators are active, the wakeup time can be determined with the following equation:
Total wakeup time = wakeup time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPCRC.MSTPC0 = 0 (cancel the CAC module-stop state)).

Note 2. HOCO clock frequency = 32 MHz

Note 3. This value is a reference value because the shipment test is not performed.

Note 4. Wait time = 3 × PCLKB period + 14 × ICLK period

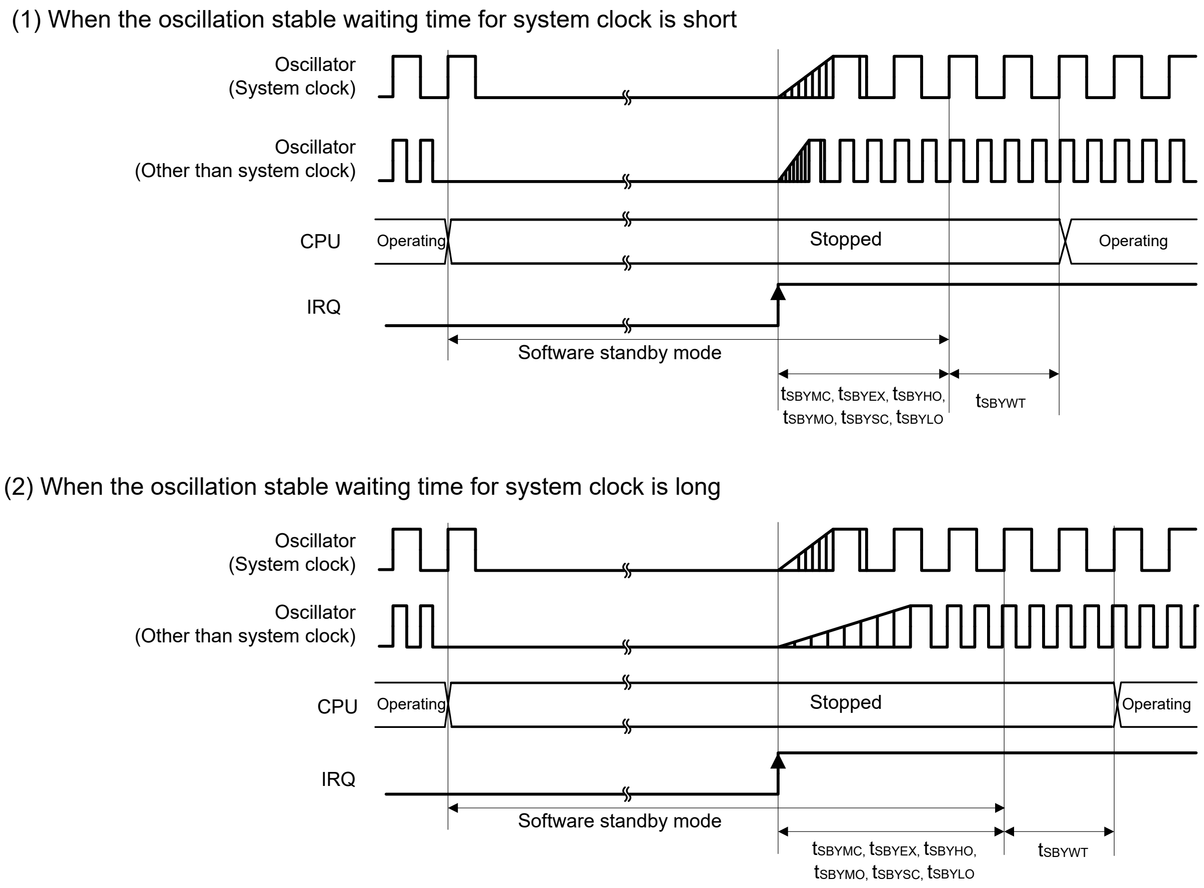


Figure 2.9 Software standby mode cancellation timing

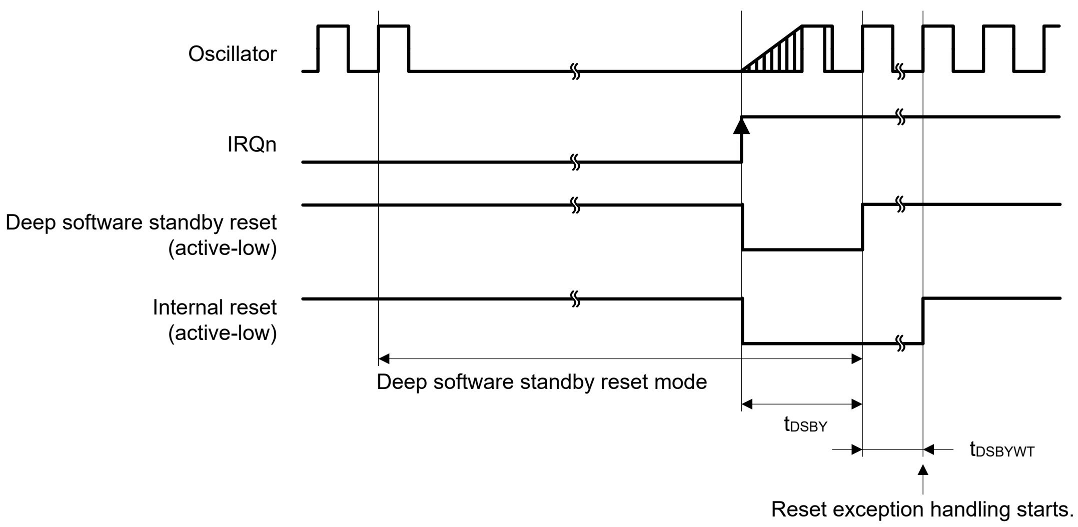


Figure 2.10 Deep software standby mode cancellation timing

Table 2.18 Wakeup time from software standby mode to snooze mode

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Wakeup time from Software Standby mode (EXFPWON) to Snooze mode (ALLPWON) *1*3	Normal	MOSC	t_{SBYMC}	—	—	3.1	ms	Figure 2.11 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.8		Figure 2.11 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		SOSC	t_{SBYSC}	—	—	3.0		
		LOCO	t_{SBYLO}	—	—	3.4		
	BOOST	MOSC	t_{SBYMC}	—	—	3.0	ms	Figure 2.11 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.9		
		MOCO	t_{SBYMO}	—	—	0.7		Figure 2.11 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
	VBB	SOSC	t_{SBYSC}	—	—	3.0	ms	
		LOCO	t_{SBYLO}	—	—	3.5		
Wakeup time from Software Standby mode (EXFPWON) to Snooze mode (EXFPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.7	ms	Figure 2.11 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		HOCO*2	t_{SBYHO}	—	—	0.6		
		MOCO	t_{SBYMO}	—	—	0.4		Figure 2.11 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
	Normal, Low-speed	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		
Wakeup time from Software Standby mode (MINPWON) to Snooze mode (MINPWON) *1*3	Normal, High-speed	MOSC	t_{SBYMC}	—	—	2.7	ms	Figure 2.11 Each division ratio of ICLK/PCLKA and PCLKB is 1/8. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
		MOCO	t_{SBYMO}	—	—	0.4		Figure 2.11 The division ratio of all oscillators is 1. SSBYPWG = 0, SSBYVBB = 0, SSBYACC = 0
	Normal, Low-speed	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5		
	VBB	SOSC	t_{SBYSC}	—	—	0.4	ms	
		LOCO	t_{SBYLO}	—	—	0.5	ms	

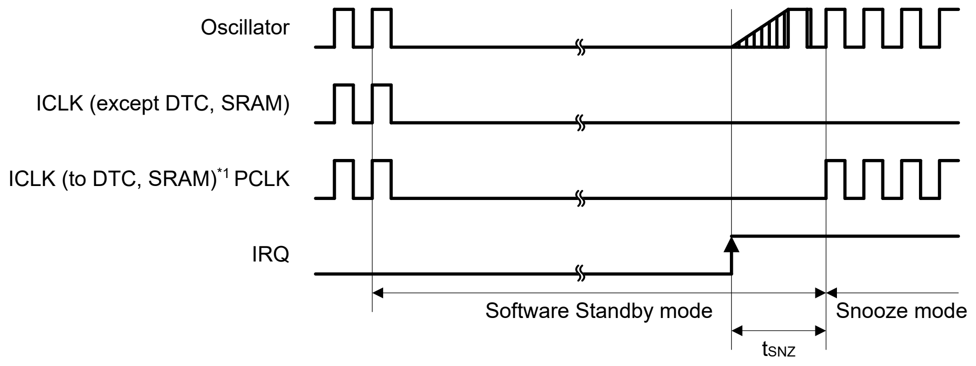
Note: When crystal frequency is 32 MHz (when Main Clock Oscillator Wait Control Register (MOSCWTCR) is 0x05).

Note 1. The wakeup time is determined by the system clock source. When multiple oscillators are active, the wakeup time can be determined with the following equation:

Total wakeup time = wakeup time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPCRC.MSTPC0 = 0 (cancel the CAC module-stop state)).

Note 2. HOCO clock frequency = 32 MHz

Note 3. This value is a reference value because the shipment test is not performed.



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.11 Wakeup time from software standby mode to snooze mode

2.3.5 Transition Time Between Operation Modes

Table 2.19 Transition time between each power supply modes (1 of 2)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit
Transition time from ALLPWON to EXFPWON	Normal (ALLPWON) → Normal High-speed (EXFPWON)	MOSC	t_{MDMC}	—	—	2.7	ms
		HOCO*1	t_{MDHO}	—	—	0.6	
		MOCO	t_{MDMO}	—	—	0.4	
	Normal (ALLPWON) → Normal Low-speed (EXFPWON)	MOCO	t_{MDMO}	—	—	0.5	ms
		SOSC	t_{MDSC}	—	—	1.7	
		LOCO	t_{MDLO}	—	—	2.1	
	VBB (ALLPWON) → VBB (EXFPWON)	SOSC	t_{MDSC}	—	—	1.7	ms
		LOCO	t_{MDLO}	—	—	2.1	
Transition time from EXFPWON to ALLPWON	Normal High-speed (EXFPWON) → Normal (ALLPWON)	MOSC	t_{MDMC}	—	—	3.0	ms
		HOCO*1	t_{MDHO}	—	—	0.9	
		MOCO	t_{MDMO}	—	—	0.7	
	Normal Low-speed (EXFPWON) → Normal (ALLPWON)	MOCO	t_{MDMO}	—	—	0.8	ms
		SOSC	t_{MDSC}	—	—	3.9	
		LOCO	t_{MDLO}	—	—	4.6	
	VBB (EXFPWON) → VBB (ALLPWON)	SOSC	t_{MDSC}	—	—	4.2	ms
		LOCO	t_{MDLO}	—	—	4.7	

Table 2.19 Transition time between each power supply modes (2 of 2)

Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit
Transition time from ALLPWON to MINPWON	Normal (ALLPWON) → Normal High-speed (MINPWON)	MOSC	t_{MDMC}	—	—	2.7	ms
		MOCO	t_{MDMO}	—	—	0.4	
	Normal (ALLPWON) → Normal Low-speed (MINPWON)	MOCO	t_{MDMO}	—	—	0.5	ms
		SOSC	t_{MDSC}	—	—	1.7	
		LOCO	t_{MDLO}	—	—	2.1	
	VBB (ALLPWON) → VBB (MINPWON)	SOSC	t_{MDSC}	—	—	1.4	ms
		LOCO	t_{MDLO}	—	—	1.8	
Transition time from MINPWON to ALLPWON	Normal High-speed (MINPWON) → Normal (ALLPWON)	MOSC	t_{MDMC}	—	—	3.0	ms
		MOCO	t_{MDMO}	—	—	0.7	
	Normal Low-speed (MINPWON) → Normal (ALLPWON)	MOCO	t_{MDMO}	—	—	0.8	ms
		SOSC	t_{MDSC}	—	—	3.9	
		LOCO	t_{MDLO}	—	—	4.6	
	VBB (MINPWON) → VBB (ALLPWON)	SOSC	t_{MDSC}	—	—	4.4	ms
		LOCO	t_{MDLO}	—	—	4.9	
Transition time from EXFPWON to MINPWON	Normal High-speed (EXFPWON) → Normal High-speed (MINPWON)	MOSC	t_{MDMC}	—	—	2.4	ms
		MOCO	t_{MDMO}	—	—	0.07	
	Normal High-speed (EXFPWON) → Normal Low-speed (MINPWON)	MOCO	t_{MDMO}	—	—	0.07	ms
		SOSC	t_{MDSC}	—	—	1.3	
		LOCO	t_{MDLO}	—	—	1.7	
	VBB (EXFPWON) → VBB (MINPWON)	SOSC	t_{MDSC}	—	—	1.4	ms
		LOCO	t_{MDLO}	—	—	1.8	
Transition time from MINPWON to EXFPWON	Normal High-speed (MINPWON) → Normal (EXFPWON)	MOSC	t_{MDMC}	—	—	2.5	ms
		MOCO	t_{MDMO}	—	—	0.2	
	Normal Low-speed (MINPWON) → Normal (EXFPWON)	MOCO	t_{MDMO}	—	—	0.2	ms
		SOSC	t_{MDSC}	—	—	1.4	
		LOCO	t_{MDLO}	—	—	1.8	
	VBB (MINPWON) → VBB (EXFPWON)	SOSC	t_{MDSC}	—	—	1.9	ms
		LOCO	t_{MDLO}	—	—	2.3	

Note: The transition time is determined by the system clock source. When multiple oscillators are active, the wakeup time can be determined with the following equation:
Total transition time = stabilization time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPCRC.MSTPC0 = 0 (cancel the CAC module-stop state)).

Note: The division ratio of all oscillators is 1.

Note: This value is a reference value because the shipment test is not performed.

Note 1. HOCO clock frequency = 32 MHz

Table 2.20 Transition time between each power control modes

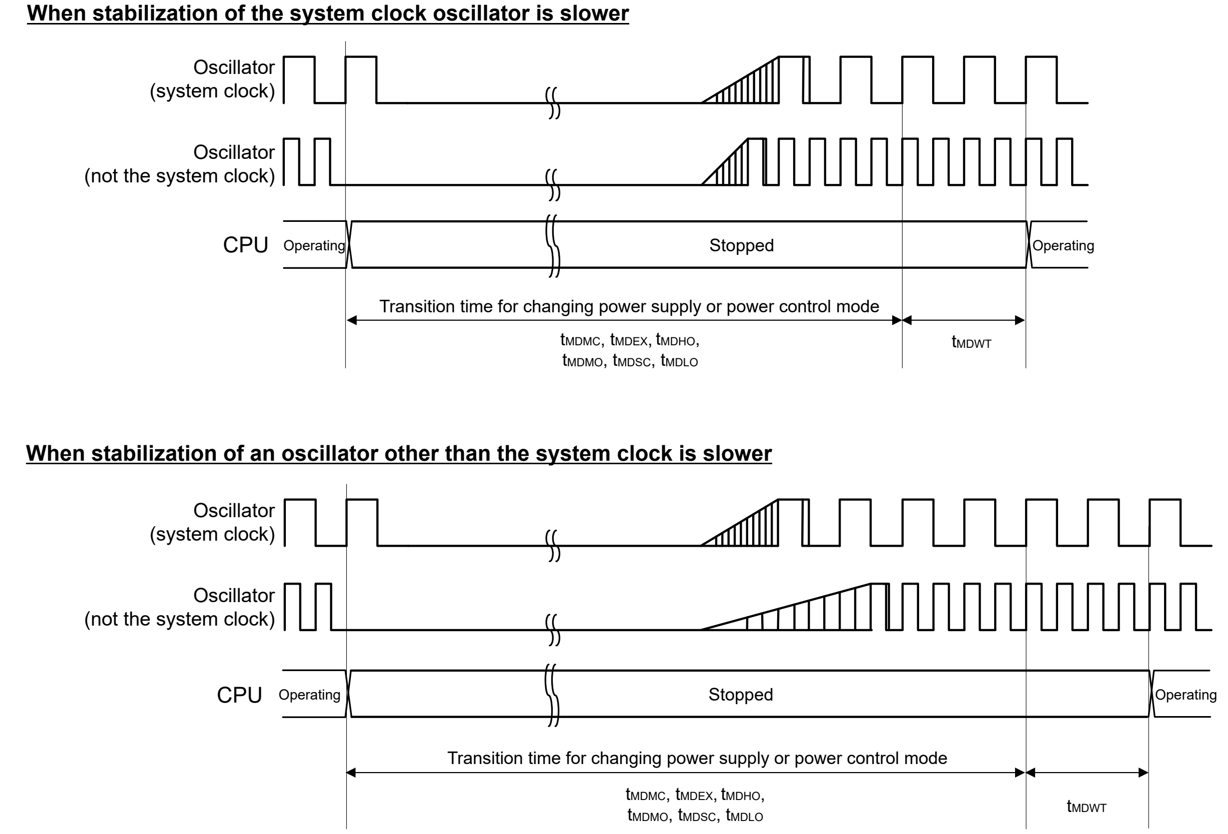
Item	Power control mode	System clock source	Symbol	Min.	Typ.	Max.	Unit
Transition between Normal and Boost	Normal (ALLPWON) → Boost (ALLPWON)	MOSC	t_{MDMC}	—	—	3.4	ms
		HOCO*1	t_{MDHO}	—	—	1.2	
		MOCO	t_{MDMO}	—	—	1.1	
	Boost (ALLPWON) → Normal (ALLPWON)	MOSC	t_{MDMC}	—	—	2.4	ms
		HOCO*1	t_{MDHO}	—	—	0.3	
		MOCO	t_{MDMO}	—	—	0.07	
Transition between Normal and VBB	Normal (ALLPWON) → VBB (ALLPWON)	SOSC	t_{MDSC}	—	—	1.8	ms
		LOCO	t_{MDLO}	—	—	2.2	
	Normal (EXFPWON) → VBB (EXFPWON)	SOSC	t_{MDSC}	—	—	1.8	ms
		LOCO	t_{MDLO}	—	—	2.2	
	Normal (MINPWON) → VBB (MINPWON)	SOSC	t_{MDSC}	—	—	1.4	ms
		LOCO	t_{MDLO}	—	—	1.8	
	VBB (ALLPWON) → Normal (ALLPWON)	SOSC	t_{MDSC}	—	—	1.7	ms
		LOCO	t_{MDLO}	—	—	2.0	
	VBB (EXFPWON) → Normal (EXFPWON)	SOSC	t_{MDSC}	—	—	1.7	ms
		LOCO	t_{MDLO}	—	—	2.1	
	VBB (MINPWON) → Normal (MINPWON)	SOSC	t_{MDSC}	—	—	1.8	ms
		LOCO	t_{MDLO}	—	—	2.2	
Transition between Boost and VBB	Boost (ALLPWON) → VBB (ALLPWON)	SOSC	t_{MDSC}	—	—	1.8	ms
		LOCO	t_{MDLO}	—	—	2.2	
	VBB (ALLPWON) → Boost (MINPWON)	SOSC	t_{MDSC}	—	—	2.6	ms
		LOCO	t_{MDLO}	—	—	3.0	
Transition from High-speed to Low-speed	ALLPWON		t_{HILOW}	—	—	0.003	ms
	EXFPWON		t_{HILOW}	—	—	0.5	
	MINPWON		t_{HILOW}	—	—	0.5	
Transition from Low-speed to High-speed	ALLPWON		t_{LOWHI}	—	—	0.003	ms
	EXFPWON		t_{LOWHI}	—	—	0.4	
	MINPWON		t_{LOWHI}	—	—	0.4	

Note: The transition time is determined by the system clock source. When multiple oscillators are active, the wakeup time can be determined with the following equation:
Total transition time = stabilization time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPCRC.MSTPC0 = 0 (cancel the CAC module-stop state)).

Note: The division ratio of all oscillators is 1.

Note: This value is a reference value because the shipment test is not performed.

Note 1. HOCO clock frequency = 32 MHz



Note: t_{MDWT} = 3 × PCLKB period + 14 × ICLK period

Figure 2.12 Transition timing between operation modes

2.3.6 Interrupt Input Timing

Table 2.21 Interrupt input timing (1 of 2)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
NMI pulse width	t_{NMIW}	6000	—	—	ns	Software Standby mode on VBB mode
		1000	—	—		Software Standby mode other than above
		300	—	—		Deep Software Standby mode
		4	—	—	t_{Pcyc}*1	Other than above
IRQn pulse width	t_{IRQW}	6000	—	—	ns	Software Standby mode on VBB mode
		1000	—	—		Software Standby mode other than above
		300	—	—		Deep Software Standby mode
		4	—	—	t_{Pcyc}*1	Other than above (IRQCRi.IRQMD[1:0] = 00b, 01b)
		5	—	—		Other than above (IRQCRi.IRQMD[1:0] = 10b)

Table 2.21 Interrupt input timing (2 of 2)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
KINT pulse width	t_{KINTW}	6000	—	—	ns	Software Standby mode on VBB mode
		1000	—	—		Software Standby mode other than above
		4	—	—	t_{Pcyc}*1	Other than above

Note 1. t_{Pcyc}: PCLKB cycle

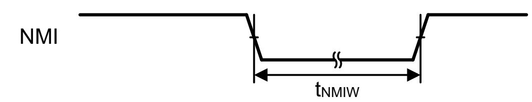


Figure 2.13 NMI interrupt input timing

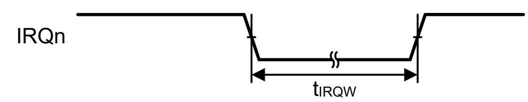


Figure 2.14 IRQn interrupt input timing

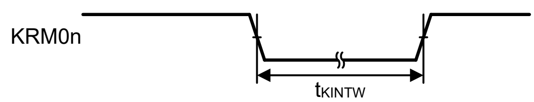


Figure 2.15 KINT interrupt input timing

2.3.7 Trigger Timing of I/O port, POE, GPT, AGT, and ADC14

Table 2.22 Trigger timing of I/O port, POE, GPT, AGT, and ADC14 (1 of 2)

Item			Symbol	Min.	Typ.	Max.	Unit*1	Measurement conditions
I/O port	Input data pulse width		t_{PRW}	2.5	—	—	t_{Pcyc}	Figure 2.16
	ELC event pulse input width			4	—	—		
POE	POE input trigger pulse width		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 2.17
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	—	t_{Pcyc}	Figure 2.18
		Both edges		2.5	—	—	t_{Pcyc}	

Table 2.22 Trigger timing of I/O port, POE, GPT, AGT, and ADC14 (2 of 2)

Item		Symbol	Min.	Typ.	Max.	Unit[*1]	Measurement conditions
AGT/AGTW	AGTIOn/AGTWIOn input cycle	t_{ACYC}	4	—	—	t_{Pcyc}	Figure 2.19, AGTMR1.TEDGPL = 0 AGTMR1.TMOD[2:0] = 010b
			9	—	—	t_{Pcyc}	Figure 2.19, AGTMR1.TEDGPL = 1 AGTMR1.TMOD[2:0] = 010b
	AGTIOn/AGTWIOn input high-level width, low-level width	t_{ACKWH}, t_{ACKWL}	1	—	—	t_{Pcyc}	Figure 2.19, AGTMR1.TEDGPL = 0 AGTMR1.TMOD[2:0] = 010b
			4	—	—	t_{Pcyc}	Figure 2.19, AGTMR1.TEDGPL = 1 AGTMR1.TMOD[2:0] = 010b
	AGTEEn/AGTWEEn input high-level width, low-level width	t_{ACKWH}, t_{ACKWL}	—	1	—	t_{ACYC}	Figure 2.19, AGTMR1.TEDGPL = 0 AGTMR1.TMOD[2:0] = 010b
			4	—	—	t_{Pcyc}	Figure 2.19, AGTMR1.TEDGPL = 1 AGTMR1.TMOD[2:0] = 010b
ADC14	14-bit A/D converter trigger input pulse width	t_{TRGW}	1.5	—	—	t_{Pcyc}	Figure 2.20

Note: n = 0, 1
Note 1. t_{Pcyc}: This indicates a clock cycle of PCLKA for GPT port, and PCLKB for I/O port, POE, AGT, and ADC14 ports.

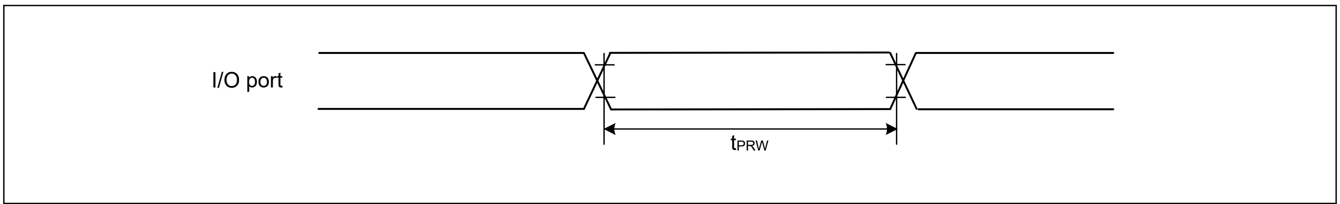


Figure 2.16 I/O port input data pulse width

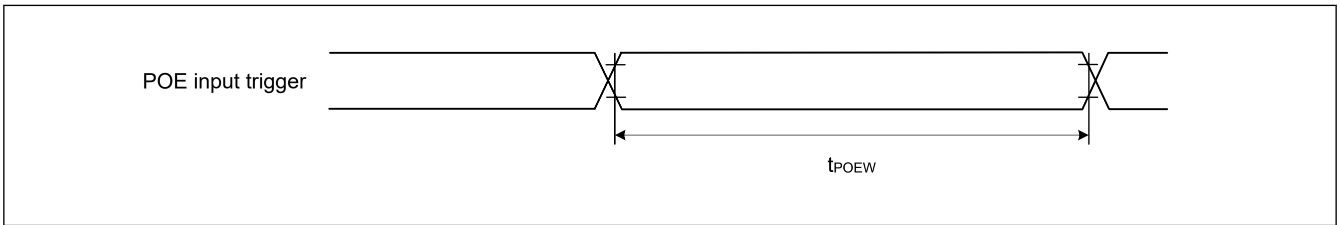


Figure 2.17 POE input trigger pulse width

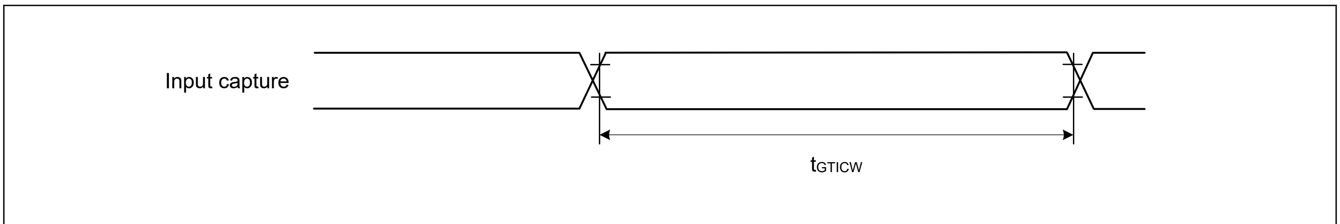


Figure 2.18 GPT input capture pulse width

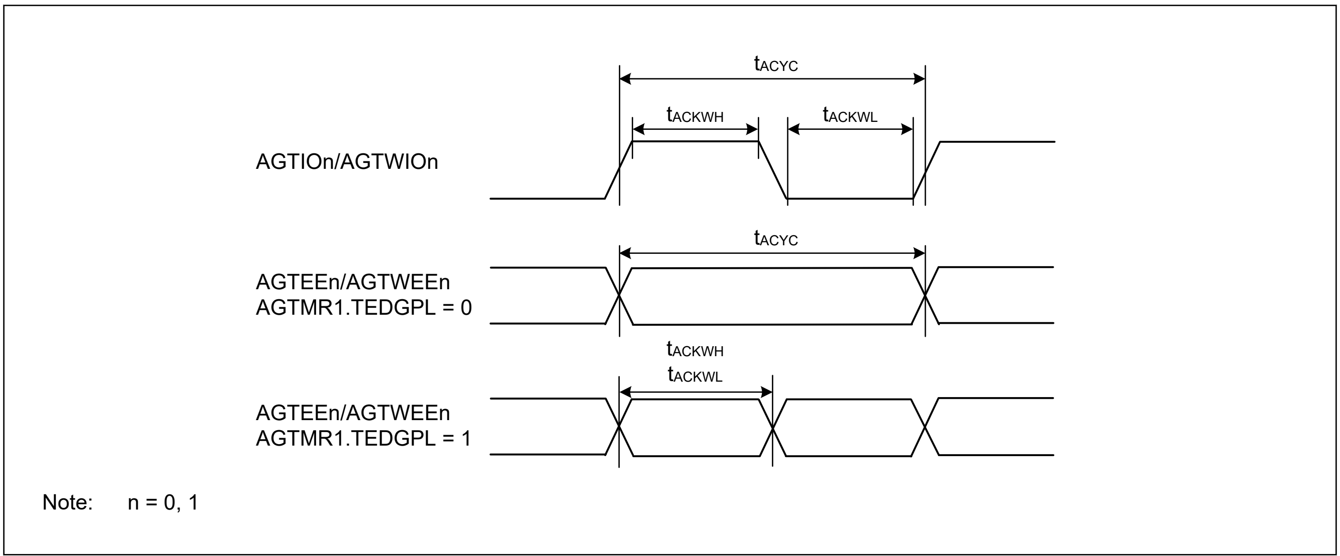


Figure 2.19 AGT/AGTW input timing

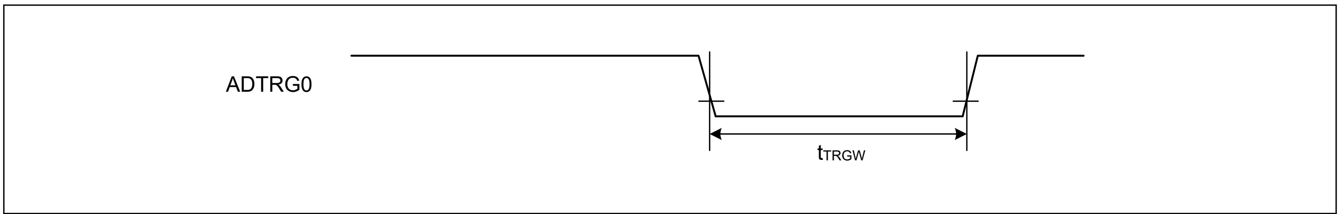


Figure 2.20 ADC14 trigger input timing

2.3.8 CAC Timing

Table 2.23 CAC timing

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{cac}*2	t_{CACREF}	$4.5t_{cac} + 3t_{Pcyc}$	—	—	ns	—
		t_{Pcyc}*1 > t_{cac}*2		$5t_{cac} + 6.5t_{Pcyc}$	—	—	ns	

Note 1. t_{Pcyc}: PCLKB clock cycle
Note 2. t_{cac}: CAC count clock source cycle

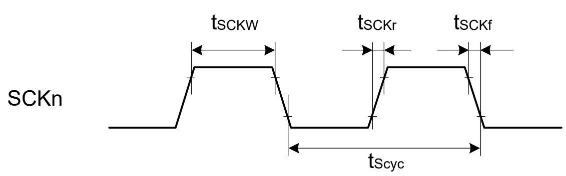
2.3.9 SCI Timing

Table 2.24 SCI timing (1)

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

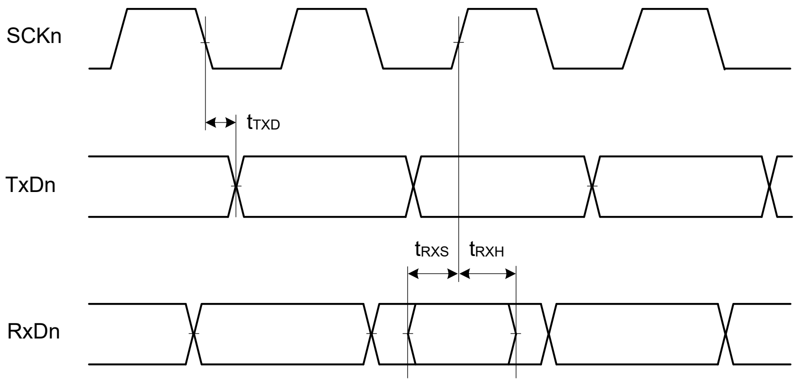
Item			Symbol	Min.	Max.	Unit*1	Measurement conditions
SCI	Frequency (SCI0, SCI1)	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	Frequency (other than SCI0 or SCI1)			—	32		
	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.21
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1 × t_{Pcyc}	ns	
	Input clock fall time		t_{SCKf}	—	1 × t_{Pcyc}	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	1 × t_{Pcyc}	ns	
	Output clock fall time		t_{SCKf}	—	1 × t_{Pcyc}	ns	
	Transmit data delay	Master	t_{TXD}	—	40	ns	Figure 2.22
		Slave		—	55	ns	
	Receive data setup time	Master	t_{RXS}	45	—	ns	
		Slave		27	—	ns	
	Receive data hold time	Master	t_{RXH}	5	—	ns	
		Slave		40	—	ns	

Note 1. t_{Pcyc}: This indicates a clock cycle of PCLKA for SCI0 and SCI1 ports, and PCLKB for the ports from SCI2 to SCI5 and SCI9 port.



Note: n = 0 to 5, 9

Figure 2.21 SCK clock input timing



Note: n = 0 to 5, 9

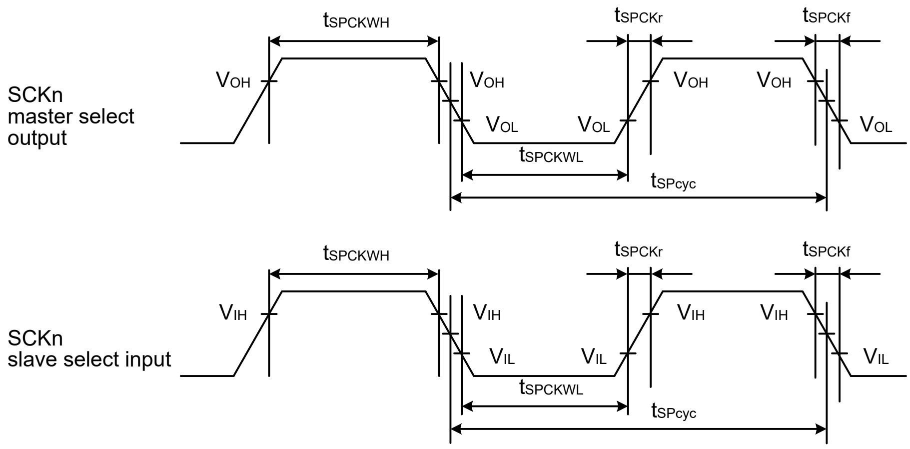
Figure 2.22 SCI input/output timing in clock synchronous mode

Table 2.25 SCI timing (2)

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

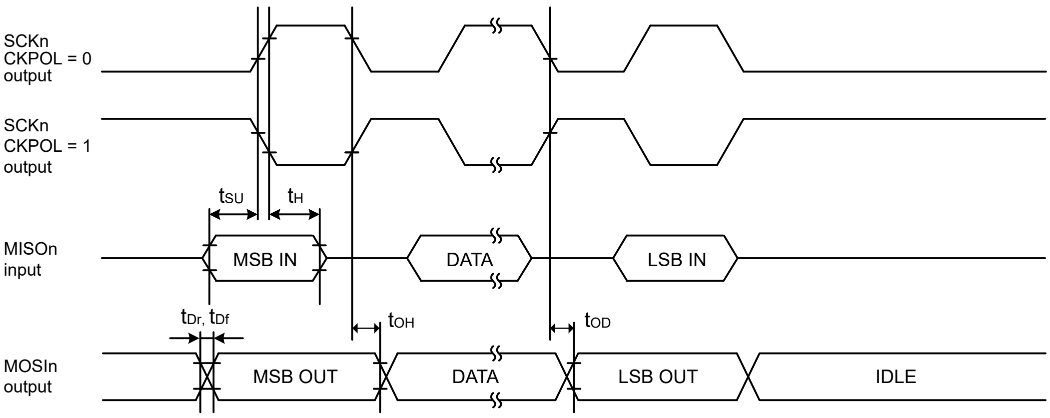
Item			Symbol	Min.	Max.	Unit*1	Measurement conditions
Simple SPI	Frequency (SCI0, SCI1)	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	Frequency (other than SCI0 or SCI1)			—	32		
	SCK clock cycle	Master	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.23
		Slave		6	—		
	SCK clock high-level pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low-level pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr}, t_{SPCKf}	—	1 × t_{Pcyc}	ns	
	Data input setup time	Master	t_{SU}	45	—	ns	Figure 2.24 to Figure 2.27
		Slave		27	—		
	Data input hold time	Master	t_H	33.3	—	ns	
		Slave		40	—		
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay	Master	t_{OD}	—	40	ns	
		Slave		—	65		
	Data output hold time	Master	t_{OH}	-10	—	ns	
		Slave		-10	—		
	Data rise and fall time		t_{Dr}, t_{Df}	—	1 × t_{Pcyc}	ns	
	Slave access time	BOOST	t_{SA}	—	8	t_{Pcyc}	Figure 2.26 Figure 2.27
		NORMAL		—	6		
	Slave output release time	BOOST	t_{REL}	—	8	t_{Pcyc}	
		NORMAL		—	6		

Note 1. t_{Pcyc}: This indicates a clock cycle of PCLKA for SCI0 and SCI1 ports, and PCLKB for the ports from SCI2 to SCI5 and SCI9 port.



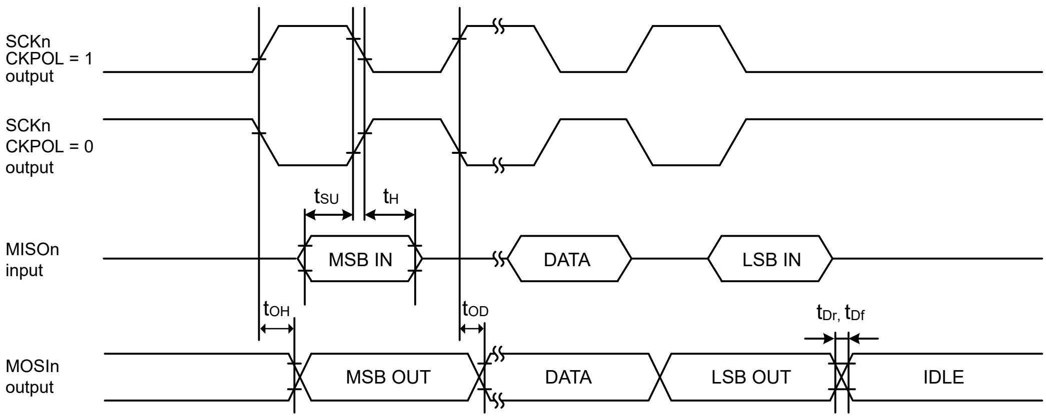
Note: n = 0 to 5, 9

Figure 2.23 SCK clock input/output timing (simple SPI mode)



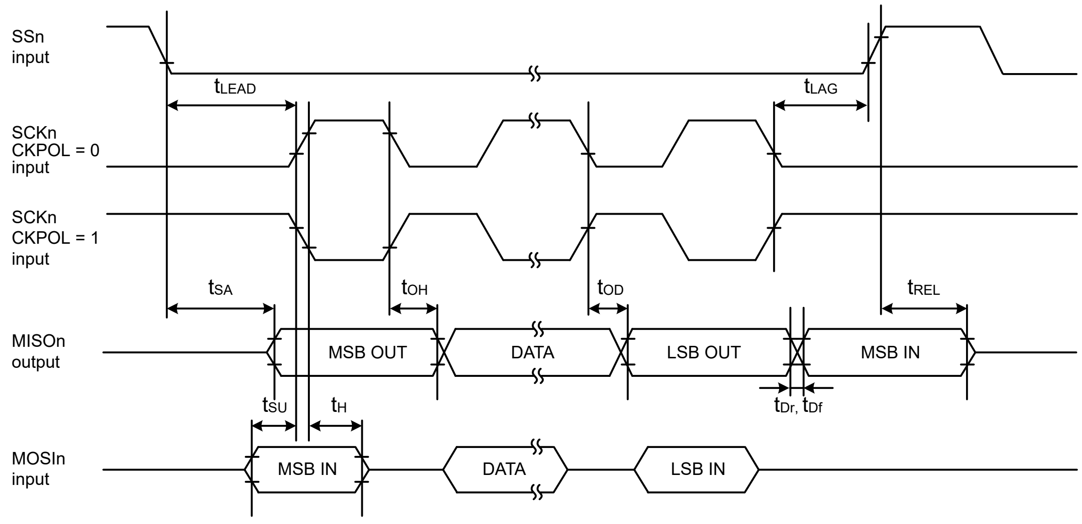
Note: n = 0 to 5, 9

Figure 2.24 SCK input/output timing (simple SPI mode) (master, SPMR.CKPH = 1)



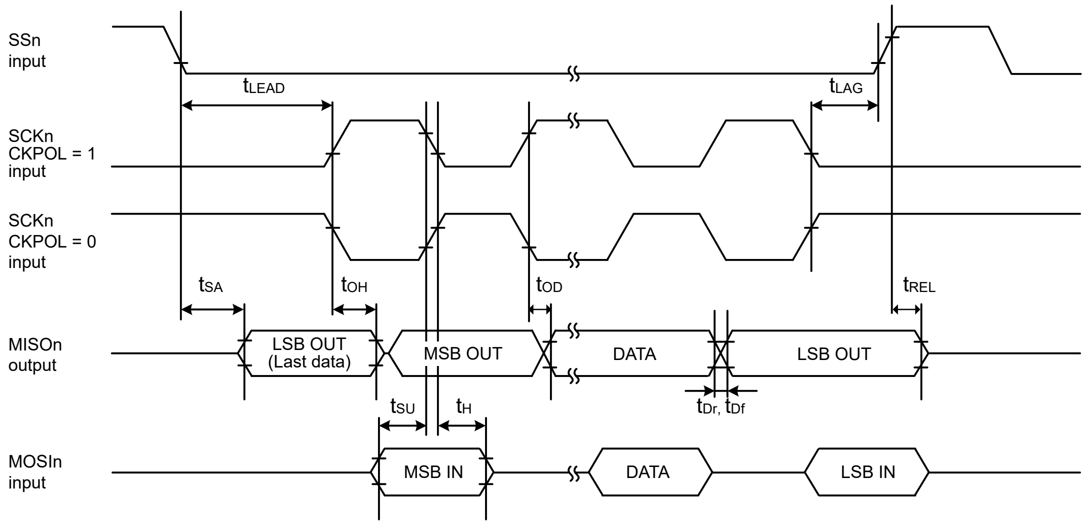
Note: n = 0 to 5, 9

Figure 2.25 SCK input/output timing (simple SPI mode) (master, SPMR.CKPH = 0)



Note: n = 0 to 5, 9

Figure 2.26 SCK input/output timing (simple SPI mode) (slave, SPMR.CKPH = 1)



Note: n = 0 to 5, 9

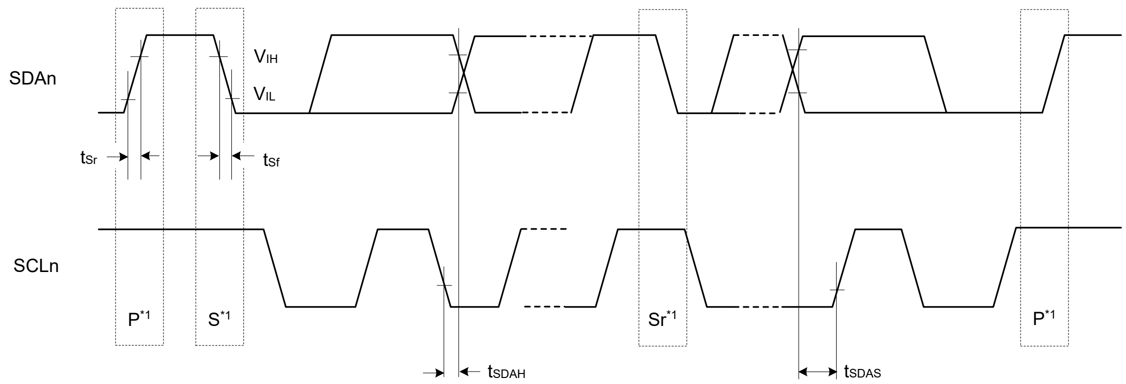
Figure 2.27 SCK input/output timing (simple SPI mode) (slave, SPMR.CKPH = 0)

Table 2.26 SCI timing (3)

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

Item			Symbol	Min.	Max.	Unit*2	Measurement conditions
Simple IIC (Standard mode)	Frequency (SCI0, SCI1)	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	Frequency (other than SCI0 or SCI1)			—	32		
	SDA input rise time		t_{Sr}	—	1000	ns	Figure 2.28
	SDA input fall time		t_{Sf}	—	300	ns	
	Data input setup time		t_{SDAS}	250	—	ns	Figure 2.28
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b*1	—	400	pF	
Simple IIC (Fast mode)	Frequency (SCI0, SCI1)	BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
	Frequency (other than SCI0 or SCI1)			—	32		—
	SCL, SDA input rise time		t_{Sr}	—	300	ns	Figure 2.28
	SCL, SDA input fall time		t_{Sf}	—	300	ns	
	Data input setup time		t_{SDAS}	100	—	ns	Figure 2.28
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b*1	—	400	pF	

Note 1. C_b indicates the total capacity of the bus line.
Note 2. t_{Pcyc}: This indicates a clock cycle of PCLKA for SCI0 and SCI1 ports, and PCLKB for the ports from SCI2 to SCI5 and SCI9 port.



Note: n = 0 to 5, 9
Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.28 SCK input/output timing (simple I²C mode)

2.3.10 SPI Timing

Table 2.27 SPI timing (1 of 2)

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

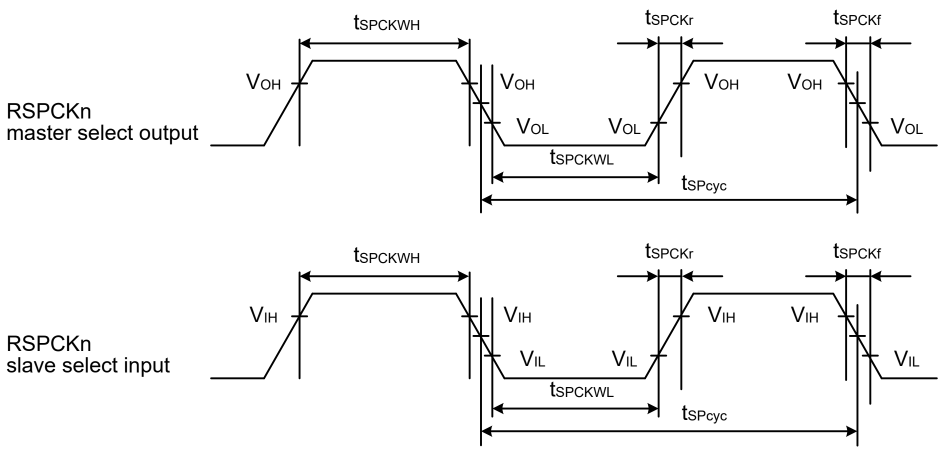
Item			Symbol	Min.	Max.	Unit*1	Measurement conditions
Frequency		BOOST	pclkfmax	—	64	MHz	—
		NORMAL		—	32		
RSPCK clock cycle	Master	BOOST	t_{SPcyc}	4	4096	t_{Pcyc}	Figure 2.29
		NORMAL		2	4096		
	Slave			6	4096		
RSPCK clock high-level pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			$3 \times t_{pcyc}$	—		
RSPCK clock low-level pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
	Slave			$3 \times t_{pcyc}$	—		
RSPCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	10	ns	Figure 2.29 IOVCCn ≥ 2.7V
	Input				1	μs	
Data input setup time	Master	BOOST	t_{SU}	25	—	ns	Figure 2.30 to Figure 2.35 IOVCCn ≥ 2.7V
		NORMAL		15	—		
	Slave			10	—		
Data input hold time	Master		t_{HF}	0	—	ns	Figure 2.30 to Figure 2.35 PCLKA division ratio is set to 1/2.
			t_H	1	—	t_{Pcyc}	Figure 2.30 to Figure 2.35 PCLKA division ratio is set to a value other than 1/2.
	Slave			20	—	ns	Figure 2.30 to Figure 2.35
SSL setup time	Master		t_{LEAD}	$-30 + N \times t_{SPcyc}$ *2	—	ns	Figure 2.30 to Figure 2.35
	Slave			$6 \times t_{pcyc}$	—	ns	
SSL hold time	Master		t_{LAG}	$-30 + N \times t_{SPcyc}$ *3	—	ns	
	Slave			$6 \times t_{pcyc}$	—	ns	
Data output delay	Master		t_{OD}	—	14	ns	Figure 2.30 to Figure 2.35 IOVCCn ≥ 2.7V
	Slave				50		
Data output hold time	Master		t_{OH}	0	—	ns	Figure 2.30 to Figure 2.35
	Slave			0	—		
Successive transmission delay	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{pcyc}$	ns	Figure 2.30 to Figure 2.35
	Slave			$6 \times t_{pcyc}$	—		

Table 2.27 SPI timing (2 of 2)

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

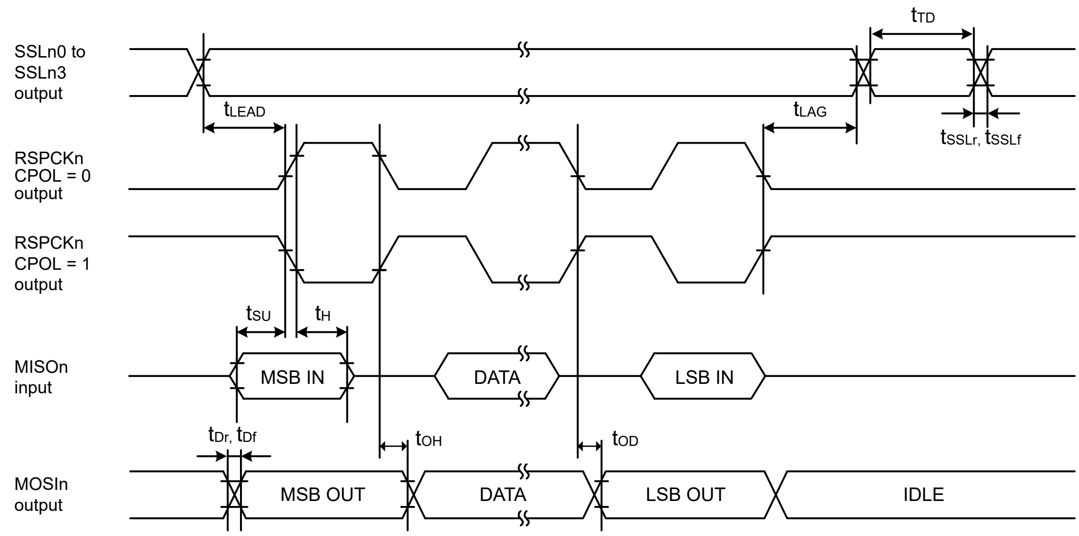
Item		Symbol	Min.	Max.	Unit[*1]	Measurement conditions
MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	10	ns	Figure 2.30 to Figure 2.35 IOVCCn ≥ 2.7V
	Input		—	1	µs	Figure 2.30 to Figure 2.35
SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	10	ns	Figure 2.30 to Figure 2.35 IOVCCn ≥ 2.7V
	Input		—	1	µs	Figure 2.30 to Figure 2.35
Slave access time		t_{SA}	—	2 × t_{pcyc} + 100	ns	Figure 2.34, Figure 2.35 IOVCCn ≥ 2.7V
Slave output release time		t_{REL}	—	2 × t_{pcyc} + 100	ns	Figure 2.34, Figure 2.35 IOVCCn ≥ 2.7V

Note 1. t_{Pcyc} indicates the clock cycle of PCLKA.
Note 2. “N” is the number of delay cycles for RSPCK clock set at SPCKD register.
Note 3. “N” is the number of delay cycles for RSPCK clock set at SSLND register.



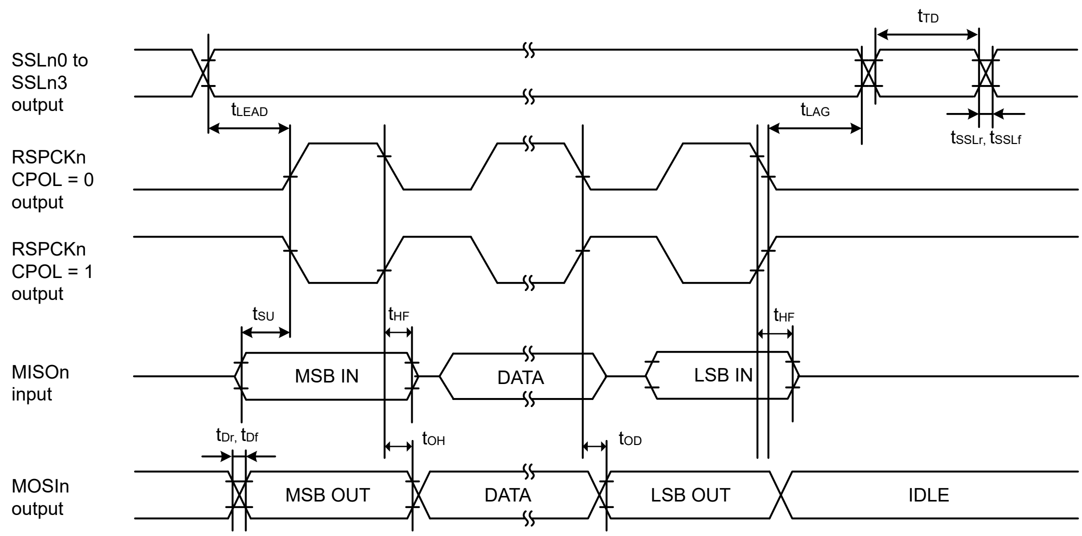
Note: n = A, B

Figure 2.29 SPI clock timing



Note: n = A, B

Figure 2.30 SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to a value other than 1/2)



Note: n = A, B

Figure 2.31 SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)

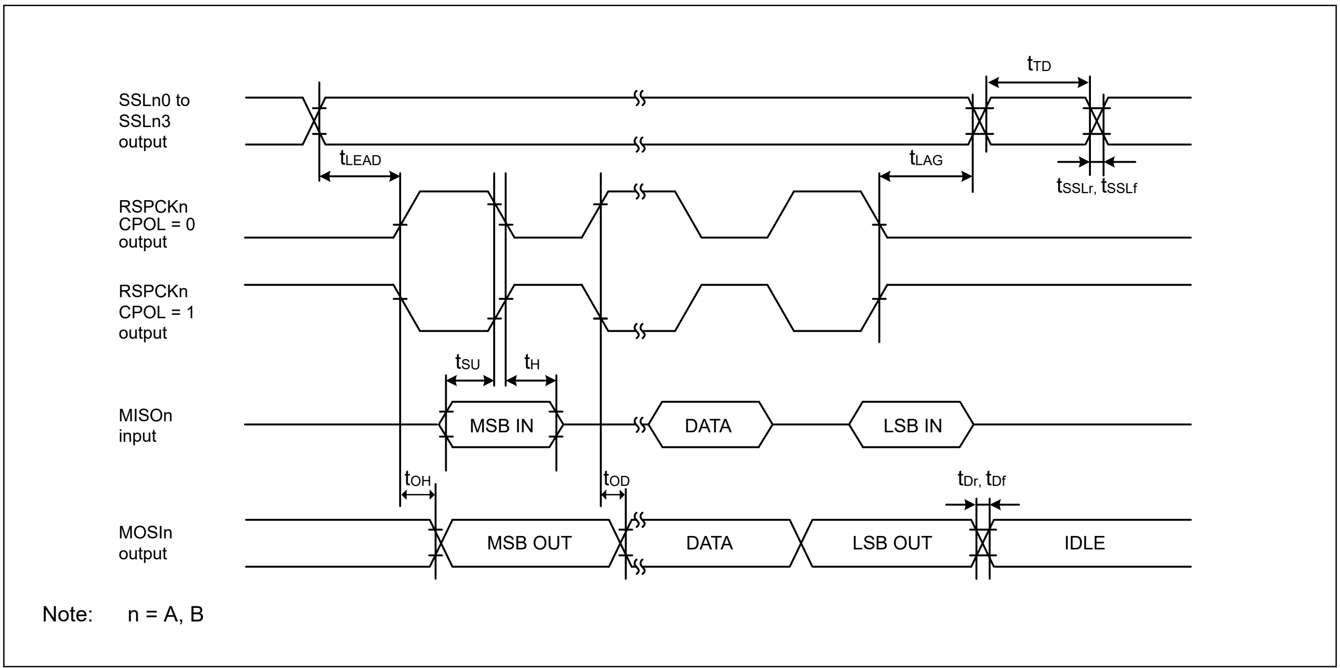


Figure 2.32 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to a value other than 1/2)

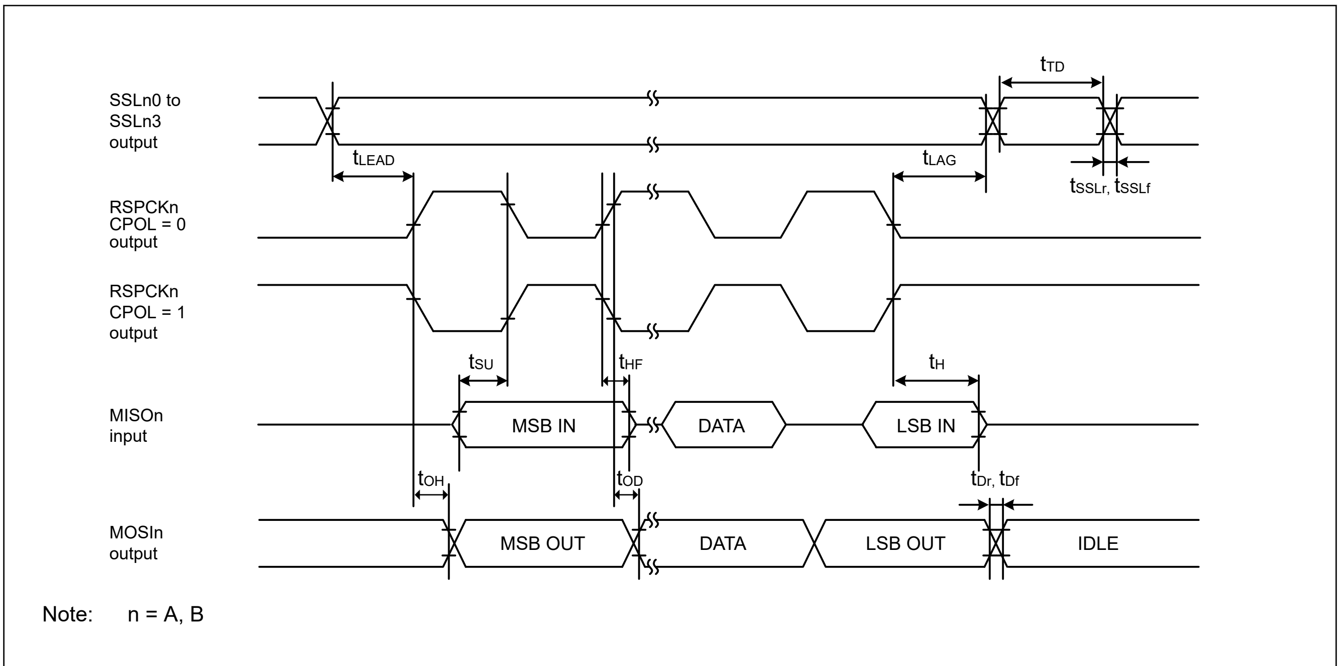
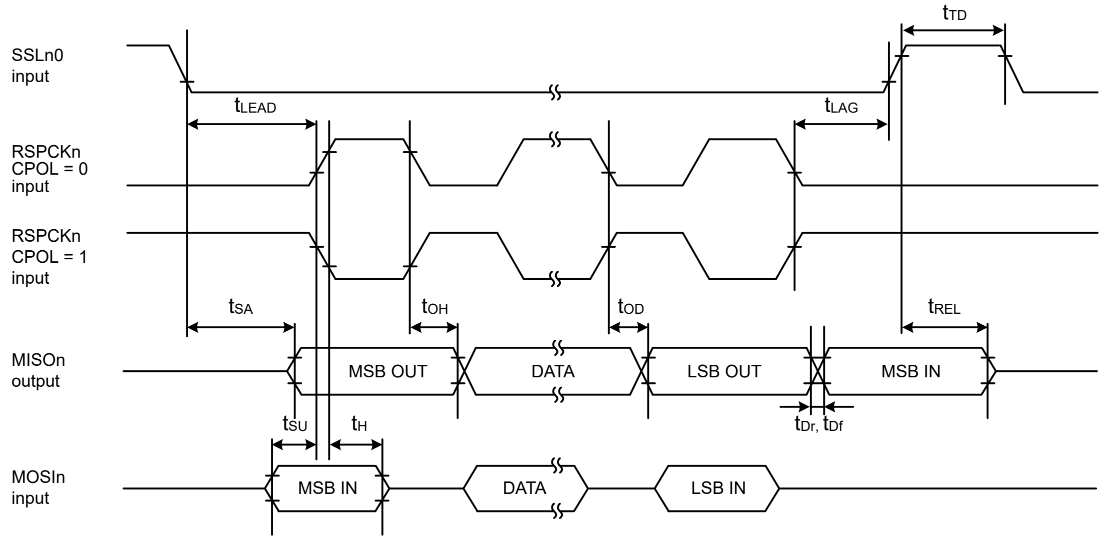
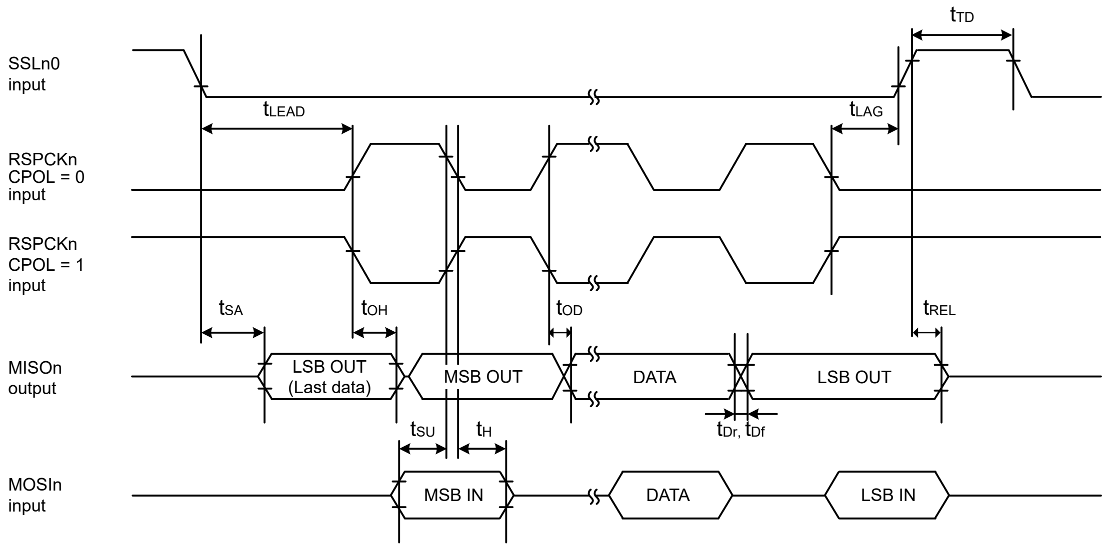


Figure 2.33 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to 1/2)



Note: n = A, B

Figure 2.34 SPI timing (slave, CPHA = 0)



Note: n = A, B

Figure 2.35 SPI timing (slave, CPHA = 1)

2.3.11 QSPI Timing

Table 2.28 QSPI timing

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

Item	Symbol	Min.	Max.	Unit*1	Measurement conditions
QSPCLK clock cycle (PCLKA > 48 MHz)	t_{QScyc}	3	4080	t_{Pcyc}	Figure 2.36
QSPCLK clock cycle (PCLKA ≤ 48 MHz)		2	4080		
QSPCLK clock high-level pulse width	t_{QSWH}	t_{Qscyc} × 0.4	—	ns	
QSPCLK clock low-level pulse width	t_{QSWL}	t_{Qscyc} × 0.4	—	ns	
Data input setup time	t_{SU}	25	—	ns	Figure 2.37 IOVCCn ≥ 2.7V
Data input hold time	t_H	12	—	ns	
QSSL setup time	t_{LEAD}	(L + 0.5) × t_{QScyc} - M*2	—	ns	
QSSL hold time	t_{LAG}	(N + 0.5) × t_{QScyc} - M*3	—	ns	
Data output delay	t_{OD}	-3.3	14	ns	
Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc} indicates the clock cycle of PCLKA.
Note 2. The value of L is the value set in the SFMSSC.SFMSLD bit. The value of M is 10 at the time of BOOST, and 15 at the time of NORMAL.
Note 3. The value of N is the value set in the SFMSSC.SFMSHD bit. The value of M is 10 at the time of BOOST, and 15 at the time of NORMAL.

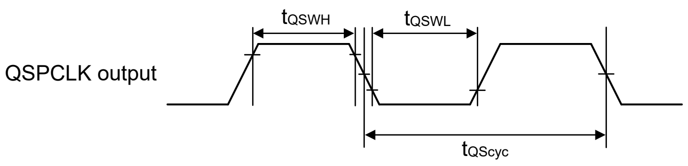


Figure 2.36 QSPI clock timing

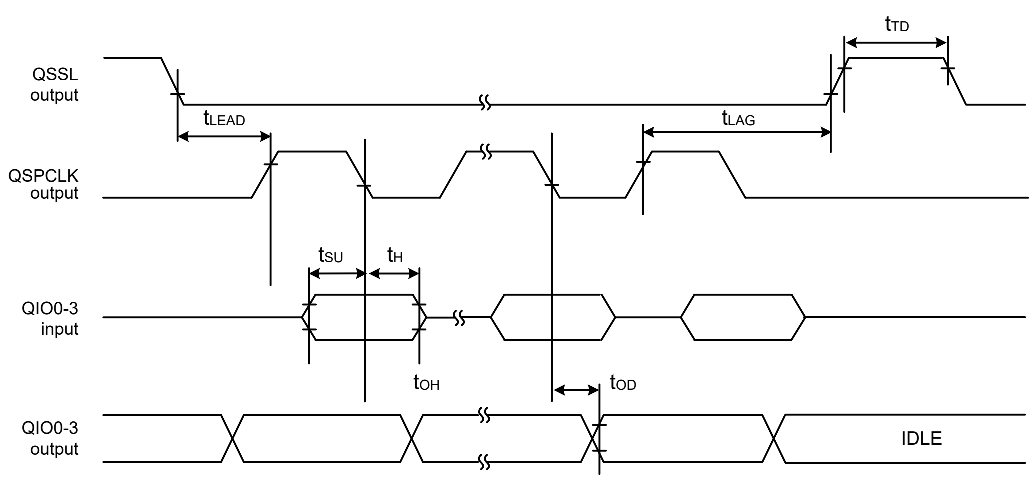


Figure 2.37 QSPI input/output timing

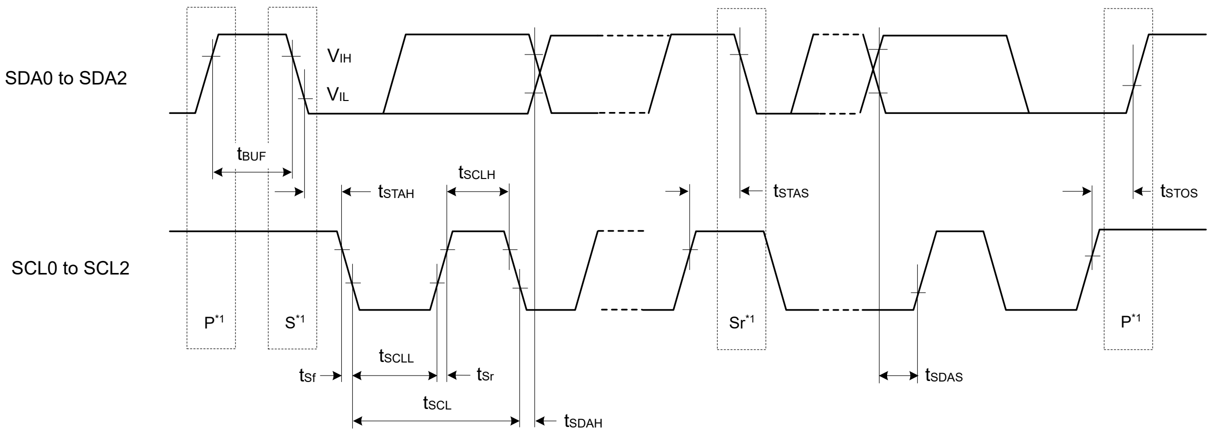
2.3.12 IIC Timing

Table 2.29 IIC timing

Condition: VCC = 3.0 to 3.6 V, V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3, V_{OH} = 0.6 V, I_{OL} = 6 mA
Condition: Normal drive output is selected in the drive capability control bits in PmnPFS register. (PmnPFS.DSCR[1:0] = 10b)

Item		Symbol	Min.*1	Max.*1	Unit	Measurement conditions
IIC (Standard mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.38
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low-level pulse width	t_{SCLL}		—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated start condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	Figure 2.38
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low-level pulse width	t_{SCLL}		—	ns	
	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated start condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc} indicates a clock cycle of IIC internal reference clock (IICφ).
Note 1. If the digital filter is enabled by setting the ICFER.NFE bit to 1, when ICMR3.NF[1:0] bits are set to 11b, values in parentheses apply.
Note 2. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.38 I2C bus interface input/output timing

2.3.13 MLCD Timing

Table 2.30 MLCD timing

Condition: High drive output is selected in the drive capability control bits in PmnPFS register.

Item	Symbol	Min.	Typ.	Max.	Unit*1	Measurement conditions
MLCD_SCLK pin output high-level pulse width	t_{wSCLKH}	1	—	255	t_{Pcyc}	Figure 2.39
MLCD_SCLK pin output low-level pulse width	t_{wSCLKL}	1		255	t_{Pcyc}	
Data transmission wait time	t_{wNOP}	—	1	—	t_{Pcyc}	
MLCD_SI pin output setup time	t_{sSI}	1	—	255	t_{Pcyc}	
MLCD_SI pin output hold time	t_{hSI}	1	—	255	t_{Pcyc}	
MLCD_DEN pin output setup time	t_{sDEN}	1	—	255	t_{Pcyc}	
MLCD_DEN pin output hold time	t_{hDEN}	1	—	255	t_{Pcyc}	
MLCD_ENBG/S pin output high-level pulse width	t_{wENBH}	2	—	1023	t_{Pcyc}	
The time between the rise of MLCD_SCLK pin output and the rise of MLCD_ENBG/S pin output.	t_{oENB}	3	—	255	t_{Pcyc}	
The time between the fall of MLCD_ENBG/S pin output and the rise of MLCD_SCLK pin output.	t_{bENB}	3	—	255	t_{Pcyc}	
Duty ratio of MLCD_VCOM pin output	—	—	50	—	%	
MLCD_VCOM pin output high-level/low-level pulse time	t_{cVCOM}	500	—	5000	ms	

Note 1. t_{Pcyc} indicates the clock cycle of PCLKA.

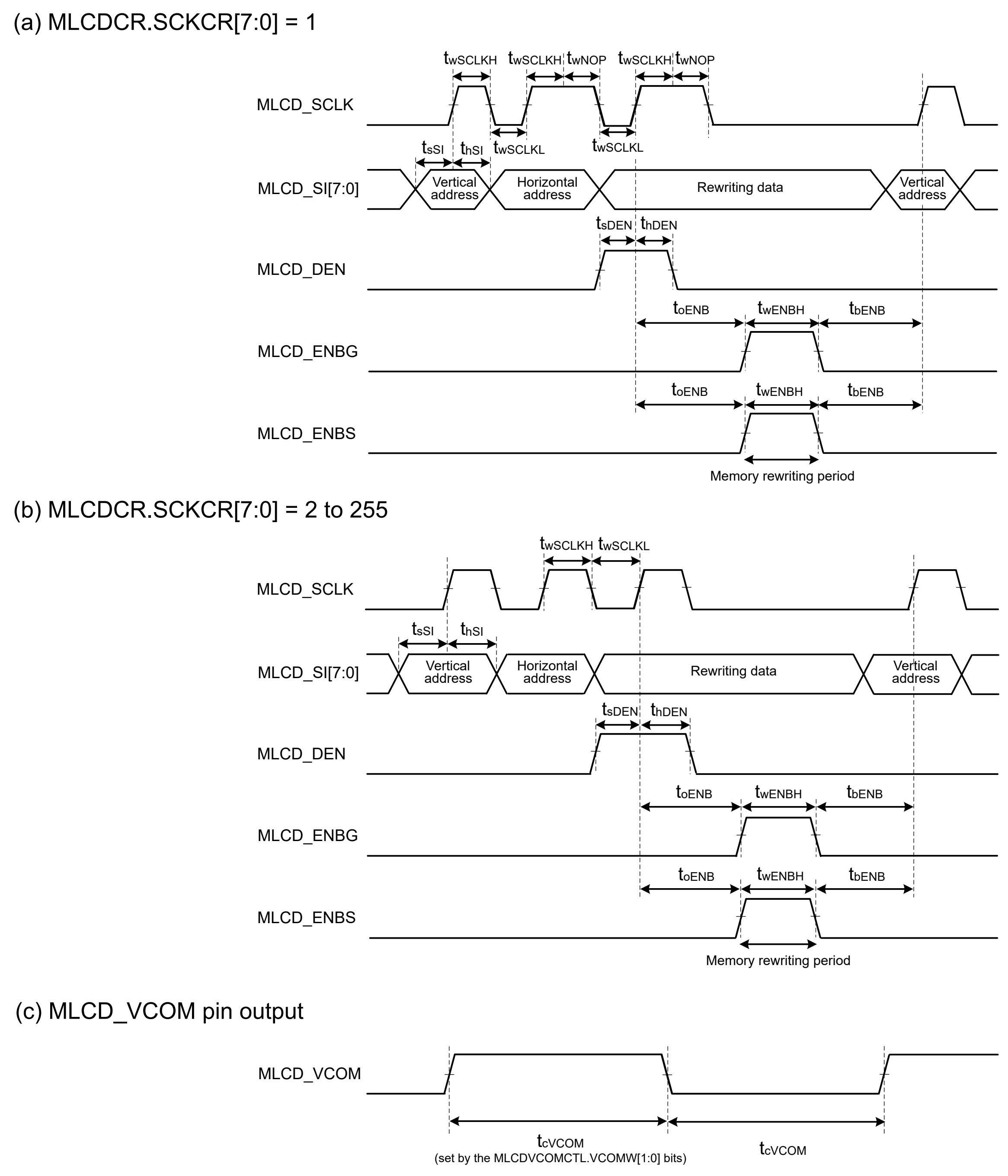


Figure 2.39 MLCD output timing

2.3.14 CLKOUT Timing

Table 2.31 CLKOUT timing

Item			Symbol	Min.	Max.	Unit	Measurement conditions
CLKOUT	CLKOUT pin output cycle[*1]	IOVCCn ≥ 2.7V	t_{Ccyc}	31.25	—	ns	Figure 2.40
		IOVCCn < 2.7V		62.5	—		
CLKOUT32	CLKOUT pin output cycle		t_{Ccyc}	30.5	—	μs	

Note 1. When the EXTAL external clock input or an sub-clock oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

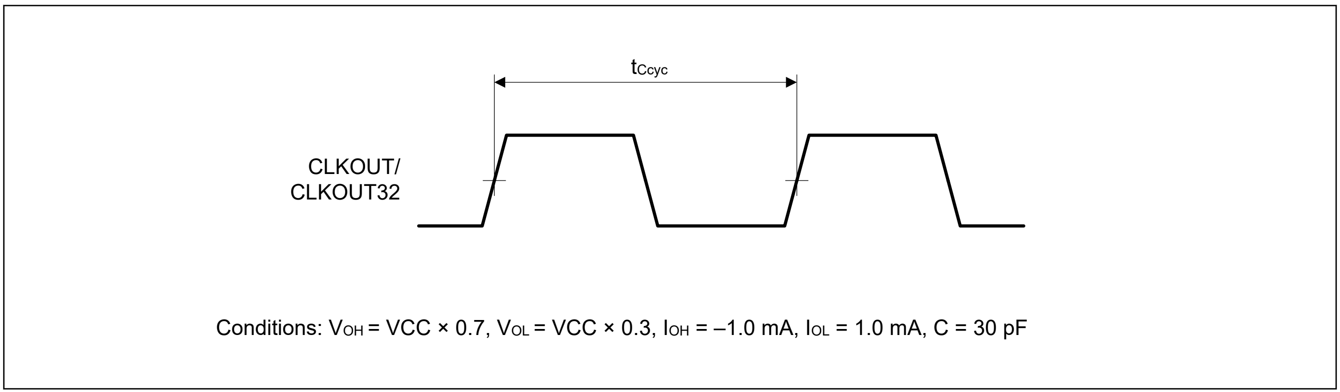


Figure 2.40 CLKOUT/CLKOUT32 pin output timing

2.3.15 TMR Timing

Table 2.32 TMR timing

Item			Symbol	Min.	Typ.	Max.	Unit[*1]	Measurement conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	—	t_{Pcyc}	Figure 2.41
		Both-edge setting		2.5	—	—		

Note 1. t_{Pcyc} indicates the clock cycle of PCLKB.

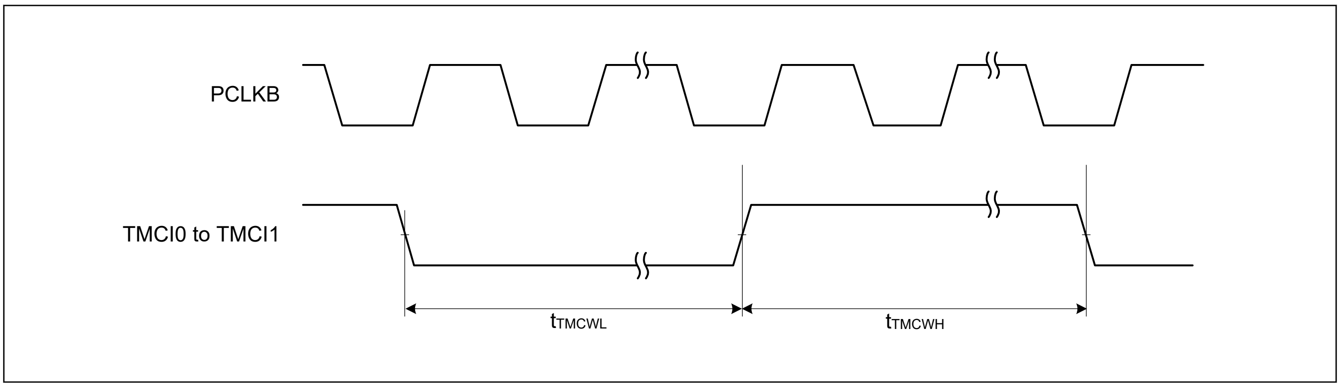


Figure 2.41 TMR clock input timing

2.4 A/D Conversion Characteristics

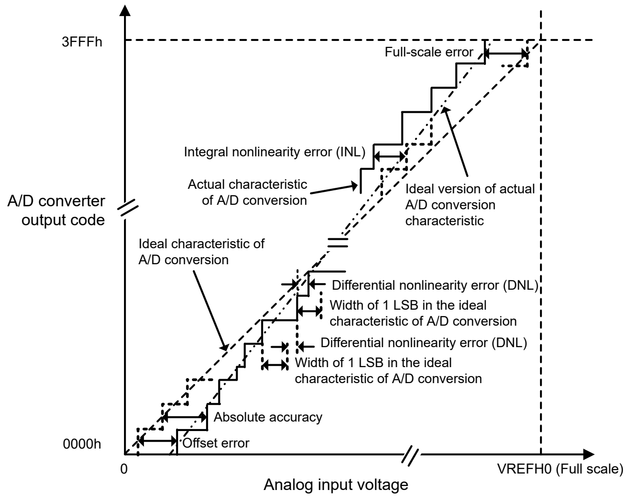


Figure 2.42 Illustration of A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output codes of the ideal A/D conversion characteristics and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. In the case of 14-bit resolution and reference voltage of VREFH0 = 3.276 V, for example, because 1-LSB width is 0.2 mV, voltages such as 0 mV, 0.2 mV, and 0.4 mV are used as the analog input voltage.

If the analog input voltage is 1.6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result ranges from 0x0003 to 0x000D though an output code of 0x0008 can be expected from the ideal A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width of the ideal A/D conversion characteristics and the width of the output code actually output.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

The conversion characteristics of A/D converter is not tested at the shipment unless otherwise specified. The values described are presented only as the design guidelines. The electrical characteristics presented are classified into the following six categories in accordance with the conditions such as voltages.

1. AVCC0 = VREFH0 = 2.7 to 3.6 V However, ±3σ of the voltage in the normal distribution is within the range of maximum value.
2. AVCC0 = VREFH0 = 2.7 to 3.6 V
3. AVCC0 = VREFH0 = 1.62 to 3.6 V, 14-bit resolution
4. AVCC0 = VREFH0 = 1.62 to 3.6 V, 12-bit resolution
5. AVCC0 = 3.3 V, AVTRO = 2.5 V (The output value of the reference voltage generator circuit is used as the reference.)

6. AVCC0 = 1.8 V, AVTRO = 1.25 V (The output value of the reference voltage generator circuit is used as the reference.)

Some points to note regarding the electrical characteristics of the A/D converter are listed below:

- The characteristics do not contain the quantization errors (±0.5 LSB).
- The characteristics are the values after the offset calibrations.
- The characteristics only apply when the 14-bit A/D converter pins are in use for A/D conversion, and not for any other functions.
- The conversion time (t_{CONV}) is the sum of the sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The values in parentheses in the conversion time indicate the sampling time.

Table 2.33 A/D conversion characteristics (1)

Condition: AVCC0 = VREFH0 = 2.7 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Frequency		1	—	32*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	1.0 (0.46875)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x0F
		1.5 (0.96875)	—	—	μs	Normal-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x1F
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST = 0x02
Offset error*1		-0.8	—	0.8	mV	High-precision channel
Full-scale error*1		-0.8	—	0.8		High-precision channel
Absolute accuracy*1		—	±4.0*2	±7.0	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.5	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5*2	±4.0	LSB	High-precision channel
ENOB (Effective number of bits) *1*2*4		—	13	—	bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 0x85), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).
Note 2. The value applies when AVCC0 = VREFH0 = 3.3 V.
Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 2.7V applies.
Note 4. The value applies when the main oscillator is selected as PCLKB and a 50-Hz sine wave is input to the analog input pin.

Table 2.34 A/D conversion characteristics (2) (1 of 2)

Condition: AVCC0 = VREFH0 = 2.7 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Frequency		1	—	32*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	bit	—

Table 2.34 A/D conversion characteristics (2) (2 of 2)

Condition: AVCC0 = VREFH0 = 2.7 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	1.0 (0.46875)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x0F
		1.5 (0.96875)	—	—	μs	Normal-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x1F
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST = 0x02
Offset error[*1]		-1.2	—	1.2	mV	High-precision channel
Full-scale error[*1]		-1.2	—	1.2		High-precision channel
Absolute accuracy[*1]		—	±4.0[*2]	±9.0	LSB	High-precision channel
DNL differential nonlinearity error[*1]		—	±1.0[*2]	±1.7	LSB	High-precision channel
INL integral nonlinearity error[*1]		—	±2.5[*2]	±5.0	LSB	High-precision channel
ENOB (Effective number of bits) [*1*2*4]		—	13	—	bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 0x85), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).
Note 2. The value applies when AVCC0 = VREFH0 = 3.3 V.
Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 2.7V applies.
Note 4. The value applies when the main oscillator is selected as PCLKB and a 50-Hz sine wave is input to the analog input pin.

Table 2.35 A/D conversion characteristics (3)

Condition: AVCC0 = VREFH0 = 1.62 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Frequency		1	—	16[*3]	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.9375)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x0F
		3.0 (1.9375)	—	—	μs	Normal-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x1F
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST = 0x02
Offset error[*1]		-1.2	—	1.2	mV	High-precision channel
Full-scale error[*1]		-1.2	—	1.2		High-precision channel
Absolute accuracy[*1]		—	±4.0[*2]	±1.2[*5]	LSB	High-precision channel
DNL differential nonlinearity error[*1]		—	±1.0[*2]	±2.5[*6]	LSB	High-precision channel
INL integral nonlinearity error[*1]		—	±2.5[*2]	±5.0	LSB	High-precision channel
ENOB (Effective number of bits) [*1*2*4]		—	13	—	bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 0x85), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).
Note 2. The value applies when AVCC0 = VREFH0 = 3.3 V.
Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 2.4 V applies.
Note 4. The value applies when the main oscillator is selected as PCLKB and a 50-Hz sine wave is input to the analog input pin.
Note 5. When AVCC0 = VREFH0 = 2.4 to 3.6 V, the maximum value is ±9.0 LSB.
Note 6. When AVCC0 = VREFH0 = 2.4 to 3.6 V, the maximum value is ±1.7 LSB.

Table 2.36 A/D conversion characteristics (4)

Condition: AVCC0 = VREFH0 = 1.62 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Frequency		1	—	16[*2]	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		—	—	12	bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.9375)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x0F
		3.0 (1.9375)	—	—	μs	Normal-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x1F
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST = 0x02
Offset error[*1]		-1.2	—	1.2	mV	High-precision channel
Full-scale error[*1]		-1.2	—	1.2		High-precision channel
Absolute accuracy[*1]		—	±2.0	±5.0	LSB	High-precision channel
DNL differential nonlinearity error[*1]		—	±1.0	±1.5	LSB	High-precision channel
INL integral nonlinearity error[*1]		—	±1.0	±2.0	LSB	High-precision channel

Note 1. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 0x00)
Note 2. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 1.62 V applies.

Table 2.37 A/D conversion characteristics when the output value of the reference voltage generator circuit is used as the reference voltage (1)

Condition: AVCC0 = 3.3 V, AVTRO = 2.50 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Frequency		1	—	16	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.46875)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x0F
		3.0 (1.9375)	—	—	μs	Normal-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x1F
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST = 0x02
Offset error[*1]		-1.2	—	1.2	mV	High-precision channel
DNL differential nonlinearity error[*1]		—	±1.5	—	LSB	High-precision channel
INL integral nonlinearity error[*1]		—	±3.0	—	LSB	High-precision channel

Note 1. The value in which 16 times conversion with enabling the averaging mode (ADADC = 0x85) is selected, and in which the conversion precision is set to 14-bit (ADCER.ADPRC[1:0] = 11b)

Table 2.38 A/D conversion characteristics when the output value of the reference voltage generator circuit is used as the reference voltage (2)

Condition: AVCC0 = 1.8 V, AVTRO = 1.25 V

Item		Min.	Typ.	Max.	Unit	Measurement conditions
Frequency		1	—	16	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		—	—	12	bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.46875)	—	—	μs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x0F
		3.0 (1.9375)	—	—	μs	Normal-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST = 0x1F
		593.75 (60.98)	—	—	μs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST = 0x02
Offset error*1		-1.2	—	1.2	mV	High-precision channel
DNL differential nonlinearity error*1		—	±1.0	—	LSB	High-precision channel
INL integral nonlinearity error*1		—	±1.0	—	LSB	High-precision channel

Note 1. The value in which the averaging mode is disabled and in which the conversion precision is set to 12-bit (ADCER.ADPRC[1:0] = 00b)

2.5 Temperature Sensor Characteristics

Table 2.39 Temperature sensor characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Relative accuracy	—	—	±5	—	°C	AVCC0 ≥ 2.6 V
	—	—	±6	—	°C	AVCC0 < 2.6 V
Temperature gradient	—	—	1.6	—	mV/°C	—
Temperature sensor start time	t_{TSTBL}	—	30	120	μs	—
Sampling time	—	—	2	7	μs	—

Note: Temperature sensor characteristics are a reference value because the shipment test is not performed.

2.6 VREF Characteristics

Table 2.40 VREF characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Output voltage	AVTRO	1.17	1.25	1.33	V	VREF.AVCR.AVSEL = 0 AVCC0 ≥ 2.8V
	AVTRO	2.34	2.50	2.66	V	VREF.AVCR.AVSEL = 1 AVCC0 ≥ 2.8V
	AVTRO	1.17	1.25	1.33	V	VREF.AVCR.AVSEL = 0 AVCC0 < 2.8V
Circuit startup stabilization wait time	t_{VRSTUP}	—	—	50	ms	—

Note: VREF characteristics are a reference value because the shipment test is not performed.

2.7 Oscillation Stop Detection Circuit Characteristics

Table 2.41 Oscillation stop detection circuit characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Detection time	t_{dr}	—	—	30	μs	Figure 2.43

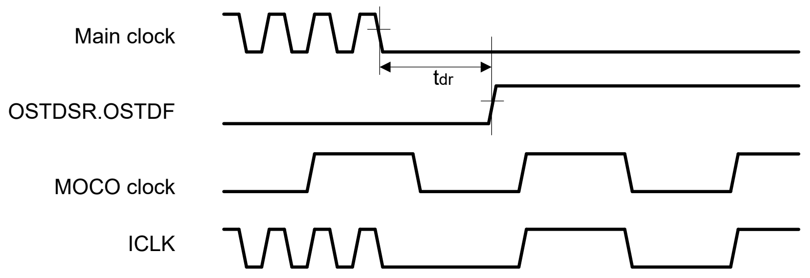


Figure 2.43 Oscillation stop detection timing

2.8 Power-on Reset Circuit and Low-voltage Detection Circuit Characteristics

Table 2.42 Power-on reset circuit and low-voltage detection circuit characteristics (1 of 2)

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Voltage detection level	Power-on reset circuit (POR)	Rise	V_{POR}	1.40	1.50	1.60	V	Figure 2.44
		Fall	V_{PORL}	1.30	1.40	1.50		
	Voltage monitoring 0 circuit (LVD0)		V_{det0_0}	2.34	2.42	2.50	V	Figure 2.45
			V_{det0_1}	2.10	2.17	2.24		
			V_{det0_2}	1.86	1.92	1.98		
			V_{det0_3}	1.62	1.67	1.72		
	Voltage monitoring 1 circuit (LVD1)		V_{det1_0}	2.74	2.83	2.92	V	Figure 2.46
			V_{det1_1}	2.58	2.66	2.74		
			V_{det1_3}	2.42	2.50	2.58		
			V_{det1_5}	2.26	2.33	2.40		
			V_{det1_7}	2.10	2.17	2.24		
			V_{det1_9}	1.94	2.00	2.06		
			V_{det1_B}	1.78	1.84	1.90		
			V_{det1_D}	1.62	1.67	1.72		
	Voltage monitoring BAT circuit (LVDBAT)		V_{detBAT_5}	2.26	2.33	2.40	V	Figure 2.47
			V_{detBAT_7}	2.10	2.17	2.24		
			V_{detBAT_9}	1.94	2.00	2.06		
			V_{detBAT_B}	1.78	1.84	1.90		
			V_{detBAT_D}	1.62	1.67	1.72		

Table 2.42 Power-on reset circuit and low-voltage detection circuit characteristics (2 of 2)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Internal reset time	Power-on reset time*8 (in the normal startup mode)	t_{PORNML}	—	—	44	ms	—
	LVD0 reset time	t_{LVD0}	—	2.5	—	ms	Figure 2.45
	LVD1 reset time	t_{LVD1}	—	0.8	—	ms	Figure 2.46
	LVDBAT reset time	t_{LVDBAT}	—	0.8	—	ms	Figure 2.47
Minimum VCC down time*1		$t_{VOFFPOR}$	4	—	—	ms	Figure 2.44
POR response delay time		t_{detpor}	—	—	500	µs	Figure 2.44
LVD0 response delay time		t_{det}	—	150	300	µs	Figure 2.45 to Figure 2.47
LVD0 response delay time			—	150	300	µs	
LVDBAT response delay time (VCC = VBAT_EHC, on connection)			—	150	300	µs	
LVDBAT response delay time (VCC ≠ VBAT_EHC, on independence)			—	400	800	µs	
LVD1 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	400	µs	Figure 2.46, Figure 2.47
LVDBAT operation stabilization time (VCC = VBAT_EHC, on connection)			—		400	µs	
LVDBAT operation stabilization time (VCC ≠ VBAT_EHC, on independence)			—		1000	µs	
Hysteresis width (LVD1)		V_{LVH}*2	—	60	—	mV	
		V_{LVH}*3	—	55	—		
		V_{LVH}*4	—	50	—		
		V_{LVH}*5	—	45	—		
		V_{LVH}*6	—	40	—		
		V_{LVH}*7	—	35	—		

Note 1. The minimum VCC down time indicates the time when VCC is below the lowest value among voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{detBAT} for POR and LVD.
Note 2. When V_{det1_0} is selected.
Note 3. When V_{det1_1} and V_{det1_3} are selected.
Note 4. When V_{det1_5} is selected.
Note 5. When V_{det1_7} is selected.
Note 6. When V_{det1_9} and V_{det1_B} are selected.
Note 7. When V_{det1_D} is selected.
Note 8. These values are based on simulation. They are not production tested.

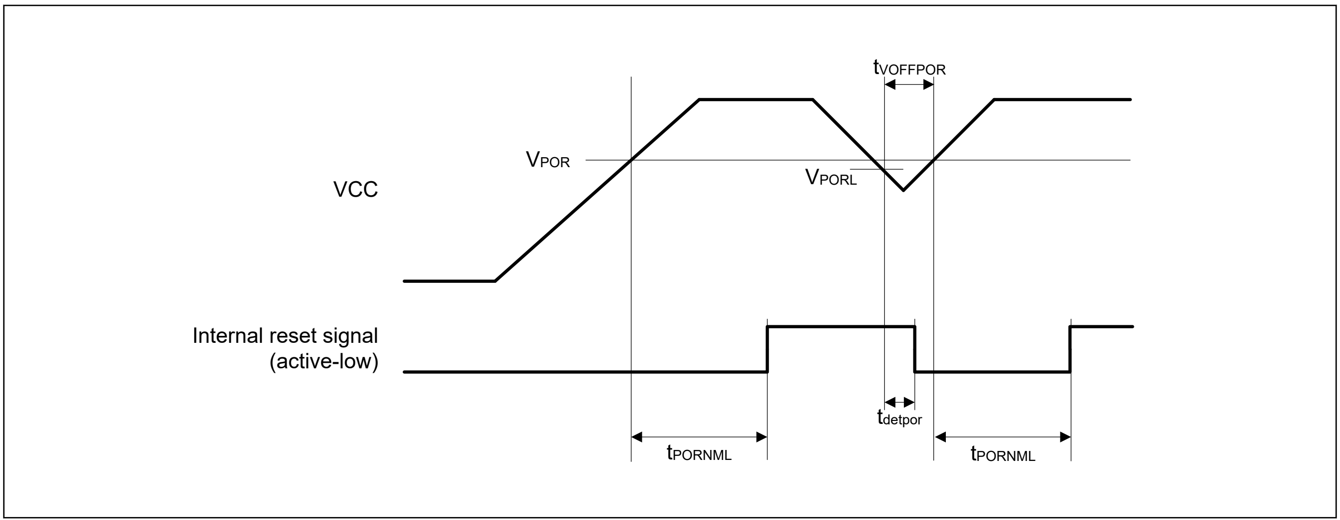


Figure 2.44 Power-on reset timing

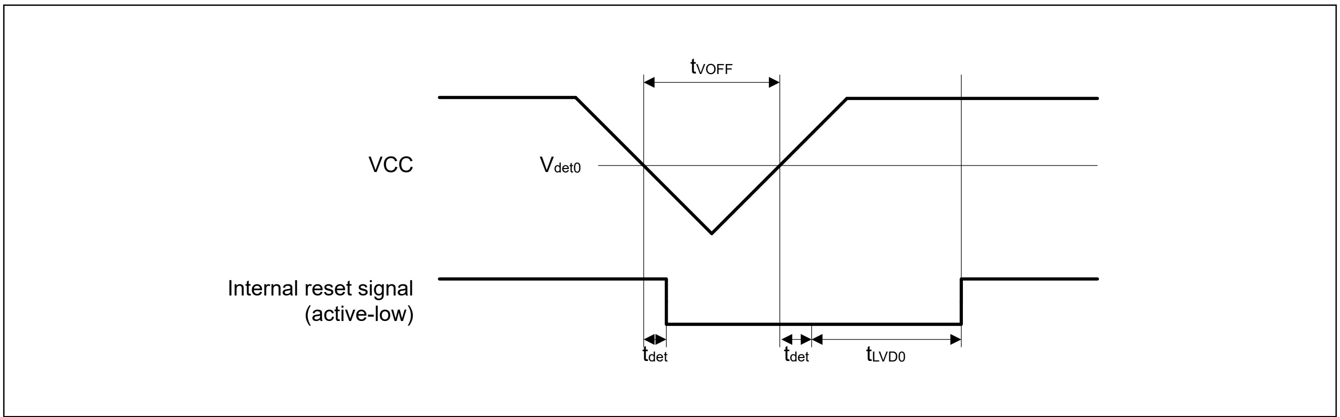


Figure 2.45 Voltage monitoring 0 circuit detection voltage timing (V_{det0})

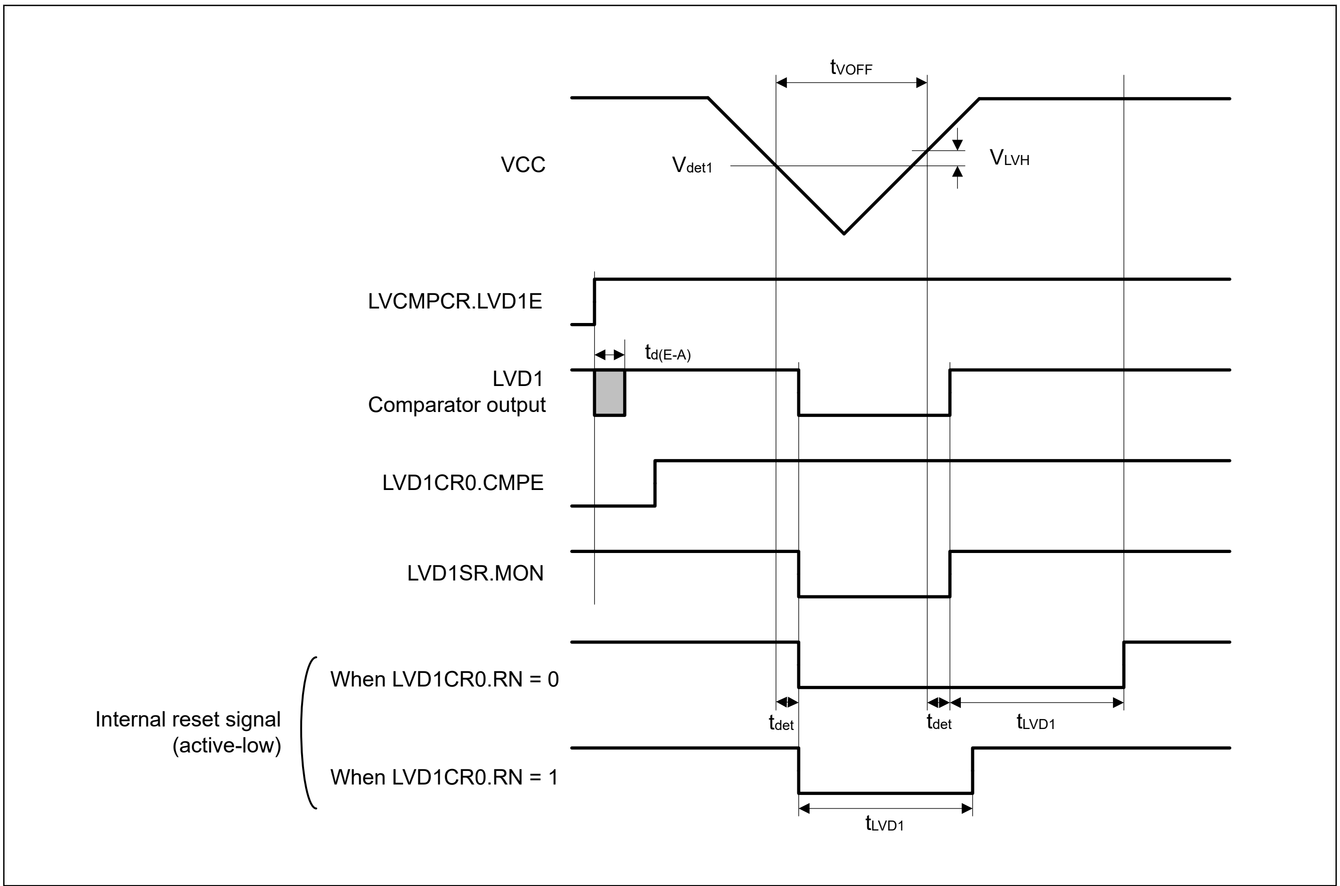


Figure 2.46 Voltage monitoring 1 circuit detection voltage timing (V_{det1})

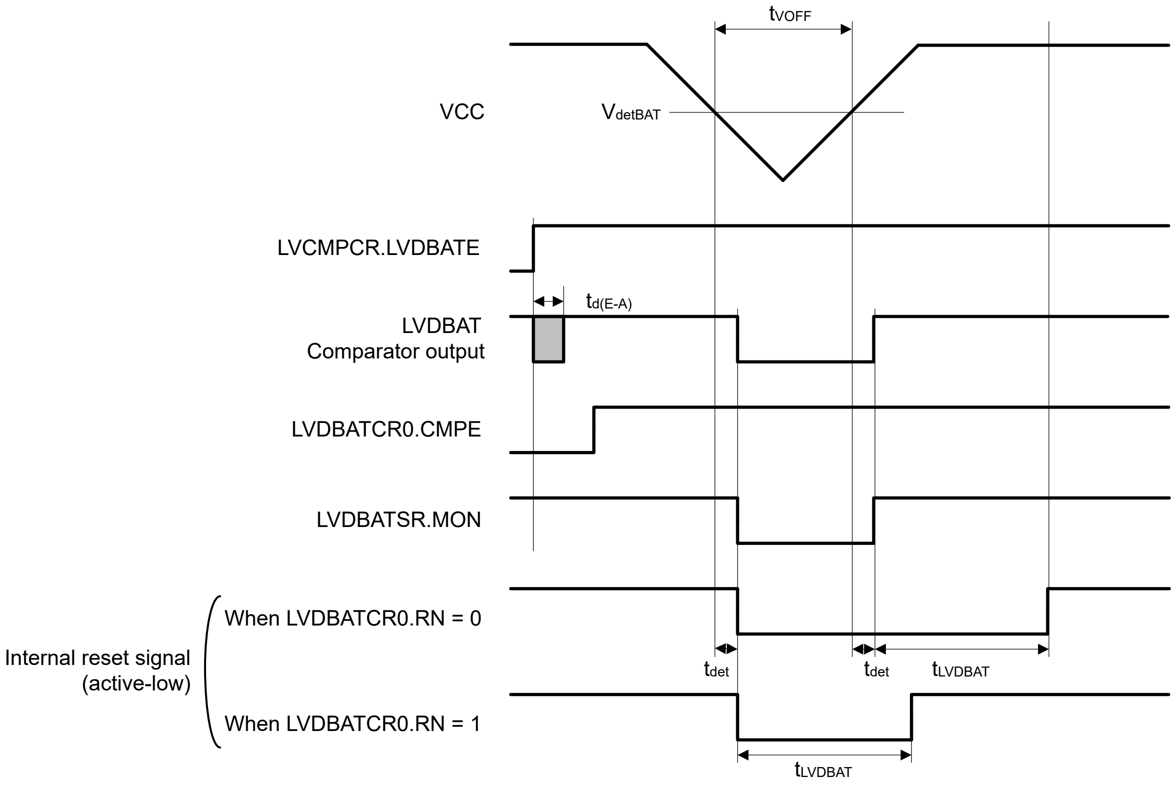


Figure 2.47 Voltage monitoring BAT circuit detection voltage timing (V_{detBAT})

2.9 EHC Characteristics

Table 2.43 EHC characteristics (1 of 2)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Current during reset	I_{CC}	—	0.02	—	μA	Ta = 25°C VCC = VSC_VCC = 0 V, VCC_SU = VBAT_EHC = 2.5 V
Capacitance value of capacitor for electricity accumulation at VCC_SU side[*2]	C_{VCCSU}	—	100	—	μF	EHMD = 1 Ta = –40 to 60°C
		—	47	—		EHMD = 0 Ta = –40 to 50°C
		—	150	—		EHMD = 1 Ta = –40 to 85°C
Capacitance value of smoothing capacitor at VCC side	C_{VCC}	—	10	—	μF	Ta = –40 to 85°C
Current that can flow from VSC_VCC to the inside of MCU	I_{SC}	—	—	10	mA	VSC_VCC ≤ 3.6 V
Current that can flow from VBAT_EHC to IOVCCn[*1]	I_{VBAT}	—	—	30	mA	—
Current that can flow from VCC/ IOVCC to IOVCCn[*1]	I_{VCC}	—	—	30	mA	—
Permissible value of output impedance at VBAT_EHC side	R_{VBAT}	—	—	10	Ω	VSC_VCC ≤ 3.6 V

Table 2.43 EHC characteristics (2 of 2)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Threshold voltage for charging protection of secondary cells at VBAT side	VBAT_CHG	2.340	2.390	2.440	V	I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 2.4 V
		2.438	2.488	2.538		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 2.5 V
		2.535	2.585	2.635		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 2.6 V
		2.633	2.683	2.733		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 2.7 V
		2.730	2.780	2.830		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 2.8 V
		2.827	2.877	2.927		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 2.9 V
		2.924	2.974	3.024		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 3.0 V
		3.020	3.070	3.120		I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC = 3.1 V
Threshold voltage for charging protection of secondary cells at VCC side	VCC_CHG	3.021	3.071	3.121	V	I_{SC} = 3 µA to 10 mA, VSC_VCC = VCC
Threshold voltage for high-speed startup of EHC capacitor charging at H side	VCC_SU_H	—	2.63	—	V	VSC_VCC = VCC and rise of VCC VBAT_EHC = 2.4 to 2.7 V
		—	2.92	—		VSC_VCC = VCC and rise of VCC VBAT_EHC = 2.8 to 3.1 V
Threshold voltage for high-speed startup of EHC capacitor charging at L side	VCC_SU_L	—	2.33	—		VSC_VCC = VCC and drop of VCC VBAT_EHC = 2.4 to 2.7 V
		—	2.61	—		VSC_VCC = VCC and drop of VCC VBAT_EHC = 2.8 to 3.1 V
Startup threshold voltage at the time of starting up the energy harvest mode	VCC_SU_H	—	2.60	—	V	I_{SC} = 3 µA to 10 mA
Power generation status flag	V_{ENOUT}	—	0.42	—	V	VCC_SU = 2.5 V
Minimum startup current required for starting up the energy harvest mode	I_{SC}	—	3	—	µA	Ta = 25 °C, Connect capacitors of 100 µF to VCC_SU and 10 µF to VCC.

Note 1. IOVCCn indicates IOVCC0 and IOVCC1.

Note 2. Figure 2.49 shows the relationship between the upper limit of temperature and the capacitance value of capacitor for electricity accumulation at VCC_SU side.
If the capacitance value is insufficient for the temperature used, the startup current shown in Figure 2.50 is required.

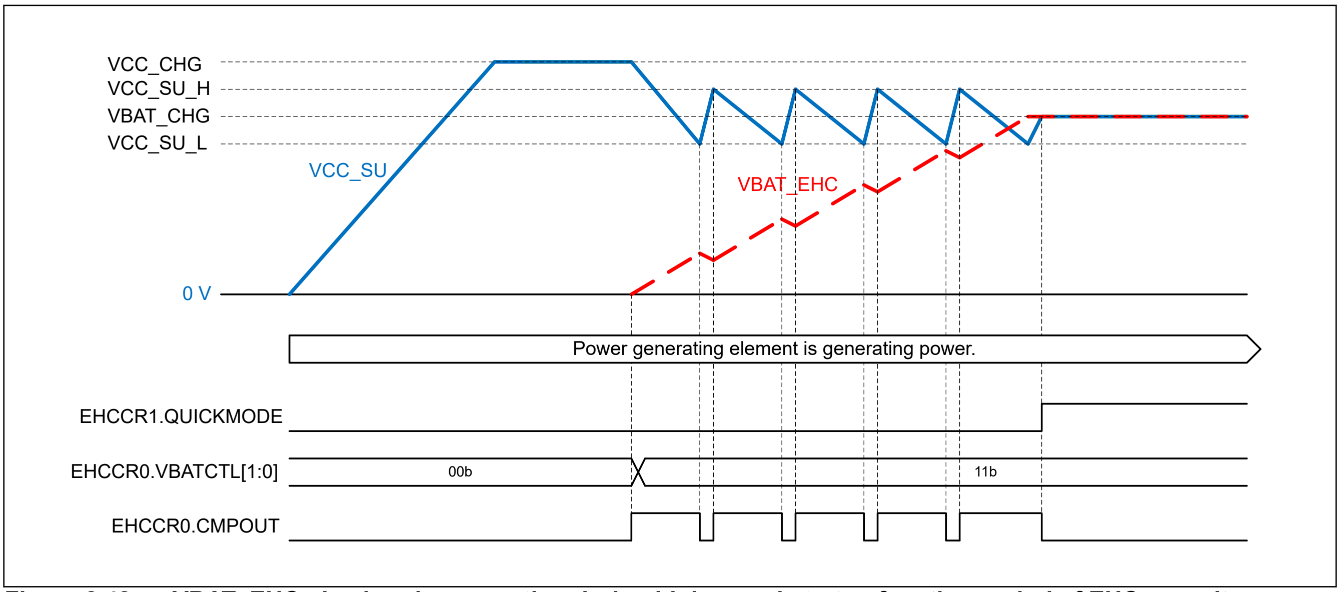


Figure 2.48 VBAT_EHC pin charging operation during high-speed startup function period of EHC capacitor charging

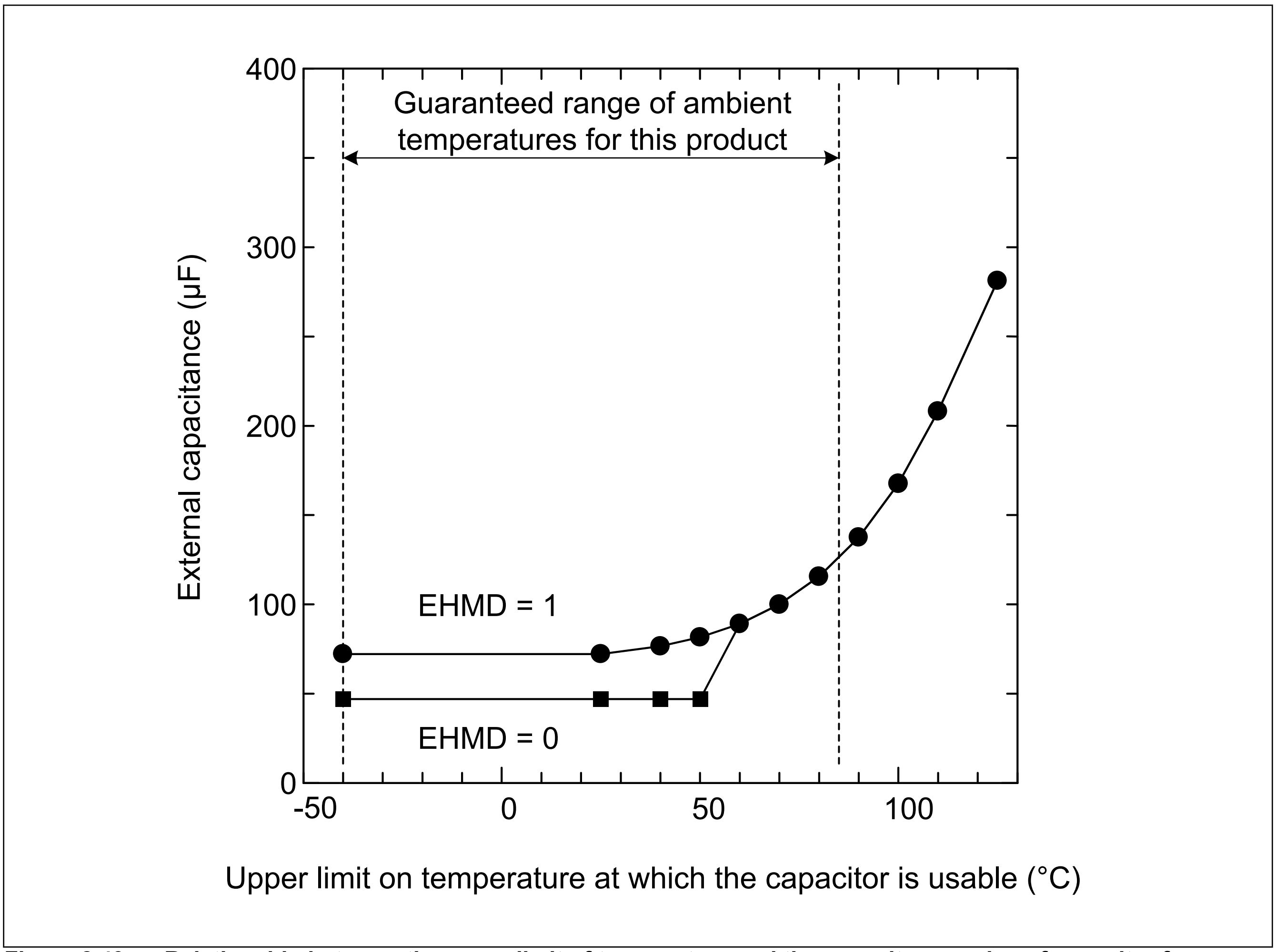


Figure 2.49 Relationship between the upper limit of temperature and the capacitance value of capacitor for electricity accumulation at VCC_SU side

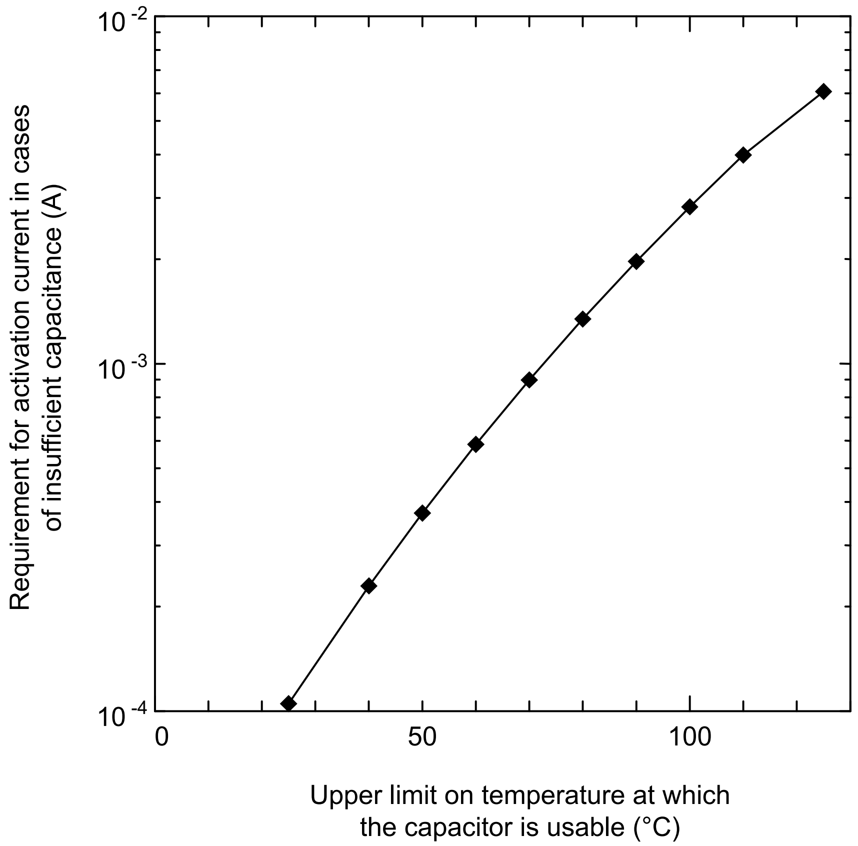


Figure 2.50 Relationship between the upper limit of temperature and the startup current in case that the capacitance is insufficient

2.10 Back Bias Voltage Control (VBBC) Circuit Characteristics

Table 2.44 Initial setup time of VBBC circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
VBBC initial setup time*1	$t_{VBBSTUP}$	—	100*2	400*2 *3	ms	Figure 2.51
Internal voltage discharge time	t_{VBBDIS}	1	—	—	ms	Figure 2.52

Note 1. This is the time period between when 1 is written to VBBCR.VBBEN and when VBBST.VBBSTUP is changed to 1.
Note 2. This is the time when the value of the smoothing capacitor connected between the VBP and VBN pins is 0.56 μF ± 20 %.
Note 3. We do not inspect the characteristics of the back-bias voltage control circuit before shipment. The values presented in this manual are only for reference.

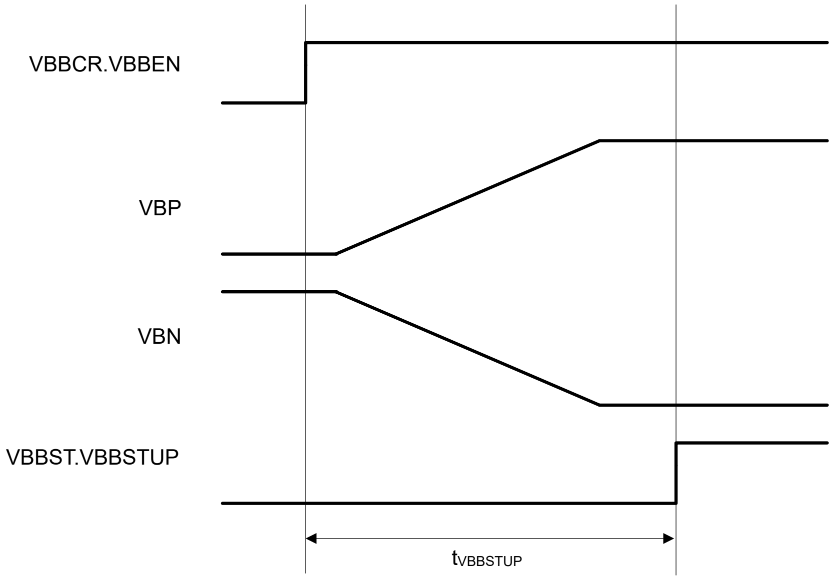


Figure 2.51 VBBC initial setup timing

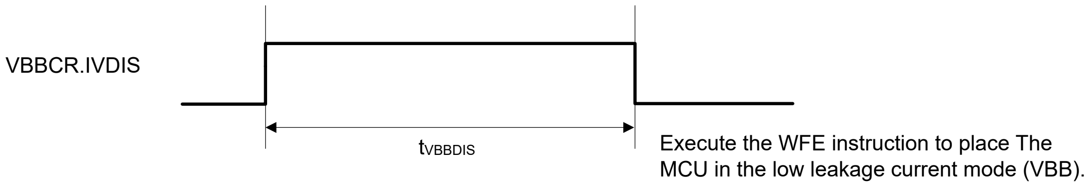


Figure 2.52 Internal voltage discharge time

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.45 Code flash memory characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Reprogramming/erasure cycle*1	N_{PEC}	10000	—	—	Times	JEDEC compliance
Data retention time	t_{DRP}	10	—	—	Year	JEDEC compliance

Note 1. The number of cycles of reprogramming and erasure defines the number of times a block can be erased. When the number of cycles of reprogramming and erasure is n, a block can be erased n times. For instance, if 8 bytes of data are written to the 256 different addresses on 8-byte boundaries within a 2-KB block, erasing the whole block is counted as a single cycle of reprogramming and erasure. Note that programming of the same address is only allowed once; that is, overwriting is prohibited.

Table 2.46 Code flash memory characteristics (2)

Item		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8 bytes	t_{P8}	—	5	6	—	5	6	ms
	256 bytes	t_{P256}	—	5	6	—	5	6	
Erasure time	4 KB	t_{E4K}	—	10	12	—	10	12	
Delay until first suspension during programming		t_{SPD1}	—	—	0.2	—	—	0.1	
Delay after second suspension during programming		t_{SPD2}	—	—	2.4	—	—	2	
Delay until first suspension during erasure		t_{SED1}	—	—	0.2	—	—	0.1	
Delay after second suspension during erasure		t_{SED2}	—	—	2.4	—	—	2	
Forced stop command		t_{FD}	—	—	0.2	—	—	0.1	

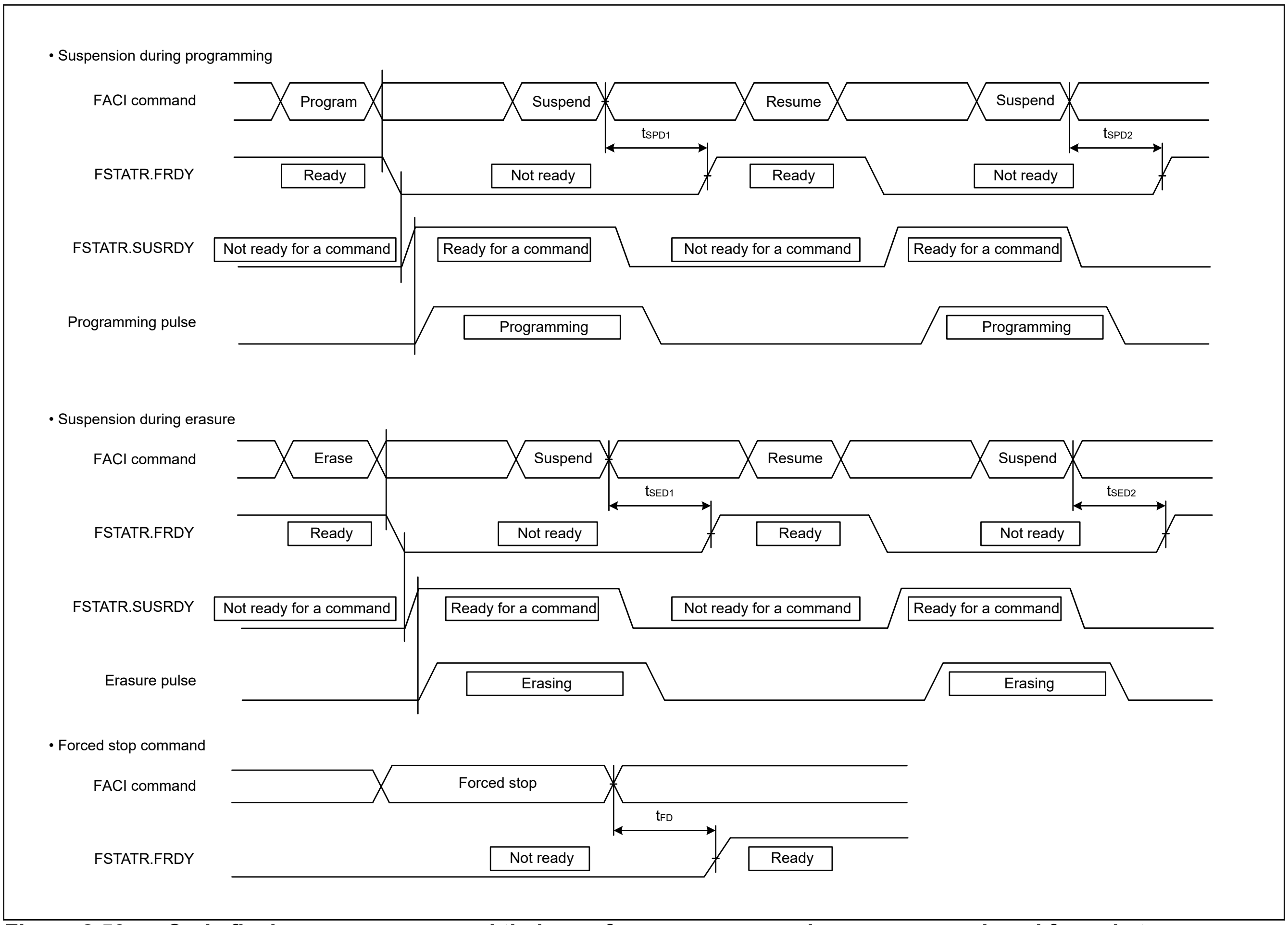


Figure 2.53 Code flash memory command timings of program suspend, erase suspend, and forced stop

2.12 Boundary Scan Characteristics

Table 2.47 Boundary scan characteristics

Condition: High drive output is selected in the drive capability control bits in PmnPFS register. (PmnPFS.DSCR[1:0] = 11b)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 2.54
TCK clock high-level pulse width	t_{TCKH}	43	—	—		
TCK clock low-level pulse width	t_{TCKL}	43	—	—		
TCK rise time	t_{TCKr}	—	—	7		
TCK fall time	t_{TCKf}	—	—	7		
TMS setup time	t_{TMSS}	15	—	—		Figure 2.55
TMS hold time	t_{TMSH}	15	—	—		
TDI setup time	t_{TDIS}	15	—	—		
TDI hold time	t_{TDIH}	15	—	—		
TDO data delay time	t_{TDOD}	—	—	100		

Note: This is normal mode (high-speed mode).

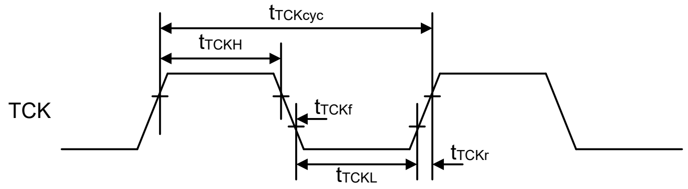


Figure 2.54 Boundary scan TCK timing

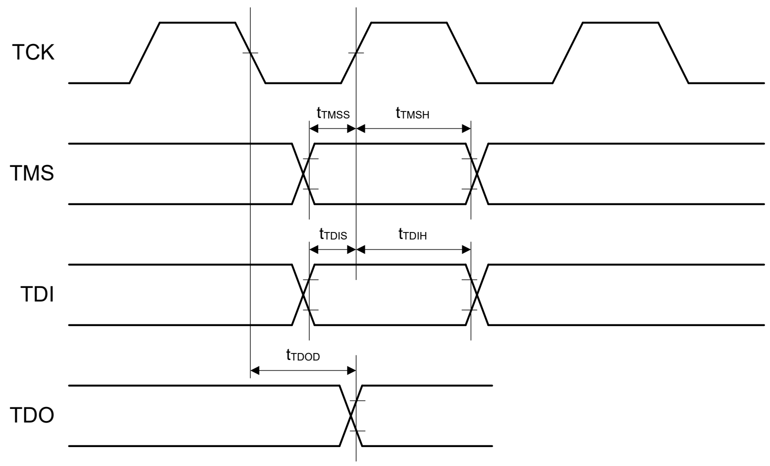


Figure 2.55 Boundary scan input/output timing

2.13 Serial Wire Debug (SWD) Characteristics

Table 2.48 SWD characteristics

Condition: VCC = AVCC0 = 1.62 to 3.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
NORMAL	SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.56
	SWCLK clock high-level pulse width	t_{SWCKH}	$t_{SWCKcyc}$ x 0.5 - t_{SWCKr}	—	—	ns	
	SWCLK clock low-level pulse width	t_{SWCKL}	$t_{SWCKcyc}$ x 0.5 - t_{SWCKf}	—	—	ns	
	SWCLK rise time	t_{SWCKr}	—	—	7	ns	
	SWCLK fall time	t_{SWCKf}		—	7	ns	
	SWDIO setup time	t_{SWDS}	$t_{SWCKcyc}$ x 0.2	—	—	ns	Figure 2.57
	SWDIO hold time	t_{SWDH}	$t_{SWCKcyc}$ x 0.2	—	—	ns	
	SWDIO data delay time	t_{SWDD}	2	—	50	ns	
VBB	SWCLK clock cycle time	$t_{SWCKcyc}$	30000	—	—	ns	Figure 2.56
	SWCLK clock high-level pulse width	t_{SWCKH}	$t_{SWCKcyc}$ x 0.5 - t_{SWCKr}	—	—	ns	
	SWCLK clock low-level pulse width	t_{SWCKL}	$t_{SWCKcyc}$ x 0.5 - t_{SWCKf}	—	—	ns	
	SWCLK rise time	t_{SWCKr}	—	—	7	ns	
	SWCLK fall time	t_{SWCKf}		—	7	ns	
	SWDIO setup time	t_{SWDS}	1000	—	—	ns	Figure 2.57
	SWDIO hold time	t_{SWDH}	1000	—	—	ns	
	SWDIO data delay time	t_{SWDD}	2	—	1000	ns	

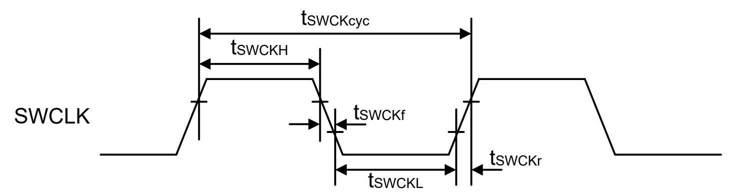


Figure 2.56 SWD SWCLK timing

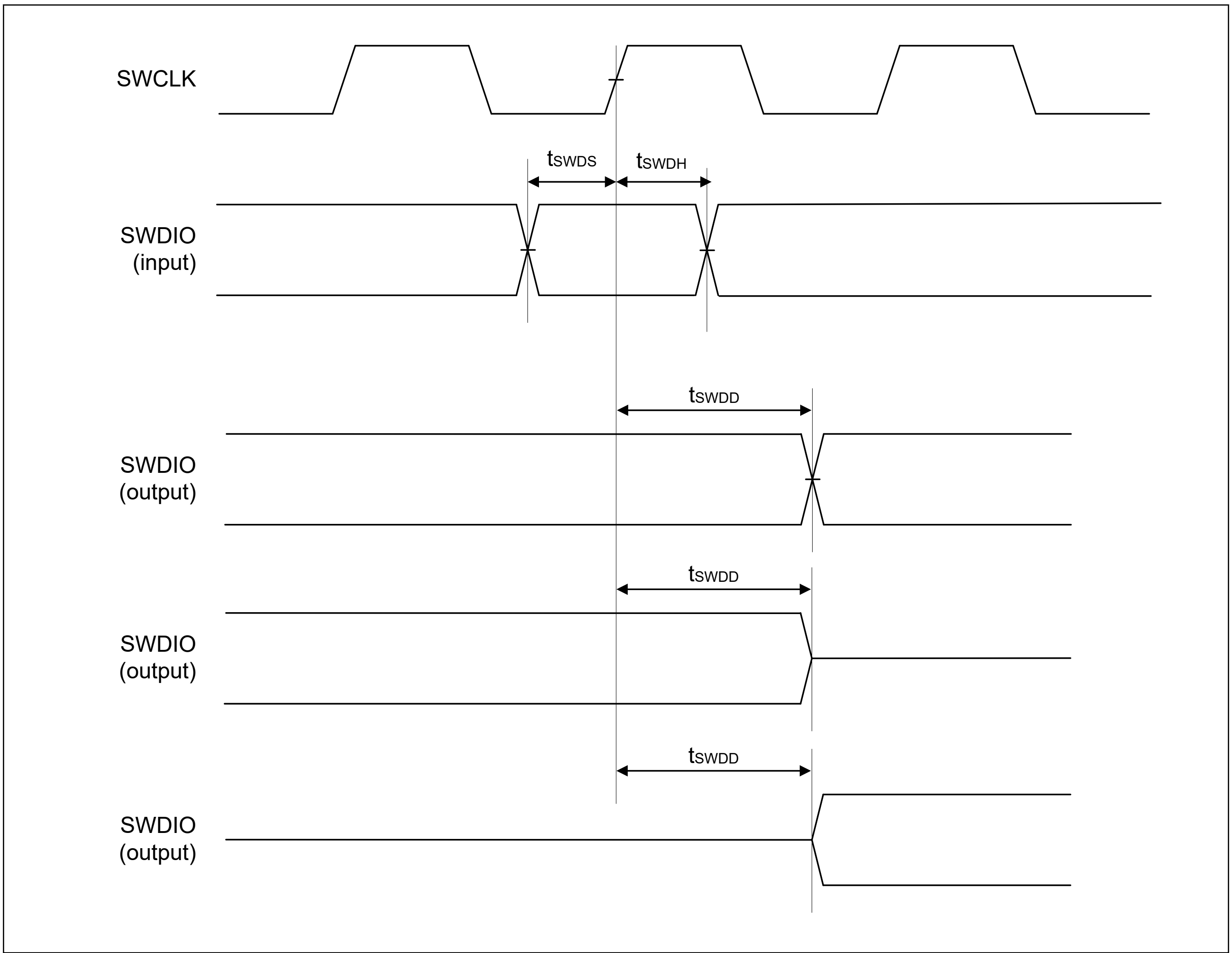


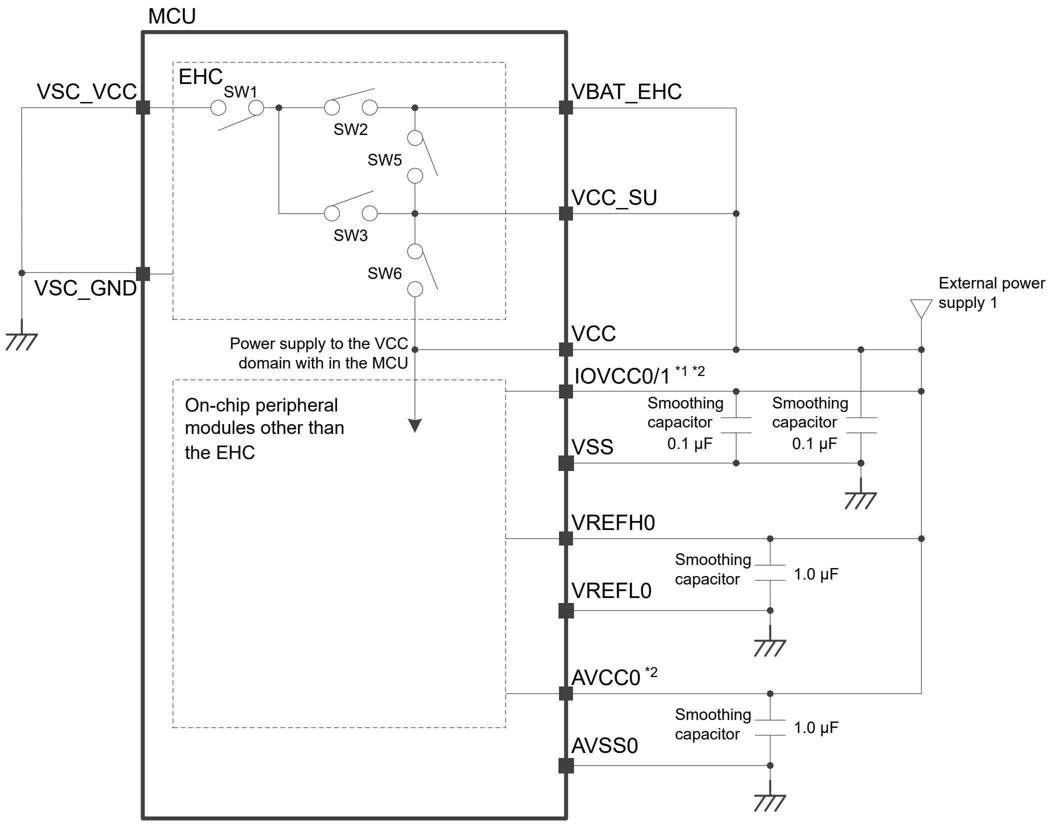
Figure 2.57 SWD input/output timing

Appendix 1. Connecting the Capacitors to the Power Supply Pins

The power supply pins should be connected to the ground through smoothing capacitors placed close to each of the power supply pins. This appendix shows representative examples of connections. Setting the power supply open control register (VOCR) enables the external supply of power. In an environment where much external noise is present, place a 10-µF capacitor close to each of the power supply pins as required, in addition to the capacitors in th relevant example, to improve robustness against external noise and obtain stable operation of the circuit.

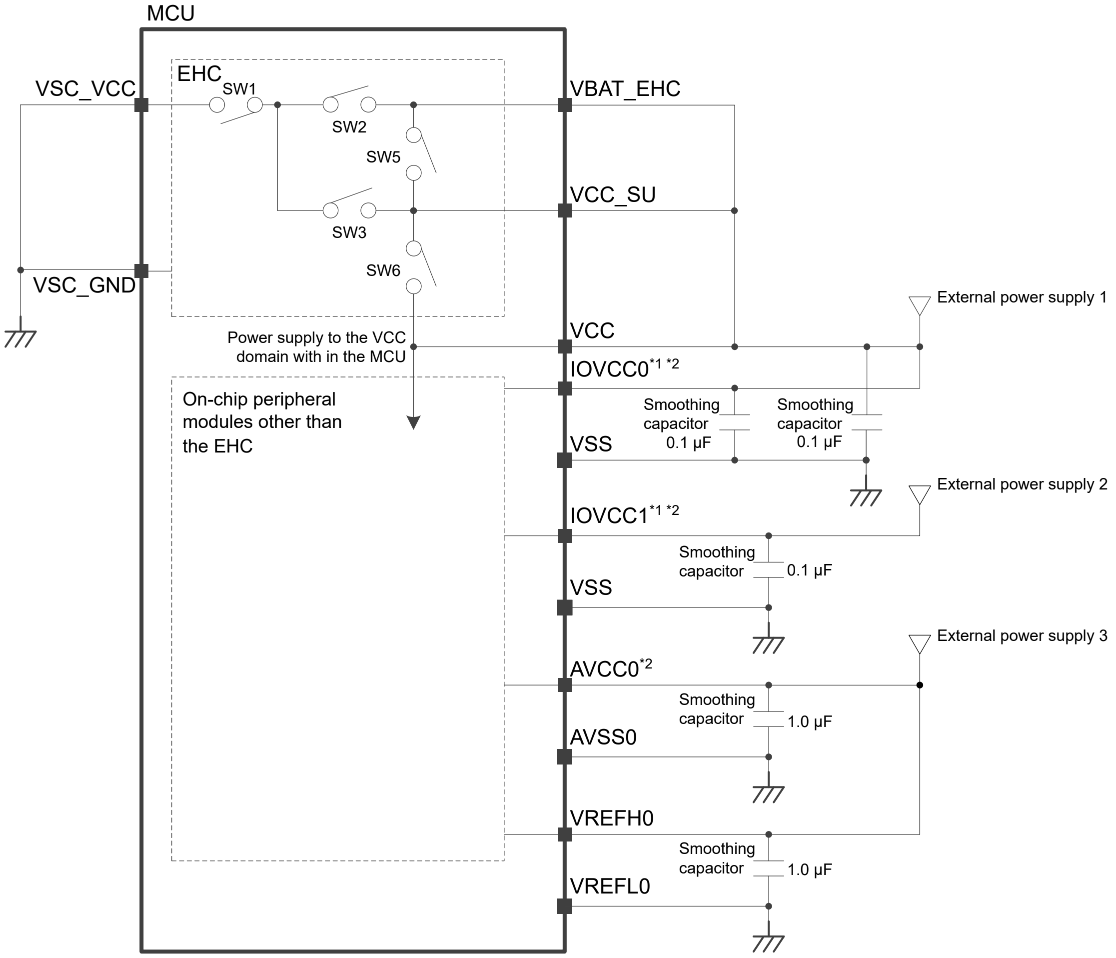
1.1 Example of Connections for Normal Startup Mode

Figure 1.1 and Figure 1.2 show examples of connection for normal startup mode with a single power source and multiple power sources when EHC is not used.



Note 1. A smoothing capacitor should be connected to each of IOVCC0/1.
Note 2. Set the VOCR register to enable the supply of power to these pins.

Figure 1.1 Normal startup mode with a single power source

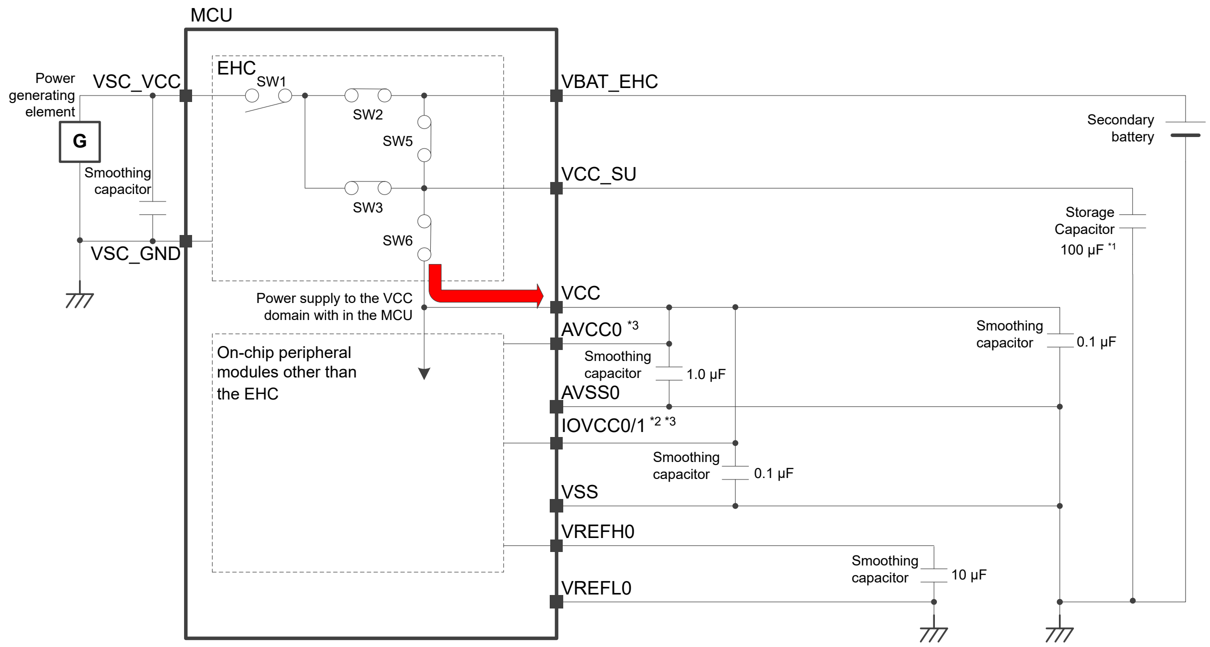


Note 1. A smoothing capacitor should be connected to each of IOVCC0/1.
Note 2. Set the VOCR register to enable the supply of power to these pins.

Figure 1.2 Normal startup mode with multiple power sources

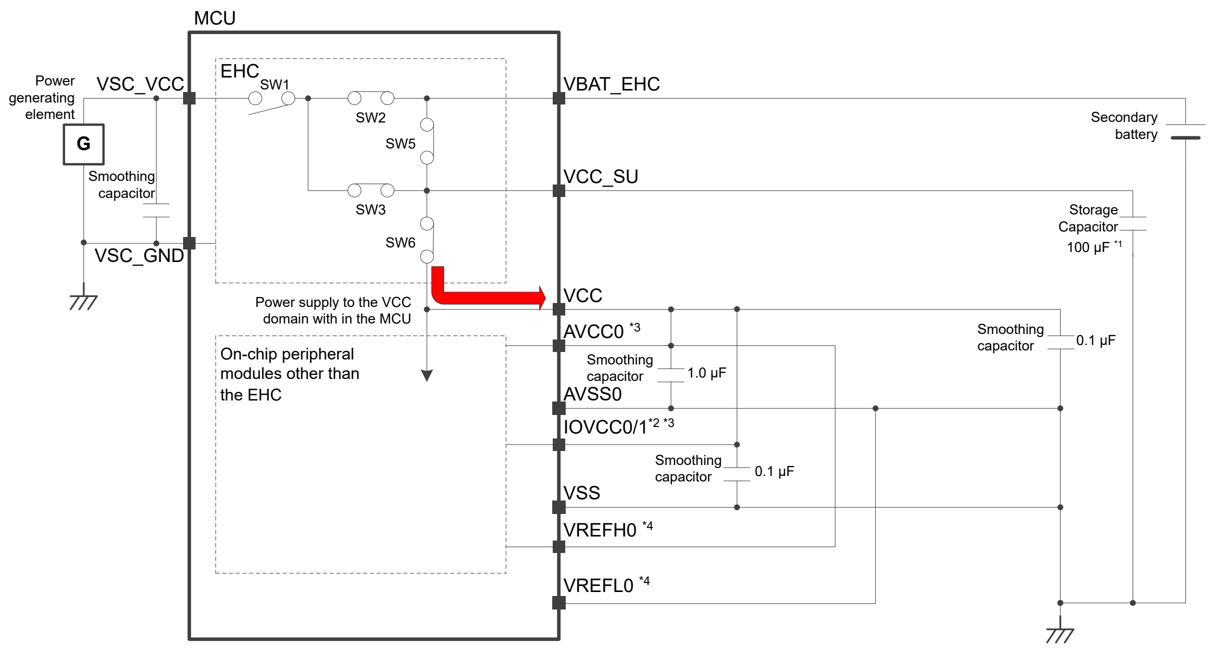
1.2 Example of Connections in Energy Harvesting Startup Mode (1)

Figure 1.3 shows an example of connections in energy harvesting startup mode with the EHC and VREF in use, and no external power supplies. Figure 1.4 shows an example where AVCC0 is the reference voltage.



Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range.
Note 2. A smoothing capacitor should be connected to each of IOVCC0/1.
Note 3. Set the VOCR register to enable the supply of power to these pins.

Figure 1.3 Energy harvesting startup mode with the VREF in use

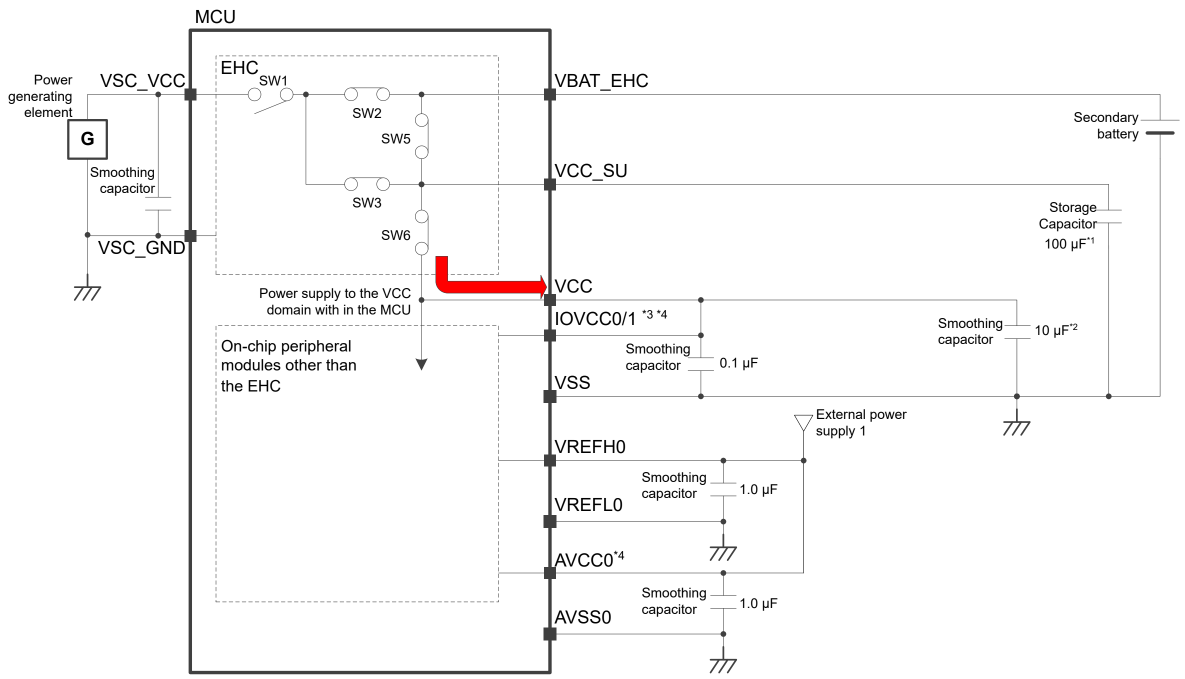


Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range.
Note 2. A smoothing capacitor should be connected to each of IOVCC0/1.
Note 3. Set the VOCR register to enable the supply of power to these pins.
Note 4. In this example, the setting of the ADHVREFCNT register in the ADC14 is 0x00 (selecting AVCC0 as the reference voltage).

Figure 1.4 Energy harvesting startup mode with AVCC0 as the reference voltage

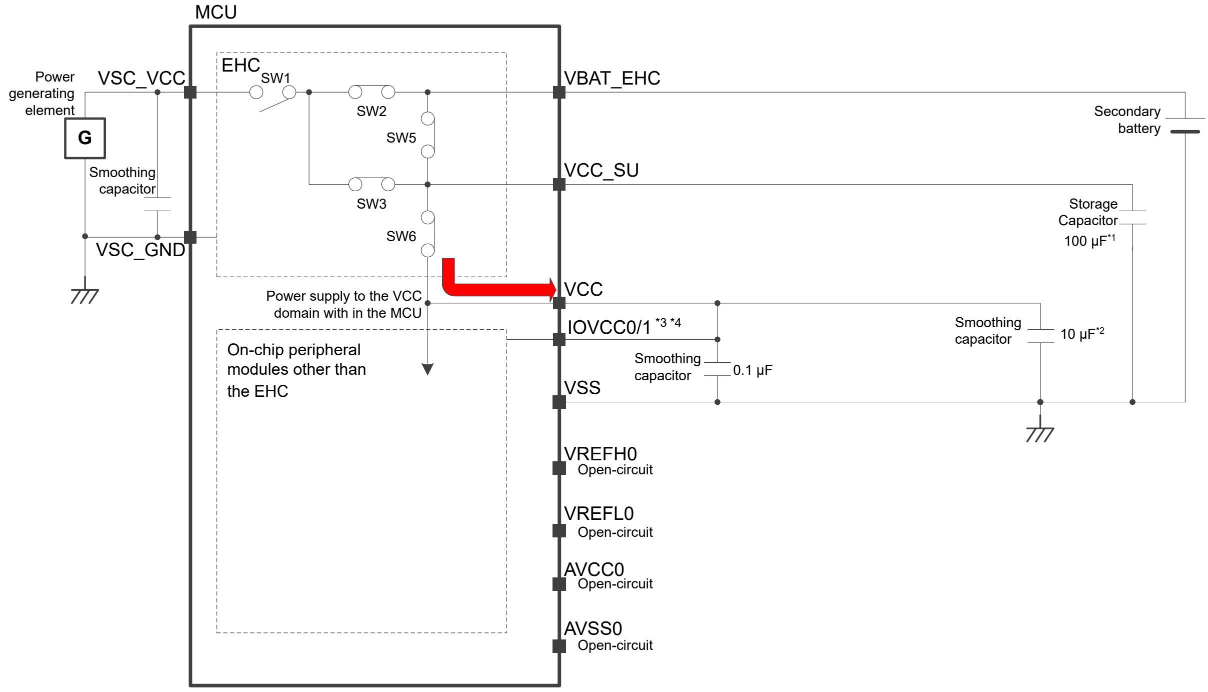
1.3 Example of Connections in Energy Harvesting Startup Mode (2)

Figure 1.5 shows an example of connections in energy harvesting startup mode with the EHC in use and separate power sources for the analog circuits. Figure 1.6 shows shows an example of a connection when an analog circuit is not used. Figure 1.7 shows an example of minimum connections in energy harvesting startup mode.



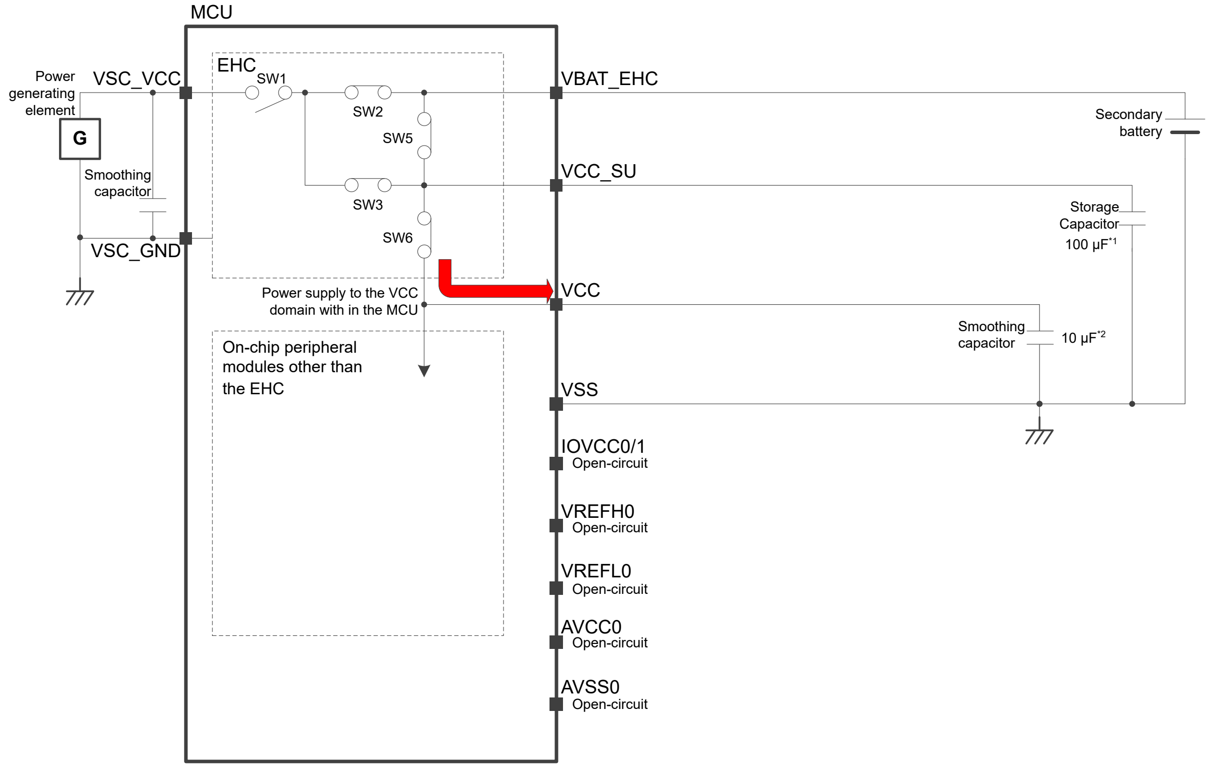
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range.
Note 2. The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.
Note 3. A smoothing capacitor should be connected to each of IOVCC0/1.
Note 4. Set the VOCR register to enable the supply of power to these pins.

Figure 1.5 Energy harvesting startup mode with the VREF in use



Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range.
Note 2. The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.
Note 3. A smoothing capacitor should be connected to each of IOVCC0/1.
Note 4. Set the VOCR register to enable the supply of power to these pins.

Figure 1.6 Energy harvesting startup mode with AVCC0 as the reference voltage



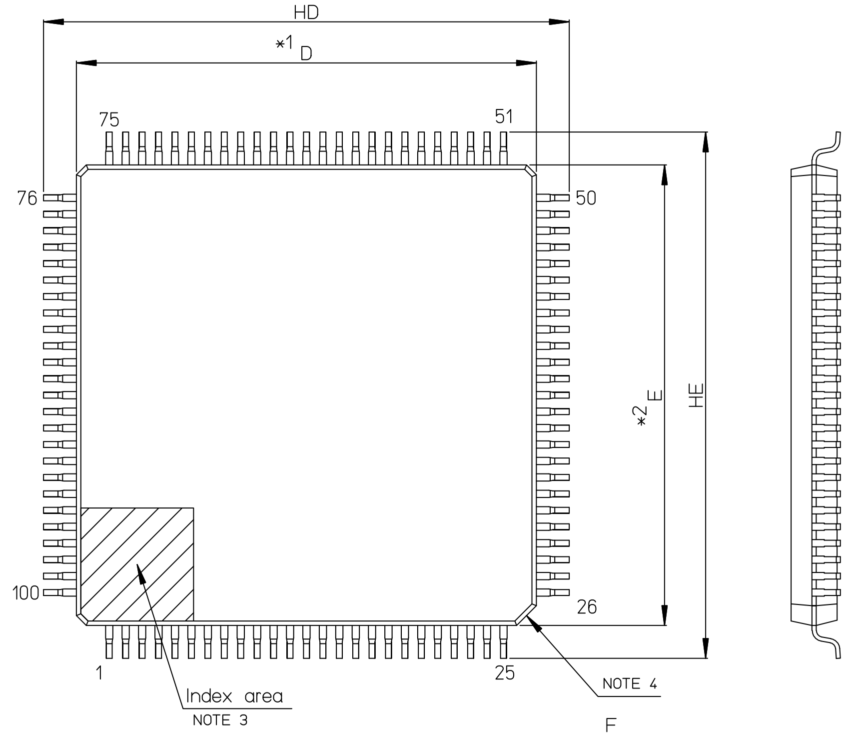
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range.
Note 2. The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.

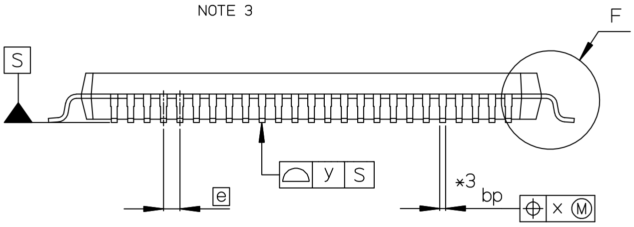
Figure 1.7 Energy harvesting startup mode as a minimum connection

Appendix 2. Package Dimensions

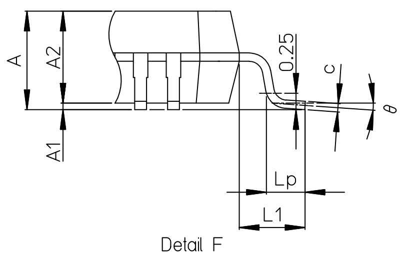
Information on the latest version of the package dimensions or mountings is displayed in "Packages" on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	——	0.6g





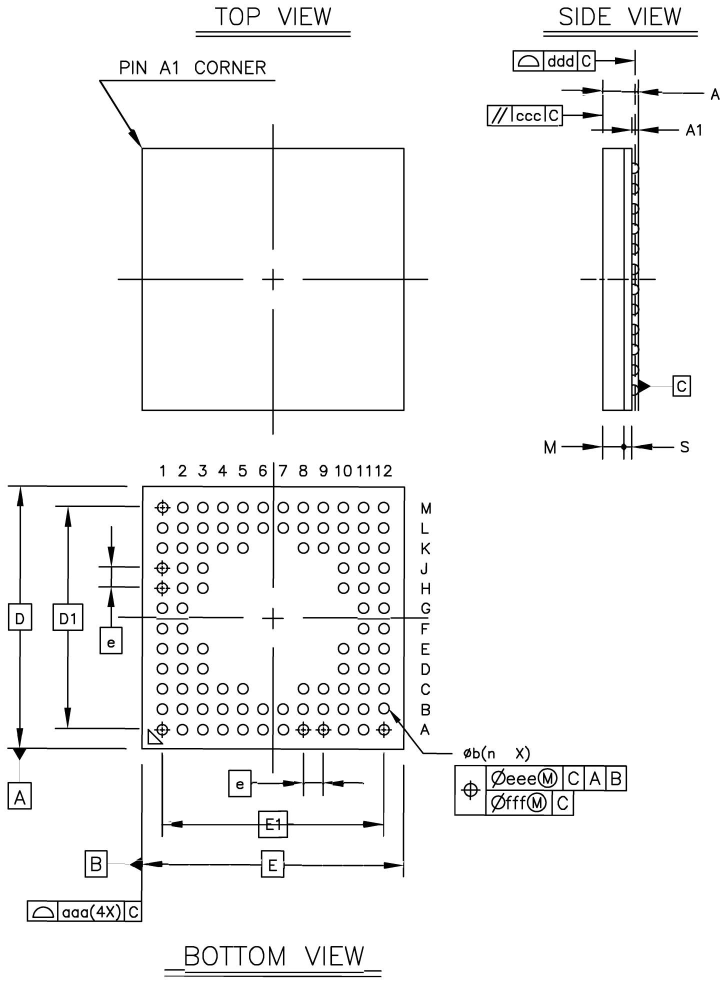
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A2	——	1.4	——
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure 2.1 LFQFP 100-pin

TBD

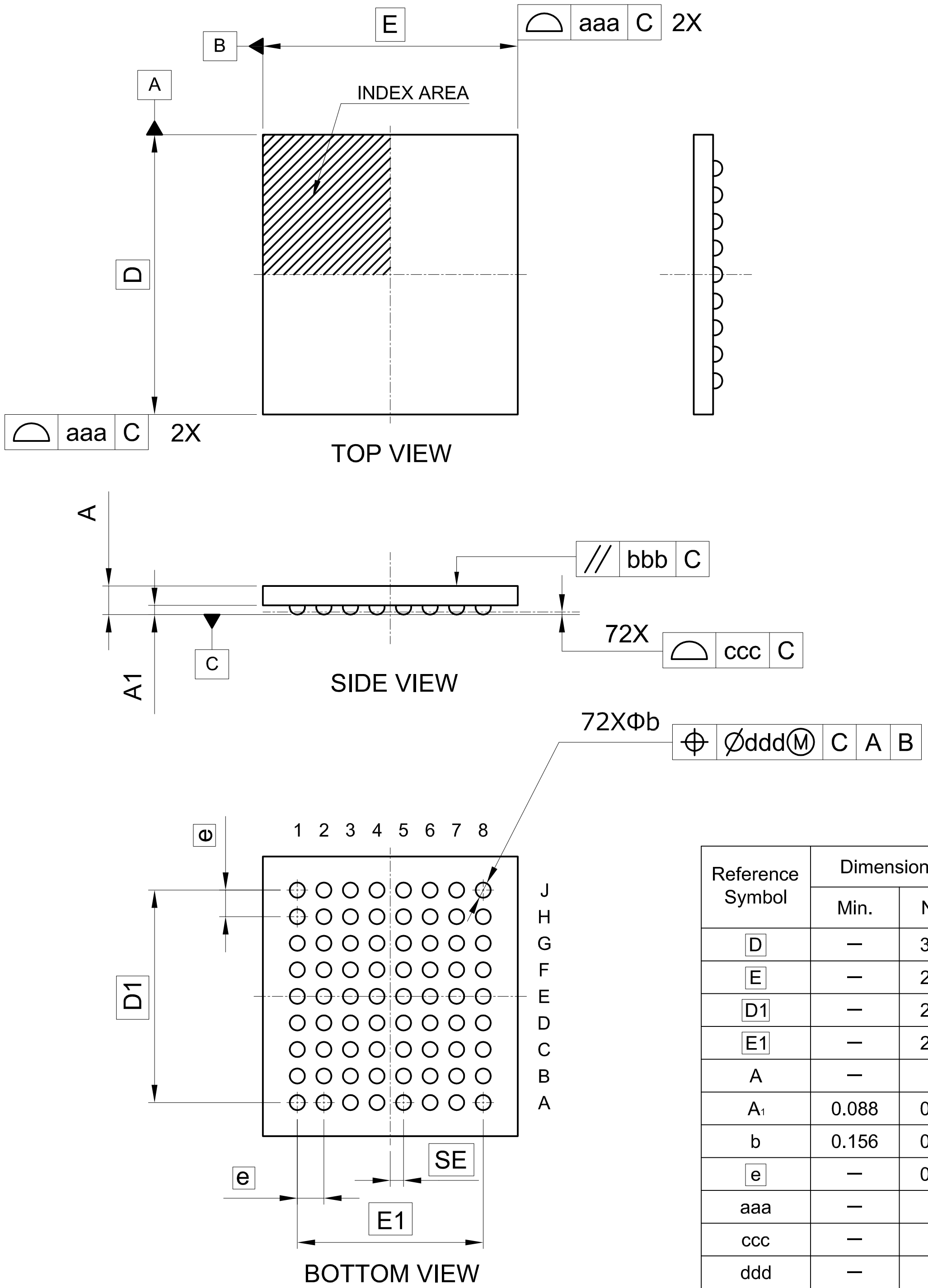


		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package :				LFBGA	
Body Size:	X	E		6.5	
	Y	D		6.5	
Ball Pitch :		e		0.500	
Total Thickness :		A	–	–	1.000
Mold Thickness :		M		0.530 Ref.	
Substrate Thickness :		S		0.196 Ref.	
Ball Diameter :				0.250	
Stand Off :		A1	0.110	–	0.210
Ball Width :		b	0.200	–	0.300
Package Edge Tolerance :		aaa		0.100	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		100	
Edge Ball Center to Center :	X	E1		5.500	
	Y	D1		5.500	

Ball pad opening: 0.25 mm

Figure 2.2 BGA 100-pin (TBD)

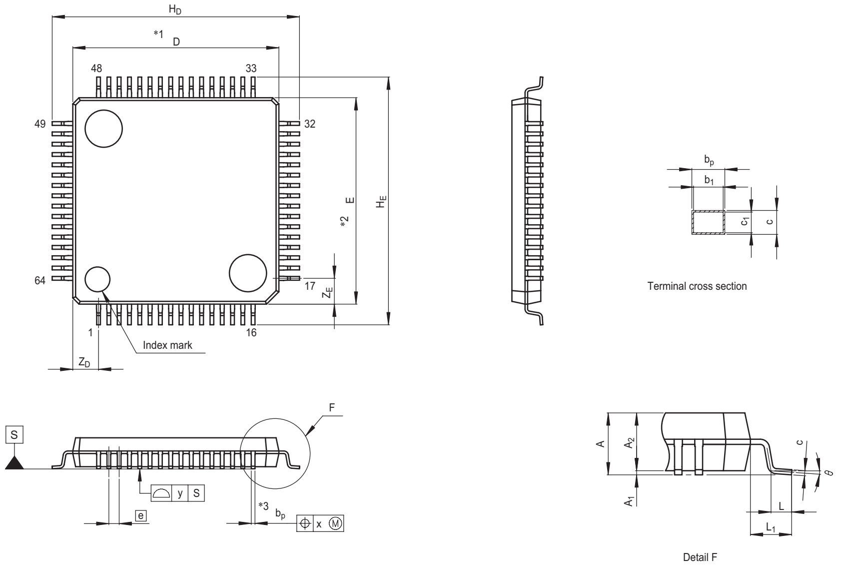
JEITA Package code	RENESAS code	MASS(TYP.)[g]
S-XBGA72-2.88x3.16-0.30	SXBG0072MA-A	T.B.D



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	3.160	—
E	—	2.880	—
D1	—	2.400	—
E1	—	2.100	—
A	—	—	0.360
A_1	0.088	0.104	0.120
b	0.156	0.173	0.208
e	—	0.300	—
aaa	—	—	0.025
ccc	—	—	0.030
ddd	—	—	0.015
SE	—	0.150	—

Figure 2.3 WLBGA 72-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

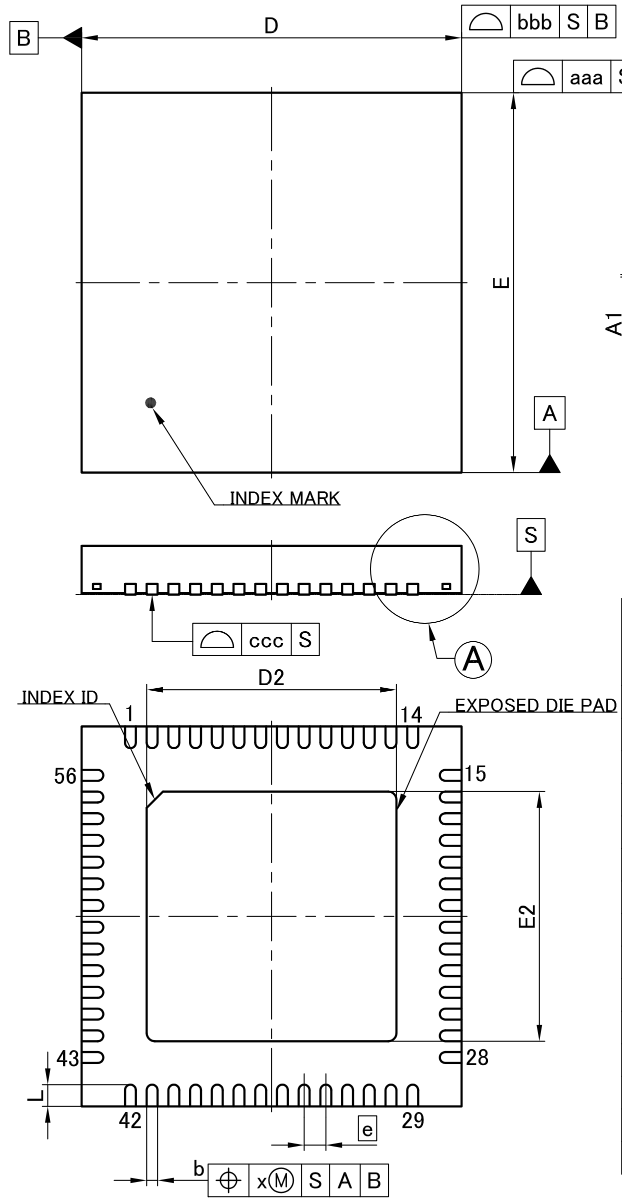


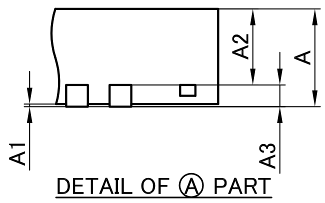
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.4 LFQFP 64-pin

JEITA Package Code	RENESAS Code	MASS(Typ.) [g]
P-HVQFN56-7×7-0.40	PVQN0056LA-A	0.13





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	0.90
A1	—	—	0.05
A2	—	0.65	0.70
A3	—	0.20	—
b	0.15	—	0.25
D	—	7.00	—
D2	—	4.60	—
E	—	7.00	—
E2	—	4.60	—
L	0.35	0.40	0.45
e	—	0.40	—
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.05
x	—	—	0.10

Figure 2.5 QFN 56-pin

Revision History

Revision 1.00 — April 3, 2020

First edition, issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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