Description

The P91E0 is a highly programmable, multiple channel power management integrated circuit (PMIC) designed for the Intel® Atom® System-on-Chip (SoC) to meet the high performance requirements as well as to provide a high level of integration to minimize system board area and BOM cost.

The P91E0 includes sub-systems for voltage regulation, power sequencing management, analog-to-digital (A/D) conversion, GPIOs, PWMs and others. The P91E0 is controlled and programmed via an I2C interface that operates in conjunction with the SoC. There is also a SerialVID (SVID) interface between the SoC and the PMIC for controlling the VCC, VNN, and VDDQ voltage rails, supporting the VR12.1 and IMVP8 specification.

The P91E0 is capable of providing current levels sufficient for entry-level platforms with its internal regulators, and it is scalable to higher current requirements by adding IDT's unique Distributed Power Units (DPUs) (P9148) to source additional current for those DCDC rails.

Also included are 7 low drop-out regulators (LDOs) which are programmable over a wide output voltage range and offer output currents up to 550mA. These LDOs are designed for low noise, high PSRR, and excellent transient response.

The default output voltages of all regulators as well as device sequencing can be programmed in the one-time programmable (OTP) memory (at the factory) to adjust to nonstandard configurations. Contact IDT marketing for specific requirements.

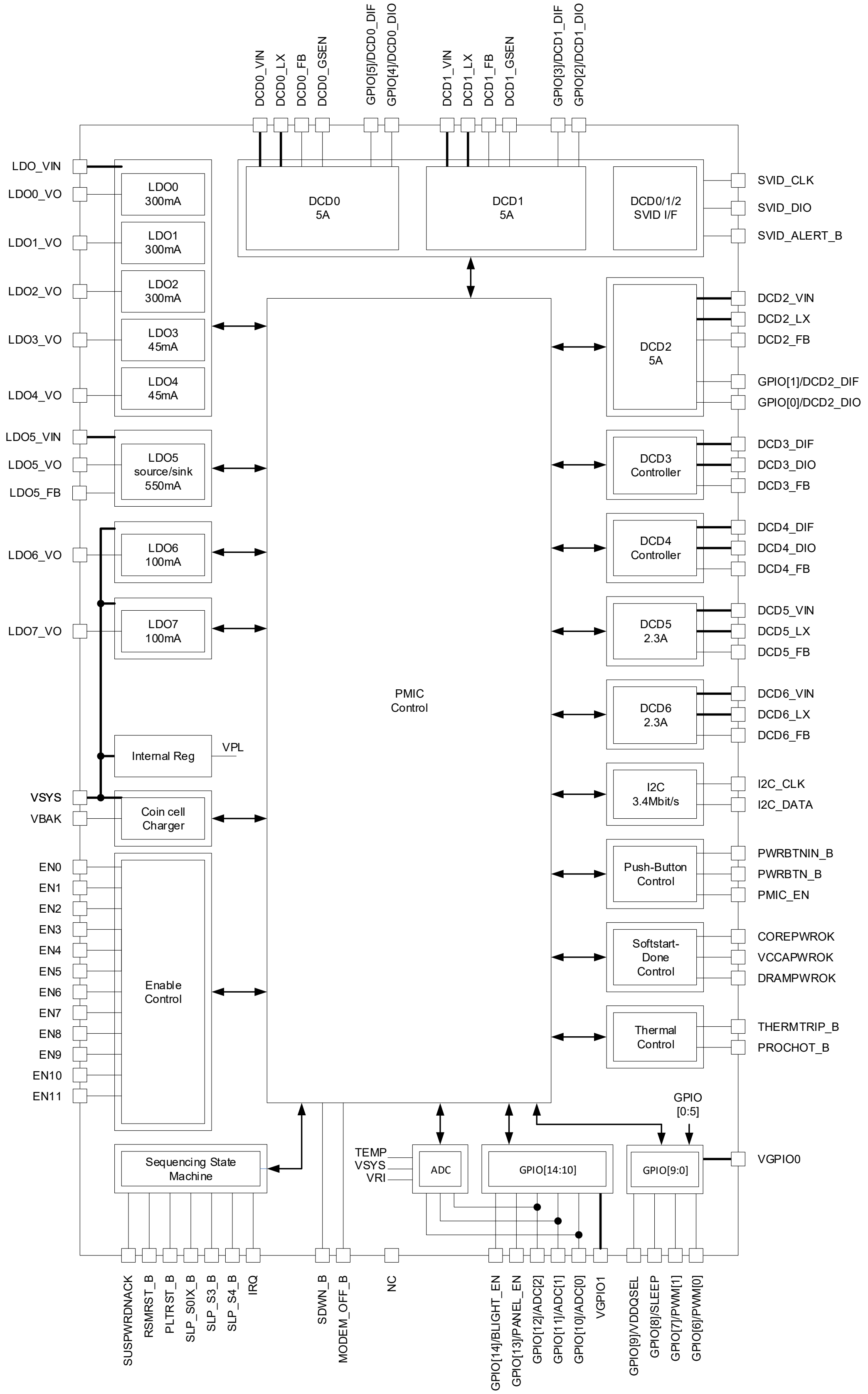
Typical Applications

- General Embedded Applications
- Print Imaging and Multi-function Printers
- µServers and Storage
- Industrial and Embedded Systems

Features

- Single 3.15V to 5.25V supply input
- 3 × SVID IMVP8/VR12.1 compatible 5A synchronous step-down switching regulators with DPU interface to support up to four additional 6A phases
- 2 × step-down switching controller with DPU interface to support up to four 6A phases
- 2 × 2.3A synchronous step-down switching regulators
- Programmable mode selection:
  - Automatic PWM/PFM Mode transition for high efficiency at light load or
  - PWM-Only Mode for low-noise applications
- 7 × (45mA to 300mA) linear regulators; LDO0, LDO1, and LDO2 have an optional pass switch feature
- 1 × ±550mA Vtt linear regulator LDO5
- 10-bit analog-to-digital converter (ADC) monitors internal and external voltages, currents, and temperature
- Host interface and system management
  - Interrupt controller with mask-able interrupts
  - Reset function
  - Power control state machine
  - Programmable sequencing of output rails
  - High speed I2C interface (3.4MHz)
- Programmable enable outputs for external switches
- 15 × GPIOs
- -40°C to +85°C industrial temperature range
- Thermally-enhanced 9.0 × 9.0 × 0.85 mm 100-VFQFPN

Block Diagram



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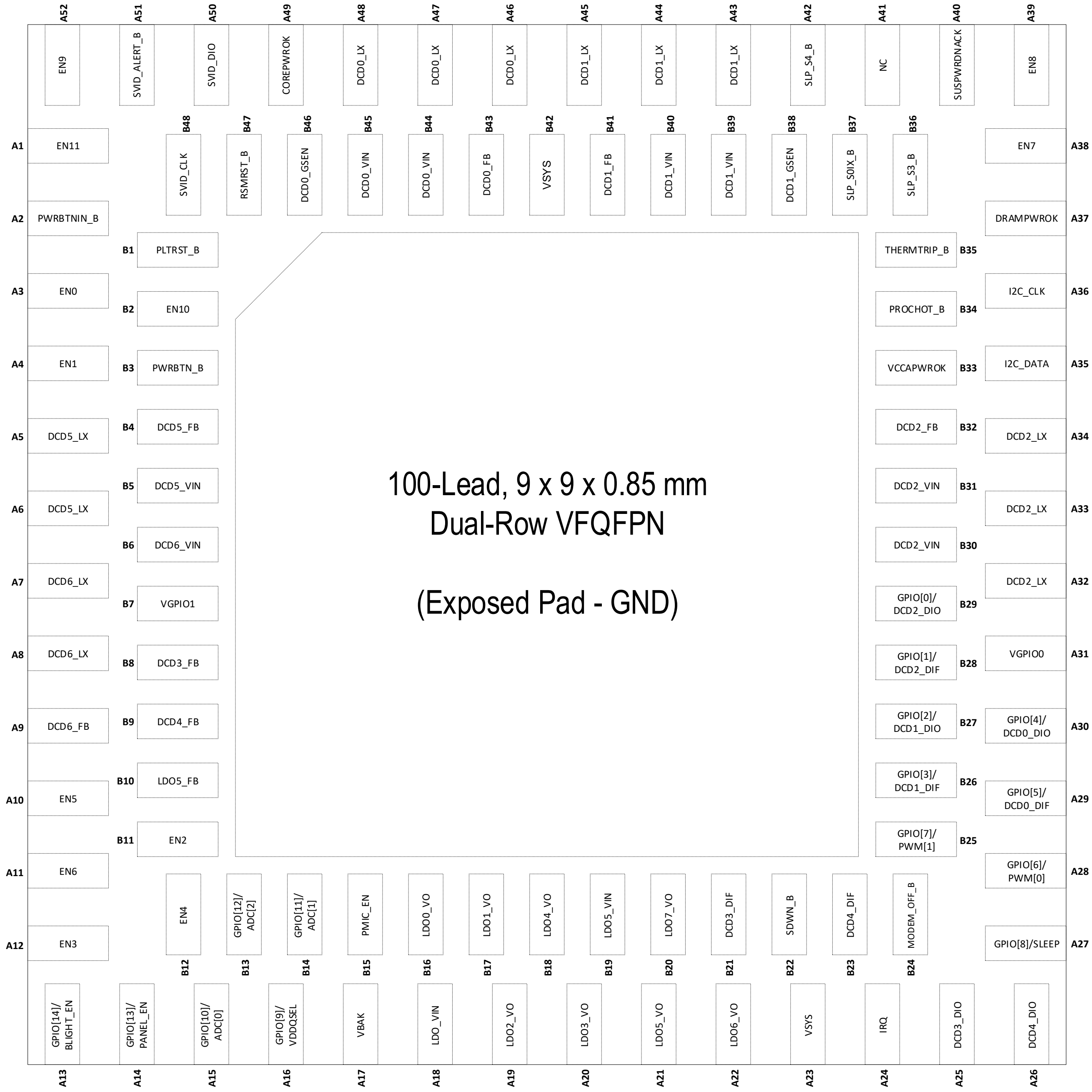
1. Pin Assignments

Figure 1. Pin Assignments for 9.0 × 9.0 × 0.85 mm 100-VFQFPN Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
A1	EN11	Output	Open drain output enable signal.
A2	PWRBTNIN_B	Input	System power button input (active-LOW). The button must be pressed for longer than 36ms (30ms typical) to turn on all the A-type power rails. If PWRBTNIN_B is used, PMIC_EN should be connected to GND. If PMIC_EN is used to power the P91E0 ON/OFF, the PWRBTNIN_B pin should be left floating (unconnected).
A3	EN0	Output	Open-drain output-enable signal.
A4	EN1	Output	Open-drain output-enable signal.
A5, A6	DCD5_LX	Output	DCD5 switch node. This pin connects to the output inductor.
A7, A8	DCD6_LX	Output	DCD6 switch node. This pin connects to the output inductor.
A9	DCD6_FB	Input	Feedback voltage for DCD6. This pin must be connected to the output voltage of the DCD6.
A10	EN5	Output	Open-drain output enable signal.
A11	EN6	Output	Open-drain output enable signal.
A12	EN3	Output	Open-drain output-enable signal.
A13	GPIO[14]/BLIGHT_EN	Input / Output	General purpose input/output 14 or backlight enable output.
A14	GPIO[13]/PANEL_EN	Input / Output	General purpose input/output 13 or LCD panel enable output.
A15	GPIO[10]/ADC[0]	Input / Output	General purpose input/output 10 or ADC[0] input.
A16	GPIO[9]/VDDQSEL	Input / Output	General purpose input/output 9 or DCD2 output voltage select.
A17	VBAK	Output	Coin-cell backup battery connection. If the VBAK is used, connect a 0.1µFcapacitor (minimum) between VBAK and ground. If the VBAK function is not used, connect this pin to ground.
A18	LDO_VIN	Input	Input supply voltage for LDO0, LDO1, LDO2, LDO3, and LDO4.
A19	LDO2_VO	Output	Linear regulator 2 output terminal.
A20	LDO3_VO	Output	Linear regulator 3 output terminal.
A21	LDO5_VO	Output	Source-sink regulator 5 output terminal. Leave this pin floating if the function is not used.
A22	LDO6_VO	Output	Linear regulator 6 output terminal.
A23, B42	VSYS	Input	Input power supply powering the P91E0 internal circuitry. Connect a 2.2µF from this pin to ground. Place the capacitor as close as possible to VSYS.
A24	IRQ	Output	Interrupt request output.
A25	DCD3_DIO	Input / Output	DCD3 regulator digital interface input/output signal. Connect to the DIO pin of the P9148, or leave open if unused.
A26	DCD4_DIO	Input / Output	DCD4 regulator digital interface input/output signal. Connect to the DIO pin of the P9148, or leave open if unused.

Pin Number	Name	Type	Description
A27	GPIO[8]/SLEEP	Input / Output	General purpose input/output 8 or Sleep Mode control signal.
A28	GPIO[6]/PWM[0]	Input / Output	General purpose input/output 6 or PWM[0] output control signal.
A29	GPIO[5]/DCD0_DIF	Input / Output	General purpose input/output 5 or DCD0 regulator digital interface output.
A30	GPIO[4]/DCD0_DIO	Input / Output	General purpose input/output 4 or DCD0 regulator digital interface input/output.
A31	VGPIO0	Input	Input supply voltage for GPIO[0] to GPIO[9]. This pin must be connected to 1.8V voltage rail.
A32, A33, A34	DCD2_LX	Output	DCD2 switch node. This pin connects to the output inductor.
A35	I2C_DATA	Input / Output	I2C data.
A36	I2C_CLK	Input	I2C clock.
A37	DRAMPWROK	Output	Active-HIGH, open-drain soft-start-done signal.
A38	EN7	Output	Open-drain output enable signal.
A39	EN8	Output	Open-drain output enable signal.
A40	SUSPWRDNACK	Input	Suspend power-down acknowledgment.
A41	NC	–	No connect
A42	SLP_S4_B	Input	Active-LOW input signal. When SLP_S4_B is connected to logic HIGH, all the "U" type power rails are enabled. When pulled LOW, the regulators are shutdown.
A43, A44, A45	DCD1_LX	Output	DCD1 switch node. This pin connects to the output inductor.
A46, A47, A48	DCD0_LX	Output	DCD0 switch node. This pin connects to the output inductor.
A49	COREPWROK	Output	Active-HIGH soft-start-done-signal. Connect to the SOC_PWROK/COREPWROK input pin on the SoC IC.
A50	SVID_DIO	Input / Output	SVID data input and open drain output. Note: Refer to Intel's Serial VID (SVID) protocol specification for details.
A51	SVID_ALERT_B	Output	SVID interrupt from the P91E0 to the SOC. Open-drain output.
A52	EN9	Output	Open drain output enable signal.
B1	PLTRST_B	Input	Platform reset is an active-LOW reset input signal from the SoC to the P91E0.
B2	EN10	Output	Open-drain output enable signal.
B3	PWRBTN_B	Output	Power button output signal. It is a level-shifted copy of the PWRBTNIN_B pin after the 30ms de-bouncing circuit.
B4	DCD5_FB	Input	Feedback voltage for DCD5. This pin must be connected to the output voltage of the DCD5.
B5	DCD5_VIN	Input	Input voltage for DCD5. Connect a bypass capacitor from this pin to ground.
B6	DCD6_VIN	Input	Input voltage for DCD6. Connect a bypass capacitor from this pin to ground.
B7	VGPIO1	Input	Supply voltage for GPIO[10] through GPIO[14]. This pin must be connected to 3.3V.
B8	DCD3_FB	Input	Feedback voltage for DCD3 controller. This pin must be connected to the output voltage of the DCD3.

Pin Number	Name	Type	Description
B9	DCD4_FB	Input	Feedback voltage for DCD4. This pin must be connected to the output voltage of the P9148.
B10	LDO5_FB	Input	Feedback voltage for LDO5. This pin must be connected to the output voltage of the LDO5. This pin is internally connected to LDO5_VO with 180Ω.
B11	EN2	Output	Open-drain output-enable signal.
B12	EN4	Output	Open-drain output-enable signal.
B13	GPIO[12]/ADC[2]	Input / Output	General purpose input/output 12 or ADC[2] input.
B14	GPIO[11]/ADC[1]	Input / Output	General purpose input/output 11 or ADC[1] input.
B15	PMIC_EN	Input	PMIC enable input. If PMIC_EN is used to power the P91E0 ON/OFF, the PWRBTNIN_B pin should be left floating (unconnected). If PWRBTNIN_B is used, PMIC_EN should be connected to GND.
B16	LDO0_VO	Output	Linear regulator 0 output terminal.
B17	LDO1_VO	Output	Linear regulator 1 output terminal.
B18	LDO4_VO	Output	Linear regulator 4 output terminal.
B19	LDO5_VIN	Input	Input supply voltage for source-sink regulator LDO5. Tie to ground if this function is not used.
B20	LDO7_VO	Output	1.8V regulator output terminal for DPS control interface and internal biasing.
B21	DCD3_DIF	Output	DCD3 switching regulator digital interface output signal. Connect to the DIF pin of the P9148 or leave open if unused.
B22	SDWN_B	Output	Shutdown warning. In the event of a system shutdown, the P91E0 issues a system shutdown warning to the modem.
B23	DCD4_DIF	Output	DCD4 switching regulator digital interface output signal. Connect to the DIF pin of the P9148 or leave open if unused.
B24	MODEM_OFF_B	Output	Active-LOW Modem Reset signal (see section 9.4.7).
B25	GPIO[7]/PWM[1]	Input / Output	General purpose input/output 7 or PWM[1] output control signal.
B26	GPIO[3]/DCD1_DIF	Input / Output	General purpose input/output 3 or DCD1 regulator digital interface output.
B27	GPIO[2]/DCD1_DIO	Input / Output	General purpose input/output 2 or DCD1 regulator digital interface input/output.
B28	GPIO[1]/DCD2_DIF	Output	General purpose input/output 1 or DCD2 regulator digital interface output.
B29	GPIO[0]/DCD2_DIO	Input / Output	General purpose input/output 0 or DCD2 regulator digital interface input/output.
B30, B31	DCD2_VIN	Input	Input voltage for DCD2. Connect two 10µF bypass capacitors from this pin to ground.
B32	DCD2_FB	Input	Feedback voltage for DCD2. This pin must be connected to the output filter of the regulator.
B33	VCCAPWROK	Output	Active-HIGH, open-drain soft-start-done signal.
B34	PROCHOT_B	Output	Active-LOW open-drain output signal.
B35	THERMTRIP_B	Input	Active-LOW thermal trip input signal. Catastrophic thermal event indicator to the P91E0 to shut off all power rails.
B36	SLP_S3_B	Input	Active-LOW input signal. When connected to logic HIGH, all the "S" type power rails are enabled. When pulled LOW, the regulators are shutdown.

Pin Number	Name	Type	Description
B37	SLP_S0Ix_B	Input	Active-LOW input signal. When connected to logic HIGH, all the “SX” type power rails are enabled. When pulled LOW, the regulators are shutdown.
B38	DCD1_GSEN	Input	DCD1 ground sense pin.
B39, B40	DCD1_VIN	Input	Input voltage for DCD1. Connect two 10µF bypass capacitors from this pin to ground.
B41	DCD1_FB	Input	Feedback voltage for DCD1. This pin must be connected to the output filter of the DCD1.
B42	VSYS	Input	P91E0 input supply voltage. Connect a 2.2µF capacitor from this pin to ground. Place the capacitor as close as possible to VSYS.
B43	DCD0_FB	Input	Feedback voltage for DCD0. This pin must be connected to the output filter of the DCD0.
B44, B45	DCD0_VIN	Input	Input voltage for DCD0. Connect two 10µF bypass capacitors from this pin to ground.
B46	DCD0_GSEN	Input	DCD0 ground sense pin.
B47	RSMRST_B	Output	Resume reset pin is an active-LOW soft-start-done signal.
B48	SVID_CLK	Input	SVID clock input.
EPAD	PGND	Ground	Ground. This exposed pad is the connection for the current return path and is also used for thermal dissipation. Connect to PCB ground with sufficient vias to support the returned current and thermal requirement.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the P91E0 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction Temperature		-40	+125	°C
	ESD – Human Body Model (HBM)	All pins	-1500	+1500	V
	ESD – Charged Device Model (CDM)	All pins	-500	+500	V
	Maximum Voltage	LDO_VIN, LDO5_VIN, VGPIO0, LDO0_VO, LDO1_VO, LDO2_VO, LDO3_VO, LDO4_VO, LDO5_VO, DCD0_FB, DCD1_FB, DCD2_FB, DCD0_DIO, DCD1_DIO, DCD2_DIO, DCD3_DIF, DCD3_DIO, DCD4_DIF, DCD4_DIO, GPIO[9:0]	-0.3	2.2	V
		GPIO[14:10]	-0.3	3.6	V
		Maximum DC Voltage (t > 500ns): DCD0_LX, DCD1_LX, DCD2_LX, DCD5_LX, DCD6_LX	-0.3	6.0	V
		Maximum AC Voltage (t < 500ns): DCD0_LX, DCD1_LX, DCD2_LX, DCD5_LX, DCD6_LX	-1.2	6.5	V
		All other pins	-0.3	6.0	V
	Latch-up	GPIO pins, Grade II	–	40	mA
		All other pins, Grade II	–	100	mA

4. Thermal Characteristics

The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the device will enter thermal shutdown.

Table 3. Thermal Characteristics – 100-VFQFPN

Symbol	Parameter	Rating	Units
θ_{JA}	Thermal Resistance Junction to Ambient [a], [b]	24.0	°C/W
$\theta_{JC(TOP)}$	Thermal Resistance Junction to Top of the Case [a], [b]	19.3	°C/W
$\theta_{JB(BOT)}$	Thermal Resistance Junction to Exposed Pad [a], [b]	0.7	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	125	°C
T_A	Ambient Operating Temperature (Industrial Range)	-40 to +85	°C
T_{STOR}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The thermal rating is calculated based on a JEDEC standard 2S2P 4-layer board (114mm × 101mm in still air conditions with 2 oz. internal planes) and 5 × 5 mm EPAD soldered down and a 25 thermal via array to the internal plane.

[b] Actual thermal resistance is affected by the printed circuit board (PCB) size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

5. Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{SYS}	P91E0 Input Voltage	3.15	–	5.25	V
V_{PVIN}	DCD0, DCD1, DCD2, DCD5, and DCD6 Power Stage Input Voltage	2.80	–	5.25	V
V_{IN_LDO}	LDO0, LDO1, LDO2, LDO3, LDO4 Input Voltage	1.00	1.80	2.00	V
V_{IN_LDO5}	LDO5 Input Voltage	1.20	1.35	1.50	V

6. Overview and Power Supply DC Characteristics

The P91E0 is an integrated power-management IC (PMIC) targeted for applications powered by a rechargeable battery or a regulated 3.15V to 5.25V system supply. However if the P91E0 has a P9148 DPU attached to any of the DCDx voltage output rails, operating from a 5V system supply is strongly recommended. The product offers seven configurable step-down converters capable of delivering up to 5.0A of load current for the memory, processor core, I/O, auxiliary, and pre-regulation for LDOs. In addition, the device includes 8 low-dropout (LDO) linear regulators that can be supplied from a battery or a regulated supply. The P91E0 is configured/controlled via I2C. Other features include 15 general purpose I/O (GPIO), push button control, integrated state machine for power sequencing, and thermal management.

There are six defined states that are determined by the behavior of the platform power rails, SoC sideband signals (COREPWROK, PLTRST_B, SLP_Sx_B), and internal state machine modes. The states are G3, SoC-G3, SoC-S0, SoC-S0Ix, SoC-S3, and SoC-S4/S5. See section 9.3 for details.

Table 5 lists the regulators and their DC characteristics.

Table 5. Overview of Power Supplies

Note: See important notes at the end of the table.

Regulator	I_{OUT_DC} [A]	I_{OUT_MAX} [A]	I_{OUT_MAX} with DPUs[a], [b] [A]	V_{IN} Range (V)[c]	V_O Range (V)	Output Inductance (L) and Capacitance[e] (C_O)
DCD0[d]	4.0	5.0	29	$V_{SYS} = V_{IN\_DCD0}$ = 3.15V to 5.25V	SVID: 0.25V to 1.3V Non-SVID: 1.1V to 1.9V	Factory-enabled load line (DCD0 and DCD1 default): L_{5VIN} = 0.47µH $C_{O\_Total} = 6 \times 47µF$ Refer to the DPU datasheet for additional C_O.
DCD1[d]	4.0	5.0	29	$V_{SYS} = V_{IN\_DCD1}$ = 3.15V to 5.25V	SVID: 0.25V to 1.3V Non-SVID: 1.1V to 1.9V	
DCD2[d]	4.0	5.0	29	$V_{SYS} = V_{IN\_DCD02}$ = 3.15V to 5.25V	SVID: 0.25V to 1.3V Non-SVID: 1.1V to 1.9V	Factory-disabled load line (DCD2 default): L_{5VIN} = 0.47µH $C_O = 3 \times 47µF$ Refer to the DPU datasheet for additional C_O.
DCD3_CTRL	–		24	V_{SYS} = 3.15V to 5.25V	0.525V to 3.6V	$C_O = 3 \times 47µF$ per DPU; see DPU datasheet for L
DCD4_CTRL	–		24	V_{SYS} = 3.15V to 5.25V	0.525V to 3.6V	$C_O = 3 \times 47µF$ per DPU; see DPU datasheet for L
DCD5	2.0	2.3	–	$V_{SYS} = V_{IN\_DCD5}$ = 3.15V to 5.250V	0.525V to 3.375V	$L_{3.3VIN}$ = 0.68µH; L_{5VIN} = 1.0µH $C_O = 2 \times 47µF$
DCD6	2.0	2.3	–	$V_{SYS} = V_{IN\_DCD6}$ = 3.15V to 5.25V	0.525V to 3.375V	$L_{3.3VIN}$ = 0.68µH; L_{5VIN} = 1.0µH $C_O = 2 \times 47µF$
LDO0 [f]	0.300	0.325	–	V_{LDO_VIN} = 1.0V to 2.0V	1.0V to 1.65V	C_O= 2.2µF
LDO1 [f]	0.300	0.325	–		1.0V to 1.65V	C_O= 2.2µF
LDO2 [f]	0.300	0.325	–		1.0V to 1.65V	C_O= 2.2µF
LDO3	0.045	0.045	–		1.0V to 1.65V	C_O= 1.0µF
LDO4	0.045	0.045	–		1.0V to 1.65V	C_O= 1.0µF

Regulator	I_{OUT_DC} [A]	I_{OUT_MAX} [A]	I_{OUT_MAX} with DPUs[a], [b] [A]	V_{IN} Range (V)[c]	V_O Range (V)	Output Inductance (L) and Capacitance[e] (C_O)
LDO5	±0.550	±0.550	–	V_{LDO5_VIN} = 1.2V to 1.5V	V_{IN_LDO5} / 2	C_O= 22µF
LDO6	0.100	0.110	–	V_{SYS} = 3.15V to 5.25V	1.20V to 3.55V	C_O= 1.0µF
LDO7	0.100	0.110	–	V_{SYS} = 3.15V to 5.25V	1.80V	C_O= 1.0µF

[a] Ensure that the DPU's PVIN voltage is above PVIN UVLO (VUV) before VSYS reaches VSYS_MIN.

[b] PWRBTNIN_B (or PMIC_EN when used) should not be asserted until the DPU's PVIN voltage is above PVIN UVLO (V_{UV}; see the DPU datasheet).

[c] During power up ensure that the voltage seen by VSYS is monotonic, which can be achieved by adding an appropriate RC filter.

[d] The SVID voltage range can be deselected by OTP or via I2C, and the mode of operation must be set to FPWM Mode when used with DPUs.

[e] The output capacitor recommendation is for X5R, 20%, 0805 minimum case size. Derating of the ceramic capacitor due to operating conditions, such as bias voltage and temperature, should be considered as part of the component selection.

[f] Can be configured as a pass switch.

7. Electrical Characteristics and Configuration

7.1 General Specification

V_{SYS}= 5.0V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Table 6. Electrical Characteristics – PMIC VSYS, UVLO, Thermal Shutdown Threshold

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{SYS}	Input Voltage Range	–	3.15	–	5.25	V
$I_{Q(VSYS)}$	VSYS Quiescent Current	Device in SoC-G3 (OFF state)	–	7	–	µA
		Device in SoC-S4/S5 state; all regulators powered-off	–	0.75	1.1	mA
$V_{SYS(UVLO)}$	Under-Voltage Lock-Out (UVLO) Threshold	VSYS rising ($VSYSREF_R$)	–	2.9		V
		VSYS falling ($VSYSREF_F$)		2.5		V
T_{SDN}	Thermal Shutdown	Temperature increasing, GBD[a]	125	132	–	°C

[a] GBD = Guaranteed by design.

7.2 Linear Regulators LDO0, LDO1, LDO2

Table 7. Electrical Characteristics – LDO0, LDO1, LDO2

V_{SYS} = 5V, V_{IN_LDO} = 1.8V, V_{OUT} = 1.5V (default), input capacitance C_{IN} = 10µF, C_O = 2.2µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_LDO}	Input Voltage Range	–	1.0	1.8	2.0	V
V_O	Programmable Output Voltage	–	1.0	1.5	1.65	V
I_{SHDN}	Shutdown Current	–	–	0.5	–	µA
I_Q	Quiescent Current	No Load	–	22	–	µA
	Regulation Voltage Accuracy	–	-2.0	–	+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	–	–	1.0	–	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	–	–	5.0	–	µV/mA
I_O	Maximum Output Current	–	300	–	–	mA
I_{LIM}	Current Limit	–	325			mA
V_{DROP}	Dropout Voltage	I_O = 300mA	–	–	150	mV
PSRR	Power Supply Ripple Rejection	V_{IN_LDO} – V_O = 500mV, I_O = 30mA				dB
		< 200Hz	–	> 100	–	
		1kHz	–	100	–	
		10kHz	–	85	–	
		100kHz	–	55	–	
e_n	Output Noise Voltage	V_O = 1.5V, I_O = 100µA, BW = 10Hz to 100kHz	–	28	–	µVRMS
R_{DIS}	Output Discharge Resistance	–	–	10	–	kΩ
T_{SSR}	LDO Soft-Start Ramp Rate	–	–	30	–	mV/µs

Table 8. I2C Control Register – LDO0, LDO1, LDO2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO0_CTL	R/W	RSVD						LDO0_SEL	LDO0_EN	00_{HEX}	65_{HEX}
LDO1_CTL	R/W	RSVD						LDO1_SEL	LDO1_EN	00_{HEX}	61_{HEX}
LDO2_CTL	R/W	RSVD						LDO2_SEL	LDO2_EN	00_{HEX}	66_{HEX}

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	0
D[1]	LDOx_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by the configured device sequence. 1 = ON/OFF is controlled by the D[0] bit of this register.	0
D[0]	LDOx_EN	Enable bit: 0 = OFF 1 = ON	0

Table 9. ON/OFF Selection Bit Truth Table – LDO0, LDO1, LDO2

D[1]	D[0]	Sequencer Control	LDO
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 10. I2C Output Voltage Setting – LDO0, LDO1, LDO2

Note: Green shading indicates that the register values are loaded from the OTP memory.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO0_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					OTP	12_{HEX}
LDO1_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					OTP	13_{HEX}
LDO2_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					OTP	14_{HEX}

Table 11. I2C Sequencing Control Register – LDO0, LDO1, LDO2

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO0_GRP	R/W	RSVD		LDO0_TYPE		LDO0_GROUP				OTP	ED$_{HEX}$
LDO1_GRP	R/W	RSVD		LDO1_TYPE		LDO1_GROUP				OTP	EE$_{HEX}$
LDO2_GRP	R/W	RSVD		LDO2_TYPE		LDO2_GROUP				OTP	EF$_{HEX}$

Bit	Name	Function		Default
D[7:6]	RSVD	Reserved		0
D[5:4]	LDOx_TYPE	Rail type selection bits: 00$_{BIN}$ = “A” rail type. 01$_{BIN}$ = “U” rail type. 10$_{BIN}$ = “S” rail type. 11$_{BIN}$ = “SX” rail type.		OTP
D[3:0]	LDOx_GROUP	Group Delay Bits		OTP
		0000$_{BIN}$ = Group 0	1000$_{BIN}$ = Group 8	
		0001$_{BIN}$ = Group 1	1001$_{BIN}$ = Group 9	
		0010$_{BIN}$ = Group 2	1010$_{BIN}$ = Group 10	
		0011$_{BIN}$ = Group 3	1011$_{BIN}$ = Group 11	
		0100$_{BIN}$ = Group 4	1100$_{BIN}$ = Group 12	
		0101$_{BIN}$ = Group 5	1101$_{BIN}$ = Group 13	
		0110$_{BIN}$ = Group 6	1110$_{BIN}$ = Group 14	
		0111$_{BIN}$ = Group 7	1111$_{BIN}$ = Disabled	

Table 12. LDO0, LDO1, and LDO2 Output Voltage Setting

V_{OUT}	Decimal	Hexadecimal	Binary
1.000	0	00$_{HEX}$	00000$_{BIN}$
1.025	1	01$_{HEX}$	00001$_{BIN}$
1.050	2	02$_{HEX}$	00010$_{BIN}$
1.075	3	03$_{HEX}$	00011$_{BIN}$
1.100	4	04$_{HEX}$	00100$_{BIN}$
1.125	5	05$_{HEX}$	00101$_{BIN}$
1.150	6	06$_{HEX}$	00110$_{BIN}$
1.175	7	07$_{HEX}$	00111$_{BIN}$
1.200	8	08$_{HEX}$	01000$_{BIN}$
1.225	9	09$_{HEX}$	01001$_{BIN}$
1.250	10	0A$_{HEX}$	01010$_{BIN}$

V_{OUT}	Decimal	Hexadecimal	Binary
1.275	11	$0B_{HEX}$	01011_{BIN}
1.300	12	$0C_{HEX}$	01100_{BIN}
1.325	13	$0D_{HEX}$	01101_{BIN}
1.350	14	$0E_{HEX}$	01110_{BIN}
1.375	15	$0F_{HEX}$	01111_{BIN}
1.400	16	10_{HEX}	10000_{BIN}
1.425	17	11_{HEX}	10001_{BIN}
1.450	18	12_{HEX}	10010_{BIN}
1.475	19	13_{HEX}	10011_{BIN}
1.500	20	14_{HEX}	10100_{BIN}
1.525	21	15_{HEX}	10101_{BIN}
1.550	22	16_{HEX}	10110_{BIN}
1.575	23	17_{HEX}	10111_{BIN}
1.600	24	18_{HEX}	11000_{BIN}
1.625	25	19_{HEX}	11001_{BIN}
1.650	26	$1A_{HEX}$	11010_{BIN}
Pass switch	≥27	≥1B	

7.3 Linear Regulators LDO3, LDO4

Table 13. Electrical Characteristics – LDO3, LDO4

V_{IN_LDO} = 1.8V, V_{OUT} = 1.2V (default), C_{IN} = 10µF, C_O = 1.0µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_LDO}	Input Voltage Range		1.0	1.8	2.0	V
V_O	Output Voltage Range		1.0	1.2	1.65	V
I_{SHDN}	Shutdown Current		–	0.5	–	µA
I_Q	Quiescent Current	No Load	–	20	–	µA
	Regulation Voltage Accuracy		-2.0	–	+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation		–	1.0	–	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation		–	19	–	µV/mA
I_O	Maximum Output Current		45	–	–	mA
I_{LIM}	Current Limit		45	–	–	mA
V_{DROP}	Dropout Voltage	I_O = 50mA	–	–	100	mV
PSRR	Power Supply Ripple Rejection	$V_{IN\_LDO} – V_O$ = 500mV, I_O = 10mA				dB
		< 200Hz	–	> 100	–	
		1kHz	–	100	–	
		10kHz	–	85	–	
		100kHz	–	55	–	
e_n	Output Noise Voltage	V_O = 1.2V, I_O = 100µA, Bandwidth = 10Hz to 100kHz	–	28	–	µVRMS
R_{DIS}	Output Discharge Resistance		–	10	–	kΩ
T_{SSR}	LDO Soft-Start Ramp Rate		–	30	–	mV/µs

Table 14. I2C Control Register – LDO3, LDO4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO3_CTL	R/W	RSVD						LDO3_SEL	LDO3_EN	00$_{HEX}$	5E$_{HEX}$
LDO4_CTL	R/W	RSVD						LDO4_SEL	LDO4_EN	00$_{HEX}$	60$_{HEX}$

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	0
D[1]	LDOx_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	LDOx_EN	Enable bit: 0 = OFF 1 = ON	0

Table 15. Selection Bit Truth Table – LDO3, LDO4

D[1]	D[0]	Sequencer Control	LDO3/4
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 16. I2C Output Voltage Setting – LDO3, LDO4

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO3_VOUT	R/W	RSVD			Output Voltage Setting (see Table 18)					OTP	16$_{HEX}$
LDO4_VOUT	R/W	RSVD			Output Voltage Setting (see Table 18)					OTP	17$_{HEX}$

Table 17. I2C Sequencing Control Register – LDO3, LDO4

Note: Green shading indicates that the register values are loaded from the OTP.

<table>
<tr><th>Register Name</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Initial Value</th><th>Address</th></tr>
<tr><td>LDO3_GRP</td><td>R/W</td><td colspan="2">RSVD</td><td colspan="2">LDO3_TYPE</td><td colspan="4">LDO3_GROUP</td><td>OTP</td><td>F0$_{HEX}$</td></tr>
<tr><td>LDO4_GRP</td><td>R/W</td><td colspan="2">RSVD</td><td colspan="2">LDO4_TYPE</td><td colspan="4">LDO4_GROUP</td><td>OTP</td><td>F1$_{HEX}$</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Name</th><th colspan="2">Function</th><th>Default</th></tr>
<tr><td>D[7:6]</td><td>RSVD</td><td colspan="2">Reserved</td><td>0</td></tr>
<tr><td>D[5:4]</td><td>LDOx_TYPE</td><td colspan="2">Rail type selection bits:
00$_{BIN}$ = “A” rail type.
01$_{BIN}$ = “U” rail type.
10$_{BIN}$ = “S” rail type.
11$_{BIN}$ = “SX” rail type</td><td>OTP</td></tr>
<tr><td rowspan="2">D[3:0]</td><td rowspan="2">LDOx_GROUP</td><td colspan="2">Group Delay Bits</td><td rowspan="2">OTP</td></tr>
<tr><td>0000$_{BIN}$ = Group 0
0001$_{BIN}$ = Group 1
0010$_{BIN}$ = Group 2
0011$_{BIN}$ = Group 3
0100$_{BIN}$ = Group 4
0101$_{BIN}$ = Group 5
0110$_{BIN}$ = Group 6
0111$_{BIN}$ = Group 7</td><td>1000$_{BIN}$ = Group 8
1001$_{BIN}$ = Group 9
1010$_{BIN}$ = Group 10
1011$_{BIN}$ = Group 11
1100$_{BIN}$ = Group 12
1101$_{BIN}$ = Group 13
1110$_{BIN}$ = Group 14
1111$_{BIN}$ = Disable</td></tr>
</table>

Table 18. LDO3, LDO4 Output Voltage Setting

V_{OUT}	Decimal	Hexadecimal	Binary
1.000	0	00$_{HEX}$	000000$_{BIN}$
1.025	1	01$_{HEX}$	000001$_{BIN}$
1.050	2	02$_{HEX}$	000010$_{BIN}$
1.075	3	03$_{HEX}$	000011$_{BIN}$
1.100	4	04$_{HEX}$	000100$_{BIN}$
1.125	5	05$_{HEX}$	000101$_{BIN}$
1.150	6	06$_{HEX}$	000110$_{BIN}$
1.175	7	07$_{HEX}$	000111$_{BIN}$
1.200	8	08$_{HEX}$	001000$_{BIN}$
1.225	9	09$_{HEX}$	001001$_{BIN}$
1.250	10	0A$_{HEX}$	001010$_{BIN}$
1.275	11	0B$_{HEX}$	001011$_{BIN}$

V_{OUT}	Decimal	Hexadecimal	Binary
1.300	12	$0C_{HEX}$	001100_{BIN}
1.325	13	$0D_{HEX}$	001101_{BIN}
1.350	14	$0E_{HEX}$	001110_{BIN}
1.375	15	$0F_{HEX}$	001111_{BIN}
1.400	16	10_{HEX}	010000_{BIN}
1.425	17	11_{HEX}	010001_{BIN}
1.450	18	12_{HEX}	010010_{BIN}
1.475	19	13_{HEX}	010011_{BIN}
1.500	20	14_{HEX}	010100_{BIN}
1.525	21	15_{HEX}	010101_{BIN}
1.550	22	16_{HEX}	010110_{BIN}
1.575	23	17_{HEX}	010111_{BIN}
1.600	24	18_{HEX}	011000_{BIN}
1.625	25	19_{HEX}	011001_{BIN}
1.650	26	$1A_{HEX}$	011010_{BIN}

7.4 Linear Regulator LDO5

LDO5 is a source-sink linear regulator capable of delivering load currents as high as ±550mA. The output voltage is designed to regulate at V_{IN_LDO5} / 2. The regulator is controlled either through the sequencing state machine or by I2C.

Table 19. Electrical Characteristics – LDO5

V_{IN_LDO5} = 1.24V, V_{OUT} = 0.620V (default). C_{IN} = 22µF, C_O = 22µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_LDO5}	Input Voltage Range		1.20	1.24	1.50	V
V_{O_LDO5}	Output Voltage		V_{IN_LDO5} / 2			V
I_{SHDN}	Shutdown Current		–	1	–	µA
I_Q	Quiescent Current	No Load	–	60	110	µA
	Regulation Voltage Accuracy	$-550mA \le I_{LOAD} \le +550mA$	-5	–	+5	%
$I_{(source)}$	Maximum Source Output Current		550	–	–	mA
$I_{(sink)}$	Maximum Sink Output Current		550	–	–	mA
R_{DIS}	Output Discharge Resistance		–	80	–	Ω

Table 20. I2C Control Register – LDO5

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO5_CTL	R/W	RSVD						LDO5_SEL	LDO5_EN	00_{HEX}	58_{HEX}

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000_{BIN}
D[1]	LDO5_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0_{BIN}
D[0]	LDO5_EN	Enable bit: 0 = OFF 1 = ON	0_{BIN}

Table 21. Selection Bit Truth Table – LDO5

D[1]	D[0]	Sequencer Control	LDO5
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 22. I2C Sequencing Control – LDO5

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO5_GRP	R/W	RSVD		LDO5_TYPE		LDO5_GROUP				OTP	$F2_{\text{HEX}}$

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00_{BIN}
D[5:4]	LDO5_TYPE	Rail type selection bits: 00_{BIN} = “A” rail type. 01_{BIN} = “U” rail type. 10_{BIN} = “S” rail type. 11_{BIN} = “SX” rail type.	OTP

Bit	Name	Function		Default
D[3:0]	LDO5_GROUP	Group Delay Bits		OTP
		0000_{BIN} = Group 0	1000_{BIN} = Group 8	
		0001_{BIN} = Group 1	1001_{BIN} = Group 9	
		0010_{BIN} = Group 2	1010_{BIN} = Group 10	
		0011_{BIN} = Group 3	1011_{BIN} = Group 11	
		0100_{BIN} = Group 4	1100_{BIN} = Group 12	
		0101_{BIN} = Group 5	1101_{BIN} = Group 13	
		0110_{BIN} = Group 6	1110_{BIN} = Group 14	
		0111_{BIN} = Group 7	1111_{BIN} = Disable	

7.5 Linear Regulator LDO6

Table 23. Electrical Characteristics – LDO6

V_{SYS} = 5.0V, V_{OUT} = 3.3V, C_O = 1µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{SYS}	Input Voltage Range		3.15	5.0	5.25	V
V_O	Output Voltage Range		1.2	3.3	3.55	V
I_{SHDN}	Shutdown Current		–	0.5	–	µA
I_Q	Quiescent Current	No Load	–	20	–	µA
	Regulation Voltage Accuracy		-2	–	+2	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation		–	1	–	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation		–	40	–	µV/mA
I_O	Maximum Output Current		100	–	–	mA
I_{LIM}	Current Limit		110	–	–	mA
V_{DROP}	Dropout Voltage	I_O = 50mA	–	–	125	mV
PSRR	Power Supply Ripple Rejection	$V_{SYS} – V_O$ = 1V, I_O = 30mA				dB
		< 200Hz	–	> 120	–	
		1kHz	–	120	–	
		10kHz	–	95	–	
		100kHz	–	57	–	
e_n	Output Noise Voltage	V_O= 3.3V, I_O = 100µA, BW = 10Hz to 100kHz	–	28	–	µVRMS
R_{DIS}	Output Discharge Resistance		–	10	–	kΩ
T_{SSR}	LDO Soft-Start Ramp Rate		–	32	–	mV/µs

Table 24. I2C Control Register – LDO6

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO6_CTL	R/W	RSVD						LDO6_SEL	LDO6_EN	00_{HEX}	$6A_{\text{HEX}}$

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000_{BIN}
D[1]	LDO6_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0_{BIN}
D[0]	LDO6_EN	Control bit: 0 = OFF 1 = ON	0_{BIN}

Table 25. Selection Bit Truth Table – LDO6

D[1]	D[0]	Sequencer Control	LDO6
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 26. I2C Output Voltage Setting – LDO6

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO6_VOUT	R/W	RSVD		Output Voltage Setting (see Table 28)						00_{HEX}	18_{HEX}

Table 27. I2C Sequencing Control – LDO6

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO6_GRP	R/W	RSVD		LDO6_TYPE		LDO6_GROUP				OTP	F3$_{\text{HEX}}$

Bit	Name	Function		Default
D[7:6]	RSVD	Reserved		00$_{\text{BIN}}$
D[5:4]	LDO6_TYPE	Rail type selection bits: 00 = “A” rail type. 01 = “U” rail type. 10 = “S” rail type. 11 = “SX” rail type.		OTP
D[3:0]	LDO6_GROUP	Group Delay Bits		OTP
		0000$_{\text{BIN}}$ = Group 0	1000$_{\text{BIN}}$ = Group 8	
		0001$_{\text{BIN}}$ = Group 1	1001$_{\text{BIN}}$ = Group 9	
		0010$_{\text{BIN}}$ = Group 2	1010$_{\text{BIN}}$ = Group 10	
		0011$_{\text{BIN}}$ = Group 3	1011$_{\text{BIN}}$ = Group 11	
		0100$_{\text{BIN}}$ = Group 4	1100$_{\text{BIN}}$ = Group 12	
		0101$_{\text{BIN}}$ = Group 5	1101$_{\text{BIN}}$ = Group 13	
		0110$_{\text{BIN}}$ = Group 6	1110$_{\text{BIN}}$ = Group 14	
		0111$_{\text{BIN}}$ = Group 7	1111$_{\text{BIN}}$ = Disable	

Table 28. LDO6 Output Voltage Setting

V$_{\text{OUT}}$	Decimal	Hexadecimal	Binary
1.00	0	00$_{\text{HEX}}$	000000$_{\text{BIN}}$
1.05	1	01$_{\text{HEX}}$	000001$_{\text{BIN}}$
1.10	2	02$_{\text{HEX}}$	000010$_{\text{BIN}}$
1.15	3	03$_{\text{HEX}}$	000011$_{\text{BIN}}$
1.20	4	04$_{\text{HEX}}$	000100$_{\text{BIN}}$
1.25	5	05$_{\text{HEX}}$	000101$_{\text{BIN}}$
1.30	6	06$_{\text{HEX}}$	000110$_{\text{BIN}}$
1.35	7	07$_{\text{HEX}}$	000111$_{\text{BIN}}$
1.40	8	08$_{\text{HEX}}$	001000$_{\text{BIN}}$
1.45	9	09$_{\text{HEX}}$	001001$_{\text{BIN}}$
1.50	10	0A$_{\text{HEX}}$	001010$_{\text{BIN}}$
1.55	11	0B$_{\text{HEX}}$	001011$_{\text{BIN}}$
1.60	12	0C$_{\text{HEX}}$	001100$_{\text{BIN}}$

V_{OUT}	Decimal	Hexadecimal	Binary
1.65	13	0D$_{HEX}$	001101$_{BIN}$
1.70	14	0E$_{HEX}$	001110$_{BIN}$
1.75	15	0F$_{HEX}$	001111$_{BIN}$
1.80	16	10$_{HEX}$	010000$_{BIN}$
1.85	17	11$_{HEX}$	010001$_{BIN}$
1.90	18	12$_{HEX}$	010010$_{BIN}$
1.95	19	13$_{HEX}$	010011$_{BIN}$
2.00	20	14$_{HEX}$	010100$_{BIN}$
2.05	21	15$_{HEX}$	010101$_{BIN}$
2.10	22	16$_{HEX}$	010110$_{BIN}$
2.15	23	17$_{HEX}$	010111$_{BIN}$
2.20	24	18$_{HEX}$	011000$_{BIN}$
2.25	25	19$_{HEX}$	011001$_{BIN}$
2.30	26	1A$_{HEX}$	011010$_{BIN}$
2.35	27	1B$_{HEX}$	011011$_{BIN}$
2.40	28	1C$_{HEX}$	011100$_{BIN}$
2.45	29	1D$_{HEX}$	011101$_{BIN}$
2.50	30	1E$_{HEX}$	011110$_{BIN}$
2.55	31	1F$_{HEX}$	011111$_{BIN}$
2.60	32	20$_{HEX}$	100000$_{BIN}$
2.65	33	21$_{HEX}$	100001$_{BIN}$
2.70	34	22$_{HEX}$	100010$_{BIN}$
2.75	35	23$_{HEX}$	100011$_{BIN}$
2.80	36	24$_{HEX}$	100100$_{BIN}$
2.85	37	25$_{HEX}$	100101$_{BIN}$
2.90	38	26$_{HEX}$	100110$_{BIN}$
2.95	39	27$_{HEX}$	100111$_{BIN}$
3.00	40	28$_{HEX}$	101000$_{BIN}$
3.05	41	29$_{HEX}$	101001$_{BIN}$
3.10	42	2A$_{HEX}$	101010$_{BIN}$
3.15	43	2B$_{HEX}$	101011$_{BIN}$
3.20	44	2C$_{HEX}$	101100$_{BIN}$
3.25	45	2D$_{HEX}$	101101$_{BIN}$
3.30	46	2E$_{HEX}$	101110$_{BIN}$

V_{OUT}	Decimal	Hexadecimal	Binary
3.35	47	$2F_{HEX}$	101111_{BIN}
3.40	48	30_{HEX}	110000_{BIN}
3.45	49	31_{HEX}	110001_{BIN}
3.50	50	32_{HEX}	110010_{BIN}
3.55	51	33_{HEX}	110011_{BIN}
3.60	52	34_{HEX}	110100_{BIN}
3.65	53	35_{HEX}	110101_{BIN}
3.70	54	36_{HEX}	110110_{BIN}
3.75	55	37_{HEX}	110111_{BIN}

7.6 Linear Regulator LDO7

LDO7 is an always-on LDO, mainly for supplying the 1.8V rated GPIO[9:0] through the VGPIO0 input, which supplies the DIF/DIO interfaces for DCD3 and DCD4, MODEM_OFF_B, SDWN_B, PWRBTN_B, and IRQ output buffers. The LDO can also be used for general purposes, as long as the total output current is limited to below 100mA.

LDO is enabled once the PMIC is enabled, and it remains enabled until the PMIC powers down to the G3 state.

Table 29. Electrical Characteristics – LDO7

V_{SYS}= 5.0V, V_{OUT} = 1.8V, C_O = 1µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_O	Output Voltage Range		–	1.8	–	V
I_{SHDN}	Shutdown Current		–	0.5	–	µA
I_Q	Quiescent Current	No Load	–	20	–	µA
	Regulation Voltage Accuracy		-2	–	+2	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation		–	1	–	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation		–	40	–	µV/mA
I_O	Maximum Output Current		100	–	–	mA
I_{LIM}	Current Limit		110	–	–	mA
V_{DROP}	Dropout Voltage	I_O = 50mA	–	–	125	mV
PSRR	Power Supply Ripple Rejection	V_{SYS} – V_O=1V, I_O = 30mA				dB
		< 200Hz	–	> 120	–	
		1kHz	–	120	–	
		10kHz	–	95	–	
		100kHz	–	57	–	

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
e_n	Output Noise Voltage	V_O= 1.8V, I_O = 100µA, Bandwidth = 10Hz to 100kHz	–	28	–	µVRMS
R_{DIS}	Output Discharge Resistance		–	10		kΩ
	LDO Soft-Start Ramp Rate		–	32	–	mV/µs

7.7 LDO Current Limit Flags

Each linear regulator has a constant current limit behavior with a non-latching over-current flag. If the regulator's output current is above the maximum output current I_O limit, the flag asserts for the duration of the over-current condition and will de-assert when the current falls below the current limit threshold.

During start up, the maximum output current from the LDO regulator is controlled by the PMIC and gradually increased. After the voltage reaches its set point, the current specified in the "Electrical Characteristics" tables could be sourced (or sinked when LDO5 is used).

Table 30. LDO Current Limit Flags

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDOF1	R	LDO7_SC	LDO6_SC	LDO5_SC	LDO4_SC	LDO3_SC	LDO2_SC	LDO1_SC	LDO0_SC	00_{HEX}	$9D_{HEX}$

7.8 Switching Regulators for SoC Core, Graphics, and Memory Rails

DCD0, DCD1, and DCD2 are high-efficiency, synchronous step-down switching regulators capable of delivering up to 5A of peak current.

The output voltage (or boot voltage) can be individually set by OTP. It can be changed from the default setting either via I2C or SVID. The regulators support Dynamic Voltage Scaling (DVS) allowing on-the-fly, slew-rate controlled changes to the output voltage.

The regulators operate with a fixed 2.0MHz oscillator frequency allowing the use of small external components, minimizing cost and real estate. To maximize efficiency under varying load conditions, the regulators offer selectable modes of operation via I2C. Available modes are Forced PWM (FPWM) and Auto-Mode PWM/PFM. Auto-Mode PWM/PFM is selected by default and allows the regulator to switch automatically between PWM and PFM Mode, depending on the load condition. During heavy load, the regulator operates in PWM Mode at a fixed frequency. As the load decreases and the inductor valley current reaches zero, it automatically transitions into PFM Mode maintaining high efficiency under light load conditions. For noise-sensitive applications, the regulator can be forced into PWM Mode by disabling the Auto-Mode PWM/PFM.

The on/off control of the regulators can be accessed either through I2C or by toggling the appropriate SLP_Sx_B pins. Other features of the regulators include over-voltage protection, soft-start, and soft-start done flags.

The regulators include an active discharge circuitry to discharge the output capacitor and hold the output voltage at ground after the regulator has turned off.

SVID is the default interface for changing the output voltage setting. For applications not requiring SVID, the SVID interface can be deselected by OTP or via I2C.

The regulators are capable of supporting load currents greater than 5A by connecting additional phases (P9148) to the DIF interface. Each individual P9148 can deliver peak currents of up to 5A with up to four phases in parallel. The communication link between the converter and the P9148 is established by connecting the DCDx_DIF and DCDx_DIO pins to the corresponding pins of the P9148. The DIF and DIO interface is running IDT's proprietary communication protocol and controls the attached P9148. If additional phases are not required, the DIO and DIF pins can be used as regular GPIO pins or can be left floating. (Consult the P9148 datasheet for electrical characteristics and the product description.)

The power sequencing of each regulator can be changed by OTP trim. Contact IDT to change the timing and the power rail type.

7.9 Switching Regulator DCD0, DCD1

Table 31. Electrical Characteristics – DCD0, DCD1

V_{IN_DCD} = 5.0V, V_O = 1.0V (default), L = 0.47µH, C_{IN_DCD} = 10µF, C_O = 282µF; no DPU (P9148). T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_DCD}	Input Voltage Range		2.7	5.0	5.25	V
V_O	Output Voltage Range	SVID enabled	0.250	1.000	1.295	V
		SVID disabled	1.100	–	1.890	V
	Regulation Voltage Accuracy (Set Point Accuracy)	V_O = 0.7 to 1.295V	-2.0	–	+2.0	%
$R_{LL(DC)}$	DC Load Line		–	6	–	mΩ
$R_{LL(AC)}$	AC Load Line		–	10	–	mΩ
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN_DCD} = 2.75V to 5.25V	–	0.03	–	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5A to 4A, PWM Mode, load line disabled	–	0.3	–	mV/A
V_{OFFSET}	Offset Voltage in PFM Mode; $V_{O(PFM)} = V_{O(PWM)} + V_{OFFSET}$	PFM Mode	–	15	–	mV
I_O	Continuous Operating DC Current	T_J < 115°C, GBD	4.0	–	–	A
I_{PULSE}	Pulsed Load Current	t_{Load} < 1ms.	–	5.0	–	A
$I_{SHD(VIN\_DCD)}$	Shutdown Current	Regulator disabled	–	1.0	–	µA
I_{VIN_DCD}	Power Stage Supply Current	Forced PWM Mode, no load	–	300	–	µA
		Forced PFM Mode, no switching	–	200	–	µA
$R_{(DSON)}$	High-Side Switch On Resistance	$V_{SYS} = V_{IN\_DCD}$ = 5V, I_{OUT} = 500mA	–	48	80	mΩ
	Low-Side Switch On Resistance	$V_{SYS} = V_{IN\_DCD}$ = 5V, I_{OUT} = 500mA	–	28	80	mΩ
R_{DIS}	Output Discharge Resistance		–	280	450	Ω
f_{SW}	Switching Frequency	PWM Mode, GBD	1.8	2.0	2.2	MHz
$t_{ON(MIN)}$	Minimum On-Time		–	70	–	ns
t_{DCDSSR}	DCD Soft-Start Ramp Rate	15% to 90% of V_O	–	2.5	–	mV/µs
ΔG_{SEN}	G_{SEN} Pin Differential Voltage Range		–	250	–	mV
Z_{SEN}	G_{SEN} Pin Input Impedance		–	1	–	MΩ

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{FB}	FB Input Bias Current		–	–	10	µA
V_{OVP} [a]	Over-Voltage Protection Threshold	SVID enabled	–	1.8	–	V
		SVID disabled	–	2.4	–	V
	Over-Voltage Protection Threshold Tolerance	GBD	-5.0	–	+5.0	%

[a] An over-voltage fault response is to shut down the PMIC.

Table 32. VBOOT Register – DCD0, DCD1

Note: Green shading indicates that the register values are loaded from the OTP.

Note: At start-up, if VBOOT[7:1] = 00_{HEX}, then VBOOT[0] = 0; otherwise VBOOT[0] = 1.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_VBOOT	R/W	VBOOT[7:1]							VBOOT[0]	OTP	BC_{HEX}
DCD1_VBOOT	R/W	VBOOT[7:1]							VBOOT[0]	OTP	CC_{HEX}

Bit	Name	Function	Default
D[7:0]	DCDx_VBOOT	VBOOT (refer to Table 46 and Table 47). Note: At start-up, if VBOOT[7:1] = 0, then VBOOT[0] = 0; otherwise VBOOT[0] = 1. If VBOOT[7:1] ≠ 0, then VBOOT[0] together with VBOOT[7:1] will follow the SVID command voltage setting.	OTP

Table 33. VID Register – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_VID	R/W	VID[7:0]								00_{HEX}	BE_{HEX}
DCD1_VID	R/W	VID[7:0]								00_{HEX}	CE_{HEX}

Bit	Name	Function	Default
D[7:0]	VID CODE	VID (refer to Table 46 and Table 47)	00_{HEX}

Table 34. I2C Control Register – DCD0, DCD1

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_CTL	R/W	RSVD			SVID	RSVD		DCD0_SEL	DCD0_EN	OTP	53_{HEX}
DCD1_CTL	R/W	RSVD			SVID	RSVD		DCD1_SEL	DCD1_EN	OTP	54_{HEX}

Bit	Name	Function	Default
D[7:5]	RSVD	Reserved	000_{BIN}
D[4]	SVID	SVID ON/OFF selection bit: 0 = SVID disabled. 1 = SVID enabled.	OTP
D[3:2]	RSVD	Reserved	00_{BIN}
D[1]	DCDx_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0_{BIN}
D[0]	DCDx_EN	Enable bit: 0 = OFF 1 = ON	0_{BIN}

Table 35. On/Off Selection Bit Table – DCD0, DCD1

D[1]	D[0]	Sequencer Control	DCD0
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 36. I2C Output Voltage Register – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_SLEW	R/W	RSVD		Fast_Rate		RSVD		Slow_Rate		01_{HEX}	$A8_{HEX}$
DCD1_SLEW	R/W	RSVD		Fast_Rate		RSVD		Slow_Rate		01_{HEX}	$A9_{HEX}$

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00_{BIN}
D[5:4]	Fast_Rate	SetVID fast output voltage slew rate: 00 = 10mV/µs 10 = 40mV/µs 01 = 20mV/µs 11 = Reserved	00_{BIN}
D[3:1]	RSVD	Reserved	0_{BIN}
D[0]	Slow_Rate	SetVID slow output voltage slew rate: 0 = 2.5mV/µs 1 = 5mV/µs	1_{BIN}

Table 37. I2C Sequencing Control – DCD0, DCD1

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_GRP	R/W	RSVD		DCD0_TYPE		DCD0_GROUP				OTP	$E6_{HEX}$
DCD1_GRP	R/W	RSVD		DCD1_TYPE		DCD1_GROUP				OTP	$E7_{HEX}$

Bit	Name	Function		Default
D[7:6]	RSVD	Reserved		00_{BIN}
D[5:4]	DCDx_TYPE	Rail type selection bits: 00_{BIN} = “A” rail type. 01_{BIN} = “U” rail type. 10_{BIN} = “S” rail type. 11_{BIN} = “SX” rail type.		OTP
D[3:0]	DCDx_GROUP	Group Delay Bits		OTP
		0000_{BIN} = Group 0 0001_{BIN} = Group 1 0010_{BIN} = Group 2 0011_{BIN} = Group 3 0100_{BIN} = Group 4 0101_{BIN} = Group 5 0110_{BIN} = Group 6 0111_{BIN} = Group 7	1000_{BIN} = Group 8 1001_{BIN} = Group 9 1010_{BIN} = Group 10 1011_{BIN} = Group 11 1100_{BIN} = Group 12 1101_{BIN} = Group 13 1110_{BIN} = Group 14 1111_{BIN} = Disable	

Table 38. I2C Core-Type Exit Control – DCD0, DCD1

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
CORE_TYPE_EXIT	R/W	RSVD						DCD1_TYPE_EXIT	DCD0_TYPE_EXIT	00_{HEX}	10_{HEX}

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000_{BIN}
D[1]	DCD1_TYPE_EXIT	0 = Exit sequence disabled. DCD1 follows I2C Sequencing Control for DCD1 in register $E7_{HEX}$. 1 = Exit sequence enabled. DCD1 is powered on as an “A” rail type (DCD1_TYPE = 00_{BIN}) with the group delay set by DCD1_GRP[3:0]. It maintains an “A” Type (type 00_{BIN}) until RSMRST_B and PLTRST_B are both asserted. Once assertion of both signals is detected, the DCD_TYPE is changed to DCD1_TYPE[5:4], which is programmable via OTP. DCD1_TYPE[5:4] is then used for enabling and disabling DCD1 until the system is reset.	0_{BIN}
D[0]	DCD0_TYPE_EXIT	0 = Exit sequence disabled. DCD0 follows I2C Sequencing Control for DCD0 in register $E6_{HEX}$. 1 = Exit sequence enabled. DCD0 is powered on as an “A” rail type (DCD0_TYPE = 00_{BIN}) with the group delay set by DCD0_GRP[3:0]. It maintains an “A” Type (Type 00_{BIN}) until RSMRST_B and PLTRST_B are both asserted. Once assertion of both signals is detected, the DCD_TYPE is changed to DCD0_TYPE[5:4], which is programmable via OTP. DCD0_TYPE[5:4] is then used for enabling and disabling of DCD0 until the system is reset.	0_{BIN}

7.10 Switching Regulator DCD2

Table 39. Electrical Characteristics – DCD2

V_{IN_DCD} = 5.0V, V_O = 1.8V (default), L = 0.47µH, C_{IN_DCD} = 10µF, C_O = 141µF; no DPU (P9148). T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_DCD}	Input Voltage Range		2.7	5.0	5.25	V
V_O	Output Voltage Range	SVID enabled	0.250	1.000	1.295	V
		SVID disabled	1.100	–	1.890	V
	Regulation Voltage Accuracy (Set Point Accuracy)	$V_O \geq 0.7V$	-2.0	–	+2.0	%
$R_{LL(DC)}$	DC Load Line		–	6	–	mΩ
$R_{LL(AC)}$	AC Load Line		–	10	–	mΩ
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation	V_{IN_DCD} = 2.75V to 5.25V	–	0.03	–	%/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5A to 4A, PWM Mode, load line disabled	–	0.3	–	mV/A
V_{OFFSET}	Offset Voltage in PFM Mode $V_{O(PFM)} = V_{O(PWM)} + V_{OFFSET}$	PFM Mode	–	15	–	mV
I_O	Continuous Operating DC Current	T_J < 115°C, GBD	4.0	–	–	A

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{PULSE}	Pulsed Load Current	t_{Load} < 1ms	–	5.0	–	A
$I_{SHD(VIN\_DCD)}$	Shutdown Current	Regulator disabled	–	1.0	–	µA
I_{VIN_DCD}	Power Stage Supply Current	Forced PWM Mode, no load	–	300	–	µA
		Forced PFM Mode, no switching	–	200	–	µA
$R_{(DSON)}$	High-Side Switch On Resistance	$V_{SYS} = V_{IN\_DCD} = 5V$, I_{OUT} = 500mA	–	50	80	mΩ
	Low-Side Switch On Resistance	$V_{SYS} = V_{IN\_DCD} = 5V$, I_{OUT} = 500mA	–	48	80	mΩ
R_{DIS}	Output Discharge Resistance		–	280	450	Ω
f_{SW}	Switching Frequency	PWM Mode, GBD	1.8	2.0	2.2	MHz
$t_{ON(MIN)}$	Minimum On-Time		–	70	–	ns
t_{DCDSSR}	DCD Soft-Start Ramp Rate	15% to 90% of V_O	–	3.5	–	mV/µs
I_{FB}	FB Input Bias Current		–	–	10	µA

Table 40. VBOOT Register – DCD2

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_VBOOT	R/W	VBOOT[7:1]							VBOOT[0]	OTP	DC_{HEX}

Bit	Name	Function	Default
D[7:0]	DCD2_VBOOT	VBOOT (refer to Table 46 and Table 47) Note: At start-up, if VBOOT[7:1] = 0, then VBOOT[0] = 0; otherwise VBOOT[0] = 1. If VBOOT[7:1] ≠ 0, then VBOOT[0] together with VBOOT[7:1] will follow the SVID command voltage setting.	OTP

Table 41. VID Register – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_VID	R/W	VID[7:0]								00_{HEX}	DE_{HEX}

Bit	Name	Function	Default
D[7:0]	DCD2_VID	VID (refer to Table 46 and Table 47)	00_{HEX}

Table 42. I2C Control Register – DCD2

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_CTL	R/W	RSVD			SVID	RSVD		DCD2_SEL	DCD2_EN	00_{HEX}	$5F_{HEX}$

Bit	Name	Function	Default
D[7:5]	RSVD	Reserved	000_{BIN}
D[4]	SVID	SVID ON/OFF selection bit: 0 = SVID disabled. 1 = SVID enabled.	0_{BIN}
D[3:2]	RSVD	Reserved	00_{BIN}
D[1]	DCD2_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by the configured device sequence. 1 = ON/OFF is controlled by the D[0] register.	0_{BIN}
D[0]	DCD2_EN	Enable bit: 0 = OFF 1 = ON	0_{BIN}

Table 43. On/Off Selection Bit Table – DCD2

D[1]	D[0]	Sequencer Control	DCD2
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 44. I2C Output Voltage Register – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_SLEW	R/W	RSVD		Fast_Rate		RSVD			Slow_Rate	01_{HEX}	AA_{HEX}

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00_{BIN}
D[5:4]	Fast_Rate	Fast output voltage slew rate: 00 = 10mV/µs 10 = 40mV/µs 01 = 20mV/µs 11 = Reserved	00_{BIN}
D[3:1]	RSVD	Reserved	000_{BIN}
D[0]	Slow_Rate	Slow output voltage slew rate: 0 = 2.5mV/µs 1 = 5mV/µs	1

Table 45. I2C Sequencing Control – DCD2

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_GRP	R/W	RSVD		🟩 DCD2_TYPE		🟩 DCD2_GROUP				OTP	$E8_{HEX}$

Bit	Name	Function		Default
D[7:6]	RSVD	Reserved		00_{BIN}
D[5:4]	DCD2_TYPE	Rail type selection bits: 00_{BIN} = “A” rail type. 01_{BIN} = “U” rail type. 10_{BIN} = “S” rail type. 11_{BIN} = “SX” rail type.		OTP
D[3:0]	DCD2_GROUP	Group Delay Bits		OTP
		0000_{BIN} = Group 0	1000_{BIN} = Group 8	
		0001_{BIN} = Group 1	1001_{BIN} = Group 9	
		0010_{BIN} = Group 2	1010_{BIN} = Group 10	
		0011_{BIN} = Group 3	1011_{BIN} = Group 11	
		0100_{BIN} = Group 4	1100_{BIN} = Group 12	
		0101_{BIN} = Group 5	1101_{BIN} = Group 13	
		0110_{BIN} = Group 6	1110_{BIN} = Group 14	
		0111_{BIN} = Group 7	1111_{BIN} = Disable	

Table 46. Output Voltage Settings – DCD0/DCD1/DCD2, SVID Enabled

D7	D6	D5	D4	D3	D2	D1	D0	Hexadecimal	Voltage
0	0	0	0	0	0	0	0	00_{HEX}	OFF / 0.250[a]
0	0	0	0	0	0	0	1	01_{HEX}	0.250
0	0	0	0	0	0	1	0	02_{HEX}	0.255
0	0	0	0	0	0	1	1	03_{HEX}	0.260
…									
1	1	0	1	0	0	0	0	$D0_{HEX}$	1.285
1	1	0	1	0	0	0	1	$D1_{HEX}$	1.290
1	1	0	1	0	0	1	0	$D2_{HEX}$	1.295[b]
1	1	0	1	0	0	1	1	$D3_{HEX}$	1.300[b]

[a] If bit[1] = 1 in register $7B_{HEX}$ (see Table 97), then the voltage is OFF; if bit[1] = 0, then the voltage is 0.250V. Register $7B_{HEX}$ (VSLEEP) can be configured in OTP.

[b] Maximum default = 1.295V. To allow VID code $D3_{HEX}$ (1.30V), the *Vout max* register must be adjusted accordingly (see Table 121).

Table 47. Output Voltage Settings – DCD0/DCD1/DCD2, SVID Disabled

D7	D6	D5	D4	D3	D2	D1	D0	Hexadecimal	Voltage
0	0	1	1	0	0	1	1	33_{HEX}	1.100
0	0	1	1	0	1	0	0	34_{HEX}	1.105
0	0	1	1	0	1	0	1	35_{HEX}	1.110
…									
1	1	0	1	0	0	0	0	$D0_{HEX}$	1.885
1	1	0	1	0	0	0	1	$D1_{HEX}$	1.890
1	1	0	1	0	0	1	0	$D2_{HEX}$	1.895
1	1	0	1	0	0	1	1	$D3_{HEX}$	1.900

7.11 Controllers DCD3, DCD4

DCD3 and DCD4 are step-down controllers and require at least one DPU (P9148) connected to the DIF bus. The regulators have no power stage in the PMIC. The PMIC provides only the control and analog circuitry for the regulators and relies on the external DPU to provide power to the load.

The output voltage is factory set to a default value, but it can be changed from the default setting via I2C. (See Table 53 for available voltages.)

The regulators operate with a fixed 2MHz oscillator frequency allowing the use of small external components, minimizing cost and real estate. The mode of operation supported by DCD3/4 is Forced PWM (FPWM) with a maximum output voltage of 3.6V. If power saving is needed, it is recommended to configure the rails for sleep mode (SLP_) or disabling. The on/off control of DCD3 and DCD4 can be accessed through I2C or it will be managed by the programmed sequence.

The controllers must be used in conjunction with P9148s. The communication link between the P91E0 and P9148 is established by connecting the DCD3_DIF/DCD4_DIF and DCD3_DIO/DCD4_DIO pins to the corresponding pins of the P9148. For each additional phase, the P9148 can deliver peak currents of 5A supporting up to four phases connected in parallel. If the regulators are not used, the DIO and DIF pins can be left floating. (Consult the P9148 datasheet for electrical characteristics and product description.)

Table 48. Electrical Characteristics – DCD3, DCD4

V_{SYS} = 5.0V, V_O = 3.3V_{DCD3}, V_O = 1.8V_{DCD4} (default), T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Note: DCD3, DCD4 must be used in conjunction with the P9148.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_O	Output Voltage Range		0.525	–	3.6	V
	Regulation Voltage Accuracy (set point accuracy)	For factory programmed V_O, test mode	–2.0	–	+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN_P9148} = 4.5V to 8.4V	–	0.03	–	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5A to 4A, PWM Mode	–	0.3	–	mV/A
	Offset Voltage in PFM Mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM Mode	–	15	–	mV
F_{SW}	Switching Frequency	PWM Mode, GBD	1.8	2.0	2.2	MHz
t_{DCDSSR}	DCD Soft-Start Ramp Rate	15% to 90% of V_O	–	2.5	–	mV/µs
I_{FB}	Feedback Input Bias Current	GBD	–	–	9	µA

Table 49. I2C Control Register – DCD3, DCD4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD3_CTL	R/W	RSVD						DCD3_SEL	DCD3_EN	00_{HEX}	67_{HEX}
DCD4_CTL	R/W	RSVD						DCD4_SEL	DCD4_EN	00_{HEX}	$5A_{HEX}$

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000_{BIN}
D[1]	DCDx_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by the D[0] bit of this register.	0
D[0]	DCDx_EN	Enable bit: 0 = OFF 1 = ON	0

Table 50. On/Off Selection Bit Table – DCD[3/4]

D[1]	D[0]	Sequencer Control	DCD[3/4]
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 51. I2C Output Voltage Setting – DCD3, DCD4

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD3_VOUT	R/W	DCD3_RNG		DCD3_VOUT						OTP	$A4_{HEX}$
DCD4_VOUT	R/W	DCD4_RNG		DCD4_VOUT						OTP	$A5_{HEX}$

Bit	Name	Function	Default
D[7:6]	DCDx_RNG	Output voltage range selection bits: 00_{BIN} = 0.5250 to 1.3125 increment of 12.5mV. 01_{BIN} = 1.2875 to 2.0750 increment of 12.5mV. 10_{BIN} = 2.0500 to 2.8375 increment of 12.5mV. 11_{BIN} = 2.8125 to 3.6000 increment of 12.5mV.	OTP
D[5:0]	DCDx_VOUT	DCD3, DCD4 output voltage setting (see Table 53).	OTP

Table 52. I2C Sequencing Control – DCD3, DCD4

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD3_GRP	R/W	RSVD		DCD3_TYPE		DCD3_GROUP				OTP	$E9_{\text{HEX}}$
DCD4_GRP	R/W	RSVD		DCD4_TYPE		DCD4_GROUP				OTP	EA_{HEX}

Bit	Name	Function		Default
D[7:6]	RSVD	Reserved		00_{BIN}
D[5:4]	DCDx_TYPE	Rail type selection bits: 00_{BIN} = “A” rail type. 01_{BIN} = “U” rail type. 10_{BIN} = “S” rail type. 11_{BIN} = “SX” rail type.		OTP
D[3:0]	DCDx_GROUP	Group Delay Bits		OTP
		0000_{BIN} = Group 0 0001_{BIN} = Group 1 0010_{BIN} = Group 2 0011_{BIN} = Group 3 0100_{BIN} = Group 4 0101_{BIN} = Group 5 0110_{BIN} = Group 6 0111_{BIN} = Group 7	1000_{BIN} = Group 8 1001_{BIN} = Group 9 1010_{BIN} = Group 10 1011_{BIN} = Group 11 1100_{BIN} = Group 12 1101_{BIN} = Group 13 1110_{BIN} = Group 14 1111_{BIN} = Disable	

Table 53. Output Voltage Setting – DCD3, DCD4

Range [00]	Range [01]	Range [10]	Range [11]	Decimal	Hexadecimal	Binary
0.5250	1.2875	2.0500	2.8125	0	00_{HEX}	000000_{BIN}
0.5375	1.3000	2.0625	2.8250	1	01_{HEX}	000001_{BIN}
0.5500	1.3125	2.0750	2.8375	2	02_{HEX}	000010_{BIN}
…						
1.2875	2.0500	2.8125	3.5750	61	$3D_{\text{HEX}}$	111101_{BIN}
1.3000	2.0625	2.8250	3.5875	62	$3E_{\text{HEX}}$	111110_{BIN}
1.3125	2.0750	2.8375	3.6000	63	$3F_{\text{HEX}}$	111111_{BIN}

7.12 Switching Regulator DCD5, DCD6

DCD5 and DCD6 are high efficiency, synchronous step-down switching regulators capable of delivering up to 2.3A of current.

The regulators operate with a fixed 2.0MHz oscillator frequency allowing the use of small external components, minimizing cost and real estate. To maximize efficiency under varying load conditions, the converter offers selectable modes of operation via I2C. Available modes are Forced PWM (FPWM) and Auto-Mode PWM/PFM. When Auto-Mode PWM/PFM is selected, the regulator switches automatically between PWM and PFM Mode, depending on the load condition. During heavy load conditions, the regulator operates in PWM Mode at a fixed frequency. As the load decreases and the inductor valley current reaches zero, it automatically transitions into PFM Mode maintaining high efficiency under light load conditions. For noise-sensitive applications, the regulator can be forced into PWM Mode by disabling the power-saving PFM Mode. The default mode is set to Auto-Mode PWM/PFM.

The on/off control of DCD5 and DCD6 can be accessed either via I2C, or it will be managed by the programmed sequence.

The regulator includes an active discharge circuitry to discharge the output capacitor and hold the output voltage at ground after the regulator powers off.

Table 54. Electrical Characteristics – DCD5, DCD6

Conditions unless otherwise specified: $V_{IN\_DCD} = 5.0V$, $V_O = 1.05V$ (default), $L = 1.0\mu H$, $C_{IN\_DCD} = 10\mu F$, $C_O = 94\mu F$. $T_J = -40°C$ to $+125°C$, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_DCD}	Input Voltage Range	$V_O < 1.8V$ for $V_{IN\_DCD} < 3.0V$ $V_O > 0.6V$ for $V_{IN\_DCD} > 5.0V$	2.70	5.0	5.25	V
V_O	Output Voltage Range		0.525	1.05	3.3375	V
	Regulation Voltage Accuracy	For factory programmed V_O	-2.0	–	+2.0	%
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation	$V_{IN\_DCD} = 2.75V$ to $5V$	–	0.03	–	%/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	$I_{OUT} = 0.5$ to $2A$, PWM Mode	–	0.3	–	mV/A
	Offset Voltage in PFM Mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM Mode	–	15	–	mV
I_O	Maximum Output Current	GBD	2.0	–	–	A
I_{PULSE}	Pulsed Load Current	$t_{Load} < 1ms$	–	2.3	–	A
I_{SHD}	Shutdown Current		–	1.0	–	µA
I_{VIN_DCD}	Power Stage Supply Current	Forced PWM Mode, no load	–	150	–	µA
		Forced PFM Mode, no switching	–	65	–	µA
$R_{(DSON)}$	High Side Switch	$V_{SYS} = V_{IN\_DCD} = 5V$; $I_{OUT} = 100mA$	–	110	160	mΩ
	Low Side Switch	$V_{SYS} = V_{IN\_DCD} = 5V$; $I_{OUT} = 100mA$	–	57	85	mΩ
R_{DIS}	Output Discharge Resistance		–	850	1100	Ω
f_{SW}	Switching Frequency	PWM Mode, GBD	1.8	2.0	2.2	MHz
$t_{ON(MIN)}$	Minimum On-Time		–	70	–	ns
t_{DCDSSR}	DCD Soft-Start Ramp Rate	15% to 90% of V_O	–	2.5	–	mV/µs
I_{FB}	Feedback Input Bias Current for DCD5 and DCD6.		–	2.0	–	µA

Table 55. DCD5, DCD6 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD5_CTL	R/W	RSVD						DCD5_SEL	DCD5_EN	00_{HEX}	59_{HEX}
DCD6_CTL	R/W	RSVD						DCD6_SEL	DCD6_EN	00_{HEX}	55_{HEX}

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000_{BIN}
D[1]	DCDx_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by the D[0] bit of this register.	0_{BIN}
D[0]	DCDx_EN	Enable bit: 0 = OFF 1 = ON	0_{BIN}

Table 56. On/Off Selection Bit Table

D[1]	D[0]	Sequencer Control	DCDx
0	X	SLP_x signal LOW	OFF
0	X	SLP_x signal HIGH	ON
1	0	X	OFF
1	1	X	ON

Table 57. I2C Output Voltage Setting

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD5_VOUT	R/W	DCD5_RNG		DCD5_VOUT						OTP	$A6_{\text{HEX}}$
DCD6_VOUT	R/W	DCD6_RNG		DCD6_VOUT						OTP	$A7_{\text{HEX}}$

Bit	Name	Function	Default
D[7:6]	DCDx_RNG	Output voltage range selection bits: 00_{BIN} = 0.5250 to 1.3125 increment of 12.5mV [default]. 01_{BIN} = 1.2000 to 1.9875 increment of 12.5mV. 10_{BIN} = 1.8750 to 2.6625 increment of 12.5mV. 11_{BIN} = 2.5500 to 3.3375 increment of 12.5mV.	OTP
D[5:0]	DCDx_VOUT	Output voltage setting (see Table 58).	OTP

Table 58. Output Voltage Setting – DCD5, DCD6

Range [00]	Range [01]	Range [10]	Range [11]	Decimal	Hexadecimal	Binary
0.5250	1.2000	1.8750	2.5500	0	00$_{\text{HEX}}$	000000$_{\text{BIN}}$
0.5375	1.2125	1.8875	2.5625	1	01$_{\text{HEX}}$	000001$_{\text{BIN}}$
0.5500	1.2250	1.9000	2.5750	2	02$_{\text{HEX}}$	000010$_{\text{BIN}}$
...						
1.2875	1.9625	2.6375	3.3125	61	3D$_{\text{HEX}}$	111101$_{\text{BIN}}$
1.3000	1.9750	2.6500	3.3250	62	3E$_{\text{HEX}}$	111110$_{\text{BIN}}$
1.3125	1.9875	2.6625	3.3375	63	3F$_{\text{HEX}}$	111111$_{\text{BIN}}$

Table 59. I2C Sequencing Control – DCD5, DCD6

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD5_GRP	R/W	RSVD		DCD5_TYPE		DCD5_GROUP				OTP	EB$_{\text{HEX}}$
DCD6_GRP	R/W	RSVD		DCD6_TYPE		DCD6_GROUP				OTP	EC$_{\text{HEX}}$

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00$_{\text{BIN}}$
D[5:4]	DCDx_TYPE	Rail type selection bits: 00$_{\text{BIN}}$ = “A” rail type. 01$_{\text{BIN}}$ = “U” rail type. 10$_{\text{BIN}}$ = “S” rail type. 11$_{\text{BIN}}$ = “SX” rail type.	OTP
D[3:0]	DCDx_GROUP	Group Delay Bits 0000$_{\text{BIN}}$ = Group 0 0001$_{\text{BIN}}$ = Group 1 0010$_{\text{BIN}}$ = Group 2 0011$_{\text{BIN}}$ = Group 3 0100$_{\text{BIN}}$ = Group 4 0101$_{\text{BIN}}$ = Group 5 0110$_{\text{BIN}}$ = Group 6 0111$_{\text{BIN}}$ = Group 7 1000$_{\text{BIN}}$ = Group 8 1001$_{\text{BIN}}$ = Group 9 1010$_{\text{BIN}}$ = Group 10 1011$_{\text{BIN}}$ = Group 11 1100$_{\text{BIN}}$ = Group 12 1101$_{\text{BIN}}$ = Group 13 1110$_{\text{BIN}}$ = Group 14 1111$_{\text{BIN}}$ = Disable	OTP

7.13 General Registers for DCDs

7.13.1 Forcing PWM Mode for DCDx

DCDs regulators and controllers can be independently forced into the PWM Mode (FPWM Mode) by setting the corresponding bit of the *FPWM* register (AD$_{\text{HEX}}$; see Table 60) to 1 via I2C communication. Note that in OTP, whichever settings are written to the *FPWM* register's bits D[3] (sets the mode for the DCD3 regulator) and D[5] (sets DCD5) are automatically replicated in D[4] (sets DCD4) and D[6] (sets DCD6) respectively; however, each setting can be changed independently via I2C after the OTP is loaded. Refer to section 7.11 for modes of operation supported by DCD3 and DCD4.

Table 60. Forced PWM Register – DCD0 through DCD6

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
FPWM	R/W	RSVD	DCD6_FPWM[a]	DCD5_FPWM	DCD4_FPWM[b]	DCD3_FPWM	DCD2_FPWM	DCD1 FPWM	DCD0_FPWM	OTP	AD$_{\text{HEX}}$

[a] This bit is loaded from OTP with the same value as bit DCD5_ FPWM. Then it can be changed via I2C to a different value.

[b] This bit is loaded from OTP with the same value as bit DCD3_ FPWM. Then it can be changed via I2C to a different value.

Bit	Name	Function	Default
D[7]	RSVD	Reserved	0$_{\text{BIN}}$
D[6:0]	DCDx_FPWM	Selection bits for Auto PFM/PWM Mode or FPWM Mode: 0 = Auto PFM/PWM. 1 = FPWM.	OTP

7.13.2 DC Load-Line Control

Table 61. DC Load-Line Control

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCLL_CTL	R/W	RSVD					DCLL_2	DCLL_1	DCLL_0	03$_{\text{HEX}}$	1F$_{\text{HEX}}$

Bit	Name	Function	Default
D[7:3]	RSVD	Reserved	00000$_{\text{BIN}}$
D[2:0]	DCLL_[X]	0 = Disable DC load line for DCD[X]. 1 = Enable DC load line for DCD[X].	011$_{\text{BIN}}$

7.13.3 AC Load-Line Control

Table 62. AC Load-Line Control

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
ACLL_CTL	R/W	RSVD					ACLL_DCD2	ACLL_DCD1	ACLL_DCD0	03_{HEX}	25_{HEX}

Bit	Name	Function	Default
D[7:3]	RSVD	Reserved	00000_{BIN}
D[2:0]	ACLL_x	0 = Disable AC load line for DCD[X] 1 = Enable AC load line for DCD[X]	011_{BIN}

7.13.4 DCD Rail Select for DRAMPWROK Monitor

Table 63. DCD Rail Select for DRAMPWROK Monitor

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DRAMPWROK	R/W	RSVD					DCD_SEL[2:0]			02_{HEX}	$7C_{HEX}$

Bit	Name	Function	Default
D[7:3]	RSVD	Reserved	00000_{BIN}
D[2:0]	DCD_SEL[2:0]	Select DCD rail for which DRAMPWROK monitors the voltage: 000 = DCD0 001 = DCD1 010 = DCD2 011 = DCD3 100 = DCD4 101 = DCD5 110 = DCD6 111 = OFF; DRAMPWROK always stays LOW	010_{BIN}

7.13.5 DCDx Internal Soft-Start Complete Status

Table 64. DCD Internal Soft-Start Complete Status

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD_PG	R	RSVD	DCD6_PG	DCD5_PG	DCD4_PG	DCD3_PG	DCD2_PG	DCD1_PG	DCD0_PG	00_{HEX}	$8F_{HEX}$

Bit	Name	Function	Default
D[7]	RSVD	Reserved	0
D[6:0]	DCD[X]_PG	0 = Internal soft-start of DCD[x] has not been completed or DCD[x] is disabled. 1 = Internal soft-start of DCD[x] is complete.	0000000_{BIN}

7.13.6 DPS_IDLE_CFG Operation

To decrease power consumption in light current load conditions, operate in the Auto PFM/PWM Mode (Idle Mode). For example, to set DCD2 in Auto PFM/PWM Mode, with or without DPUs connected, set bit[2] = 1_{BIN} in the *DPS_IDLE_CFG* register ($7A_{HEX}$), and set bit [2] =0 $_{BIN}$ in the *FPWM* register (AD_{HEX}); see tables below.

To control the switching noise at a single frequency, operate in the Forced PWM Mode (FPWM). For example, for DCD2 with or without DPUs connected, set bit[2] = 1_{BIN} in the *FPWM* register; see tables below.

Table 65. DPS_IDLE_CFG Operation with DPU

DCD[X]_FPWM Bit in *FPWM* Register (AD_{HEX})	EN_PS_IDLEx Bit in *DPS_IDLE_CFG* Register ($7A_{HEX}$)	
	0_{BIN} = Idle Mode Disable (FPWM Mode)	1_{BIN} = Idle Mode Enable (Auto PFM/PWM Mode)
0_{BIN} = Auto PFM/PWM Mode	FPWM	Auto PFM/PWM
1_{BIN} = FPWM Mode	FPWM	FPWM

Table 66. DPS_IDLE_CFG Operation with No DPU

DCD[X]_FPWM Bit in *FPWM* Register (AD_{HEX})	EN_PS_IDLEx Bit in *DPS_IDLE_CFG* Register ($7A_{HEX}$)	
	0_{BIN} = Idle Mode Disable (FPWM Mode)	1_{BIN} = Idle Mode Enable (Auto PFM/PWM Mode)
0_{BIN} = Auto PFM/PWM Mode	Auto PFM/PWM	Auto PFM/PWM
1_{BIN} = FPWM Mode	FPWM	FPWM

When phase shedding is enabled/disabled, the tables below explain the operation of DCD regulator. See Table 71, Table 72, and Table 73 for phase shedding settings.

Table 67. Disable Phase Shedding – Example for DCD2: DPS2_CONFIG Register ($1B_{HEX}$) Bits[1:0] = 11_{BIN}

DCD[X]_FPWM Bit in *FPWM* Register (AD_{HEX})	EN_PS_IDLEx Bit in *DPS_IDLE_CFG* Register ($7A_{HEX}$)	
	0_{BIN} = Idle Mode Disable (FPWM Mode)	1_{BIN} = Idle Mode Enable (Auto PFM/PWM Mode)
0_{BIN} = Auto PFM/PWM Mode	FPWM	FPWM
1_{BIN} = FPWM Mode	FPWM	FPWM

Table 68. Enable Phase Shedding – Example DCD2: DPS2_CONFIG ($1B_{HEX}$) Bits[1:0] = 00_{BIN}, 01_{BIN}, or 10_{BIN}

DCD[X]_FPWM Bit in FPWM Register (AD_{HEX})	EN_PS_IDLEx Bit in DPS_IDLE_CFG Register ($7A_{HEX}$)	
	0_{BIN} = Idle Mode Disable (FPWM Mode)	1_{BIN} = Idle Mode Enable (Auto PFM/PWM Mode)
0_{BIN} = Auto PFM/PWM Mode	FPWM	Auto PFM/PWM
1_{BIN} = FPWM Mode	FPWM	FPWM

Table 69. DPS_IDLE_CFG Register

Note: Idle means operation in Auto PFM/PWM.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS_IDLE_CFG	R/W	RSVD					EN_PS_IDLE2	EN_PS_IDLE1	EN_PS_IDLE0	00_{HEX}	$7A_{HEX}$

Bit	Name	Function	Default
D[7:3]	RSVD	Reserved	00000_{BIN}
D[2]	EN_PS_IDLE2	Set Idle Mode for DCD2: 0 = Idle Mode Disable (FPWM). 1 = Idle Mode Enable (Auto PFM/PWM).	0_{BIN}
D[1]	EN_PS_IDLE1	Set Idle Mode for DCD1: 0 = Idle Mode Disable (FPWM). 1 = Idle Mode Enable (Auto PFM/PWM).	0_{BIN}
D[0]	EN_PS_IDLE0	Set Idle Mode for DCD0: 0 = Idle Mode Disable (FPWM). 1 = Idle Mode Enable (Auto PFM/PWM).	0_{BIN}

Note: SVID must be disabled if *DPS_IDLE_CFG* is changed in the register via I2C in order to make changes to EN_PS_IDLEx. Changing EN_PS_IDLEx from 1 to 0 (Auto PFM/PWM to FPWM) requires powering down and then power up the rail.

7.13.7 Active DPU and DPU Count Status

Table 70. PMSTATUS

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS0_PMSTATUS	R	DPS0_PMSTATUS[7:0]								00_{HEX}	07_{HEX}
DPS1_PMSTATUS	R	DPS1_PMSTATUS[7:0]								00_{HEX}	$0A_{HEX}$
DPS2_PMSTATUS	R	DPS2_PMSTATUS[7:0]								00_{HEX}	$1C_{HEX}$
DPS3_PMSTATUS	R	DPS3_PMSTATUS[7:0]								00_{HEX}	$1E_{HEX}$
DPS4_PMSTATUS	R	DPS4_PMSTATUS[7:0]								00_{HEX}	24_{HEX}

Bit	Name	Function	Default
D[7:0]	DPSx_PMSTATUS[7:0]	PMSTATUS has two modes: MODE1: If the rail is off, the PMSTATUS will report in hexadecimal how many DPUs are available to that rail. Each bit represents a DPU. $0_{HEX} = 0000_{BIN}$ = 0 DPU $1_{HEX} = 0001_{BIN}$ = 1 DPU available to the rail $3_{HEX} = 0011_{BIN}$ = 2 DPUs available to the rail $7_{HEX} = 0111_{BIN}$ = 3 DPUs available to the rail $F_{HEX} = 1111_{BIN}$ = 4 DPUs available to the rail MODE2: If the rail is active, the PMSTATUS will report in decimal how many DPUs are active (have switching activity) at that moment: 0_{DEC} = 0 DPU 1_{DEC} = 1 DPU active (even if ≥ 2 DPUs are available) 2_{DEC} = 2 DPUs active 3_{DEC} = 3 DPUs active 4_{DEC} = 4 DPUs active	00000000_{BIN}

7.13.8 DCD0-2 Compensation and DPU Phase Shedding Control Registers

Table 71. DCD0-2 Compensation and DPU Phase Shedding Control Registers

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS0_CONFIG	R/W	RSVD		GM0	RSVD			OFF_DLY[1:0]		20_{HEX}	06_{HEX}
DPS1_CONFIG	R/W	RSVD		GM1	RSVD			OFF_DLY[1:0]		20_{HEX}	09_{HEX}
DPS2_CONFIG	R/W	RSVD		GM2	RSVD			OFF_DLY[1:0]		20_{HEX}	$1B_{HEX}$

Bit	Name	Function	Default
D[7]	RSVD	Reserved	0_{BIN}
D[5]	GM[x]	Gain Margin (GM) selection: 0 = Set to lower GM gain. 1 = Set to normal GM gain.	1_{BIN}
D[4:2]	RSVD	Reserved	000_{BIN}
D[1:0]	OFF_DLY[1:0]	DPU Phase Shedding Timer (valid only for Auto-Mode PWM/PFM (FPWM=0)): 00 = Drop a phase 130µs after load current drops below PFM level. 01 = Drop a phase 65µs after load current drops below PFM level. 10 = Drop a phase 20µs after load current drops below PFM level. 11 = Disable phase-shedding.	00_{BIN}

7.13.9 DCD3-4 Compensation and DPU Phase Shedding Control Registers

Table 72. DCD3-4 Compensation and DPU Phase Shedding Control Registers

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS3_CONFIG	R/W	RSVD	DAMPB3	GM3	RSVD			OFF_DLY[1:0]		30_{HEX}	$1D_{HEX}$
DPS4_CONFIG	R/W	RSVD	DAMPB4	GM4	RSVD			OFF_DLY[1:0]		30_{HEX}	23_{HEX}

Bit	Name	Function	Default
D[7]	RSVD	Reserved.	0_{BIN}
D[6]	DAMPB[X]	0 = Select default compensation. 1 = Select alternative compensation.	0_{BIN}
D[5]	GM	GM Gain Selection: 0 = Set to lower GM gain. 1 = Set to normal GM gain.	1_{BIN}

Bit	Name	Function	Default
D[4:2]	RSVD	Reserved	100_{BIN}
D[1:0]	OFF_DLY[1:0]	DPU phase shedding timer: 00_{BIN} = Drop a phase 130µs after load current drops below PFM level 01_{BIN} = Drop a phase 65µs after load current drops below PFM level 10_{BIN} = Drop a phase 0µs after load current drops below PFM level 11_{BIN} = Disable phase shedding	00_{BIN}

7.13.10 DCD5-6 Compensation Control Registers

Table 73. DCD5-6 Compensation Control Registers

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS56_CONFIG	R/W	RSVD				GM6	BW6	GM5	BW5	$0A_{HEX}$	$0D_{HEX}$

Bit	Name	Function	Default
D[7:4]	RSVD	Reserved	0000_{BIN}
D[3]	GM6	Gain Margin (GM) selection for DCD6: 0 = Set to lower GM gain 1 = Set to normal GM gain	1_{BIN}
D[2]	BW6	Bandwidth Selection for DCD6: 0 = Use normal bandwidth 1 = Set to lower bandwidth	0_{BIN}
D[1]	GM5	Gain Margin (GM) selection for DCD5: 0 = Set to lower GM gain 1 = Set to normal GM gain	1_{BIN}
D[0]	BW5	Bandwidth Selection for DCD5: 0 = Use normal bandwidth 1 = Set to lower bandwidth	0_{BIN}

7.13.11 Over-Current (OC) Warning and Over-Current Limit

The DCDs use switch peak current information to compare with the internal thresholds for output current warning and limiting. The DCDs operate in Constant Current Mode during an over-current event.

If the peak current reaches the first threshold over-current warning level (see Table 76), the DCDx_OC warning status bit in the *DCD_OC* register (AE$_{HEX}$; see Table 74) is set to 1. With DCD[x]_ILIM = 1 and DILIM2 = 0 (the P91E0's default setting), the current limiting feature is activated. The P91E0 allows the actual output current to increase and eventually clamps at an average value close to the over-current warning level. For DCD0, DCD1, and DCD2, the limiting action starts if the peak current level exceeds the warning level (8A typical) for a duration of 10µs or 100µs depending on the *DCD_ILIM* register bit[7] setting (A0$_{HEX}$; see Table 75). For DCD5 and/or DCD6, the limiting action of each DCD at this warning level 2.7A (typical) can be bypassed by setting the corresponding bit in the *DCD[x]_ILIM* register to 0, or both DCDs can be bypassed by setting DILIM2 = 1, which can also be done with OTP from the factory.

Recommendation: For DCD5 and DCD6, use the default setting for output current delivery up to 1.3A. DCD5 and DCD6 can achieve 2A DC output current and 2.3A peak across conditions by bypassing the current limit at the OC warning level in combination with proper inductor selection where IDC satisfies considerations for a possible temperature rise and ISAT (inductor saturation current) is chosen based on the expected peak current up to a current limit of 4A peak.

7.13.12 DCD Over-Current Warning Status

Table 74. DCD Over-Current Warning Status

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD_OC	R/W	RSVD	DCD6_OC	DCD5_OC	RSVD		DCD2_OC	DCD1_OC	DCD0_OC	00$_{HEX}$	AE$_{HEX}$

Bit	Name	Function	Default
D[7]	RSVD	Reserved.	0$_{BIN}$
D[6]	DCD6_OC	0 = Peak switch current is below the OC warning level for DCD6. 1 = Peak switch current has been above the OC warning level. Write ‘1’ to clear.	0$_{BIN}$
D[5]	DCD5_OC	0 = Peak switch current is below the OC warning level for DCD5. 1 = Peak switch current has been above the OC warning level. Write ‘1’ to clear.	0$_{BIN}$
D[4:3]	RSVD	Reserved.	00$_{BIN}$
D[2]	DCD2_OC	0 = Peak switch current is below the OC warning level for DCD2. 1 = Peak switch current has been above the OC warning level. Write ‘1’ to clear.	0$_{BIN}$
D[1]	DCD1_OC	0 = Peak switch current is below the OC warning level for DCD1. 1 = Peak switch current has been above the OC warning level. Write ‘1’ to clear.	0$_{BIN}$
D[0]	DCD0_OC	0 = Peak switch current is below the OC warning level for DCD0. 1 = Peak switch current has been above the OC warning level. Write ‘1’ to clear.	0$_{BIN}$

Table 75. Individual DCD First Over-Current-Limit Level Activation

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD_ILIM	R/W	ILIM100US	DCD6_ILIM	DCD5_ILIM	RSVD					67$_{\text{HEX}}$	A0$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	ILIM100US	Sets the duration when the current limit comparator is bypassed (disabled) during a DVS event to allow higher output current for a limited time for DCD0, DCD1, and DCD2. This function is enabled with DCD0_ILIM, DCD1_ILIM, and DCD2_ILIM. 0 = Allow 10µs before activating current limit action. 1 = Allow 100µs before activating current limit action.	0$_{\text{BIN}}$
D[6]	DCD6_ILIM	DCD6 first-level current limit activation. 0 = Use current limit function at the second OC level 1 = Enable the current limit function when the peak switch current has reached the OC warning level	1$_{\text{BIN}}$
D[5]	DCD5_ILIM	DCD5 first-level current limit activation. 0 = Use current limit function at the second OC level 1 = Enable the current limit function when the peak switch current has reached the OC warning level	1$_{\text{BIN}}$
D[4:0]	RSVD	Reserved. Always write a 00111$_{\text{BIN}}$ to these bits.	00111$_{\text{BIN}}$

Table 76. DCD Group First Over-Current-Limit Level Activation

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DILIM	R/W	RSVD						DILIM2	RSVD	00$_{\text{HEX}}$	70$_{\text{HEX}}$

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000$_{\text{BIN}}$
D[1]	DILIM2	0 = DCD5 and DCD6 current-limit function uses the setting in the *DCD_ILIM* register (A0$_{\text{HEX}}$). 1 = Bypass the first-level current-limit function for DCD5/6 independent of the settings in the DCD_ILIM register. This may be redundant to DCD5_ILIM and DCD6_ILIM in *DCD_ILIM.*	0$_{\text{BIN}}$
D[0]	RSVD	Reserved. Always write a 0 to this bit.	0$_{\text{BIN}}$

7.14 Power Consumption at Light Load Considerations

Power dissipation at light load is predominantly from the current used by internal circuitry through VSYS, current consumption from switching activity of the DCD's switching power supply, and quiescent current of the LDOs. To achieve the greatest power saving, rails can be manually disabled via I2C. When DPUs are used with regulators (DCD0, DCD1, and DCD2) or controllers (DCD3 and DCD4), there is additional current consumption used by the DPU's internal logic for performing switching activity. To minimize the power consumption from switching activity, Auto-Mode PWM/PFM can be used. For the DCD0, DCD1, and DCD2 regulators, the internal FETs are performing the switching activity in light load, so there is no switching activity done by the DPU(s); thus there is minimal power dissipation on the DPU(s). For DCD3 and DCD4, the switching activity is always performed by the DPU(s).

Table 77 shows the typical consumption of an example configuration without any output current load and P9148 as the DPU. The Vsys logic is the baseline current with the internal circuitry still operating, while all DCDs and all LDOs, except LDO7, are OFF. The values in the P91E0 I_Q column represent the additional current into the VSYS pin and DCD_VIN or LDO_VIN pin of the respective rail. DCD3 and DCD4 are manually set to Auto-Mode PWM/PFM for the greatest power savings. The power consumption in each state (e.g., SoC-S3, SoC-S4/S5) can be calculated from summing the power loss of the rails that remain active in that state.

Table 77. Typical Light-Load Power Consumption using the P9148

Vin = 5.0V, Temperature = 25°C.

	Number of DPUs	Vin [V]	Vout [V]	P91E0 I_Q [mA]	P9148 I_Q [mA]	Power Loss [mW]
Vsys Logic	–	5.0	–	1.000	-	5.00
DCD0	4	5.0	OFF	0.105	0.720	4.13
DCD1	0	5.0	1.00	0.500	-	2.50
DCD2	1	5.0	1.10	0.500	0.180	3.40
DCD3	1	5.0	1.05	0.250	0.550	4.00
DCD4	1	5.0	3.30	0.250	0.550	4.00
DCD5	–	5.0	1.80	0.500	–	2.50
DCD6	–	5.0	1.24	0.500	–	2.50
LDO0	–	1.8	–	0.022	–	0.04
LDO1	–	1.8	–	0.022	–	0.04
LDO2	–	1.8	–	0.022	–	0.04
LDO3	–	1.8	–	0.020	–	0.04
LDO4	–	1.8	–	0.020	–	0.04
LDO5	–	1.1	–	0.095	–	0.10
LDO6	–	5.0	–	0.020	–	0.10
					Total:	28.42

7.15 Enable Pins

All enable signals are open-drain output signals. The polarity is set to active-LOW by default. EN0 to EN4 can be fuse-programmed to be active-HIGH upon PMIC start-up. The on/off control of each regulator is controlled either through the programmed sequence or by I2C.

Table 78. Electrical Characteristics – Enable Pins

Conditions unless otherwise specified: T_A= 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{pullup}	External Pull-up Voltage	–	–	–	5.25	V
V_{OL}	Output Voltage LOW	I_{OUT} = 10mA	–	–	0.4	V
I_{SNK}	Current Sink	V_{ENx} = 0.4V	–	10	–	mA
I_{LKG}	Leakage Current	–	–	100	–	nA

Table 79. I2C Control Register – EN0 to EN11

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
EN0_CTL	R/W	RSVD					Polarity	EN0_SEL	EN0_EN	00$_{HEX}$	56$_{HEX}$
EN1_CTL	R/W	RSVD					Polarity	EN1_SEL	EN1_EN	00$_{HEX}$	57$_{HEX}$
EN2_CTL	R/W	RSVD					Polarity	EN2_SEL	EN2_EN	00$_{HEX}$	5B$_{HEX}$
EN3_CTL	R/W	RSVD					Polarity	EN3_SEL	EN3_EN	00$_{HEX}$	5C$_{HEX}$
EN4_CTL	R/W	RSVD					Polarity	EN4_SEL	EN4_EN	00$_{HEX}$	5D$_{HEX}$
EN5_CTL	R/W	RSVD					Polarity	EN5_SEL	EN5_EN	00$_{HEX}$	69$_{HEX}$
EN6_CTL	R/W	RSVD					Polarity	EN6_SEL	EN6_EN	00$_{HEX}$	68$_{HEX}$
EN7_CTL	R/W	RSVD					Polarity	EN7_SEL	EN7_EN	00$_{HEX}$	64$_{HEX}$
EN8_CTL	R/W	RSVD					Polarity	EN8_SEL	EN8_EN	00$_{HEX}$	62$_{HEX}$
EN9_CTL	R/W	RSVD					Polarity	EN9_SEL	EN9_EN	00$_{HEX}$	6B$_{HEX}$
EN10_CTL	R/W	RSVD					Polarity	EN10_SEL	EN10_EN	00$_{HEX}$	6C$_{HEX}$
EN11_CTL	R/W	RSVD					Polarity	EN11_SEL	EN11_EN	00$_{HEX}$	6D$_{HEX}$

Bit	Name	Function	Default
D[7:3]	RSVD	Reserved	00000$_{BIN}$
D[2]	Polarity	Polarity bit: 0 = Active LOW. 1 = Active HIGH.	EN0 to EN4: OTP EN5 to EN11: 0
D[1]	ENx_SEL	ON/OFF selection bit: 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by the D[0] bit in this register.	0$_{BIN}$
D[0]	ENx_EN	Enable bit: 0 = OFF 1 = ON	0$_{BIN}$

Table 80. On/Off Selection Bit Table – Enable Pins

D[1]	D[0]	Sequencer Control	Enable Pin
0	X	0	HIGH
0	X	1	LOW
1	0	X	HIGH
1	1	X	LOW

Table 81. I2C Sequencing Control – EN0 to EN11

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
EN0_GRP	R/W	RSVD		🟩 EN0_TYPE		🟩 EN0_GROUP				OTP	$F4_{HEX}$
EN1_GRP	R/W	RSVD		🟩 EN1_TYPE		🟩 EN1_GROUP				OTP	$F5_{HEX}$
EN2_GRP	R/W	RSVD		🟩 EN2_TYPE		🟩 EN2_GROUP				OTP	$F6_{HEX}$
EN3_GRP	R/W	RSVD		🟩 EN3_TYPE		🟩 EN3_GROUP				OTP	$F7_{HEX}$
EN4_GRP	R/W	RSVD		🟩 EN4_TYPE		🟩 EN4_GROUP				OTP	$F8_{HEX}$
EN5_GRP	R/W	RSVD		🟩 EN5_TYPE		🟩 EN5_GROUP				OTP	$F9_{HEX}$
EN6_GRP	R/W	RSVD		🟩 EN6_TYPE		🟩 EN6_GROUP				OTP	FA_{HEX}
EN7_GRP	R/W	RSVD		🟩 EN7_TYPE		🟩 EN7_GROUP				OTP	FB_{HEX}
EN8_GRP	R/W	RSVD		🟩 EN8_TYPE		🟩 EN8_GROUP				OTP	FC_{HEX}
EN9_GRP	R/W	RSVD		🟩 EN9_TYPE		🟩 EN9_GROUP				OTP	FD_{HEX}
EN10_GRP	R/W	RSVD		🟩 EN10_TYPE		🟩 EN10_GROUP				OTP	FE_{HEX}
EN11_GRP	R/W	RSVD		🟩 EN11_TYPE		🟩 EN11_GROUP				OTP	$7D_{HEX}$

Bit	Name	Function		Default
D[7:6]	RSVD	Reserved		0_{BIN}
D[5:4]	ENx_TYPE	Rail type selection bits: 00_{BIN} = “A” rail type. 01_{BIN} = “U” rail type. 10_{BIN} = “S” rail type. 11_{BIN} = “SX” rail type.		OTP
D[3:0]	ENx_GROUP	Group Delay Bits		OTP
		0000_{BIN} = Group 0 0001_{BIN} = Group 1 0010_{BIN} = Group 2 0011_{BIN} = Group 3 0100_{BIN} = Group 4 0101_{BIN} = Group 5 0110_{BIN} = Group 6 0111_{BIN} = Group 7	1000_{BIN} = Group 8 1001_{BIN} = Group 9 1010_{BIN} = Group 10 1011_{BIN} = Group 11 1100_{BIN} = Group 12 1101_{BIN} = Group 13 1110_{BIN} = Group 14 1111_{BIN} = Disable	

7.16 Sequencing Configuration Registers

7.16.1 PMIC Sequencing Status

Table 82. PMIC Sequencing Status

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
SEQ_STATUS	R	MTEST_ MODE	STARTUP _ABORT	STARTUP _DONE	TRIM_ DONE	PWR_STATE[3:0]				00_{HEX}	63_{HEX}

Bit	Name	Function	Default
D[7]	MTEST_MODE	Debug Mode enabled.	0_{BIN}
D[6]	STARTUP_ABORT	Error occurs during start-up.	0_{BIN}
D[5]	STARTUP_DONE	Internal initialization status is complete.	0_{BIN}
D[4]	TRIM_DONE	Trim code is loaded.	0_{BIN}
D[3:0]	PWR_STATE[3:0]	Pin status and state (see section 9.3): SoC_G3 = 0000; (All rails off) SoC_S4/S5 = 0001; (A rails active) SoC_S3 = 0011; (A rails and U rails active) SoC_S0Ix = 0111; (A, U, S rails active) SoC_S0 = 1111; (All rails active (A, U, S, SX)).	0000_{BIN}

Table 83. Power Sequence Configuration

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PWRSEQCFG	R/W	RSVD				VCCAPWROKCFG	SUSPWRDNACKCFG	DTPWROK[1:0]		$0E_{HEX}$	$2A_{HEX}$

Bit	Name	Function	Default
D[7:4]	RSVD	Reserved	0000_{BIN}
D[3]	VCCAPWROKCFG	0 = VCCAPWROK de-asserts in S0Ix state. 1 = VCCAPWROK remains asserted in S0Ix state.	1_{BIN}
D[2]	SUSPWRDNACKCFG	0 = SUSPWRDNACK signal is ignored. The PMIC will not go to G3 when SUSPWRDNACK goes HIGH in the SoC-S4/S5 state. 1 = PMIC responses to the SUSPWRDNACK signal.	1_{BIN}
D[1:0]	DTPWROK[1:0]	Delay time between SX14 rail and the first assertion of COREPWROK and VCCAPWROK. Note that the value should not be changed while COREPWROK and VCCAPWROK are asserted HIGH; i.e. in the S0 and S0Ix states. 00 = 1ms 01 = 10ms 10 = 100ms 11 = 120ms	10_{BIN}

Table 84. S0Ix Configuration

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
S0IxCFG	R/W	RSVD							🟩 NOS0Ix	00_{HEX}	50_{HEX}

Bit	Name	Function	Default
D[7:1]	RSVD	Reserved	0_{BIN}
D[0]	NOS0Ix	0 = S0Ix state is used. 1 = S0Ix state is not used. Operation and timing sequence are associated with SX-type rails and the SLP_S0Ix_B signal is ignored.	0_{BIN}

7.16.2 Group-Delay Timing

Group-delay timing registers define the time delay between two consecutive group-delay indexes and are applicable to LDOs, DCDs, and ENs (LDOx_GROUP, DCDx_GROUP, ENx_GROUP) as they are assigned to a respective rail type (A, U, S, SX). With OTP, the group-delay within each type during turn-on and turn-off are the same.

Table 85. Group-Delay Timing

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
SEQA_TIM	R/W	RSVD	🟩 DLY_GRP_OFF_A[2:0][a]			RSVD	🟩 DLY_GRP_ON_A[2:0]			OTP	$C3_{\text{HEX}}$
SEQU_TIM	R/W	RSVD	🟩 DLY_GRP_OFF_U[2:0][a]			RSVD	🟩 DLY_GRP_ON_U[2:0]			OTP	$C4_{\text{HEX}}$
SEQS_TIM	R/W	RSVD	🟩 DLY_GRP_OFF_S[2:0][a]			RSVD	🟩 DLY_GRP_ON_S[2:0]			OTP	$D3_{\text{HEX}}$
SEQSX_TIM	R/W	RSVD	🟩 DLY_GRP_OFF_SX[2:0][a]			RSVD	🟩 DLY_GRP_ON_SX[2:0]			OTP	$D4_{\text{HEX}}$

[a] These bits are loaded from OTP with the same value as DLY_GRP_ON_xx[2:0]. They can be changed via I2C if a different turn-off timing is needed.

Bit	Name	Function	Default
D[7]	RSVD	Reserved	0_{BIN}
D[6:4]	DLY_GRP_OFF_X[2:0]	Group delay when group-type turns off: 000_{BIN} = 0.25ms 001_{BIN} = 0.50ms 010_{BIN} = 1.00ms (default) 011_{BIN} = 1.50ms 100_{BIN} = 2.00ms 101_{BIN} = 2.50ms 110_{BIN} = 3.00ms 111_{BIN} = 5.00ms	OTP
D[3]	RSVD	Reserved	0_{BIN}

Bit	Name	Function	Default
D[2:0]	DLY_GRP_ON_X[2:0]	Group delay when group-type turns on: 000_{BIN} = 0.25ms 001_{BIN} = 0.50ms 010_{BIN} = 1.00ms (default) 011_{BIN} = 1.50ms 100_{BIN} = 2.00ms 101_{BIN} = 2.50ms 110_{BIN} = 3.00ms 111_{BIN} = 5.00ms	OTP

7.16.3 Minimum Sleep Time from Group-Delay Timing and the First Rail in a Rail Type

Each rail type (A, U, S, SX) has 14 group members, resulting in a total sequence of each rail type of 14 × SEQ[x]_TIM (see Table 85). For the start-up sequence (sleep sequence exit), each rail type starts from index 0 to 14, and for the shut-down sequence (sleep sequence entry), each rail type stops in reverse order. The minimum sleep time (SLP_ signal = LOW) is equal to the duration that the SLP_ signal must be LOW from Group 14 to the lowest used index group number with a 20% additional margin recommended.

For example, for the -I5 configuration, the following applies:

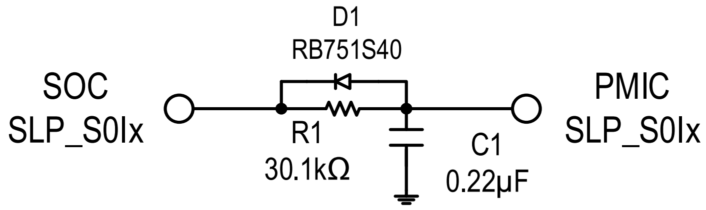
(1) The S-type rail has SEQS_TIM = 1ms

(2) The SX-type rail has SEQSX_TIM = 0.25ms with DCD1 = SX07 as the first of this rail type to turn on and DCD0 = SX14 as the last.

The minimum time for SLP_S0Ix to be LOW is $0.25\text{ms} \times (14 - 7) \times 1.2 = 2.1\text{ms}$. This minimum sleep time can be satisfied by setting the SoC's Minimum Assertion Width, for example the PMU SLP S3 B Minimum Assertion Width (slp_s3_min_asst_wdth) can be set to 50ms to ensure that it is longer than 14 × 1ms = 14ms.

In the case that the setting is not available, the application circuit shown in Figure 2 can be used to prolong the SLP_LOW signal seen by the PMIC. The values of the R1 resistor and C1 capacitor are selected such that the duration of the PMIC_SLP_S0Ix signal reaching V_{IH} (1.35V) after exiting S0Ix-sleep state is longer than the minimum sleep time (2.1ms in this example) but shorter than the time out delay of the SoC (7ms in this example) with a 3.3V SOC_SLP_S0Ix push-pull output. The diode D1 is a signal Schottky diode with a forward-voltage below the V_{IL} of the SLP_ signals and oriented such that when SOC_SLP_S0Ix goes LOW, the PMIC_SLP_S0Ix is pulled LOW immediately and thus quickly enters Sleep Mode but has a time delay created by R1 and C1 when exiting Sleep Mode. When choosing the diode, select a part that has low reverse-leakage current at the minimum and maximum operating temperatures of the system.

Figure 2. Application Circuit for -I5 Configuration for SX-type Minimum Sleep Time: 2.1ms < SLP_S0Ix < 7ms



7.17 General Purpose IOs

The P91E0 offers 15 general purpose input/output ports (GPIO) divided into two banks. Each bank has a separated power supply input dividing the GPIOs into a 1.8V (VGPIO0) and 3.3V (VGPIO1) domain. VGPIO0 powers GPIO[9:0], the VGPIO1 supply input powers GPIO[14:10].

Each GPIO can be configured either as CMOS output, open-drain output or input. Unless specified, all the GPIOs are defaulted as CMOS input with a weak 50kΩ pull down.

Table 86. Electrical Characteristics – GPIO[9:0]

Conditions unless otherwise specified: T_A= 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VGPIO0	Input Power Supply	C_{IN} = 1µF	1.71	1.8	1.89	V
Input Configuration						
V_{IL}	Input LOW Voltage		–	–	0.35 × VGPIO0	V
V_{IH}	Input HIGH Voltage		0.65 × VGPIO0	–	–	V
V_{HYS}	Hysteresis		–	0.33	–	V
I_{IL}	Input LOW Current	V_{IL} = GND	–	0	–	µA
I_{IH}	Input HIGH Current	V_{IH} = 1.8V, 50kΩ pull-down	–	36	–	µA
CMOS Output Configuration						
V_{OL}	Output LOW Voltage		–	–	0.4	V
V_{OH}	Output HIGH Voltage		VGPIO0 – 0.4	–	–	V
I_{OL}	Output LOW Current		–	4	–	mA
I_{OH}	Output HIGH Current		–	4	–	mA
t_{RISE}	Rise Time	Load capacitance C_L= 150pF, 10% to 90%, GBD	10	–	45	ns
t_{FALL}	Fall Time	C_L= 150pF, 90% to 10%, GBD	10	–	45	ns
Open Drain Configuration						
V_{OL}	Output LOW Voltage		–	–	0.40	V
I_{OL}	Output LOW Current		–	12	–	mA
I_{LKG}	Leakage Current		–	100	–	nA

Table 87. Electrical Characteristics – GPIO[14:10]

Conditions unless otherwise specified: T_A= 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VGPIO1	Input Power Supply	C_{IN} = 1μF	3.0	3.3	3.6	V
Input Configuration						
V_{IL}	Input LOW Voltage		–	–	0.35 × VGPIO1	V
V_{IH}	Input HIGH Voltage		0.65 × VGPIO1	–	–	V
V_{HYS}	Hysteresis		–	0.33	–	V
I_{IL}	Input LOW Current	V_{IL} = GND	–	0	–	μA
I_{IH}	Input HIGH Current	V_{IH} = 3.3V, 50kΩ pull-down	–	66	–	μA
CMOS Output Configuration						
V_{OL}	Output LOW Voltage		–	–	0.40	V
V_{OH}	Output HIGH Voltage		VGPIO1 – 0.40	–	–	V
I_{OL}	Output LOW Current		–	4.0	–	mA
I_{OH}	Output HIGH Current		–	4.0	–	mA
t_{RISE}	Rise Time	Load capacitance C_L = 150pF, 10 to 90%, GBD	10	–	45	ns
t_{FALL}	Fall Time	C_L = 150pF, 90 to 10%, GBD	10	–	45	ns
Open Drain Configuration						
V_{OL}	Output LOW Voltage		–	–	0.40	V
I_{OL}	Output LOW Current		–	12	–	mA
I_{LKG}	Leakage Current		–	100	–	nA

Table 88. GPIO Output Configuration Register

Note: Green shading indicates that the bit values are loaded from the OTP.

Note: Yellow shading indicates that the bit values are paired with bits in other registers for the OTP setting. See the subsequent bit function description table for details.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIOCTLO0	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	7C$_{HEX}$	3B$_{HEX}$
GPIOCTLO1	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	7C$_{HEX}$	3C$_{HEX}$
GPIOCTLO2	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	7C$_{HEX}$	3D$_{HEX}$
GPIOCTLO3	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	7C$_{HEX}$	3E$_{HEX}$
GPIOCTLO4	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	7C$_{HEX}$	3F$_{HEX}$
GPIOCTLO5	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	7C$_{HEX}$	40$_{HEX}$
GPIOCTLO6	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0C$_{HEX}$	41$_{HEX}$
GPIOCTLO7	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0C$_{HEX}$	42$_{HEX}$
GPIOCTLO8	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0C$_{HEX}$	2B$_{HEX}$

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIOCTLO9	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	$0C_{HEX}$	$2C_{HEX}$
GPIOCTLO10	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	$0C_{HEX}$	$2D_{HEX}$
GPIOCTLO11	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	$0C_{HEX}$	$2E_{HEX}$
GPIOCTLO12	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	$0C_{HEX}$	$2F_{HEX}$
GPIOCTLO13	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	$0C_{HEX}$	30_{HEX}
GPIOCTLO14	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	$0C_{HEX}$	31_{HEX}

<table>
<tr><th>Bit</th><th>Name</th><th colspan="2">Function</th><th>Default</th></tr>
<tr><td>D[7]</td><td>RSVD</td><td colspan="2">Reserved.</td><td>0_{BIN}</td></tr>
<tr><td rowspan="10">D[6]</td><td rowspan="10">ALT_FUNC</td><td colspan="2">Alternative Function:
0 = Disabled.
1 = Enabled. Note that in OTP, the D[6] settings associated with DIO and DIF for DCDx are paired as follows: GPIOCTLO0 with GPIOCTLO1, GPIOCTLO2 with GPIOCTLO3, GPIOCTLO4 with GPIOCTLO5. The OTP settings for GPIOCTLO6 to GPIOCTLO14 can be configured independently.
Note: These settings can be changed via I2C after the download from OTP.</td><td rowspan="10">1_{BIN} for GPIOCTLO0 to GPIOCTLO5
0_{BIN} for GPIOCTLO6 to GPIOCTLO14</td></tr>
<tr><td colspan="2">Alternative Function Disabled/Enabled</td></tr>
<tr><td>GPIO0 / DCD2_DIO [default DCD2_DIO]</td><td>GPIO8 / SLEEP [default GPIO8]</td></tr>
<tr><td>GPIO1 / DCD2_DIF [default DCD2_DIF]</td><td>GPIO9 / VDDQSEL [default GPIO9]</td></tr>
<tr><td>GPIO2 / DCD1_DIO [default DCD1_DIO]</td><td>GPIO10 / ADC0 [default GPIO10]</td></tr>
<tr><td>GPIO3 / DCD1_DIF [default DCD1_DIF]</td><td>GPIO11 / ADC1 [default GPIO11]</td></tr>
<tr><td>GPIO4 / DCD0_DIO [default DCD0_DIO]</td><td>GPIO12 / ADC2 [default GPIO12]</td></tr>
<tr><td>GPIO5 / DCD0_DIF [default DCD0_DIF]</td><td>GPIO13 / PANEL_EN [default GPIO13]</td></tr>
<tr><td>GPIO6 / PWM0 [default GPIO6]</td><td>GPIO14 / BACKLIGHT_EN [default GPIO14]</td></tr>
<tr><td>GPIO7 / PWM1 [default GPIO7]</td><td></td></tr>
<tr><td>D[5]</td><td>DIR</td><td colspan="2">Pin Direction:
0 = Input.
1 = Output.</td><td>1_{BIN} for GPIOCTLO0 to GPIOCTLO5
0_{BIN} for GPIOCTLO6 to GPIOCTLO14</td></tr>
<tr><td>D[4]</td><td>DRV</td><td colspan="2">Output Driver Type:
0 = Open drain.
1 = CMOS (push-pull).</td><td>1_{BIN} for GPIOCTLO0 to GPIOCTLO5
0_{BIN} for GPIOCTLO6 to GPIOCTLO14</td></tr>
<tr><td>D[3]</td><td>REN</td><td colspan="2">Internal Pull Up Enable/Disable:
0 = Pull-up/pull-down disabled.
1 = Pull-up/pull-down enabled.</td><td>1_{BIN}</td></tr>
</table>

Bit	Name	Function	Default
D[2:1]	RVAL	Internal Pull Up Resistor Value: 00_{BIN} = 2kΩ pull down. 10_{BIN} = 50kΩ pull-down. 01_{BIN} = 2kΩ pull up. 11_{BIN} = 50kΩ pull-up.	10_{BIN}
D[0]	DOUT	Pin Output Value: 0 = LOW. 1 = HIGH or high-Z.	0_{BIN}

Table 89. GPIO Input Configuration Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIOCTLI0	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	43_{HEX}
GPIOCTLI1	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	44_{HEX}
GPIOCTLI2	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	45_{HEX}
GPIOCTLI3	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	46_{HEX}
GPIOCTLI4	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	47_{HEX}
GPIOCTLI5	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	48_{HEX}
GPIOCTLI6	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	49_{HEX}
GPIOCTLI7	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	$4A_{HEX}$
GPIOCTLI8	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	33_{HEX}
GPIOCTLI9	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	34_{HEX}
GPIOCTLI10	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	35_{HEX}
GPIOCTLI11	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	36_{HEX}
GPIOCTLI12	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	37_{HEX}
GPIOCTLI13	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	38_{HEX}
GPIOCTLI14	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	00_{HEX}	39_{HEX}

Bit	Name	Function	Default
D[7:5]	RSVD	Reserved	000_{BIN}
D[4]	GPIGLBYP	Glitch Filter By-Pass Enable: 0 = Glitch filter enabled. 1 = Glitch filter by-passed.	0_{BIN}
D[3]	GPIDBNC	De-Bounce Enable: 0 = De-bounce disabled. 1 = De-bounce enabled.	0_{BIN}
D[2:1]	INTCNT	Interrupt Detect: 00 = Disable. 01 = Negative edge. 10 = Positive edge. 11 = Both edges.	00_{BIN}
D[0]	DIN	Pin Status: 0= Input LOW. 1= Input HIGH.	0_{BIN}

7.17.1 VDDQ Select (VDDQSEL)

If the alternate function of the GPIO[9]/VDDQSEL pin has been selected, the VDDQSEL feature allows using a single OTP configuration to supply different voltages for the VDDQ rail, depending on the type of memory used. This is achieved with a single resistor connected between the GPIO[9]/VDDQSEL pin and either GND or the LDO7_VO output, as shown in Table 90. The resistor is sensed during start-up, and depending on the value, the DCD2 boot voltage is set according to Table 90. This value overrides the *DCD2_VBOOT* value (see Table 40). The default configuration for GPIO[9]/VDDQSEL is to act as GPIO[9], so if the VDDQSEL functionality is required, it must be set in the corresponding register (see Table 88) or OTP configuration.

Table 90. DCD2 Output Voltage vs. VDDQSEL Connection

VDDQSEL Connection	DCD2_VBOOT (V)	Memory Type
100Ω to GND [a]	1.1	LPDDR
100kΩ to GND	1.2	DDR4
100kΩ to LDO7_VO	1.24	LPDDR3
100Ω to LDO7_VO	1.35	DDR3L

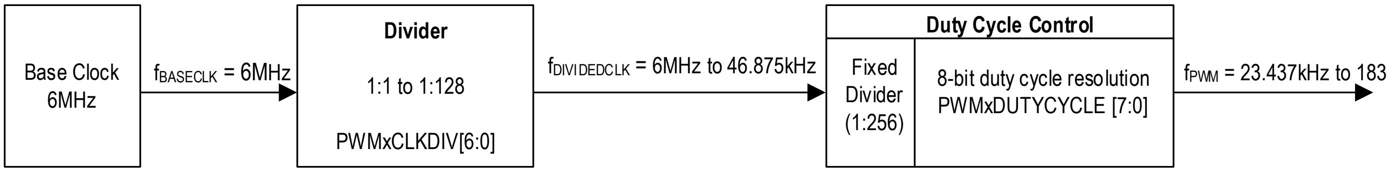
[a] Contact IDT for use of this option. See the last page for contact information.

7.17.2 Pulse Width Modulation (PWM) Generator

The P91E0 supports two PWM outputs with programmable frequencies of ~183Hz to a maximum required frequency of ~23.4kHz and duty cycle granularity of 1/256. To use the PWM0 and PWM1, the GPIO[6]/PWM[0] [default GPIO6] and GPIO[7]/PWM[1] [default GPIO7] pins must be set accordingly to enable the alternative functions (see Table 88), and the pin direction must be set to "Output." Both push-pull and open-drain configurations are supported.

Figure 3 shows the PWM block diagram. Each individual PWM output has two control registers to set the clock divider and one to set the duty cycle of each PWM output. See Table 91 for the *PWMxCLKDIV* registers and Table 92 for the *PWMxDUTYCYCLE* registers.

Figure 3. PWM Block Diagram



The PWM "Divider" sub-block is clocked by the 6MHz internal oscillator (BASECLK). A 7-bit counter counts from 0 to CLKDIVx[6:0], which is a bit field in the *PWMxCLKDIV* register (see Table 91). When CLKDIVx [6:0] is reached, a 7-bit comparator resets the 7-bit counter to 0. This effectively divides the BASECLK by the 7-bit value CLKDIVx [6:0], giving divider options of 1 (no dividing CLKDIVx[6:0] = 0) to 128 (CLKDIVx[6:0] = $7F_{HEX}$). The result of this division is the intermediate clock value $f_{DIVIDEDCLK}$.

The "Duty Cycle Control" block uses a fixed divider (1/256) to perform an additional frequency reduction to obtain f_{PWM}, which is the frequency used for the PWM output. The "Duty Cycle Control" block also uses an 8-bit counter responsible for the duty cycle control, which is selected via the DUTYCYCLEx bit field in the *PWMxDUTYCYCLE r*egister (see Table 92). The duty cycle ranges from 0.39% (DUTYCYCLEx[7:0] = 0) to 100% (DUTYCYCLEx[7:0]=FF_{HEX}) with a 0.39% step. The desired duty cycle of the PWM output is set by DUTYCYCLEx[7:0] with the following formula: (DUTYCYCLEx[7:0] + 1)/256. When the 8-bit counter output is less than the value of DUTYCYCLEx[7:0], the output is HIGH. When the counter value is equal to or greater than the value of DUTYCYCLEx[7:0], the output is LOW. In the case when DUTYCYCLEx[7:0] = FF_{HEX}, the output always stays HIGH. When the counter value reaches FF_{HEX}, the counter is reset to 00_{HEX}, and the next PWM period starts. The counter output is buffered before driving the external pin. The buffer's power supply is 1.8V (VGPIO0).

Note: The PWM frequency is not intended to change on-the-fly (asynchronously). The PWM output must be first disabled by writing 0 to enable bit [7] in the *PWMxCLKDIV* registers before writing to the *PWMxCLKDIV* registers. The PWM duty cycle however is expected to be changed while the PWM output is enabled.

Table 91. PWMxCLKDIV –Clock Divider Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PWM0CLKDIV	R/W	Enable	CLKDIV0[6:0]							00_{HEX}	$4B_{HEX}$
PWM1CLKDIV	R/W	Enable	CLKDIV1[6:0]							00_{HEX}	$4C_{HEX}$

Bit	Name	Function	Default
D[7]	Enable	1=PWM output enabled 0=PWM output disabled	0_{BIN}
D[6:0]	CLKDIVx[6:0]	Clock divider for PWM[x]: 00_{HEX}: Pass-through. No divider. $f_{DIVIDEDCLK} = f_{BASECLK}$ 01_{HEX} to $7F_{HEX}$: $f_{DIVIDEDCLK} = f_{BASECLK}$ / (CLKDIVx[6:0] + 1) $f_{PWM}= f_{DIVIDEDCLK}$ / 256	0000000_{BIN}

Table 92. PWMxDUTYCYCLE – Duty Cycle Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PWM0DUTYCYCLE	R/W	DUTYCYCLE0[7:0]								00_{HEX}	$4E_{HEX}$
PWM1DUTYCYCLE	R/W	DUTYCYCLE1[7:0]								00_{HEX}	$4F_{HEX}$

Bit	Name	Function	Default
D[7:0]	DUTYCYCLEx[7:0]	00_{HEX} to FF_{HEX}: Duty cycle = (DUTYCYCLEx[7:0] + 1)/256 (0.39% to 100%)	00000000_{BIN}

Table 93. PWM Examples

PWMxCLKDIV[6:0]	PWMxDUTYCYCLE[7:0]	f_{PWM}	Duty Cycle
0_{HEX}	0_{HEX}	23.437kHz	0.39%
63_{HEX}	1_{HEX}	0.234kHz	0.78%
$7F_{HEX}$	$A0_{HEX}$	0.183kHz	62.89%
XX_{HEX}	FF_{HEX}	–	100.00%[a]

[a] The output pin is constantly ON.

7.17.3 BLIGHT_EN and PANEL_EN Overview

The P91E0 provides two outputs for display panel controls: BLIGHT_EN to enable the display backlight and PANEL_EN to enable the display panel electronics. The functions to control the backlight and display are turned-off by default and must be enabled first. The registers that control the display panel are described in the following tables.

Table 94. BLIGHT_EN Output Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
BLIGHT_EN	R/W	RSVD							BACKLIGHT_ENOUT	00_{HEX}	51_{HEX}

Bit	Name	Function	Default
D[7:1]	RSVD	Reserved	0000000_{BIN}
D0	BACKLIGHT_ENOUT	Enable Pin Output Value: 0 = LOW 1 = HIGH (CMOS)	0_{BIN}

Table 95. PANEL_EN Output Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PANEL_EN	R/W	RSVD							PANEL_ENOUT	00_{HEX}	52_{HEX}

Bit	Name	Function	Default
D[7:1]	RSVD	Reserved	0000000_{BIN}
D0	PANEL_ENOUT	Enable Pin Output Value: 0 = LOW 1 = HIGH (CMOS)	0_{BIN}

7.17.4 SLEEP_CTL Overview

The PMIC provides control signals for sleep control. The function to control the sleep state is turned-off by default and must be enabled first. The registers that control the sleep state are described in Table 96.

Table 96. SLEEP_CTL Output Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
SLEEP_CTL	R/W	RSVD							EN	04_{HEX}	$4D_{HEX}$

Bit	Name	Function	Default
D[7:1]	RSVD	Reserved	0000000_{BIN}
D0	EN	Enable bit: 0 = OFF 1 = ON	0_{BIN}

Table 97. Voltage during Sleep State

Settings for DCD0, DCD1, and DCD2. Use only if these DCDs are *not* SVID-controlled regulators.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VSLEEP	R/W	VSLEEP[7:0]								47_{HEX}	$7B_{HEX}$

Bit	Name	Function	Default
D[7:0]	VSLEEP	Vsleep voltage setting value; use the same table as VBOOT. Refer to Table 47.	01000111_{BIN}

7.17.5 Sleep State Inputs, Soft-Start-Done, and Reset Signals

Table 98. Electrical Characteristics – SLP_S4_B, SLP_S3_B, SLP_S0Ix_B, SUSPWRDNACK, PLTRST_B, THERMTRIP_B

Conditions unless otherwise specified: T_A = 25°C. Note that these pins can support both the 1.8V and 3.3V SoC interfaces (up to 5.25V).

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IL}	Input LOW Voltage	–	–	–	0.65	V
V_{IH}	Input HIGH Voltage	–	1.35	–	–	V

Table 99. Electrical Characteristics – RSMRST_B, COREPWROK

Conditions unless otherwise specified: T_A = 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VGPIO1	Input Power Supply	C_{IN} = 1µF	3.0	3.3	3.6	V
V_{OL}	Output LOW Voltage	–	–	–	0.40	V
V_{OH}	Output HIGH Voltage	–	VGPIO1 – 0.40	–	–	V
I_{OL}	Output LOW Current	–	–	4.0	–	mA
I_{OH}	Output HIGH Current	–	–	4.0	–	mA
t_{RISE}	Rise Time	C_L= 150pF, 10% to 90%, GBD	10	–	45	ns
t_{FALL}	Fall Time	C_L= 150pF, 90% to 10%, GBD	10	–	45	ns

Table 100. Electrical Characteristics – VCCAPWROK, DRAMPWROK

Conditions unless otherwise specified: T_A = 25°C. Note that these pins can support an external pull-up voltage up to 5.25V.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OL}	Output LOW Voltage	–	–	–	0.40	V
I_{OL}	Output LOW Current	–	–	12	–	mA
I_{LKG}	Leakage Current	–	–	100	–	nA

Table 101. Electrical Characteristics – IRQ, SDWN_B, MODEM_OFF_B, PWRBTN_B

Conditions unless otherwise specified: T_A = 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VGPIO0	Input Power Supply	C_{IN} = 1µF	1.71	1.8	1.89	V
V_{OL}	Output LOW Voltage		–	–	0.40	V
V_{OH}	Output HIGH Voltage		VGPIO0 – 0.40	–	–	V
I_{OL}	Output LOW Current		–	4.0	–	mA
I_{OH}	Output HIGH Current		–	4.0	–	mA
t_{RISE}	Rise Time	C_L= 150pF, 10% to 90%, GBD	10	–	45	ns
t_{FALL}	Fall Time	C_L= 150pF, 90% to 10%, GBD	10	–	45	ns

Table 102. Electrical Characteristics – PROCHOT_B

Conditions unless otherwise specified: T_A = 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OL}	Output LOW Voltage		–	–	0.40	V
I_{OL}	Output LOW Current		–	12	–	mA
I_{LKG}	Leakage Current		–	100	–	nA

7.18 I2C Interface

The P91E0 is a slave device only. It is designed to operate with a wide frequency range of 100kHz to 3.4MHz (Standard Mode and High-Speed Mode). The PMIC is accessed using a 7-bit addressing scheme. The P91E0 I2C slave is not allowed to stretch the clock and is capable of being multi-mastered in a debugging environment. The I2C bus is only used for non-latency critical register access and communication between the SoC and P91E0 and is active when PLTRST_B is de-asserted. The I2C pins are open-drain and need pull-up resistors to a voltage in the range from 1.8 to 5.25V.

Table 103. Electrical Specifications – I2C

Conditions unless otherwise specified T_A = 25°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Typical Pull-up Voltage		1.71	1.8	1.89	V
V_{IL}	Input LOW Voltage		–	0.3 × VDD	–	V
V_{IH}	Input HIGH Voltage		0.7 × VDD	–	–	V
V_{HYS}	Hysteresis		0.1	–	–	V
V_{OL}	Output LOW Voltage		–	–	0.2 × V_{DD}	V
C_{PIN}	Capacitance	SDA and SCL pins; GBD	2	–	5	pF
t_{FALL_HS}	t_{FALL} – High Speed	3.33Mb/s operation; GBD	10	–	40	ns
t_{FALL_FS}	t_{FALL} – Full Speed	400Kb/s operation; GBD	20	–	300	ns
t_R/t_F	Rise and Fall Times	GBD	30	–	70	%

The P91E0 supports the standard I2C read and write functions. The configuration register space is one 256-byte partition. The P91E0 supports four 7-bit device addresses configurable via the PMIC_ADR_CONFIG bits[1:0] in the *EXP2* register (92$_{HEX}$; see Table 104). The address can be configured as 5E$_{HEX}$ (1011110$_{BIN}$), 6E$_{HEX}$ (1101110$_{BIN}$), 4F$_{HEX}$ (1001111$_{BIN}$), or 77$_{HEX}$ (1110111$_{BIN}$) to allow for cases where multiple P91E0s are used on the same board or other I2C address conflicts arise. Note that in 8-bit format (7 bits for the address and 1 bit for R/W), these addresses correspond to BC$_{HEX}$, DC$_{HEX}$, 9E$_{HEX}$, and EE$_{HEX}$ for writes, and BD$_{HEX}$, DD$_{HEX}$, 9F$_{HEX}$, and EF$_{HEX}$ for reads as shown in Table 105.

Table 104. I2C Addresses Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
EXP2	R/W	RSVD						PMIC_ADR_CONFIG		00$_{HEX}$	92$_{HEX}$

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000$_{BIN}$
D[1:0]	PMIC_ADR_CONFIG	7-bit device address configuration: 00 = 5E$_{HEX}$ 01 = 6E$_{HEX}$ 10 = 4F$_{HEX}$ 11 = 77$_{HEX}$	00$_{BIN}$

Table 105. I2C Address Options

Address Option Selected by PMIC_ADR_CONFIG Bit Field	7-Bit	8-Bit (Write)	8-Bit (Read)
Device 1	5E$_{HEX}$	BC$_{HEX}$	BD$_{HEX}$
Device 2	6E$_{HEX}$	DC$_{HEX}$	DD$_{HEX}$
Device 3	4F$_{HEX}$	9E$_{HEX}$	9F$_{HEX}$
Device 4	77$_{HEX}$	EE$_{HEX}$	EF$_{HEX}$

Reading data back from the P91E0 registers follows the "combined protocol" as described in the I2C specification in which the first byte written is the register offset to be read and the first byte read (after a repeat START condition) is the data from that register offset. Refer to Figure 4 and Figure 5 for details.

The following diagrams capture the different high-speed and fast-speed transaction format/protocol.
Sequential offset accesses within a single transaction ("burst" reads and writes) are supported by the P91E0's I2C module.

Figure 4. I2C Fast Speed Write

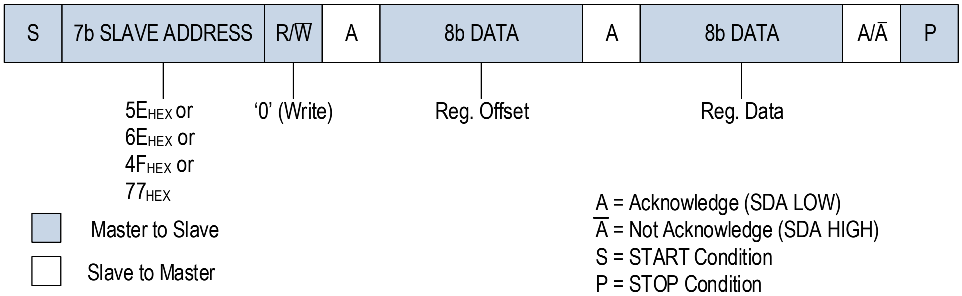


Figure 5. I2C Fast Speed Read

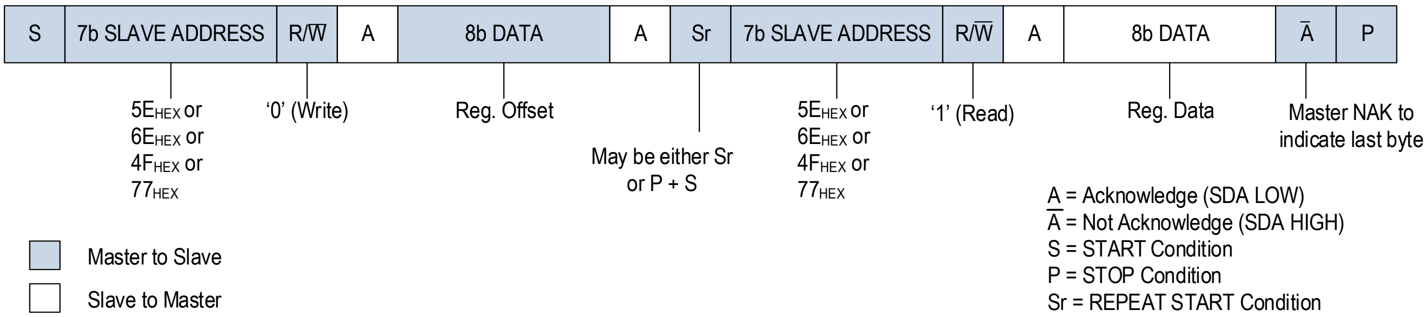


Figure 6. I2C High Speed Write

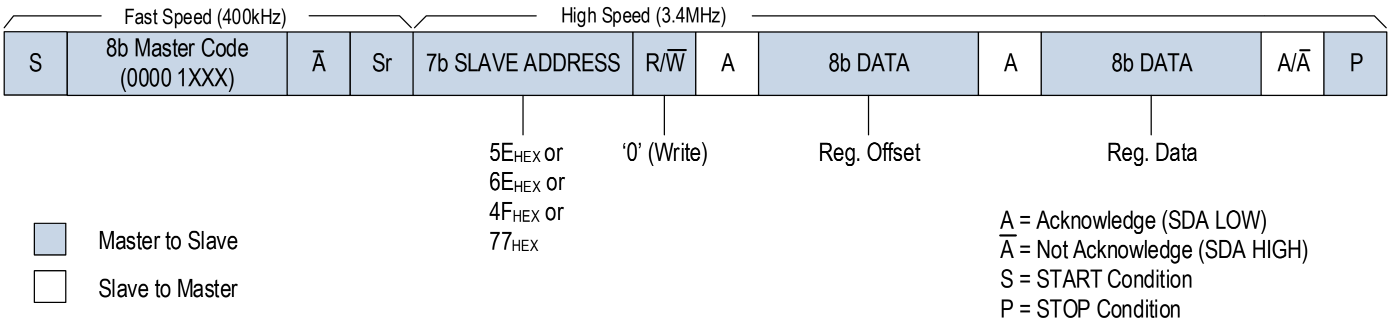
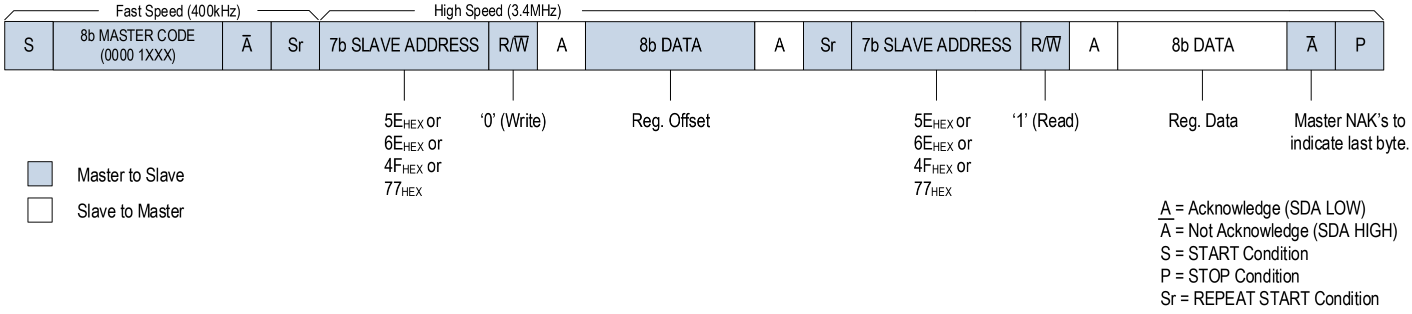


Figure 7. I2C High Speed Read



7.18.1 Register Requirements

Two read-only registers are provided to allow the customer to track the vendor and revision of their P91E0 chip as defined in Table 106 and Table 107.

Table 106. Vendor Identification Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VENDOR_ID	R	VENDOR_ID[7:0]								28_{HEX}	00_{HEX}

Table 107. Chip Revision Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
REVISION	R	RSVD		MAJREV0[2:0]			MINREV0[2:0]			02_{HEX}	01_{HEX}

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00_{BIN}
D[5:3]	MAJREV0[2:0]	Major Revision: The first stepping should start with '000' and increment by 1 for each new complete mask stepping. 000 = A 100 = E 001 = B 101 = F 010 = C 110 = G 011 = D 111 = H	000_{BIN}
D[2:0]	MINREV0[2:0]	Minor Revision: The first stepping should start with '000' and increment by 1 for each new metal layer stepping. Resets to '000' when MAJREV increments. 000 = 0 100 = 4 001 = 1 101 = 5 010 = 2 110 = 6 011 = 3 111 = 7	010_{BIN}

7.19 Analog-to-Digital Converter (ADC)

The P91E0 includes a general purpose 10-bit analog-to-digital converter. It is used for measuring system voltages, die temperature, and regulator output currents, and it places the conversion results in the *RSLT* registers. Table 108 summarizes the various channels of the ADC.

Table 108. ADC Channels

Channel	Description	External Pins	Signal Range	RSLTh	RSLTl
1	P91E0 Die Temperature	Internal	-30˚C to 125˚C	$7E_{HEX}$	$7F_{HEX}$
2	VSYS Voltage	VSYS	3V to 5.525V	80_{HEX}	81_{HEX}
3	System Voltage 0	GPIO[10]/ADC[0]	0 to 1.2V	74_{HEX}	75_{HEX}
4	System Voltage 1	GPIO[11]/ADC[1]	0 to 1.2V	76_{HEX}	77_{HEX}
5	System Voltage 2	GPIO[12]/ADC[2]	0 to 1.2V	78_{HEX}	79_{HEX}
6	DCD0 Current	Internal	DCD0 maximum current	84_{HEX}	85_{HEX}
7	DCD1 Current	Internal	DCD1 maximum current	86_{HEX}	87_{HEX}
8	DCD2 Current	Internal	DCD2 maximum current	$8C_{HEX}$	$8D_{HEX}$
9	DCD5 Current	Internal	DCD5 maximum current	88_{HEX}	89_{HEX}
10	DCD6 Current	Internal	DCD6 maximum current	$8A_{HEX}$	$8B_{HEX}$

[a] The alternate function of the pin must be enabled and the direction must be set to use the ADCx function.

7.19.1 Current Monitor

The switching regulators DCD0, DCD1, DCD2, DCD5, and DCD6 are monitored for output current. The current sensing is done internally with 100µs filtering. The filtered current is digitalized by using a 10-bit ADC (see section 7.19) and stored in 2 x 8 bits registers for each voltage rail in both SVID and I2C registers shown in 9.11.

Table 109. Analog-to-Digital Converter Electrical Characteristics

Conditions unless otherwise specified: T_A = 25°C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V_{REF}	ADC Reference Voltage	Internally provided	–	1.2	–	V
$I_{DD(ADC)}$	Supply Current	Full-scale current	–	60	–	µA
RES	ADC Resolution		–	10	–	Bits
INL	Integral Nonlinearity	GBD	-2	–	+2	LSB
DNL	Differential Nonlinearity	GBD	-1	–	+1	LSB
Gain	Gain Error	Midscale	-1.2	–	+1.2	%
$V_{MEAS(ADC)}$	ADC Input Voltage	External pins ADC[2:0]	0	–	1.2	V
		VSYS	0	–	5.6	V
SF	Voltage Scale Factor	External pins ADC[2:0]	–	1.0	–	V/V
		VSYS	–	$\frac{3}{14}$	–	V/V
$R_{IN(ADC[x])}$	ADC[2:0] Input Resistance		–	10	–	MΩ

7.20 Power Buttons PWRBTNIN_B and PMIC_EN

The P91E0 offers two ways to trigger the system to power ON or OFF: the PMIC_EN and PWRBTNIN_B pins. It is recommended that only one power ON/OFF method is used, either with PWRBTNIN_B or PMIC_EN. If PWRBTNIN_B is used, PMIC_EN should be connected to GND. If PMIC_EN is used to power the P91E0 ON/OFF, the PWRBTNIN_B pin should be left floating (unconnected). However, the PWRBTNIN_B pin is still monitored and will pass level changes to the PWRBTN_B output. When the P91E0 is used with DPU(s), PWRBTNIN_B (or PMIC_EN when used) should not be asserted until the DPUs' input voltage is above their UVLO level.

7.20.1 PMIC Enable (PMIC_EN)

PMIC_EN is an active-HIGH signal and is usually driven by a system controller or power-good signal of a pre-regulator. After the PMIC_EN pin has been asserted HIGH, the P91E0 powers on without delay and the rails are turned on following the programmed sequence. PMIC_EN can be asserted HIGH above its V_{IH} after VSYS has reached a steady-state level and is above $VSYSREF_R$ (see Table 122). This can be achieved by adding an RC filter (e.g. 10kΩ and 1µF) from VSYS to the PMIC_EN pin. De-asserting the PMIC_EN signal initiates a shutdown of all rails, following the programmed shut-down sequence (Cold OFF). When the P91E0 is enabled with PMIC_EN assertion, a de-assertion is required for the next re-enabled cycle after a shutdown event (due to faults or PWRBTNIN_B held > 4s). To disable the rails, pull PMIC_EN below its V_{IL} for a time equal to the Cold OFF duration. The V_{IL} and V_{IH} thresholds for various VSYS input voltages (±10% tolerance included) are listed in Table 110.

Table 110. V_{IL} and V_{IH} Levels for PMIC_EN for Various VSYS Input Voltages

V_{SYS} Input Voltage (V)	PMIC_EN V_{IL}(V)	PMIC_EN V_{IH} (V)
3.3	0.60	1.35
4.0	0.70	1.50
5.0	0.80	1.70

7.20.2 Power Button Input (PWRBTNIN_B) and Power Button Output (PWRBTN_B)

The power button pin (PWRBTNIN_B) is an active-LOW input to the P91E0. It is internally connected to VSYS through a weak pull-up current source (50µA, ±10%). It includes a 30ms de-bouncing circuit to ensure that spurious transitions are not logged while the switch contacts bounce on initial contact. The output of the de-bouncing circuit enters the edge-detect circuits. A falling edge below V_{IL} can trigger a transition out of the SoC-G3 State. This pin is usually connected through a push-button switch to ground (below V_{IL}). Pressing the PWRBTNIN_B button longer than 36ms (30ms typical) will turn on the P91E0. If the P91E0 is powered-on, holding down the power button for longer than 4.24 seconds (for the default setting of 4 seconds) will force a Cold OFF. The LOW (V_{IL}) and HIGH (V_{IH}) thresholds of PWRBTNIN_B depend on V_{SYS} for the Normal Power Mode of operation as shown in Table 111 with the thresholds for the Debug Mode (special entry mode before rails are powered up).

Table 111. V_{IL} and V_{IH} Levels for PWRBTNIN_B

Operating Mode	PWRBTNIN_B V_{IL}(V)	PWRBTNIN_B V_{IH} (V)
Normal Power Mode	$0.19 \times V_{SYS}$	$0.81 \times V_{SYS}$
Debug Mode	$0.69 \text{ x } V_{SYS}$	$0.81 \times V_{SYS}$

The output of the de-bouncing circuit also goes to the timer logic block that measures the length of time that the power button has been held down, and this value can be read from the hold time field (PBHT[3:0]) in the *PBSTATUS* register (see Table 113). The P91E0 always passes the power button information via the output signal PWRBTN_B to the SoC. The PWRBTN_B pin is a level-shifted copy of PWRBTNIN_B after the 30ms de-bouncing circuit. PWRBTN_B is valid when control signal RSMRST_B = 1 (de-asserted).

If the system is off (SoC-G3 state), pressing the power button by itself for greater than 36ms (30ms typical) will cause the PMIC to turn on all the “A” type rails, de-assert RSMRST_B (PWRBTN_B should be HIGH before this), and pass the power button information to the SoC. If the system is on (SoC-S4/S5, SoC-S3, SoC-S0Ix, and SoC-S0 states), pressing this button will cause the P91E0 to pass a level-shifted copy of PWRBTNIN_B (via PWRBTN_B) after the 30ms de-bouncing circuit to the SoC, which will initiate actions for the P91E0 to perform.

7.20.3 Forcing a Cold OFF using the Power Button

The signal from the power button is fed into a fault timer which measures the time from when the button is pressed until it is released. This duration (in half-seconds) can be read from the hold time bit field, PBHT[3:0]. The timer retains this value until the next time both buttons are pressed simultaneously, or if the timer logic is reset by the CLRHT bit in the *PBCONFIG* register (see Table 112).

The P91E0 triggers a Cold OFF if the fault timer exceeds the duration set in the fault time field (FLT[3:0]) in the *PBCONFIG* register with a default setting of 4 seconds (4.24 seconds to include margin). If enabled (FLT is not equal to 0_{HEX}), the power-down logic compares the hold time bits to the fault time bits and forces a Cold OFF upon a match.

If software control is desired, FLT can be set to 0_{HEX} during the P91E0 initialization, but this default will allow a forced power-down if for some reason the software cannot boot properly. Software must set the CLRHT bit in PBCONFIG before updating FLT to prevent the fault condition from possibly triggering immediately from a previous value.

7.20.4 Configuration Registers

Table 112. Power Button Configuration Register

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PBCONFIG	R/W	RSVD		CLRHT	CLRFLT	FLT[3:0]				08_{HEX}	26_{HEX}

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00_{BIN}
D[5]	CLRHT	This bit is self-clearing and always reads 0: 0 = No action performed. 1 = Reset the HT timer logic.	0_{BIN}
D[4]	CLRFLT	This bit is self-clearing and always reads 0: 0 = No action performed. 1 = Reset the FLT timer logic.	0_{BIN}
D[3:0]	FLT[3:0]	Time that the power button has to be held down, in half-second intervals, before a system shut-down is triggered. Recommendation: Hold down the power button with an additional time duration of 6% from the setting. 0000 = Disabled. 0001 = 0.5 second. 0010 = 1.0 seconds. 0011 = 1.5 seconds. 0100 = 2 seconds. ... 1111 = 7.5 seconds.	1000_{BIN}

Table 113. Power Button Status Register

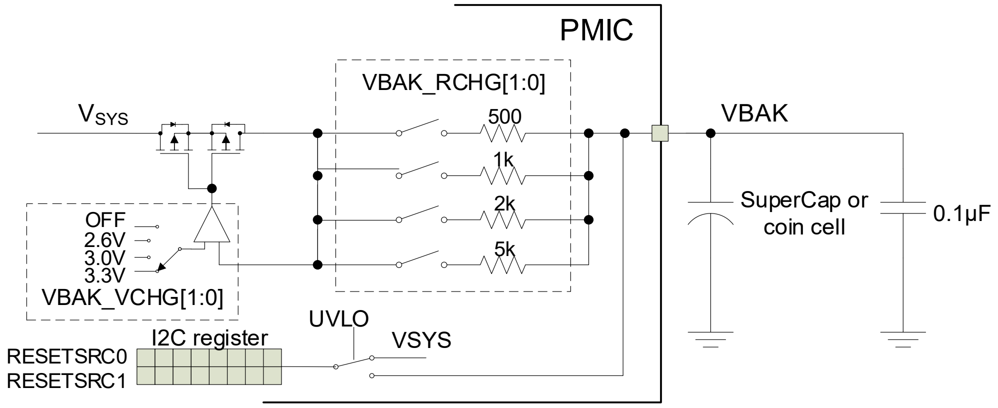
Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PBSTATUS	R/W	RSVD			PBLVL	PBHT[3:0]				10_{HEX}	27_{HEX}

Bit	Name	Function	Default
D[7:5]	RSVD	Reserved	000_{BIN}
D[4]	PBLVL	0 = Power button pressed. 1 = Power button released.	1_{BIN}
D[3:0]	PBHT	Time that the power button has been held down, in half-second intervals: 0000 = 0 seconds. 0001 = 0.5 second. 0010 = 1.0 seconds. 0011 = 1.5 seconds. 0100 = 2 seconds. … 1111 = 7.5 seconds.	0000_{BIN}

7.21 VBAK Charger

The P91E0 is capable of charging an external super cap or coin cell. The charger output is on the VBAK pin. The VBAK voltage domain powers two PMIC-internal registers which store system events, such as over-temperature shutdown or UVLO shutdown, and the charger configuration VBAK_VCHG and VBAK_RCHG. See Table 140.

Figure 8. VBAK Charger Block Diagram



If VSYS is disconnected and below the UVLO threshold, VBAK is powered by the SuperCap or coin cell and will retain information until the battery or SuperCap voltage on VBAK drops below 0.8V and stored data is reset.

The charger output remains active after the P91E0 enters SoC-G3 state; however, after the system exits SoC-G3 via PWRBTNIN_B, the charger registers VBAK_VCHG and VBAK_RCHG are reset and must be re-enabled via I2C.

Table 114. Electrical Characteristics – VBAK

V_{SYS}= 5.0V, C_O = 1µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.

Symbol	Parameter	Conditions		MIN	TYP	MAX	Units
$V_{O(BAK)}$	Output Voltage Setting	VBAK_VCHG[1:0] = 00 in the *RESETSRC1* register (see Table 140)			Disabled		V
		VBAK_VCHG[1:0] = 01			2.6		
		VBAK_VCHG[1:0] = 10			3.0		
		VBAK_VCHG[1:0] = 11			3.3		
I_{SHDN}	Shutdown Current				790		µA
	Regulation Voltage Accuracy			-2		+2	%
$R_{CHG(BAK)}$	Internal Series Resistance	VBAK_RCHG[1:0] = 00 in the *RESETSRC1* register (see Table 140)			500		Ω
		VBAK_RCHG[1:0] = 01			1k		
		VBAK_RCHG[1:0] = 10			2k		
		VBAK_RCHG[1:0] = 11			5k		
$I_{LIM(BAK)}$	Maximum Output Current	VBAK_VCHG[1:0] (VSYS = 3.5V to 5.25V VBAK_RCHG[1:0] = 500Ω)	2.6V	0.95	1.1	1.25	mA
			3.0V	1.65	1.9	2.15	
			3.3V	2.15	2.5	2.85	

8. Theory of Operation

Also see section 6 for an overview of P91E0 PMIC operation.

8.1 Control Signals

8.1.1 RSMRST_B

The resume reset is an output signal. When all A-rails are switched on and are in regulation, the RSMRST_B pin is pulled HIGH to VGPIO1 (3.3V). RSMRST_B is pulled LOW when the A-rails regulators are powered down and the device enters SoC-G3 State.

8.1.2 DRAMPWROK

DRAMPWROK is an open-drain output signal. The DRAMPWROK pin is pulled HIGH when DCD2 (SOC VDDQ rail) is above 90% of its regulating voltage during the soft-start process. DRAMPWROK is logic LOW when DCD2 is shutdown.

8.1.3 VCCAPWROK

VCCAPWROK is an active-HIGH open-drain output signal. The VCCAPWROK pin asserts when the soft-start sequences for all the voltage rails assigned to be on in the S0Ix and S0 groups are completed with the delay defined by the DTPWROK bit field in the *PWRSEQCFG* register ($2A_{HEX}$; see Table 83) from the first assertion of the last event defined in the SX group (i.e., timing group number 14). VCCAPWROK de-asserts without delay in the S3 state. The nominal voltage of VCCAPWROK is HIGH when asserted and 0V when de-asserted.

8.1.4 COREPWROK

COREPWROK is an active-HIGH dedicated output signal. The COREPWROK pin asserts when the soft-start sequences for all the voltage rails assigned to be on in the S0Ix and S0 groups are completed with the delay defined by the DTPWROK bit field in the *PWRSEQCFG* register ($2A_{HEX}$; see Table 83) from the first assertion of the last event defined in the SX group (i.e., timing group number 14). COREPWROK de-asserts without delay in the S3 state. The nominal voltage of COREPWROK is VGPIO1 (3.3V) when asserted, 0V when de-asserted. COREPWROK does not de-assert in the S0Ix state.

8.1.5 Shallow Sleep State (SLP_S0Ix_B)

SLP_S0Ix_B is an input signal from the SoC indicating Shallow Sleep State. When the SLP_S0Ix_B pin is pulled LOW, the SoC launches the Shallow Sleep State entry task list. All the active SX-type switching regulators are placed in the Power Save Mode as defined for the S0Ix state. Prior to initiating the Shallow Sleep State entry, the SoC will program exit VID values for VCC over SVID and communicate Standby State information to the PMIC over I2C.

8.1.6 Sleep State 3 (SLP_S3_B)

SLP_S3_B is a dedicated input pin for enabling and disabling the low-power Sleep State 3. When SLP_S3_B is pulled LOW, Sleep State 3 is initiated, and all S-type rails are turned off according the timing diagram. Prior to activating this sleep state, the SoC will program the exit VID values for VCC/VNN over SVID and communicate standby state information to the P91E0 via I2C. It is valid when RSMRST_B = 1 (i.e., de-asserted) regardless of the SLP_S0Ix_B state. In the previous SoC and PMIC generations, SLP_S0Ix_B is required to be asserted before asserting SLP_S3_B LOW. For P91E0 if SLP_S3_B=0 (asserted) while SLP_S0Ix_B=1 (de-asserted), then the SX-type rails will be sequenced off first followed by the S-type rails.

8.1.7 Deep Sleep State (SLP_S4_B)

SLP_S4_B is a dedicated input pin for enabling and disabling the Deep Sleep State. When pulled LOW, Deep Sleep State is initiated, and all U-type rails are turned off according the timing diagram. Prior to activating the Deep Sleep State, the SoC will program exit VID values for VCC/VNN via SVID and communicate Standby State information to the P91E0 via I2C. SLP_S4_B is valid when the pins RSMRST_B = 1 (de-asserted) and SLP_S3_B = 0 (asserted). If SoC asserts SLP_S# signals simultaneously, P91E0 will operate in sequential order following the configuration setting.

8.1.8 Platform Reset (PLTRST_B)

Platform reset pin is an input signal from the SoC that indicates the SoC has already come out of reset upon de-assertion (PLTRST_B = 1). The nominal voltage of the PLTRST_B pin is 0V when asserted, 1.8V when de-asserted.

8.1.9 Suspend Power-Down Acknowledgement (SUSPWRDNACK)

Suspend Power-Down Acknowledgement is an input signal from the SoC on the SUSPWRDNACK pin telling the PMIC to turn off all A-type rails. It is valid when RSMRST_B = 1 (de-asserted) and SLP_S4 = 0 (asserted). The nominal voltage of SUSPWRDNACK is 1.8V when asserted and 0V when de-asserted.

8.1.10 Interrupt Request (IRQ)

The interrupt request is an output signal generating interrupts to the SoC. It is pulled HIGH when at least one unmasked interrupt bit is set in the *IRQLVL1* level 1 interrupt register (02_{HEX}; see Table 142). It is valid when RSMRST_B = 1 (de-asserted). IRQ is pulled HIGH to VPGIO0 (1.8V nominal) and 0V when pulled LOW. The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms. Refer to section 9.6 for further details.

8.1.11 Thermal Trip (THERMTRIP_B)

THERMTRIP_B is an active-LOW dedicated input signal that notifies the P91E0 of an SoC thermal event. The THERMTRIP_B pin status is valid when RSMRST_B = 1 and PLTRST_B = 1 (de-asserted). The nominal voltage of THERMTRIP_B is 0V when asserted, 1.8V when de-asserted. Upon sensing that the THERMTRIP_B signal has transitioned LOW, the P91E0 must shut down all rails immediately (hard shut-down, not executing a Cold-Off task list). To avoid spurious detection during power sequencing, the THERMTRIP_B signal is only to be sampled if PLTRST_B is de-asserted.

8.1.12 Processor HOT (PROCHOT_B)

PROCHOT_B is an active-LOW, open-drain output signal used to notify the SoC of a thermal event affecting the P91E0, battery, or system. The PROCHOT_B pin will be asserted when the P91E0 temperature, battery temperature, or system temperature has crossed the alert thresholds defined in the thermal monitoring section. It is valid when RSMRST_B = 1 and PLTRST_B = 1 (de-asserted). The nominal voltage of PROCHOT_B is 0V when asserted and 1.8V when de-asserted. The SoC must go into a lower power state until the P91E0 thermal event is cleared and the pin is de-asserted.

8.1.13 Shutdown Warning (SDWN_B)

The shut-down warning is an output signal sent from P91E0 to the modem as a warning that a system shut-down event is about to take place. During power down task lists, the SDWN_B pin is pulled to ground. If the power-down is not initiated, the output signal is pulled HIGH (1.8V).

If the P91E0 enters a catastrophic shutdown condition that would normally bypass a Cold OFF Task List being run, the SDWN_B pin is asserted a minimum of 90µs prior to this catastrophic shutdown commencing.

The nominal voltage of SDWN_B is 0V when asserted and pulled HIGH to VPGIO0 (1.8V) when de-asserted.

8.2 SVID Interface

Table 115. Electrical Characteristics – SVID_CLK, SVID_DIO, SVID_ALERT_B

Conditions unless otherwise specified: T_A= 25°C.

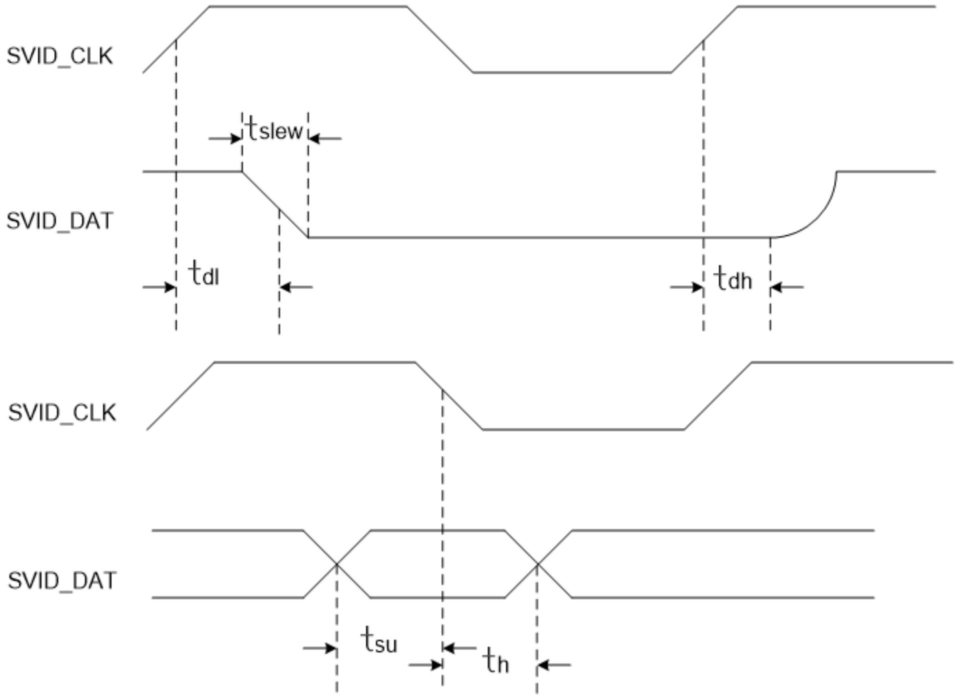
Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V_{CC}	I/O Voltage	–	1.0	1.05	1.1	V
V_{OL}	Output Voltage LOW	ILOAD = 3mA	–	–	0.367	V
V_{IL}	Input LOW Voltage	V_{CC} = 1.05V nominal	–	–	0.451	V
V_{IH}	Input HIGH Voltage	V_{CC} = 1.05V nominal	0.6825	–	–	V
I_{LKG}	Leakage Current	V_{CC} = 1.08V	–	100	–	nA

Table 116. SVID Signal Group AC Specification

Note: Measure at 0.5 × Vcc, with 30pF test load, Rpu = 85Ω, and series R = 20Ω.

Symbol	Parameter	MIN	TYP	MAX	Units
t_{slew}	TX pad Slew Rate	2.9	2.9	3.1	ns
t_{dl}	Tx Rising Clock to Data Output Delay	3.2	6.7	7.3	ns
t_{dh}	Tx Falling Clock to Data Output Delay	5.5	5.7	5.8	ns
t_{su}	Rx Data Setup Time to CLK Rising Edge	6			ns
t_h	Rx Data Hold Time to CLK Rising Edge	4			ns

Figure 9. Tx Timing (SVID)



8.2.1 Serial Voltage Identification (SVID)

To dynamically adjust the voltage settings of the SoC rails, the SoC communicates with the P91E0 through the SVID interface. The SVID commands comprise 9 bits: 4 MSBs determine the address and 5 LSBs are the command bits. The P91E0 supports 3 SVID-controlled voltage regulators: DCD0, DCD1, and DCD2. The SVID address of each voltage regulator can be changed via OTP setting or an I2C register write.

Table 117. SVID_EN – SVID EN Setting for DCD0/DCD1/DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
S0Ix_EN	R/W	RSVD					S0Ix_DCD2	S0Ix_DCD1	S0Ix_DCD0	00_{HEX}	AB_{HEX}

Bit	Name	Function	Default
D[7:3]	RSVD	Reserved	00000_{BIN}
D[2]	S0Ix_DCD2	SVID=0: 0 = No Sleep Mode support 1 = Rail slews to lower voltage in Sleep Mode SVID=1: 0 = No S0Ix Mode support 1 = Rail slews to lower voltage defined in VID_S0Ix (SVID domain)	0_{BIN}
D[1]	S0Ix_DCD1	SVID=0: 0 = No Sleep Mode support 1 = Rail slews to lower voltage in Sleep Mode SVID=1: 0 = No S0Ix Mode support 1 = Rail slews to lower voltage defined in VID_S0Ix (SVID domain)	0_{BIN}
D[0]	S0Ix_DCD0	SVID=0: 0 = No Sleep Mode support 1 = Rail slews to lower voltage in Sleep Mode SVID=1: 0 = No S0Ix Mode support 1 = Rail slews to lower voltage defined in VID_S0Ix (SVID domain)	0_{BIN}

Table 118. SVID_ID – SVID ID Setting for DCD0/DCD1/DCD2

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
SVID_ID	R/W	RSVD		SVID_ID_DCD2		SVID_ID_DCD1		SVID_ID_DCD0		00	AC_{HEX}

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved	00_{BIN}
D[5:4]	SVID_ID_DCD2	DCD2 SVID address: 00_{BIN} = 2_{HEX} (default) 01_{BIN} = 0_{HEX} 10_{BIN} = 1_{HEX} 11_{BIN} = 3_{HEX}	00_{BIN}
D[3:2]	SVID_ID_DCD1	DCD1 SVID address: 00_{BIN} = 1_{HEX} (default) 01_{BIN} = 0_{HEX} 10_{BIN} = 2_{HEX} 11_{BIN} = 5_{HEX}	00_{BIN}
D[1:0]	SVID_ID_DCD0	DCD0 SVID address: 00_{BIN} = 0_{HEX} (default) 01_{BIN} = 1_{HEX} 10_{BIN} = 3_{HEX} 11_{BIN} = 4_{HEX}	00_{BIN}

8.2.2 Serial Voltage Identification (SVID) Command Set

DCD0, DCD1, and DCD2 implement the VR12.1/IMVP8 SVID protocol. Table 119 lists the SVID command set supported by the P91E0.

Note: Refer to Intel's Serial VID (SVID) protocol specification for details.

Table 119. Serial Voltage Identification (SVID) Command Set

#	Command	Master Payload Contents	Slave Payload Contents	Description
01_{HEX}	SetVID-fast (individual address and all call addresses)	VID code	NA	Applicable for DCD0, DCD1 and DCD2. This command sets the new VID target; the voltage regulator (VR) jumps to the new VID target with a controlled (up or down) slew rate programmed by the VR. When the VR receives a VID command to increase the voltage, it will exit all low-power states and enter the normal state to ensure the fastest slew rate to the new voltage. The VR sets the VR_settled bit [D0] in the *Status_1* register for SVID (see Table 121) and issues an alert when the VR has reached the new VID target.
02_{HEX}	SetVID-slow (individual address and all call addresses)	VID code	NA	Applicable for DCD0, DCD1 and DCD2. This command sets the VID target; the VR jumps to the new VID target with a controlled slew rate (up or down) programmed by the VR. When VR receives a VID command to increase the voltage, it will exit all low-power states and enter the normal state. The VR sets the VR_settled bit and issues an alert when VR has reached the new VID target. An SVID read back of the Slow_Rate bit field in the *Slew Rate Slow* register (25_{HEX}) (see Table 120) is always 2.5mV/µs.
03_{HEX}	SetVID-decay (individual address and all call addresses)	VID code	NA	Applicable for DCD0, DCD1 and DCD2. This command sets the VID target; the VR jumps to the new VID target but *does not* control the slew rate. The output voltage decays at a rate proportional to the load current. SetVID-decay is only used in the VID down direction and implies VR enters the PS2 State. The VR sets the VR_settled bit [D0] in the *Status_1* SVID register, and the SVID_ALERT_B pin is asserted for SetVID-decay.
04_{HEX}	SetPS	Byte indicating the power status of the voltage rail	NA	Applicable for DCD0, DCD1 and DCD2. The SoC uses this command to set the power state of the VR according to the core P-state and C-state so that the VR controller can be configured to improve efficiency, especially at light loads.
05_{HEX}	SetRegADR (individual address only; NAK all call addresses)	Address of the index in the data table	NA	Sets the address pointer in the data register table. Typically the next command, SetRegDAT, is the payload that gets loaded into this address. However for multiple writes to the same address, only one SetRegADR is needed.
06_{HEX}	SetRegDAT (individual address only; NAK all call addresses)	New data register contents	NA	Writes the contents to the data register that was previously identified by the address pointer with SetRegADR.
07_{HEX}	GetReg (individual address only; NAK all call addresses)	Define which register	Specified register contents	Slave returns the contents of the specified register as the payload. The majority of the VR monitoring data is accessed through the GetReg command.

8.2.3 VR 12.1 Compatibility

The P91E0 has been developed according to the VR12.0 specification but does support the VR12.1 extension with the IMVP8 features required for the Intel© "Apollo Lake" SoC. Table 120 documents the implementation.

Table 120. VR12.1 Compliance

Note: In the following table, R = required, O = optional, Yes = supported, and No = not supported.

Feature	VR12.1	P91E0	Notes
VID 0.25-1.52V	R	0.25V to 1.30V	0.5V to 1.30V according to the Apollo Lake Specification.
Dynamic VID Fast	R	Yes	Minimum or target slew rate.
Dynamic VID Slow	R	Yes	Minimum or target slew rate.
Decay Slew Rate	R	Yes	
Voltage Settled	R	Yes	
PS0/PS1 VR Power States	R	Yes	Normal Power Mode.
PS2 - VR Power State	R	Yes	Very Low Power Mode.
PS3 - VR Power State	R	Yes	Ultra-Low Power State.
PS4 - VR Power State	R	Yes	Near Off Mode.
Temperature Maximum	O	Yes	OTP or pin programmed; read by master; supports temperature zones and the VR_HOT trip point (the VR_HOT pin is equivalent to the PROCHOT_B pin on the P91E0).
Temperature Sensor Input	R	Yes	Rails that support turbo must have temperature sensor inputs.
DCLL	R	Yes	Register support for OTP programming of DCLL is optional. However, DCLL programmability is required.
Enable	R	Yes	VR enable.
VR Ready	R	Yes	Single-phase output ready.
VR_Hot#	R	Yes	Active-LOW thermal monitor output, utilizing either temperature sensor input.
Address	R	Yes	OTP or pin programmed.
Capability (06_{HEX})	1xxx $xxx1_{BIN}$	Yes	
Icc_Max (21_{HEX})	R	Yes	Must be programmed by the platform designer to reflect the capability of the platform. The default 00_{HEX} indicates this value is not programmed and the platform will not boot.
Temp_Max (22_{HEX})	O	No	
Slew Rate Fast (24_{HEX})	R	Yes	Indicate the slew-rate fast capability of the VR.
Slew Rate Slow (25_{HEX})	R	Yes	Indicate the slew-rate slow capability of the VR.
Vboot (26_{HEX})	R	Yes	OTP or pin programmed; not read by the master. The PWM must support various VBOOT levels.
VR Tolerance (27_{HEX})	O	No	Optional read by master.
Current Calibration Offset (28_{HEX})	O	No	OTP or pin programmed; not read by master; used in PWM only.

Feature	VR12.1	P91E0	Notes
Temp Calibration (29_{HEX})	O	No	OTP or pin programmed; not read by master; used in PWM only.
Vout Max (30_{HEX})	R	Yes	Programmed by master.
Voltage Offset (33_{HEX})	R	Yes	Programmed by master.
Iout (15_{HEX})	R	Yes	Read by master.
VR Temperature (17_{HEX}) (ADC)	O	No	Read by master.
Output Voltage (16_{HEX}) (ADC)	O	No	Read by master.
Output Power (18_{HEX}) (ADC)	O	No	Read by master.
Temperature Zone (12_{HEX})	R	Yes	Read by master.
Multi VR Config (34_{HEX})	R	Yes	

Table 121 lists the SVID register set and the corresponding I2C register supported by the P91E0 for DCD0, DCD1, and DCD2.

For details of SVID specification, refer to Intel's specification.

Table 121. Serial Voltage Identification (SVID) Register Set

Note: See important notes at the end of the table.

SVID Register	I2C Register	Register	Description	Access (SOC)	Default
00_{HEX}	00_{HEX}	Vendor ID	Uniquely identifies the VR vendor (IDT). The vendor ID is assigned by Intel. This register is mandatory and the VR must return the assigned vendor ID.	Read Only	28_{HEX}
01_{HEX}	$B3_{HEX}$	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	Read Only	00_{HEX}
02_{HEX}	01_{HEX}	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The vendor assigns this data.	Read Only	02_{HEX}
05_{HEX}	$B4_{HEX}$	PROTOCOL_ID	Supported SVID protocol: 5_{HEX} = IMVP8.	Read Only	05_{HEX}
06_{HEX}	$B5_{HEX}$[a] $C5_{HEX}$[b] $D5_{HEX}$[c]	Capability	Supported SVID features. $C1_{HEX}$ indicates that I_{MAX} is full scale and temperature and Iout reporting are supported	Read Only	$C1_{HEX}$
10_{HEX}	$B6_{HEX}$[a] $C6_{HEX}$[b] $D6_{HEX}$[c]	Status_1	Data register read after the active-LOW SVID_ALERT_B pin is asserted, which gives the status of the VR.	Read Only	00_{HEX}
11_{HEX}	$B7_{HEX}$[a] $C7_{HEX}$[b] $D7_{HEX}$[c]	Status_2	Data register for the Status_2 data, which is the status of the SVID bus.	Read Only	00_{HEX}

SVID Register	I2C Register	Register	Description	Access (SOC)	Default
15_{HEX}	84_{HEX}[a] 86_{HEX}[b] $8C_{\text{HEX}}$[c]	DCD0/DCD1/DCD2 Output Current, Iout (H)	Running update of the conversion results from the 10-bit ADC. The upper 8 MSB of the ADC output is stored in this register.	Read Only	00_{HEX}
$1C_{\text{HEX}}$	$B8_{\text{HEX}}$[a] $C8_{\text{HEX}}$[b] $D8_{\text{HEX}}$[c]	Status2_last read	This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command (see Table 119). In the case of a communications error or parity error, when the VR is sending the payload back to the master, the master can read the *Status2_lastread* register so the alert data is not lost.	Read Only	00_{HEX}
21_{HEX}	$B9_{\text{HEX}}$[a] $C9_{\text{HEX}}$[b] $D9_{\text{HEX}}$[c]	ICC_MAX	Defines full scale for digital current reporting (in Amps). OC should be ~20% above. Use ICC_MAX = 5A + (6A × num dpu)	Read Only	05_{HEX}
24_{HEX}	BA_{HEX}[a] CA_{HEX}[b] DA_{HEX}[c]	SR_FAST	Reading this register returns the slew rate from SetVID Fast in the *DCDXSLEW* register	Read Only	14_{HEX}
25_{HEX}	BB_{HEX}[a] CB_{HEX}[b] DB_{HEX}[c]	SR_SLOW	Reading this register returns the slew rate from SetVID Slow in the *DCDXSLEW* register	Read Only	02_{HEX}
26_{HEX}	BC_{HEX}[a] CC_{HEX}[b] DC_{HEX}[c]	DCD0_VBOOT DCD1_VBOOT DCD2_VBOOT	Data register containing VBOOT voltage, which is OTP programmed, in the VR12.1 VID format; for example, 97_{HEX} = 1.0V.	Read Only	97_{HEX}
30_{HEX}	BD_{HEX}[a] CD_{HEX}[b] DD_{HEX}[c]	Vout max	This register is programmable by the master and sets the maximum VID that the VR will support. If a higher VID code is received, the VR should respond with the "Reject, not supported" acknowledge. VR12.1 VID data format. **Important:** *Vout max* must be programmed by the master during the boot up sequence if a value other than the default is selected. Offset (33_{HEX}) does not affect *Vout_max*; i.e. *VID setting* + *Offset* can be > *Vout_max*.	Read/Write	$D2_{\text{HEX}}$ (setting = 1.295V)
31_{HEX}	BE_{HEX}[a] CE_{HEX}[b] DE_{HEX}[c]	VID setting	Data register containing the currently programmed VID voltage in the VID data format. The default is 00_{HEX}; i.e., zero volts out, VR off.	Read/Write	00_{HEX}
32_{HEX}	BF_{HEX}[a] CF_{HEX}[b] DF_{HEX}[c]	PWR state	Register containing the current programmed power state. The default is 00_{HEX} = Normal Power Mode.	Read/Write	00_{HEX}

SVID Register	I2C Register	Register	Description	Access (SOC)	Default
33_{HEX}	$C0_{HEX}$[a] $D0_{HEX}$[b] $E0_{HEX}$[c]	Offset	This register sets the offset in VID steps added to the VID setting for the voltage margining. Bit 7 is the sign bit: 0 = positive margin, 1 = negative margin. Remaining 7 bits are the number of VID steps for the margin 2's complement. 00_{HEX} = no margin. 01_{HEX} = +1 VID step 02_{HEX} = +2 VID steps FF_{HEX} = -1 VID step	Read/Write	00_{HEX}
34_{HEX}	$C1_{HEX}$[a] $D1_{HEX}$[b] $E1_{HEX}$[c]	Multi_VR	This register is programmable by the master. Lock slave to current VID and power state setting, reject AllCall commands.	Read/Write	00_{HEX}
35_{HEX}	$C2_{HEX}$[a] $D2_{HEX}$[b] $E2_{HEX}$[c]	SET_REG_ADR	Scratch pad register for temporary storage of the *SetRegADR* pointer register (see Table 119)	Read/Write	00_{HEX}

[a] For DCD0.

[b] For DCD1.

[c] For DCD2.

9. Control and Monitoring

9.1.1 State Machine

The P91E0 implements a state machine that interprets a very limited "instruction set." Its purpose is to execute basic power sequencing and thermal monitoring tasks from code stored locally without requiring intervention by the hardware or software. This section outlines the functions that the state machine performs.

In the P91E0, power-state transition (power sequencing) related tasks and general purpose analog-to-digital converter tasks are handled concurrently. The intention is to ensure that power sequencing tasks are always handled in a time-deterministic manner (that is, they cannot be delayed by other tasks being requested of the ADC, etc.).

9.1.2 Execution

On power-up, the state machine begins in the Idle State. When an event occurs (the Cold Boot event is set by default), execution of tasks associated with that event are started automatically. Once the end of the task list is reached, the state machine will cease execution and return to the Idle State.

9.2 Input Power Source Detection

The P91E0 supports only analog detection of VSYS. The P91E0 can operate with a VSYS rising slew rate up to 5V/ms (measured between 10% and 90% of the target voltage), and rails with DPUs can be enabled when the DPUs' input voltage exceeds their UVLO level.

9.2.1 System Voltage (VSYS) Detection Threshold

A voltage comparator is used to compare the VSYS voltage level to a reference voltage in order to determine whether VSYS is up and valid. The output of the comparator is used to inform the P91E0 of a power state transition between the G3 and SoC-G3 states.

VSYS Rising

When the VSYS level at the comparator rises higher than the reference voltage (including the rising-edge hysteresis), VSYS is considered valid.

VSYS Falling

When the VSYS level at the comparator falls lower than the reference voltage (including the falling-edge hysteresis), VSYS is considered invalid.

The requirements of the VSYSREF analog reference voltage used as the threshold for a valid VSYS are detailed in Table 122. When the P91E0 shuts down due to VSYS falling below $VSYSREF_F$, i.e., an under-voltage lockout (UVLO) event occurs, the PVIN of the DPUs should be brought below the DPU.UVLO falling level (see the datasheet for the DPU) for a proper restart.

Table 122. VSYSREF Definition

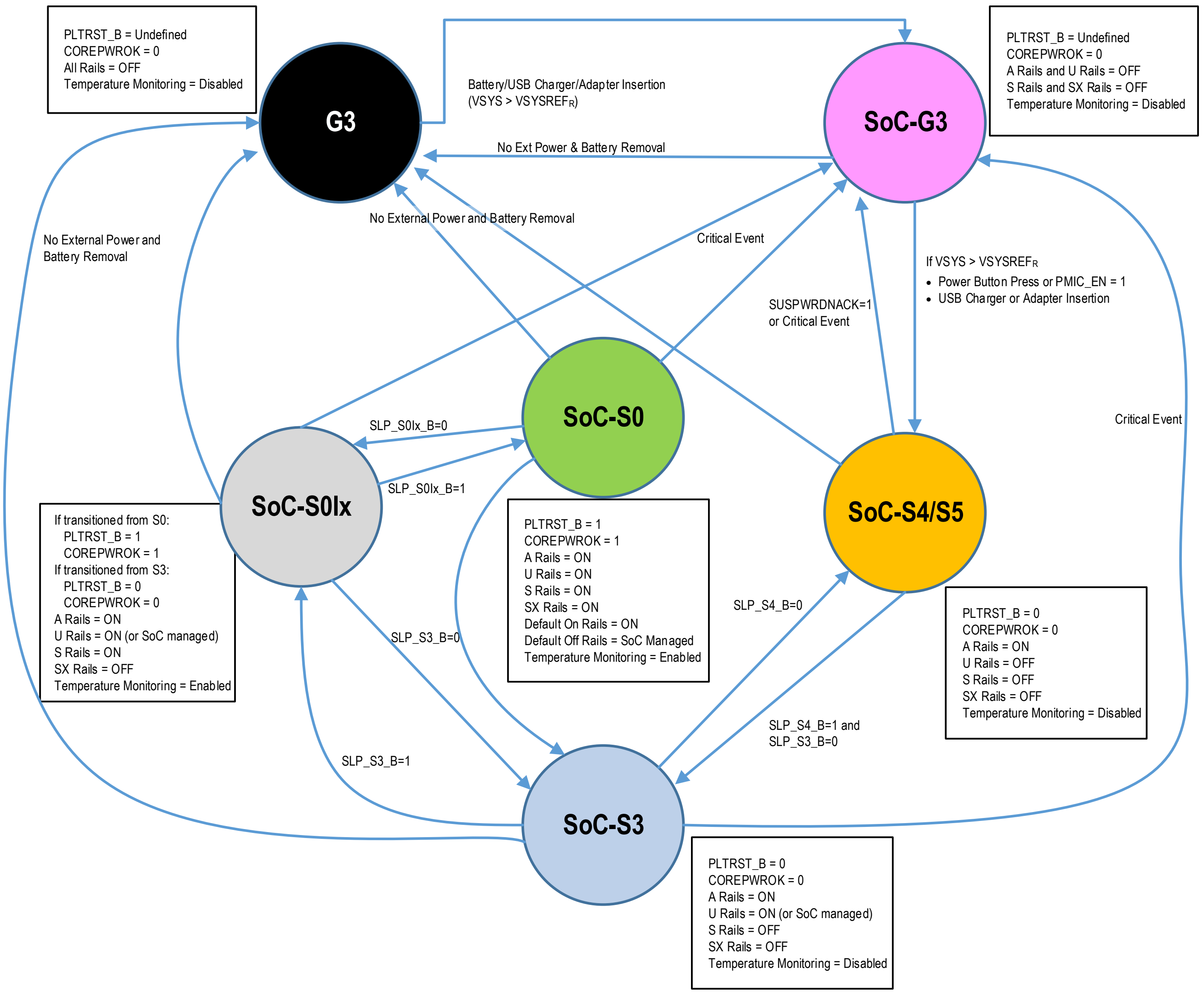
Parameter	Description	Min	Typical	Max	Unit
$VSYSREF_R$	VSYS Rising Threshold	–	2.90	–	V
$VSYSREF_F$	VSYS Falling Threshold	–	2.50	–	V

9.3 Power States

The PMIC has six defined states that are characterized by the behavior of the platform power rails, SoC sideband signals (COREPWROK, PLTRST_B, SLP_Sx_B), and internal state machine modes. Below is the description of each of the states. See Figure 10 for an illustration.

- G3 State:
  - No valid platform power sources are on.
  - VBAT and VBAK are below $VSYSREF_F$ (see Table 122) for the P91E0's internal logic power rail VPL.
  - This is a true "G3" state. No power is consumed in this state.
- SoC-G3 State:
  - The P91E0's internal logic power rail VPL is powered, either from the RTC backup battery (VBAK > $VSYSREF_F$), main battery, or an adapter (VSYS > $VSYSREF_R$).
  - The P91E0 can enter this state with sequential shutdown via Cold OFF events or with immediate shutdown due to critical events. Critical events are DCD0/DCD1 over-voltage events, THERMTRIP events, P91E0 critical temperature shutdowns, and input voltage UVLO events.
- SoC-S0 State:
  - All SoC rails have been powered up.
  - COREPWROK is asserted (LOW to HIGH) by the P91E0. Then PLTRST_B is de-asserted (LOW to HIGH) by the SoC. The SoC has begun code execution.
  - The SoC can choose to power up/down any of the "Default Off" rails as software demands.
- SoC-S0Ix State:
  - This is a low-power platform state that is entered and exited as controlled by the sleep state signal SLP_S0Ix_B.
  - PLTRST_B is de-asserted. COREPWROK is asserted.
  - The temperature monitoring state machine enters the Standby Mode with reduced frequency of temperature measurements.
- SoC-S3 State:
  - This is a low-power platform state that is entered and exited as controlled by the sleep state signal SLP_S3_B.
  - PLTRST_B is asserted. COREPWROK is de-asserted.
- SoC-S4 and Soc-S5 States:
  - These are low-power platform states that are entered and exited as controlled by the sleep state signal SLP_S4_B.
  - PLTRST_B is asserted. COREPWROK is de-asserted.
  - The SoC-S4 and SoC-S5 states are identical from a power perspective. The differentiation is that S4 is software determined.

Figure 10. P91E0 PMIC Power State Diagram



PLTRST_B = Undefined
COREPWROK = 0
All Rails = OFF
Temperature Monitoring = Disabled

PLTRST_B = Undefined
COREPWROK = 0
A Rails and U Rails = OFF
S Rails and SX Rails = OFF
Temperature Monitoring = Disabled

If transitioned from S0:
  PLTRST_B = 1
  COREPWROK = 1
If transitioned from S3:
  PLTRST_B = 0
  COREPWROK = 0
A Rails = ON
U Rails = ON (or SoC managed)
S Rails = ON
SX Rails = OFF
Temperature Monitoring = Enabled

PLTRST_B = 1
COREPWROK = 1
A Rails = ON
U Rails = ON
S Rails = ON
SX Rails = ON
Default On Rails = ON
Default Off Rails = SoC Managed
Temperature Monitoring = Enabled

PLTRST_B = 0
COREPWROK = 0
A Rails = ON
U Rails = OFF
S Rails = OFF
SX Rails = OFF
Temperature Monitoring = Disabled

PLTRST_B = 0
COREPWROK = 0
A Rails = ON
U Rails = ON (or SoC managed)
S Rails = OFF
SX Rails = OFF
Temperature Monitoring = Disabled

9.3.1 G3 State

In the “G3” state, the P91E0 is completely powered off, and no valid power sources are available on the platform. To enter this state, all power sources (battery and adapter) must have been removed from the system.

In this state, no rails are in regulation. No P91E0 logic is active. In this state, the device appears to be “off” to the user.

Exiting from this state is triggered by the application of a valid power source. Transitions out of this state are summarized in Table 123.

Table 123. G3 State Transition Table

Event Trigger	Conditions (all must be met)	Next State	Notes
Main Battery Insertion	VSYS > VSYSREF$_R$	SoC-G3	When the VSYS input voltage is sufficiently high (above VSYSREF$_R$), the P91E0 waits for PWRBTNIN_B or PMIC_EN to be pressed/toggled. The I2C register map is reset to defaults.
Main Battery Becomes Valid			
USB or DC Adapter Insertion			

9.3.2 SoC-G3 State

By default, in the SoC-G3 State, the only system rail present is VPL, which is an internal standby rail powering the battery-backed logic.

The events causing a transition out of the SoC-G3 State are shown in Table 124.

Table 124. SoC-G3 State Transition Table

Event Trigger	Conditions (all must be satisfied)	Next State	Notes
Main Battery Removal / Depletion	VSYS < VSYSREF$_F$	G3	VPL-powered logic loses state and resets to defaults.
Adapter Removal			
Power Button Pressed or PMIC_EN toggles HIGH	VSYS > VSYSREF$_R$	SoC-S4/S5	Start Cold Boot sequence to boot platform.

9.3.3 SoC-S0 State

In the SoC-S0 State, the P91E0 has completed bringing up the platform and released the SoC from reset. In this state, the behavior of the P91E0 state machines can be directly modified and controlled by the SoC via commands issued over the I2C and SVID interfaces. In this state, the device will appear "on" to the user.

The events causing a transition out of the SoC-S0 State are shown in Table 125.

Table 125. SoC-S0 State Transition Table

Event Trigger	Conditions (all must be met)	Next State	Notes
Power Source Removal	$VSYS < VSYSREF_F$	G3	VPL-powered logic loses state and resets to defaults.
Thermal Critical Events		SoC-G3	Hardware-enforced shut-down of rails.
Non-Thermal Critical Event		SoC-G3	Execute Cold Off Task List.
Power Button Held	Power button fault timer exceeded	SoC-S3	The P91E0 passes PWRBTNIN_B information to the SoC. The SoC has the option to toggle SLP_S3_B=0 then SLP_S4_B=0, then SUSPWRDNACK=1 to finally enter SoC-G3. This is determined by the SoC.
Power Button Held	Power button fault timer has not yet been exceeded	SoC-S0Ix or SoC-S3	PMIC passes PWRBTNIN_B information to SoC. The SoC has these options: ▪ Toggle SLP_S0Ix_B = 0 enter SoC-S0Ix or ▪ Toggle SLP_S3_B = 0 then SLP_S4_B = 0, then SUSPWRDNACK = 1 to enter the SoC-G3 state as the final state This is determined by the SoC.
Warm Reset	PLTRST_B = 0	SoC-S0	Resets I2C and SVID.
SLP_S0Ix	SLP_S0Ix_B = 0	SoC-S0Ix	Enter S0Ix task list.

9.3.4 Shallow Sleep State (SoC-S0Ix)

The P91E0 supports three possible standby states: SoC-S0Ix (Shallow Sleep State), SoC-S3 (Sleep State), and SoC-S4/S5 (Deep Sleep State). Each of these states represents a different level of SoC standby, with SoC-S0Ix being the "shallowest" sleep state (highest consumed power) and SoC-S4/S5 being the "deepest" sleep state (lowest consumed power). Each of these three sub-states has its own entry task list, required because of the different states of power rails in each.

Entering and exiting each SoC-S0Ix state is controlled by a signal that is delivered to the P91E0 by the SoC via a dedicated physical pin SLP_S0Ix_B.

- Rails that are on:
  - Rails that are on are shown in the power sequencing diagrams (see Figure 11)
  - Switching regulators can be placed in Power-Save Mode (PFM)
  - Internal PMIC rails are on
- Interfaces available:
  - SVID is ON in SoC-S0Ix State
  - I2C is ON in SoC-S0Ix State
- Input source comparators and interrupts are active.
- All P91E0 registers are powered with states retained.
- Thermal monitoring of the P91E0 is disabled.

The events causing a transition out of the SoC-S0Ix state are shown in Table 126.

Table 126. SoC-S0Ix State Transition Table

Event Trigger	Conditions (all must be met)	Next State	Notes
Power Source Removal	VSYS < VSYSREF$_F$	G3	VPL-powered logic loses state; resets to defaults.
Thermal Critical Event		SoC-G3	Hardware-enforced shutdown of rails (no Task List).
Non-Thermal Critical Event		SoC-G3	Execute Cold Off Task List.
Power Button Held	Power button fault timer exceeded	SoC-S3 Determined by the SoC	PMIC passes PWRBTNIN_B information via the PWRBTN_B to the SoC. The SoC can toggle SLP_S3_B = 0 then SLP_S4_B = 0, then SUSPWRDNACK = 1 to enter SoC-G3 as the final state. This is determined by the SoC.
Power Button Held	Power button fault timer has not yet been exceeded	SoC-S0 Determined by the SoC	The P91E0 passes PWRBTNIN_B information via the PWRBTN_B to the SoC as a wake event. The SoC can toggle SLP_S0Ix_B = 1 to go to SoC-S0. or The SoC can determine the state.
		SoC-S3 Determined by the SoC	PMIC passes PWRBTNIN_B information via PWRBTN_B to the SoC. Toggle SLP_S3_B = 0 then SLP_S4_B = 0, then SUSPWRDNACK = 1 to enter the SoC-G3 state as the final state.

Event Trigger	Conditions (all must be met)	Next State	Notes
PMIC_EN is LOW (if enabled with HIGH on PMIC_EN)		SoC-G3	The P91E0 will enter the Cold OFF task list and SoC-G3 State regardless of the SLP_x signals and SUSPWRDNACK state.
Warm Reset	PLTRST_B = 0	SoC-S0Ix	Resets I2C and SVID.
SLP_S0Ix	SLP_S0Ix_B = 1	SoC-S0	Exit the sequence for the S0Ix task list.
SLP_S3	SLP_S3_B = 0	SoC-S3	Enter the sequence for the S3 task list.

9.3.5 Sleep Mode State (SoC-S3)

The entering and exiting of each of the SoC-S3 states is controlled by a signal that is delivered to the P91E0 by the SoC via a dedicated physical pin SLP_S3_B.

- Rails that are on:
  - Rails that are on are shown in the power sequencing diagrams (see Figure 11)
  - Switching regulators can be placed in Power-Save Mode (PFM)
  - Internal PMIC rails are on
- Interfaces available:
  - SVID is OFF in SoC-S3 State.
  - I2C is OFF in SoC-S3 State.
- Input source comparators and interrupts are active.
- All registers are powered with states retained.
- Thermal monitoring of the PMIC is disabled.

The events causing a transition out of the SoC-S3 State are shown in Table 127.

Table 127. SoC-S3 State Transition Table

Event Trigger	Conditions (All must be met)	Next State	Notes
Power Source Removal	VSYS < VSYSREF_F	G3	VPL-powered logic loses state and resets to defaults.
Thermal Critical Event		SoC-G3	Hardware-enforced shutdown of rails (no Task List).
Non-Thermal Critical Event		SoC-G3	Execute Cold Off Task List.
Power Button Held	Power button fault timer exceeded	SoC-S4/S5	PMIC passes PWRBTNIN_B information to the SoC. The SoC can toggle SLP_S4_B = 0 then SUSPWRDNACK = 1 to enter SoC-G3 as the final state. This is determined by the SoC.

Event Trigger	Conditions (All must be met)	Next State	Notes
Power Button Held	Power button fault timer has not been exceeded	SoC-S0 Determined by the SoC	The P91E0 passes PWRBTNIN_B information to the SoC as a wake event. The SoC toggles SLP_S3_B = 1 and SLP_S0Ix_B = 1 to go to the SoC-S0 State. or The SoC can determine the state.
		SoC-S4/S5 Determined by the SoC	The P91E0 passes PWRBTNIN_B information to the SoC to wake to the SoC-S0 State and then to transition to the SoC-S4/S5 State: SLP_S0Ix_B = 0 (if available), SLP_S3_B = 0, SLP_S4_B = 0.
SLP_S3	SLP_S3_B = 1	SoC-S0Ix or SoC-S0 (if S0Ix is unused)	Exit the sequence for the S3 task list.
SLP_S4	SLP_S4_B = 0	SoC-S4/S5	Enter the sequence for the SoC-S4/S5 task list.

9.3.6 Deep Sleep State (SoC-S4/S5 State)

Entering and exiting each of the SoC-S4/S5 states is controlled by a signal that is delivered to the P91E0 by the SoC via the dedicated physical pin SLP_S4_B.

- Rails that are on:
  - Rails that are on are shown in the power sequencing diagrams (see Figure 11)
  - Switching regulators can be placed in Power-Save Mode (PFM)
  - Internal PMIC rails are on
- Interfaces available:
  - SVID is OFF in SoC-S4/S5 State.
  - I2C is OFF in SoC-S4/S5.
- Interrupts are active.
- All registers are powered with states retained.
- Thermal monitoring of the PMIC is disabled.

The events causing a transition out of the SoC-S4/S5 State are shown in Table 128.

Table 128. Deep Sleep Mode (SoC-S4/S5) State Transition Table

Event Trigger	Conditions (All must be met)	Next State	Notes
Power Source Removal	$VSYS < VSYSREF_F$	G3	VPL-powered logic loses state and resets to defaults.
SUSPWRDNACK	SUSPWRDNACK = 1	SoC-G3	Cold OFF task list
Thermal Critical Event		SoC-G3	Hardware-enforced shutdown of rails (no Task List).
Non-Thermal Critical Event		SoC-G3	Execute Cold Off Task List.

Event Trigger	Conditions (All must be met)	Next State	Notes
Power Button Held	Power button fault timer has been exceeded	SoC-G3	PMIC passes PWRBTNIN_B information to the SoC. The SoC can set SUSPWRDNACK = 1 to enter SoC-G3. This is determined by the SoC
Power Button Held	Power button fault timer has not been exceeded	SoC-S3	PMIC passes PWRBTNIN_B information to the SoC. Toggle SLP_S4_B = 1 to exit SoC-S4/S5. This is determined by the SoC.
		SoC-G3	PMIC passes PWRBTNIN_B information to the SoC. Toggle SLP_S4_B = 0 then SUSPWRDNACK = 1 to enter SoC-G3 as the final state. This is determined by the SoC.
SLP_S4	SLP_S4_B = 1	SoC-S3	Exit the sequence for the SoC-S4/S5 task list.

9.4 Power State Transitions

The following is a summary of the 10 power state transitions defined for the P91E0-I5 as an example. The P91E0-I5 is OTP-configured for the Intel® Leaf Hill CRB.

- Cold Boot
- Warm Reset
- Enter Standby SoC-S0Ix
- Exit Standby SoC-S0Ix
- Enter Standby SoC-S3
- Exit Standby SoC-S3
- Enter Standby SoC-S4/S5
- Exit Standby SoC-S4/S5
- Cold OFF
- Modem Reset

Some of these state transitions are triggered by hardware events, such as the power button being pressed or power source insertion. Other transitions are gated by signals such as SLP_S0Ix_B, SLP_S3_B, SLP_S4_B and SUSPWRDNACK, usually connected to the SoC.

The behaviors associated with each of these state transitions are stored in the P91E0's power sequencing state machine. The following sections discuss the trigger sources of each transition and the default sequencing behavior during each.

The voltage rails are classified in the following categories, which are used to simplify the power state transition (power sequencing) diagrams:

- SUS rails (A rails): DCD4 (3.3V), DCD1* (1.0V), DCD5 (1.8V), and DCD6 (V1.25A). They remain on in the SoC-S4/S5 state. They are turned off in the SoC-G3 state.
- U rails: DCD2 (VDDQ), LDO5 (VTT). This rail remains on in SoC-S3 state and is turned off in SoC-S4/S5 state.
- S rails: These include LDO6 (2.8V), LDO0 (1.2V), and LDO1 (1.2V). They remain on in the SoC-S0Ix state. They are turned off in the SoC-S3 state.
- SX rails: DCD1* (1.0V), DCD3 (1.05V), and DCD0† (0V). It is on in SoC-S0 state, and it is turned off in the SoC-S0Ix state.

---

* Note that register 10_{HEX} bit[1] (DCD1_TYPE_EXIT) is set to 1 to enable the exit sequence. DCD1 starts as an A-type rail and remains as an A-type rail until RSMRST_B and PLTRST_B are both asserted. Once assertion of both signals is detected, DCD1 changes to an SX-type rail and remains as an SX-type rail until the system is reset.

† Note that DCD0's VBOOT is set to 0V and the output voltage is expected to change according to the DCD0_VID command through SVID or I2C.

- Default ON rails: VRs that are turned on during the COLD BOOT by the power sequencing state machine.
- Defaults OFF rails: VRs that are not turned on during the COLD BOOT by the power sequencing state machine. They are managed by the SoC. Their on/off status depends on a platform device or other conditions.
- The accuracy of the built-in timer is +/-20%.

Figure 11. Power-Up Sequence Timing Diagram for P91E0-I5 Rev. H

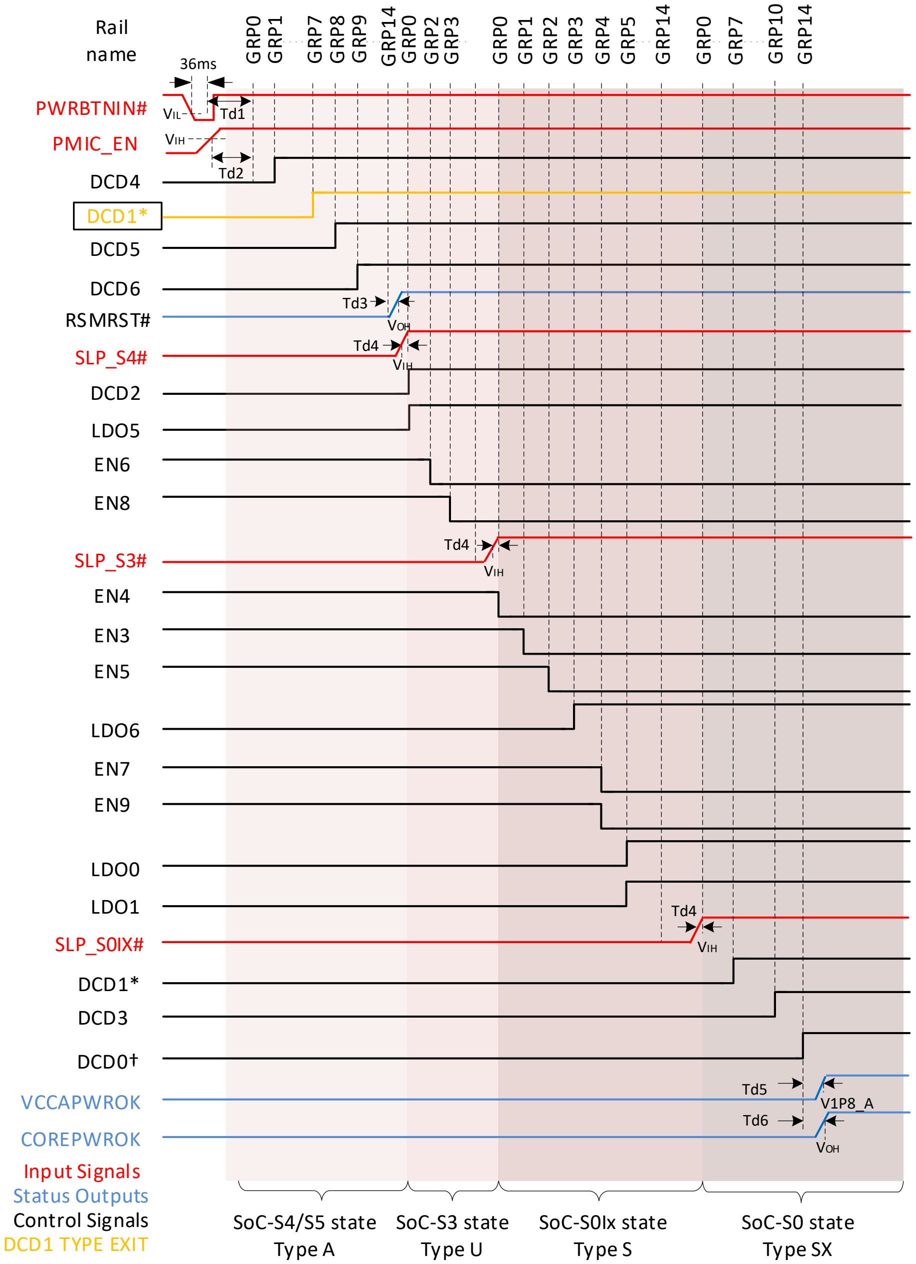
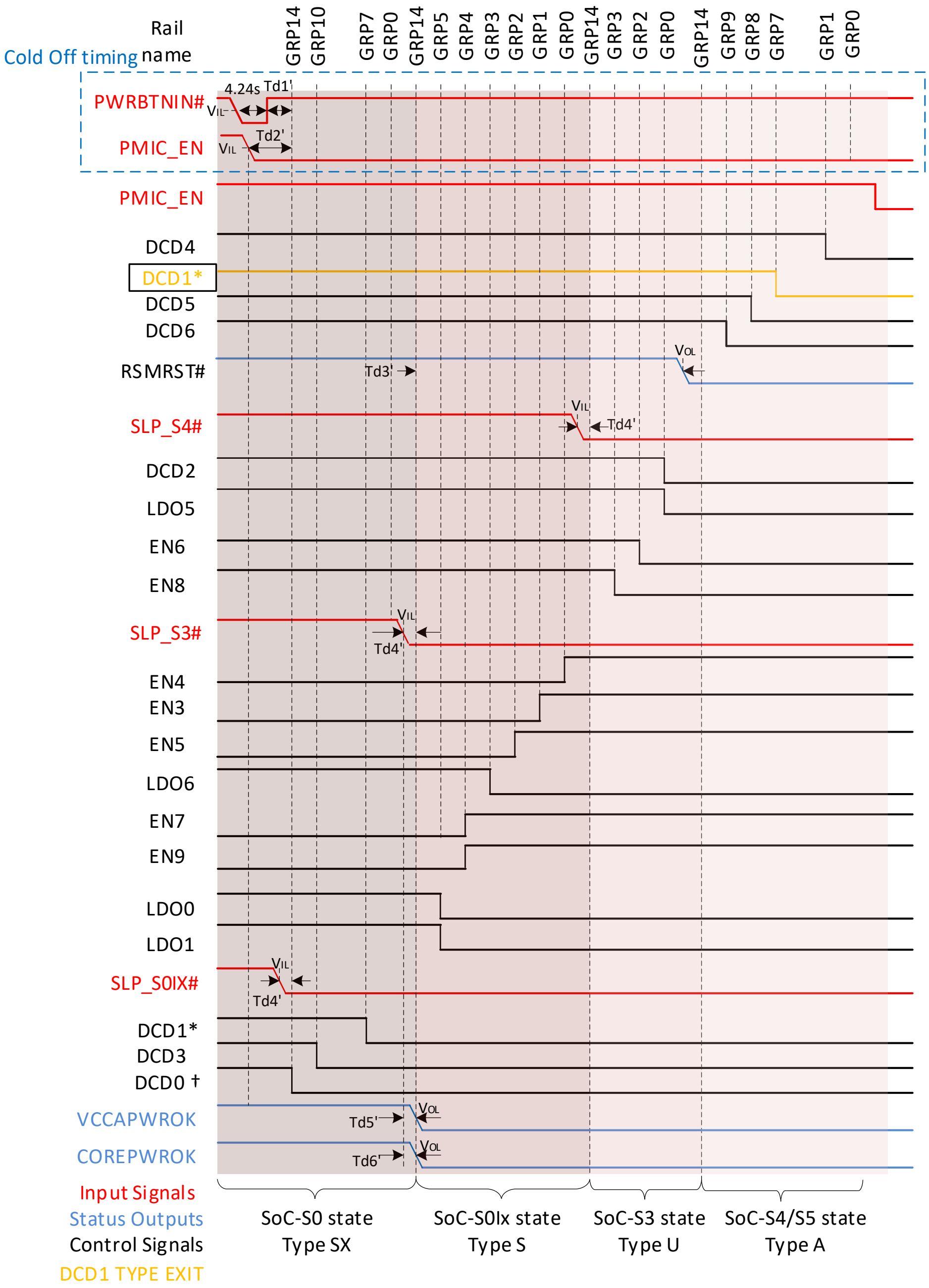


Figure 12. Power-Down Sequence Timing Diagram for P91E0-I5 Rev. H



9.4.1 Cold Boot

A Cold Boot sequence is followed whenever the P91E0 is fully turning on the system from a powered-down state. As such, a Cold Boot sequence begins at the SoC-G3 State and terminates at the SoC-S0 State. Once all of the rails are on, the COREPWROK signal will assert and the PLTRST_B will de-assert. This will effectively turn on the SoC in order for it to begin executing code and controlling the system.

During this state transition, one or more of the sleep signals (SLP_Sx_B) could be asserted at some point in time. The VRs that are turned on during the transition should not be put in low-power mode even if some of the sleep signals may still be asserted since the end state of cold boot is SoC-S0 state.

During this state transition, the SoC rails are sequenced in an order critical to SoC operation. In addition, the rails are turned on one at a time in a ramp-rate controlled manner (voltage slew rate limited) in order to avoid battery in-rush current situations that could cause shut-down events.

All the triggers listed in Table 129 will cause the P91E0 to bring up the SUS rails (A rails). After that, signals from the SoC (SLP_S4_B, SLP_S3_B, SLP_S0Ix_B) are needed for the P91E0 to complete the Cold Boot sequence.

Table 129. Cold Boot Triggers

Event	Conditions (all must be met)
Power Button Pressed	$VSYS > VSYSREF_R$

9.4.2 Warm Reset

A Warm Reset resets the SoC as well as the I2C and SVID interfaces in the P91E0. Configuration registers are not reset to defaults (unless explicitly defined otherwise).

During a Warm Reset, only the PLTRST_B pin from the SoC is toggled. All rails remain in regulation during the reset.

Table 130. Warm Reset Triggers

Event	Conditions (all must be met)
Warm Reset Request	SoC toggles the PLTRST_B = 0

9.4.3 Shallow Sleep State S0Ix (SLP_S0Ix_B)

SLP_S0Ix_B is an input signal from the SoC initiating the Shallow Sleep State. In this mode, the P91E0 consumes the highest power among the sleep states. When SLP_S0Ix_B is pulled LOW, the SoC launches the Shallow Sleep State entry task list and the SX-type rails are turned off. Prior to initiating the Sleep Mode entry, the SoC will program the exit VID values for VCC (DCD0) via SVID and communicate Standby State information to the PMIC via I2C.

When SLP_S0Ix_B is pulled HIGH (with SLP_S3_B, SLP_S4_B, and RSMRST_B already HIGH), the P91E0 exits the Shallow Sleep State. The SX-type rails are turned on. The VCC rail will be turned on by SVID commands (not by SLP_S0Ix_B). During the Cold Boot sequence or waking from deeper sleep modes, an SLP_S0Ix_B HIGH signal is valid if both the SLP_S3_B pin and the SLP_S4_B pin are connected to logic HIGH. It is valid when the RSMRST_B pin = 1.

Table 131. Enter and Exit SoC-S0Ix Triggers

Event	Conditions (all must be met)
Enter SoC-S0Ix Request	SLP_S0Ix_B = 0
Exit SoC-S0Ix Request	SLP_S0Ix_B = 1 (SLP_S3_B = 1, SLP_S4_B = 1, RSMRST_B = 1)

9.4.4 Sleep Mode State S3 (SLP_S3_B)

SLP_ S3_B is a dedicated input pin for enabling and disabling the low-power Sleep Mode State. When SLP_S3_B is pulled LOW, Sleep State is initiated and all the S-type power rails are turned off according to the programmed timing. If SLP_S0Ix_B is HIGH when SLP_S3_B is pulled LOW, the SX-type rails will turn off prior to the S-type rails turning off. Prior to activating the Sleep Mode, the SoC will program exit VID values for VCC/VNN over SVID and communicate standby state information to the P91E0 via I2C.

When SLP_S3_B is pulled HIGH (with SLP_S4_B and RSMRST_B already HIGH), the P91E0 exits the low-power Sleep Mode State. The S-type rails are turned on. During the Cold Boot sequence or waking from deeper sleep modes, an SLP_S3_B HIGH signal is valid if SLP_S4_B is connected to logic HIGH. It is valid when the RSMRST_B pin = 1.

Table 132. Low-Power Sleep Mode State Entry and Exit

Event	Conditions (all must be met)
Enter SoC-S3 Request	SLP_S3_B = 0 (optional: SLP_S0Ix_B = LOW)
Exit SoC-S3 Request	SLP_S3_B = 1 (SLP_S4_B = 1, RSMRST_B = 1)

9.4.5 Deep Sleep State S4/S5 (SLP_S4_B)

SLP_S4_B is a dedicated input pin for enabling and disabling the Deep Sleep State. When SLP_S4_B is pulled LOW (with SLP_S3_B already LOW), Deep Sleep State is initiated, and all the U-type rails are turned off according to the programmed timing sequence. Prior to activating the deep sleep mode, the SoC will program exit VID values for VCC/VNN over SVID and communicate standby state information to the P91E0 via I2C. It is valid when the RSMRST_B pin = 1 (de-asserted) and SLP_S3_B=0 (asserted).

When SLP_S4_B is pulled HIGH (with RSMRST_B already HIGH), the P91E0 exits the Deep Sleep State. The U-type rails are turned on. During the Cold Boot sequence or waking from deeper sleep modes, an SLP_S4_B HIGH signal is valid when the RSMRST_B pin = 1 (de-asserted).

Table 133. Deep Sleep State Entry and Exit

Event	Conditions (all must be met)
Enter SoC-S4/S5 Request	SLP_S4_B = 0 (SLP_S3_B = 0; optional: SLP_S0Ix_B = 0)
Exit SoC-S4/S5 Request	SLP_S4_B = 1 (RSMRST_B = 1)

9.4.6 Cold OFF

A Cold OFF, through either a SoC request or a system event, puts the P91E0 in the “Mechanical Off” state. The system remains in this state until the power button is pressed, PMIC_EN is pulled HIGH, or VSYS is removed.

Table 134. Cold OFF Triggers

Event	Conditions (all must be met)
Non-Thermal Critical Event	VSYS removal SUSPWRDNACK = 1 and SLP_S4_B = 0 and RSMRST_B = 1
Power Button Held	Power button fault timer exceeded SUSPWRDNACK = 1 RSMRST_B = 1 SLP_S4_B = 0
Power Button Held	Power button pressed for a defined length (up to SoC to define the length) SUSPWRDNACK = 1 and SLP_S4_B = 0 and RSMRST_B = 1
PMIC_EN LOW (if enabled with PMIC_EN HIGH	RSMRST_B = 1

9.4.7 Modem Reset

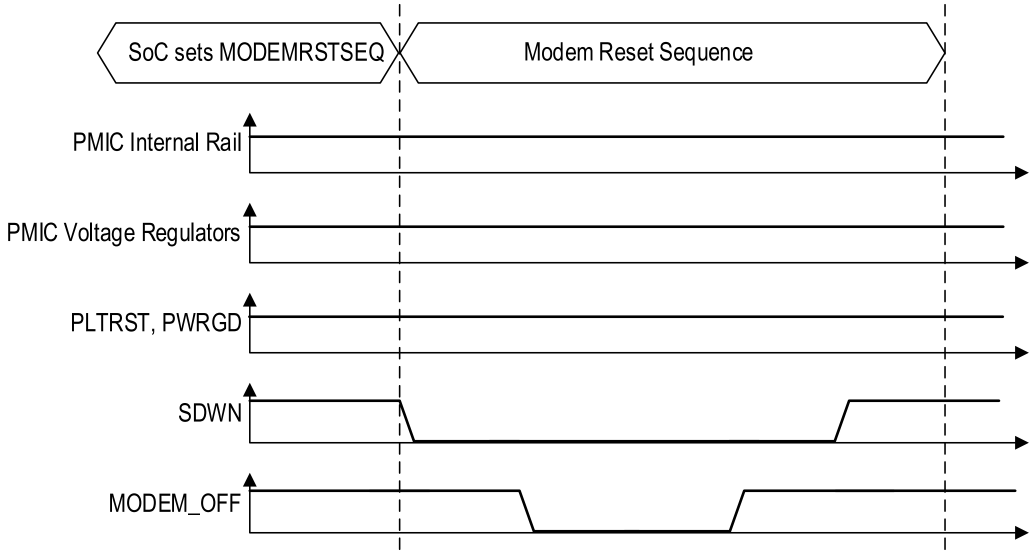
A Modem Reset task list is initiated by setting the MODEMRSTSEQ bit in the *MODEMCTRL* register (see Table 138). (The MODEMOFF bit in the same register directly controls the status of the MODEM_OFF_B output pin, but does not launch this task list.)

Table 135. Modem Reset Triggers

Event	Conditions (all must be met)
Modem Reset Request	SoC writes to the MODEMRSTSEQ bit in the *MODEMCTRL* register.

The Modem Reset task list toggles the Shutdown Warning (SDWN_B pin) and MODEM_OFF_B pins, implementing appropriate (modem-specific) delay timings. The default behavior for the Modem Reset task list is illustrated in Figure 13.

Figure 13. Modem Reset Sequence Timing Diagram



Notes:

- SDWN_B LOW to MODEM_OFF_B LOW delay time: 400µs to 800µs.
- MODEM_OFF_B LOW duration > 14ms.
- MODEM_OFF_B HIGH to SDWN_B HIGH delay time > 5ms.

9.5 PMIC Resets

The following table summarizes the reset sources for the P91E0.

Table 136. PMIC Reset Sources

Reset Source	Reset Trigger	Reset Type / Sequence
SoC Request	PLTRST_B	Warm Reset
External Button	PWRBTNIN_B held longer than the time defined in FLT[3:0] (bit field in the *PBCONFIG* register (see Table 112)	Cold Off
Critical Event	PMICTEMP	Hard shutdown of all VRs; return to SoC-G3 (do not wait for SLP_Sx from SoC).
	THERMTRIP	
Wake Event from Cold Off	PWRBTNIN_B pressed	Cold Boot

9.5.1 Mode

The *Mode* register can be written to by the SoC to manually control the P91E0's critical turn off and reset.

Table 137. Mode – Mode Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
MODE	R/W	RSVD			CHG_STAT	RSVD		TURNOFF_CRIT	RESET_CRIT	00_{HEX}	82_{HEX}

Bit	Name	Function	Default
D[7:5]	RSVD	Reserved	000_{BIN}
D[4]	CHG_STAT	This is a read only status bit 0 = Charger OFF 1 = Charger ON	0_{BIN}
D[3:2]	RSVD	Reserved	00_{BIN}
D[1]	TURNOFF_CRIT	0 = Default 1 = Enable critical event due to I2C set Rails turn off and follow the power-down sequence	0_{BIN}
D[0]	RESET_CRIT	0 = Default 1 = Enable critical reset event due to I2C set Rails turn off and follow the power down sequence, then turn back on, and follow power-on sequence	0_{BIN}

9.5.2 MODEMCTRL

The *MODEMCTRL* register can be written to by the SoC to manually control the MODEM_OFF_B pin or to launch a Modem Reset task list.

Table 138. MODEMCTRL – Modem Control Register

Note: A write must only set one bit. Action is taken immediately.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MODEMCTRL	R/W	RSVD						MODEM RSTSEQ	MODEM OFF	00HEX	29HEX

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved	000000BIN
D[1]	MODEMRSTSEQ	This bit is self-clearing and always reads 0: 0 = No action. 1 = Initiate a Modem Reset task list.	0BIN
D[0]	MODEMOFF	Controls the state of the MODEM_OFF_B pin: 0 = MODEM_OFF_B driven to logic LOW (asserted). 1 = MODEM_OFF_B driven to logic HIGH (de-asserted). If the MODEM_OFF_B pin state is modified by the task list processor's IO_CTL command, this bit updates to reflect the pin's current state.	0BIN

9.5.3 Reset Source Indicators

The PMIC contains two registers that are intended to store the cause of a shutdown or reset for FW to interrogate on next startup. These registers are backed up by the backup battery so that on the next boot, software can determine the cause of the previous shutdown even if the battery was removed and replaced. These bits are write-1-to-clear.

If the RESETSRC registers are not cleared by the SoC, stale bits (from past resets) will auto-clear. This is to ensure that between RESETSRC0 and RESETSRC1, only the most recent reset reason is flagged for SW.

Table 139. Reset Source Register 0

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
RESETSRC0	R/W	RSYSTEMP2	RSYSTEMP1	RSYSTEMP0	RI2C	RSVD	RPWRBTN	RPMICTEMP	RTHERMTRIP	00HEX	20HEX

Bit	Name	Function	Default
D[7]	RSYSTEMP2	0 = Default. 1 = Previous shut-down was due to an over-temperature condition on ADC channel 2.	0BIN
D[6]	RSYSTEMP1	0 = Default. 1 = Previous shut-down was due to an over-temperature condition on ADC channel 1.	0BIN
D[5]	RSYSTEMP0	0 = Default. 1 = Previous shut-down was due to an over-temperature condition on ADC channel 0.	0BIN
D[4]	RI2C	0 = Default. 1 = Previous shut-down was due to an I2C (software) initiated reset.	0BIN

Bit	Name	Function	Default
D[3]	RSVD	Reserved.	0_{BIN}
D[2]	RPWRBTN	0 = Default. 1 = Previous shut-down was due to a Power Button initiated reset.	0_{BIN}
D[1]	RPMICTEMP	0 = Default. 1 = Previous shut-down was due to a PMIC internal over-temperature event. (P91E0 sets this bit.)	0_{BIN}
D[0]	RTHERMTRIP	0 = Default. 1 = Previous shut-down was due to the SoC asserting THERMTRIP. (P91E0 sets this bit).	0_{BIN}

Table 140. Reset Source Register 1

Note: Green shading indicates that the register values are loaded from the OTP.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
RESETSRC1	R/W	RVSYS	ROV1	ROV0	RNORM	RCHG[1:0]		VCHG[1:0]		OTP	21_{HEX}

Bit	Name	Function	Default
D[7]	RVSYS	0 = Default. 1 = Previous shut-down was due to the user removing VSYS during operation.	OTP
D[6]	ROV1	0 = Default. 1 = Previous shut-down was due to an over-voltage condition on DCD1.	OTP
D[5]	ROV0	0 = Default. 1 = Previous shut-down was due to an over-voltage condition on DCD0.	OTP
D[4]	RNORM	0 = Default. 1 = Previous shut-down was due to a normal turn-off after SUSPWRDNOK.	OTP
D[3:2]	VBAK_RCHG[1:0]	Coin cell charger series resistor setting: 00 = 0.5kΩ 01 = 1kΩ 10 = 2kΩ 11 = 5kΩ	OTP
D[1:0]	VBAK_VCHG[1:0]	Coin cell charger output voltage setting: 00 = Charger is turned-off 01 = 2.6V 10 = 3.0V 11 = 3.3V	OTP

9.5.4 Wake Source Indicator

The P91E0 has a register for storing the cause of a wake event, so that the software can determine why the system was awaken from Cold OFF. These bits are write-1-to-clear.

If the *WAKESRC* register is not cleared by the SoC, stale bits (from past wakes) will auto-clear. This is to ensure that only the most recent wake reason is flagged for software.

Table 141. Wake Source Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
WAKESRC	R/W	RSVD							WAKEPBTN	00_{HEX}	22_{HEX}

Bit	Name	Function	Default
D[7:1]	RSVD	Reserved.	0000000_{BIN}
D[0]	WAKEPBTN	0 = Default. 1 = Wake was triggered by user pressing the power button.	0

9.6 Interrupting the SoC

See section 8.1.10 for a general description of the interrupt request.

When the P91E0 needs to interrupt the SoC, it asserts the IRQ line. The following sequence illustrates the interrupt handling flow:

1. A P91E0 event occurs, which sets the level 2 (see Table 144) and level 1 (IRQLVL1; see Table 142) I2C register flags. In response to an unmasked flag being set in IRQLVL1, the P91E0 interrupts the SoC by asserting the IRQ line. This IRQ line is connected to an interruptible GPIO pin at the SoC.
2. Because the IRQ was set, the SoC reads the P91E0's level 1 and level 2 interrupt registers via I2C, determining the cause of the interrupt.
3. The SoC clears the interrupt event in the P91E0 via a register write to the level 2 interrupt register via I2C.
4. If IRQLVL1 has all unmasked interrupts cleared, the P91E0 de-asserts the IRQ signal, signaling that the interrupt has been handled.
5. The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms.

The P91E0 may assert the IRQ line due to two separate events occurring simultaneously. It is the responsibility of the SoC to read all the interrupt registers and assign proper priority to handling the events.

9.7 Interrupt Request (IRQ) Control Unit

The interrupt control unit maintains the state of the level 1 IRQ tree and is responsible for asserting and de-asserting the P91E0's IRQ pin to the application SoC. It contains status bits for interrupts from all the second-level sub-blocks as well as the power button.

9.7.1 Interrupt Descriptions

If unmasked, the level 2 interrupts will propagate to the appropriate level 1 interrupt bit, as described below. If the level 1 interrupt is unmasked, it will propagate to the IRQ pin, which will remain HIGH as long as unmasked interrupts have not been cleared.

9.7.2 Level 1 Interrupts (IRQLVL1)

The IRQ interrupt indicator to the SoC, IRQ, is transmitted from the IRQ pin of the P91E0 to a GPIO pin of the SoC. Causes of the interrupts are investigated by the SoC by reading the IRQ status registers via I2C. The P91E0 interrupt scheme contains two levels. The level 1 interrupt register contains 7 IRQ bits and indicates which P91E0 sub-block triggered the interrupt. One bit is dedicated to each of the interrupt-causing PMIC sub-blocks. For all units, the level 2 interrupt registers indicate the specific interrupt triggers for each sub-block. A masking system is provided to enable or disable specific interrupt handlers.

If any bits are set in the first-level IRQ mask, the assertion of an interrupt from the masked sub-block(s) will not cause an assertion of the IRQ signal, nor will it set the associated level 1 IRQ bit. By limiting the level 1 IRQ bits set to only those that are unmasked, this disambiguates the dispatching of interrupts.

Level 1 IRQ bits cannot be directly cleared; they are implicitly cleared by clearing all unmasked level 2 IRQ bits. When all unmasked level 1 IRQ bits are implicitly cleared (all unmasked level 2 interrupts are directly cleared), the IRQ pin is de-asserted.

Table 142. IRQLVL1 – Level 1 Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
IRQLVL1	R/W	RSVD	VR	GPIO	RSVD	ADC	RSVD	THRM	RSVD	00_{HEX}	02_{HEX}

Bit	Name	Function	Default
D7	RSVD	Reserved.	0_{BIN}
D6	VR	0 = VR IRQ not asserted. 1 = VR IRQ asserted; write ‘1’ to clear.	0_{BIN}
D5	GPIO	0 = GPIO IRQ not asserted. 1 = GPIO IRQ asserted; write ‘1’ to clear.	0_{BIN}
D4	RSVD	Reserved.	0_{BIN}
D3	ADC	0 = ADC IRQ not asserted. 1 = ADC IRQ asserted; write ‘1’ to clear.	0_{BIN}
D2	RSVD	Reserved.	0_{BIN}
D1	THRM	0 = THRM (Thermal Unit) IRQ not asserted. 1 = THRM (Thermal Unit) IRQ asserted; write ‘1’ to clear.	0_{BIN}
D0	RSVD	Reserved.	0_{BIN}

Table 143. MIRQLVL1 – Level 1 Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MIRQLVL1	R/W	RSVD	MVR	MGPIO	RSVD	MADC	RSVD	MTHRM	RSVD	$6A_{HEX}$	$0E_{HEX}$

Bit	Name	Function	Default
D7	RSVD	Reserved.	0_{BIN}
D6	MVR	0 = VR IRQ unmasked. 1 = VR IRQ masked.	1_{BIN}
D5	MGPIO	0 = GPIO IRQ unmasked. 1 = GPIO IRQ masked.	1_{BIN}
D4	RSVD	Reserved.	0_{BIN}
D3	MADC	0 = ADC IRQ unmasked. 1 = ADC IRQ masked.	1_{BIN}
D2	RSVD	Reserved	0_{BIN}
D1	MTHRM	0 = THRM (Thermal Unit) IRQ unmasked. 1 = THRM (Thermal Unit) IRQ masked.	1_{BIN}
D0	RSVD	Reserved.	0_{BIN}

9.8 Second-Level Interrupts

While level 1 interrupt bits inform the interrupt handler of which sub-block interrupted, level 2 interrupt registers/bits provide the interrupt handler with the specific nature of the block's interrupt event.

If any bits are set in a level 2 interrupt mask, then the appropriate level 2 interrupt bit is prevented from asserting the level 1 interrupt bit for the corresponding sub-block, nor will the bit become set. (Only unmasked level 2 interrupt bits can be set).

Interrupt bits are write-1-to-clear. This includes all level 2 interrupt register locations and the power-button interrupt bit. The IRQ signal will not be de-asserted until all unmasked interrupt bits are cleared.

Table 144. Level 2 Interrupt Registers

INT Name	Register	Source	First-Level Interrupt	Related Status Bit	DESCRIPTION
VSYS	VSYSIRQ	ADC	ADC	–	This indicates that VSYS is out of range ("invalid").
VRFAULT	VRIRQ	ADC	VR	–	This indicates that a VR over-voltage or over-current fault has occurred. The VR fault interrupt will reset to 0 on Cold OFF.
PMICALRT	THRMIRQ	Thermal Control Unit	THRM	–	Set by the thermal state machine when a PMIC die temperature thermal alert occurs.
ADC2ALRT	ADCIRQ	ADC	ADC	–	Set by the thermal state machine when a system voltage 2 alert occurs.
ADC1ALRT	ADCIRQ	ADC	ADC	–	Set by the thermal state machine when a system voltage 1 alert occurs.
ADC0ALRT	ADCIRQ	ADC	ADC	–	Set by the thermal state machine when a system voltage 0 alert occurs.
SYSTEMP	ADCIRQ	ADC	ADC	–	Bit is set when a SYSTEMP conversion completes and the GPADCREQ:IRQEN bit (see Table 149) was set when the request was made.
GPIO	GPIOIRQ	GPIO	GPIO	DIN	Each GPIO pin can be configured as an input with a programmable interrupt edge for rise, falling, or both. See the *GPIOCTLIx* registers (see Table 89) for INTCNT settings. This interrupt is triggered when the conditions set in the *GPIOCTLIx* registers have been met. The status of the GPIO input can be verified by reading the DIN bit from the *GPIOCTLIx* register.

9.9 GPIO IRQ Registers

Table 145. GPIO0 Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIO0IRQ	R/W	RSVD	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	00_{HEX}	$0B_{HEX}$

Bit	Name	Function	Default
D[7]	RSVD	Reserved.	0_{BIN}
D[6]	GPIO14	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[5]	GPIO13	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[4]	GPIO12	0 = No interrupt pending. 1 = Interrupt Pending.	0_{BIN}
D[3]	GPIO11	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[2]	GPIO10	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[1]	GPIO9	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[0]	GPIO8	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}

Table 146. GPIO1 Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIO1IRQ	R/W	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	00_{HEX}	$0C_{HEX}$

Bit	Name	Function	Default
D[7]	GPIO7	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[6]	GPIO6	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[5]	GPIO5	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[4]	GPIO4	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[3]	GPIO3	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}

Bit	Name	Function	Default
D[2]	GPIO2	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[1]	GPIO1	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}
D[0]	GPIO0	0 = No interrupt pending. 1 = Interrupt pending.	0_{BIN}

Table 147. GPIO0 Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MGPIO0IRQ	R/W	RSVD	MGPIO14	MGPIO13	MGPIO12	MGPIO11	MGPIO10	MGPIO9	MGPIO8	$7F_{HEX}$	19_{HEX}

Bit	Name	Function	Default
D[7]	RSVD	RSVD	0_{BIN}
D[6]	MGPIO14	0 = No Mask. 1 = Mask Interrupt.	1_{BIN}
D[5]	MGPIO13	0 = No Mask. 1 = Mask Interrupt.	1_{BIN}
D[4]	MGPIO12	0 = No Mask. 1 = Mask Interrupt.	1_{BIN}
D[3]	MGPIO11	0 = No Mask. 1 = Mask Interrupt.	1_{BIN}
D[2]	MGPIO10	0 = No Mask. 1 = Mask Interrupt.	1_{BIN}
D[1]	MGPIO9	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[0]	MGPIO8	0 = No Mask 1 = Mask Interrupt	1_{BIN}

Table 148. GPIO1 Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MGPIO1IRQ	R/W	MGPIO7	MGPIO6	MGPIO5	MGPIO4	MGPIO3	MGPIO2	MGPIO1	MGPIO0	FF_{HEX}	$1A_{HEX}$

Bit	Name	Function	Default
D[7]	MGPIO7	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[6]	MGPIO6	0 = No Mask 1 = Mask Interrupt	1_{BIN}

Bit	Name	Function	Default
D[5]	MGPIO5	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[4]	MGPIO4	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[3]	MGPIO3	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[2]	MGPIO2	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[1]	MGPIO1	0 = No Mask 1 = Mask Interrupt	1_{BIN}
D[0]	MGPIO0	0 = No Mask 1 = Mask Interrupt	1_{BIN}

9.10 General Purpose ADC (GPADC)

The general purpose ADC (referred to as GPADC or ADC) is used for die temperature, current, and voltage measurements. It is managed at a hardware level by the ADC state machine, similar to how rail transitions sequences are handled. The state machine performs ADC operations (regular readings of the die temperature, currents, and voltages, which are programmed in registers) and may be modified by the SoC after boot and initialization. The state machine for the GPADC is distinct from any other state machine (such as the one for power sequence controlling boot flow). This prevents the management of lengthy ADC transactions from blocking time-critical power sequencing tasks.

The GPADC can perform the following task lists:

- Repeated (on-going) VR current acquisition (initiated via timer defined by VRIMONCTL; see Table 171
- SoC-requested die temperature acquisition (initiated via GPADCREQ; see Table 149)
- SoC-requested VR current acquisition (initiated via GPADCREQ)
- SoC-requested voltage measurements on ADC[2:0] inputs

The following section describes the interaction between the I2C control registers, ADC state machine, SRAM, and ADC hardware to perform temperature monitoring and GPADC acquisition.

9.10.1 GPADC Read Requests

The SoC can manually add GPADC read requests to the ADC queue whenever there is free instruction space in the queue and the BUSY bit in the *GPADCREQ* register is cleared (see Table 149). Manual GPADC requests are initiated by setting the appropriate bit in the *GPADCREQ* register. In response to this bit being set, the corresponding tasks are performed in the ADC.

When the queue fills, the BUSY bit is set, and the SoC cannot trigger any additional ADC task lists until the queue has room. The P91E0 hardware enforces that no additional commands are written by ignoring any requests from the SoC.

If the SoC sets the IRQEN bit in the *GPADCREQ* register, the PMIC will interrupt the SoC when the requested ADC task list is complete (via the *ADCIRQ* register; see Table 150).

When using the IRQ functionality with the ADC measurements, it is recommended to start only one type of measurement with the *GPADCREQ* register: VSYS, VRI, or ADC. The corresponding mask bit in the *MADCIRQ* register (see Table 151) must be unmasked (cleared), while all other flags must be masked (set).

The *GPADCREQ* register is defined in Table 149.

Table 149. GPADC Conversion Request Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPADCREQ	R/W	VSYS	VRI	RSVD	RSVD	ADC	RSVD	IRQEN	BUSY	00_{HEX}	72_{HEX}

Bit	Name	Function	Default
D[7]	VSYS	Set to 1 for capturing VSYS. Bit automatically clears after it is set.	0_{BIN}
D[6]	VRI	Set to 1 for capturing VR current of all 5 VR current channels. Bit automatically clears after it is set.	0_{BIN}
D[5]	RSVD	Reserved.	0_{BIN}
D[4]	RSVD	Reserved.	0_{BIN}
D[3]	ADC	Set to 1 for capturing ADC0, ADC1, and ADC2. Bit automatically clears after it is set.	0_{BIN}
D[2]	RSVD	Reserved.	0_{BIN}
D[1]	IRQEN	If this bit is set to 1, the GPADC conversion requested generates an SoC interrupt when complete. Bit automatically clears after it is set.	0_{BIN}
D[0]	BUSY	The GPADC state machine sets this read-only bit to 1 when there is no more room in the ADC instruction queue. Software should check that this bit is clear before setting GPADCREQ [7:3]. GPADC requests issued while BUSY = 1 will be ignored.	0_{BIN}

Table 150. GPADC Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
ADCIRQ	R/W	VSYS	VRI	RSVD		ADC	RSVD			00_{HEX}	08_{HEX}

Bit	Name	Function	Default
D[7]	VSYS	Bit is set when a VSYS conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made). Bit is cleared by writing a ‘1’.	0_{BIN}
D[6]	VRI	Bit is set when a VRI conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made). Bit is cleared by writing a ‘1’.	0_{BIN}
D[5:4]	RSVD	Reserved.	00_{BIN}
D[3]	ADC	Bit is set when a ADC conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made). Bit is cleared by writing a ‘1’.	0_{BIN}
D[2:0]	RSVD	Reserved.	000_{BIN}

Table 151. GPADC Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MADCIRQ	R/W	MVSYS	MVRI	RSVD		MADC	RSVD			C8$_{HEX}$	15$_{HEX}$

Bit	Name	Function	Default
D[7]	MVSYS	0 = No Mask. 1 = Interrupt Masked.	1$_{BIN}$
D[6]	MVRI	0 = No Mask. 1 = Interrupt Masked.	1$_{BIN}$
D[5:4]	RSVD	Reserved.	00$_{BIN}$
D[3]	MADC	0 = No Mask. 1 = Interrupt Masked.	1$_{BIN}$
D[2:0]	RSVD	Reserved.	000$_{BIN}$

When a GPADC conversion is performed, results are stored in a series of registers which are dedicated to specific channels. (*RSLT registers). These result registers are detailed in Table 152. To enable the DOUT for GPIO10, GPIO11, and GPIO12, write 41$_{HEX}$ to registers 2D$_{HEX}$, 2E$_{HEX}$, and 2F$_{HEX}$.

Table 152. ADC and Monitoring Registers – Upper Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
ADCRSLT0H	R	RSVD						ADC0[9:8]		00$_{HEX}$	74$_{HEX}$
ADCRSLT1H	R	RSVD						ADC1[9:8]		00$_{HEX}$	76$_{HEX}$
ADCRSLT2H	R	RSVD						ADC2[9:8]		00$_{HEX}$	78$_{HEX}$

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved.	000000$_{BIN}$
D[1:0]	ADCx[9:8]	Upper 2 bits of the ADC conversion result from respective ADC[x] input.	00$_{BIN}$

Table 153. ADC and Monitoring Registers – Lower Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
ADCRSLT0L	R	ADC0[7:0]								00$_{HEX}$	75$_{HEX}$
ADCRSLT1L	R	ADC1[7:0]								00$_{HEX}$	77$_{HEX}$
ADCRSLT2L	R	ADC2[7:0]								00$_{HEX}$	79$_{HEX}$

Bit	Name	Function	Default
D[7:0]	ADCx[7:0]	Lower 8 bits of the ADC conversion result from respective ADC[x] input.	00000000$_{BIN}$

Table 154. System Thermal Alert Register ADC0 – Upper Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC0_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	ADC0_ALRT_HYS [3:0]				ADC0_ALRT[9:8]		E7$_{\text{HEX}}$	94$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	PROCHOT_EN	Processor hot enable. 1= Enable, 0= Disable.	1$_{\text{BIN}}$
D[6]	ALRT_EN	System thermal alert enable. 1= Enable, 0= Disable.	1$_{\text{BIN}}$
D[5:2]	ADC0_ALRT_HYS [3:0]	Hysteresis value for ADC0_ALRT.	1001$_{\text{BIN}}$
D[1:0]	ADC0_ALRT[9:8]	Upper 2 bits of the ADC0_ALRT for the system temperature.	11$_{\text{BIN}}$

Table 155. System Thermal Alert Register ADC0 – Lower Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC0_THRMALRTL	R/W	ADC0_ALRT[7:0]								58$_{\text{HEX}}$	95$_{\text{HEX}}$

Bit	Name	Function	Default
D[7:0]	ADC0_ALRT	Lower 8 bits of the ADC0_ALRT for the system temperature.	01011000$_{\text{BIN}}$

Table 156. System Thermal Reset Register ADC0

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC0_THRMRESET	R/W	ADC0_RESET_EN	ADC0_RESET_OFS [6:0]							00$_{\text{HEX}}$	97$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	ADC0_RESET_EN	0 = Disable ADC0_RESET. 1 = Enable ADC0_RESET.	0$_{\text{BIN}}$
D[6:0]	ADC0_RESET_OFS	Defines the offset above or below the ADC1 threshold.	0000000$_{\text{BIN}}$

Table 157. System Thermal Alert Register ADC1 – Upper Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC1_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	ADC1_ALRT_HYS [3:0]				ADC1_ALRT[9:8]		E7$_{HEX}$	99$_{HEX}$

Bit	Name	Function	Default
D[7]	PROCHOT_EN	Processor hot enable. 1= Enable, 0= Disable.	1$_{BIN}$
D[6]	ALRT_EN	System thermal alert enable. 1= Enable, 0= Disable.	1$_{BIN}$
D[5:2]	ADC1_ALRT_HYS [3:0]	Hysteresis value for ADC1_ALRT.	1001$_{BIN}$
D[1:0]	ADC1_ALRT[9:8]	Upper 2 bits of the ADC1_ALRT for the system temperature.	11$_{BIN}$

Table 158. System Thermal Alert Register ADC1 – Lower Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC1_THRMALRTL	R/W	ADC1_ALRT[7:0]								58$_{HEX}$	9A$_{HEX}$

Bit	Name	Function	Default
D[7:0]	ADC1_ALRT	Lower 8 bits of the ADC1_ALRT for the system temperature.	01011000$_{BIN}$

Table 159. System Thermal Reset Register ADC1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC1_THRMRESET	R/W	ADC1_RESET_EN	ADC1_RESET_OFS [6:0]							00$_{HEX}$	9C$_{HEX}$

Bit	Name	Function	Default
D[7]	ADC1_RESET_EN	0 = Disable ADC1_RESET. 1 = Enable ADC1_RESET.	0$_{BIN}$
D[6:0]	ADC1_RESET_OFS	Defines the offset above or below the ADC1 threshold.	0000000$_{BIN}$

Table 160. System Thermal Alert Register ADC2 – Upper Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC2_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	ADC2_ALRT_HYS [3:0]				ADC2_ALRT[9:8]		E7$_{\text{HEX}}$	9E$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	PROCHOT_EN	Processor hot enable. 1= Enable, 0= Disable.	1$_{\text{BIN}}$
D[6]	ALRT_EN	System thermal alert enable. 1= Enable, 0= Disable.	1$_{\text{BIN}}$
D[5:2]	ADC2_ALRT_HYS [3:0]	Hysteresis value for ADC2_ALRT.	1001$_{\text{BIN}}$
D[1:0]	ADC2_ALRT[9:8]	Upper 2 bits of the ADC2_ALRT for the system temperature.	11$_{\text{BIN}}$

Table 161. System Thermal Alert Register ADC2 – Lower Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC2_THRMALRTL	R/W	ADC2_ALRT[7:0]								58$_{\text{HEX}}$	9F$_{\text{HEX}}$

Bit	Name	Function	Default
D[7:0]	ADC2_ALRT	Lower 8 bits of the ADC2_ALRT for the system temperature.	01011000$_{\text{BIN}}$

Table 162. System Thermal Reset Register ADC2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
ADC2_THRMRESET	R/W	ADC2_RESET_EN	ADC2_RESET_OFS [6:0]							00$_{\text{HEX}}$	A1$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	ADC2_RESET_EN	0 = Disable ADC2_RESET. 1 = Enable ADC2_RESET.	0$_{\text{BIN}}$
D[6:0]	ADC2_RESET_OFS	Defines the offset above or below the ADC2 threshold.	0000000$_{\text{BIN}}$

Table 163. THRM_STAT_CFG – Thermal Status Configuration

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
THRM_STAT_CFG	R/W	RSVD	PTC_ADC2	PTC_ADC1	PTC_ADC0	DIETEMP_EN	ADC2_EN	ADC1_EN	ADC0_EN	08_{HEX}	90_{HEX}

Bit	Name	Function	Default
D[7]	RSVD	Reserved.	0_{BIN}
D[6]	PTC_ADC2	PTC_ADCx = $1_{\text{BIN.}}$ Clear alert once ADC reading < ADCx_ALRT – ADCx_ALRT_HYS value. PTC_ADCx = 0_{BIN}. Clear alert once ADC reading > ADCx_ALRT – ADCx_ALRT_HYS value.	0_{BIN}
D[5]	PTC_ADC1		0_{BIN}
D[4]	PTC_ADC0		0_{BIN}
D[3]	DIETEMP_EN	Die temperature enable. 1= Enable, 0= Disable.	1_{BIN}
D[2]	ADC2_EN	ADC2 enable. 1= Enable, 0= Disable.	0_{BIN}
D[1]	ADC1_EN	ADC1 enable. 1= Enable, 0= Disable.	0_{BIN}
D[0]	ADC0_EN	ADC0 enable. 1= Enable, 0= Disable.	0_{BIN}

Table 164. THRMRSLTH – Thermal Result Register High (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMRSLTH	R	RSVD						DIETEMP[9:8]		See note [a] below.	$7E_{\text{HEX}}$

[a] The value depends on the operating conditions.

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved.	000000_{BIN}
D[1:0]	DIETEMP[9:8]	Upper 2 bits of the temperature result for P91E0 die temperature (DIETEMP).	–

Table 165. THRMRSLTL – Thermal Result Register Low (LSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMRSLTL	R	DIETEMP[7:0]								See note [a] below.	$7F_{HEX}$

[a] The value depends on the operating conditions.

Bit	Name	Function	Default
D[7:0]	DIETEMP[7:0]	Lower 8 bits of the temperature result for the P91E0 die temperature (DIETEMP).	–

The die temperature of the PMIC is calculated using Equation 1.

T_J conversion formula

$$T_J = DIETEMP[9:0] \times \left(\frac{180}{143}\right) - 154.6, \text{°C}$$

Equation 1

Table 166. VSYSRSLTH – VSYS Result Register High (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VSYSRSLTH	R	RSVD						VSYS[9:8]		00_{HEX}	80_{HEX}

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved.	000000_{BIN}
D[1:0]	VSYS[9:8]	Upper 2 bits of the ADC result for VSYS voltage.	00_{BIN}

Table 167. VSYSRSLTL – VSYS Result Register Low (LSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VSYSRSLTL	R	VSYS[7:0]								00_{HEX}	81_{HEX}

Bit	Name	Function	Default
D[7:0]	VSYS[7:0]	Lower 8 bits of the ADC result for VSYS voltage.	00000000_{BIN}

The actual VSYS voltage is calculated as follows:

VSYS Conversion Formula

$$VSYS = VSYS[9:0] \times \left(\frac{14}{3}\right) \times \left(\frac{1.2}{1024}\right) \text{ in V}$$

Equation 2

9.11 VR Current Monitoring

The P91E0 monitors DCD0, DCD1, DCD2, DCD5, and DCD6 switching regulator output currents and the corresponding I2C and SVID registers for current readings are shown below in volts. The output current reading of a regulator is valid and is proportion to the output current when it operates in PWM Mode and is calibrated for the number of DPUs, inductance value, and input/output voltages.

Table 168. Voltage Rails and Corresponding Result Register

Voltage Rails	I2C Register		SVID Rails Address	SVID Register
	I_{OUT_H}	I_{OUT_L}		I_{OUT} (hex)
DCD0	84_{HEX}	85_{HEX}	SVID_ID_DCD0	15_{HEX} [a]
DCD1	86_{HEX}	87_{HEX}	SVID_ID_DCD1	15_{HEX} [a]
DCD2	$8C_{HEX}$	$8D_{HEX}$	SVID_ID_DCD2	15_{HEX} [a]
DCD5	88_{HEX}	89_{HEX}	N/A	N/A
DCD6	$8A_{HEX}$	$8B_{HEX}$	N/A	N/A

[a] The reading of the output current (I_{OUT}) of DCD0, DCD1, and DCD2 using SVID is done by reading the SVID register 15_{HEX} (see Table 121). Which regulator is read is determined by the SVID address, which is part of the SVID command.

Table 169. IOUT_H – Current Result Register High (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
IOUT_H	R	IOUT[9:2]								00_{HEX}	See Table 168

Bit	Name	Function	Default
D[7:0]	IOUT[9:2]	Upper 8-bits of the current result for DCDx (IOUT).	00000000_{BIN}

Table 170. IOUT_L – Current Result Register Low (LSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
IOUT_L	R	RSVD						IOUT[1:0]		00_{HEX}	See Table 168

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved.	–
D[1:0]	IOUT[1:0]	Lower 2-bits of the current result for DCDx (IOUT). Always reads 00_{BIN}.	00_{BIN}

Normally, the regulators defined above are monitored in the SoC-S0 State. The output current is filtered and measured every 0.5ms (default). In sleep modes (standby modes), the frequency of measurement is set by VRIFRQS[1:0] bit field in the *VRIMONCTL* register (see Table 171). The *VRIMONCTL* control register provides the flexibility to enable/disable this function, define Active/Standby Mode, and set the measurement frequency.

Table 171. VR Current Monitor Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VRIMONCTL	R/W	RSVD		MODE	VRIFRQS[1:0]		VRIFRQA[1:0]		VRIMEN	$2B_{HEX}$	71_{HEX}

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved.	00_{BIN}
D[5]	MODE	Resets the two current monitoring timers based on the durations specified in VRIFRQS/VRIFRQA. 0 = Active Mode. VRIFRQA durations are used. 1 = Standby Mode. VRIFRQS durations are used. Read only bit. Active versus Standby selection set via VRI_TYPE.	1_{BIN}
D[4:3]	VRIFRQS[1:0]	Specifies the frequency at which VR current measurements are initiated while in standby mode (MODE=1). Values: 00 = Disabled 01 = 1ms (Default) 10 = 5ms 11 = 10ms	01_{BIN}
D[2:1]	VRIFRQA[1:0]	Specifies the frequency at which VR current measurements are initiated while in active mode (MODE=0). Values: 00 = 0.25s 01 = 0.5ms (Default) 10 = 1ms 11 = 3ms	01_{BIN}
D[0]	VRIMEN	Setting this bit enables ADC-based current monitoring timers. Current monitoring timers are reset when this bit is set to 1.	1_{BIN}

The result registers for VR current measurements can be defined in the same manner as the other result registers in the previous section. They are listed in the GPADC register requirements table.

Table 172. VR Current Monitor Mode Set Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VRI_MODE	R/W	RSVD		VRI_TYPE [1:0]		RSVD				30_{HEX}	E3_{HEX}

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved.	00_{BIN}
D[5:4]	VRI_TYPE	Selects the power states in which current monitoring by the ADC block is enabled: 00_{BIN} – Active = SoC-S0, SoC-S0Ix, SoC-S3, SoC-S4/S5. Standby = NA. 01_{BIN} – Active = SoC-S0, SoC-S0Ix, SoC-S3. Standby = SoC-S4/S5. 10_{BIN} – Active = SoC-S0, SoC-S0Ix. Standby= SoC-S3, SoC-S4/S5. 11_{BIN} – Active = S0. Standby= SoC-S0Ix, SoC-S3, SoC-S4/S5.	11_{BIN}
D[3:0]	RSVD	Reserved.	0000_{BIN}

9.12 Thermal Monitoring

The P91E0 is capable of monitoring the PMIC die temperature via an internal temperature measurement circuit. To provide flexibility, the *THRMMONCTL* control register is defined (see Table 173) to let the user enable/disable this function, define Active/Standby Mode, and set the measurement frequency.

The *THRMMONCTL* register is the master control for the timer-based thermal monitoring state machine.

Table 173. Thermal Monitor Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMMONCTL	R/W	RSVD			MODE	TEMPFRQS	TEMPFRQA[1:0]		THRMEN	15_{HEX}	8E_{HEX}

Bit	Name	Function	Default
D[7:5]	RSVD	Reserved.	000_{BIN}
D[4]	MODE	Resets the two thermal monitoring timers based on the durations specified in the TEMPFRQS/TEMPFRQA bits. 0 = Active Mode. TEMPFRQA durations used. 1 = Standby Mode. TEMPFRQS durations used. Read only bit. Active vs. Standby selection set via THRM_TYPE.	0_{BIN}
D[3]	TEMPFRQS	Specifies the frequency at which die temperature measurements are initiated while in Standby Mode (MODE bit = 1). Values: 0 = Disabled (Default). 1 = 30s.	0_{BIN}

Bit	Name	Function	Default
D[2:1]	TEMPFRQA[1:0]	Specifies the frequency at which die temperature measurements are initiated while in Active Mode (MODE bit = 0). Values: 00 = Disabled 01 = 5s 10 = 10s (Default) 11 = 30s	10_{BIN}
D[0]	THRMEN	Setting this bit enables the ADC-based thermal monitoring timers. Thermal monitoring timers are reset when this bit is set to 1. The P91E0 must still shut down if the die temperature exceeds its critical limit when this bit is set to 0.	1_{BIN}

Table 174. Thermal Monitor Mode Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRM_MODE	R/W	RSVD		THRM_TYPE[1:0]		RSVD				30_{HEX}	$E4_{HEX}$

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved.	00_{BIN}
D[5:4]	THRM_TYPE[1:0]	Defines sleep state(s) corresponding to the Active and Standby Mode for temperature measurement: 00_{BIN}: Active= SoC-S0, SoC-S0Ix, SoC-S3, SoC-S4/S5. Standby= NA. 01_{BIN}: Active= SoC-S0, SoC-S0Ix, SoC-S3. Standby= SoC-S4/S5. 10_{BIN}: Active= SoC-S0, SoC-S0Ix. Standby= SoC-S3, SoC-S4/S5. 11_{BIN}: Active= SoC-S0. Standby= SoC-S0Ix, SoC-S3, SoC-S4/S5.	11_{BIN}
D[3:0]	RSVD	Reserved.	0000_{BIN}

9.13 Thermal Alerts

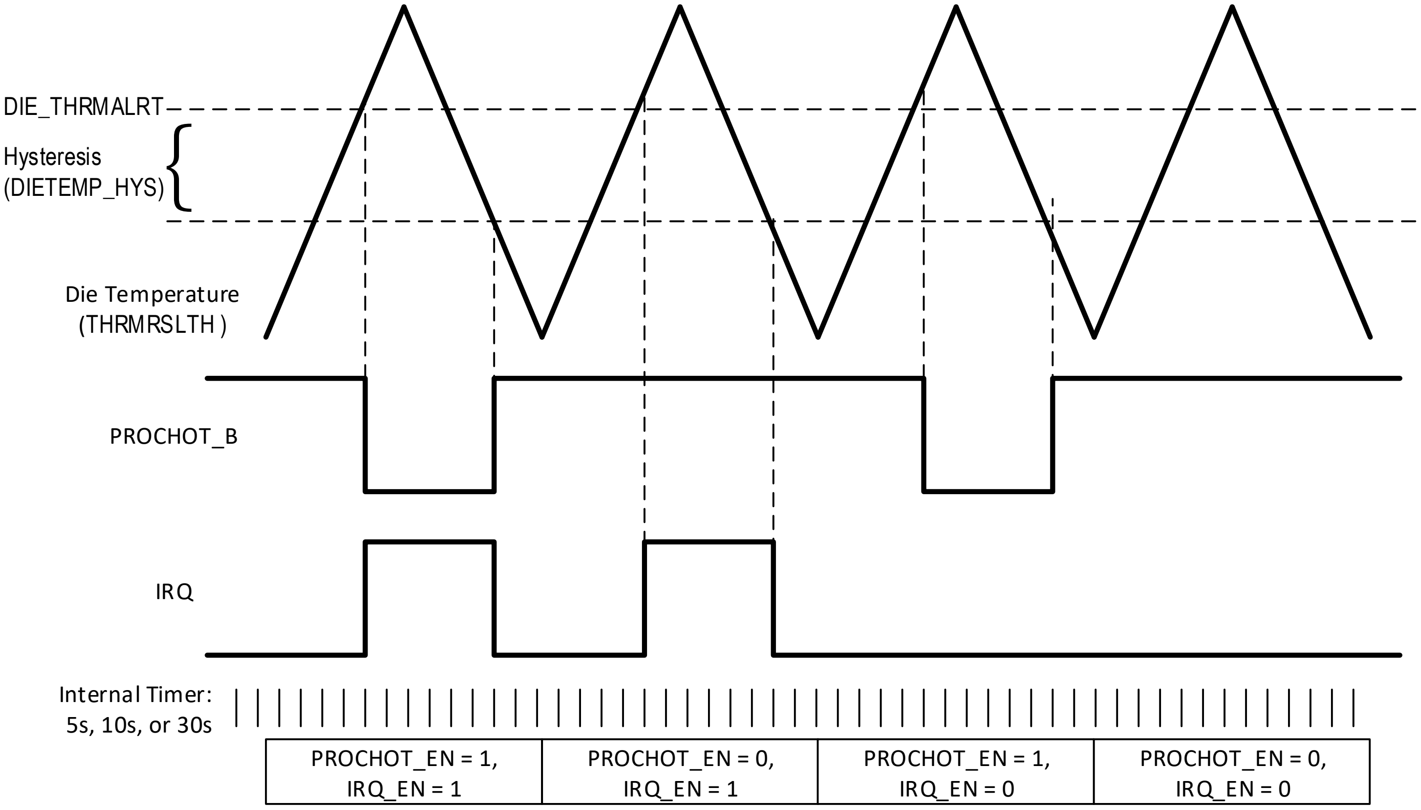
The P91E0 supports the capability to alert the SoC if the die temperature measurement value in D[1:0] of the *THRMRSLTH* register (two most-significant bits; see Table 164) combined with the *THRMRSLTL* register (lower 8 bits; see Table 165) is more than or equal to the configurable threshold value set by D[1:0] in the *DIE_THRMALRTH* register (two most-significant bits; see Table 175) combined with the *DIE_THRMALRTL* register (lower 8 bits; see Table 176). Depending on the settings in the *THRMMONCTL* control register (see Table 173), an internal timer initiates a die temperature measurement every 5, 10, or 30 seconds. After each measurement, the value is compared with the threshold setting. If the measured value is more than the threshold value, an alert condition has been detected. There are two actions that the P91E0 could initiate:

- Assert the PROCHOT_B pin (from HIGH to LOW). This pin notifies the SoC of a thermal event affecting the P91E0. This functionality is enabled by setting the PROCHOT_EN bit D[7] to 1 in the *DIE_THRMALRTH* register. When this enable bit is LOW, the PROCHOT_B pin remains HIGH, even if the die temperature exceeds the threshold value.
- Generate an interrupt request by asserting the IRQ pin (from LOW to HIGH). The IRQ_EN bit in the PMIC Die Temperature Threshold Register High (see Table 175) must be set to 1 and the interrupts must be enabled by the SoC or other device clearing the corresponding bits in the first-level IRQ mask (*MIRQLVL1* register; see Table 143) and the second-level *MTHRMIRQ* register (see Table 180). The IRQ pin stays asserted, even if the alert condition is no longer present. The SoC must clear the second-level interrupt register by writing logic 1 to the PMICALRT bit in *THRMIRQ* (see Table 179). The *STHRMIRQ* thermal monitor status register (see Table 181) is updated according to the current measured die temperature and is automatically cleared once the die temperature is outside the alert zone.

To avoid multiple assertions of the PROCHOT_B and the IRQ pins, when the die temperature is close to the threshold value, there is a configurable hysteresis, which determines the lower end of the alert zone. The upper end is determined by the die threshold value. The DIETEMP_HYS[3:0] bit field is located in the *DIE_THRMALRTH* register.

The operation of the thermal alerts of the P91E0 is shown in Figure 14.

Figure 14. Thermal Alerts



In addition to prescribing the ADC threshold for triggering an alert, there is also a register to set a die temperature threshold (*DIE_THRMALRTH),* and it can be configured to assert PROCHOT_B if the die temperature equals or exceeds the set temperature. The *DIE_THRMALRTH* register (see Table 175) includes a 4-bit field hysteresis (DIETEMP_HYS[5:2]), which defines hysteresis for the thermal alert. A hysteresis value is used to avoid spurious interrupt assertions when temperatures hover near the alert threshold.

When a thermal event is triggered for a particular sensor, the P91E0 takes the following actions:

- Sets the appropriate bit in the 2nd level thermal interrupt register (THRMIRQ)
- Setting this bit, in turn, sets the 1st level interrupt bit, triggering an interrupt to the SoC over the INT pin.
- Sets or clears (depending on ADC count) the appropriate status register in the *STHRMIRQ* status register.

The level 2 interrupt register for the thermal monitoring state machine, *THRMIRQ,* is defined in Table 179.

Table 175. PMIC Die Temperature Alert Threshold Register High

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DIE_THRMALRTH	R/W	PROCHOT_EN	EN	DIETEMP_HYS[3:0]				DIETEMP_ALRT[9:8]		E4$_{\text{HEX}}$	AF$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	PROCHOT_EN	Die Temperature Policy Action Enable. When set to 1, any crossover of the die temperature will assert PROCHOT_B and any cross below DIETEMP_HYST will de-assert PROCHOT_B.	1$_{\text{BIN}}$
D[6]	ALERT_EN	Die Measurement Enable: 1 = Enabled 0 = Disabled	1$_{\text{BIN}}$
D[5:2]	DIETEMP_HYS[3:0]	Hysteresis value for die temperature. T_{HYS} = DIETEMP_HYS[3:0] × 180/143	1001$_{\text{BIN}}$
D[1:0]	DIETEMP_ALRT[9:8]	Upper 2 bits of the temperature alert threshold for the die temperature. See Table 176 for remaining bits.	00$_{\text{BIN}}$

Table 176. PMIC Die Temperature Alert Threshold Register Low

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DIE_THRMALRTL	R/W	DIETEMP_ALRT[7:0]								D1$_{\text{HEX}}$ [a]	B0$_{\text{HEX}}$

[a] The value D1$_{\text{HEX}}$ = 11010001$_{\text{BIN}}$ corresponds to alert threshold 108°C (see Equation 1 for the relationship between the register value and temperature).

Bit	Name	Function	Default
D[7:0]	DIETEMP_ALRT[7:0]	Lower 8 bits of the temperature alert threshold for the die temperature. See Table 175 for upper two bits.	11010001$_{\text{BIN}}$

Table 177. PMIC Die Temperature Warning Threshold Register High

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
DIE_THRMWARNH	R/W	SALRT_EN	WARN_EN	DIETEMP_HYS [3:0]				DIETEMP_WARN[9:8]		E4$_{\text{HEX}}$	B1$_{\text{HEX}}$

Bit	Name	Function	Default
D[7]	SALRT_EN		1$_{\text{BIN}}$
D[6]	WARN_EN	Enable for warning for die over-temperature condition. 1= Enable, 0 = Disable.	1$_{\text{BIN}}$
D[5:2]	DIETEMP_HYS[3:0]	Hysteresis value for die over-temperature condition. T_{HYS} = DIETEMP_HYS[3:0] × 180/143.	1001$_{\text{BIN}}$
D[1:0]	DIETEMP_WARN[9:8]	Upper 2 bits of the temperature warning threshold for the die temperature.	00$_{\text{BIN}}$

Table 178. PMIC Die Temperature Warning Threshold Register Low

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
DIE_THRMWARNL	R/W	DIETEMP_WARN[7:0]								$D1_{HEX}$	$B2_{HEX}$

Bit	Name	Function	Default
D[7:0]	DIETEMP_WARN[7:0]	Lower 8 bits of temperature warning threshold for the die temperature.	11010001_{BIN}

Table 179. Thermal Monitor Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMIRQ	RW	RSVD				PMICALRT	ADC2ALRT	ADC1ALRT	ADC0ALRT	00_{HEX}	04_{HEX}

Bit	Name	Function	Default
D[7:4]	RSVD	Reserved.	0000_{BIN}
D[3]	PMICALRT	Set by the thermal state machine when the P91E0 die temperature thermal alert occurs. Write 1 to clear.	0_{BIN}
D[2]	ADC2ALRT	Set by the state machine when an ADC2 temperature thermal alert occurs.	0_{BIN}
D[1]	ADC1ALRT	Set by the state machine when an ADC1 temperature thermal alert occurs.	0_{BIN}
D[0]	ADC0ALRT	Set by the state machine when an ADC0 temperature thermal alert occurs.	0_{BIN}

Table 180. Thermal Monitor Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MTHRMIRQ	R/W	RSVD				MPMICALRT	MADC2ALRT	MADC1ALRT	MADC0ALRT	$0F_{HEX}$	11_{HEX}

Bit	Name	Function	Default
D[7:4]	RSVD	Reserved.	0000_{BIN}
D[3]	MPMICALRT	Set by the thermal state machine when a PMIC die temperature thermal alert occurs. 0 = MPMICALRT IRQ unmasked. 1 = MPMICALRT IRQ masked.	1_{BIN}
D[2]	MADC2ALRT	Set by the state machine if an ADC2 temperature thermal alert occurs.	1_{BIN}
D[1]	MADC1ALRT	Set by the state machine if an ADC1 temperature thermal alert occurs.	1_{BIN}
D[0]	MADC0ALRT	Set by the state machine if an ADC0 temperature thermal alert occurs.	1_{BIN}

The thermal interrupt status register, STHRMIRQ is defined in Table 181. If an alert condition is removed, the status bit will clear. However, the interrupt generated (D[3] in the *THRMIRQ* second-level interrupt register; see Table 179) will persist until cleared by the SoC.

Table 181. Thermal Monitor Status Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
STHRMIRQ	R/W	RSVD				SPMICALRT	SADC2ALRT	SADC1ALRT	SADC0ALRT	00_{HEX}	05_{HEX}

Bit	Name	Function	Default
D[7:4]	RSVD	Reserved.	0000_{BIN}
D[3]	SPMICALRT	Set to 1 by the thermal state machine if a P91E0 die temperature thermal alert is occurring.	0_{BIN}
D[2]	SADC2ALRT	Set to 1 by the state machine if an ADC2 temperature thermal alert is occurring.	0_{BIN}
D[1]	SADC1ALRT	Set to 1 by the state machine if an ADC1 temperature thermal alert is occurring.	0_{BIN}
D[0]	SADC0ALRT	Set to 1 by the state machine if an ADC0 temperature thermal alert is occurring.	0_{BIN}

10. Register Map

Note: Addresses 03_{HEX}, $0F_{\text{HEX}}$, 32_{HEX}, $3A_{\text{HEX}}$, $6E_{\text{HEX}}$, $6F_{\text{HEX}}$, 73_{HEX}, 83_{HEX}, 91_{HEX}, 92_{HEX}, 93_{HEX}, 96_{HEX}, 98_{HEX}, $9B_{\text{HEX}}$, $A2_{\text{HEX}}$, $A3_{\text{HEX}}$, $E5_{\text{HEX}}$, and FF_{HEX} are registers for internal debug use.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
VENDOR_ID	R	VENDOR_ID[7:0]								00
REVISION	R	RSVD		MAJREV0[2:0]			MINREV0[2:0]			01
IRQLVL1	R/W	RSVD	VR	GPIO	RSVD	ADC	RSVD	THRM	RSVD	02
THRMIRQ	R/W	RSVD				PMICALRT	ADC2ALRT	ADC1ALRT	ADC0ALRT	04
STHRMIRQ	R/W	RSVD				SPMICALRT	SADC2ALRT	SADC1ALRT	SADC0ALRT	05
DPS0_CONFIG	R/W	RSVD		GM0	RSVD			OFF_DLY[1:0]		06
DPS0_PMSTATUS	R	DPS0_PMSTATUS[7:0]								07
ADCIRQ	R/W	VSYS	VRI	RSVD	RSVD	ADC	RSVD			08
DPS1_CONFIG	R/W	RSVD		GM1	RSVD			OFF_DLY[1:0]		09
DPS1_PMSTATUS	R	DPS1_PMSTATUS[7:0]								0A
GPIO0IRQ	R/W	RSVD	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	0B
GPIO1IRQ	R/W	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	0C
DPS56_CONFIG	R/W	RSVD				GM6	BW6	GM5	BW5	0D
MIRQLVL1	R/W	RSVD	MVR	MGPIO	RSVD	MADC	RSVD	MTHRM	RSVD	0E
CORE_TYPE_EXIT	R/W	RSVD						DCD1EXIT	DCD0EXIT	10
MTHRMIRQ	R/W	RSVD				MPMICALRT	MADC2ALRT	MADC1ALRT	MADC0ALRT	11
LDO0_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					12
LDO1_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					13
LDO2_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					14
MADCIRQ	R/W	MVSYS	MVRI	RSVD		MADC_TEMP	RSVD			15
LDO3_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					16
LDO4_VOUT	R/W	RSVD			Output Voltage Setting (see Table 12)					17
LDO6_VOUT	R/W	RSVD		Output Voltage Setting (see Table 12)						18
MGPIO0IRQ	R/W	RSVD	MGPIO14	MGPIO13	MGPIO12	MGPIO11	MGPIO10	MGPIO9	MGPIO8	19
MGPIO1IRQ	R/W	RSVD	VR	GPIO	RSVD	ADC	RSVD	THRM	RSVD	1A
DPS2_CONFIG	R/W	RSVD		GM2	RSVD			OFF_DLY[1:0]		1B
DPS2_PMSTATUS	R	DPS2_PMSTATUS [7:0]								1C
DPS3_CONFIG	R/W	RSVD	DAMPB3	GM3	BW [2:0]			OFF_DLY[1:0]		1D
DPS3_PMSTATUS	R	DPS3_PMSTATUS [7:0]								1E
DCLL_CTL	R/W	RSVD					DC_LL[2:0]			1F
RESETSRC0	R/W	RSYSTEMP2	RSYSTEMP1	RSYSTEMP0	I2C_RESET	RSVD	RPWRBTIN	RPMICTEMP	RTHERMTRIP	20
RESETSRC1	R/W	RVSYSUVP	DCD1_OV	DCD0_OV	SUSPWRDNAK	VBAK_RCHG/VBAK_VCHG				21
WAKESRC	R	RSVD							WAKEPBTN	22

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
DPS4_CONFIG	R/W	RSVD	DAMPB4	GM4	BW [2:0]			OFF_DLY[1:0]		23
DPS4_PMSTATUS	R	DPS4_PMSTATUS [7:0]								24
ACLL_CTL	R/W	RSVD					AC_LL			25
PBCONFIG	R/W	RSVD		CLRHT	CLRFLT	FLT				26
PBSTATUS	R	RSVD			PBLVL	PBHT				27
RSMRSTCFG	R/W	RSVD								28
MODEMCTRL	R/W	RSVD						MODEMRSTSEQ	MODEM_OFF	29
PWRSEQCFG	R/W	RSVD				VCCAPWROK CFG	SUSPWRDNACK CFG	DTPWROK		2A
GPIOCTLO8	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	2B
GPIOCTLO9	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	2C
GPIOCTLO10	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	2D
GPIOCTLO11	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	2E
GPIOCTLO12	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	2F
GPIOCTLO13	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	30
GPIOCTLO14	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL		DOUT	31
GPIOCTLI8	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	33
GPIOCTLI9	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	34
GPIOCTLI10	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	35
GPIOCTLI11	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	36
GPIOCTLI12	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	37
GPIOCTLI13	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	38
GPIOCTLI14	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	39
GPIOCTLO0	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	3B
GPIOCTLO1	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	3C
GPIOCTLO2	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	3D
GPIOCTLO3	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	3E
GPIOCTLO4	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	3F
GPIOCTLO5	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	40
GPIOCTLO6	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	41
GPIOCTLO7	R/W	RSVD	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	42
GPIOCTLI0	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	43
GPIOCTLI1	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	44
GPIOCTLI2	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	45
GPIOCTLI3	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	46
GPIOCTLI4	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	47
GPIOCTLI5	R/W	RSVD			GPIGLBYP	GPIDBNC	INTCNT		DIN	48
GPIOCTLI6	R/W	RSVD		GPIGLBYP	GPIDBNC	INTCNT	DIN		RSVD	49

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
GPIOCTLI7	R/W	RSVD		GPIGLBYP	GPIDBNC	INTCNT	DIN		RSVD	4A
PWM0CLKDIV	R/W	ENABLE	CLKDIV0							4B
PWM1CLKDIV	R/W	ENABLE	CLKDIV0							4C
SLEEP_CTL	R/W	RSVD					POL	SEL	EN	4D
PWM0DUTYCYCLE	R/W	DUTYCYCLE0								4E
PWM1DUTYCYCLE	R/W	DUTYCYCLE1								4F
S0IxCFG	R/W	RSVD							NOS0Ix	50
BLIGHT_EN	R/W	RSVD							BKLGHT_ENOUT	51
PANEL_EN	R/W	RSVD							PANEL_ENOUT	52
DCD0_CTL	R/W	RSVD			SVID	RSVD		RAIL_SEL	RAIL_EN	53
DCD1_CTL	R/W	RSVD			SVID	RSVD		RAIL_SEL	RAIL_EN	54
DCD6_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	55
EN0_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	56
EN1_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	57
LDO5_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	58
DCD5_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	59
DCD4_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	5A
EN2_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	5B
EN3_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	5C
EN4_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	5D
LDO3_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	5E
DCD2_CTL	R/W	RSVD			SVID	RSVD		RAIL_SEL	RAIL_EN	5F
LDO4_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	60
LDO1_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	61
EN8_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	62
SEQ_STATUS	R	SEQ_STATUS								63
EN7_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	64
LDO0_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	65
LDO2_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	66
DCD3_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	67
EN6_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	68
EN5_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	69
LDO6_CTL	R/W	RSVD						RAIL_SEL	RAIL_EN	6A
EN9_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	6B
EN10_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	6C
EN11_CTL	R/W	RSVD					POLARITY	RAIL_SEL	RAIL_EN	6D
DILIM	R/W	RSVD						DILIM2	DILIM1	70
VRIMONCTL	R/W	RSVD		MODE	VRIFRQS		VRIFRQA		VRIM_EN	71

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
GRADCREQ	R/W	VSYS	VRI	RSVD		ADC_TEMP	RSVD	IRQ_EN	BUSY	72
ADCRSLT0H	R	RSVD							ADC0[9:8]	74
ADCRSLT0L	R	ADC0[7:0]								75
ADCRSLT1H	R	RSVD							ADC1[9:8]	76
ADCRSLT1L	R	ADC1[7:0]								77
ADCRSLT2H	R	RSVD							ADC2[9:8]	78
ADCRSLT2L	R	ADC2[7:0]								79
DPS_IDLE_CFG	R/W	RSVD					EN_PS_IDLE2	EN_PS_IDLE1	EN_PS_IDLE0	7A
VSLEEP	R/W	VSLEEP[7:0]								7B
DRAMPWROK	R/W	RSVD					DCD_SEL			7C
EN11_GPR	R/W	RSVD		EN11_TYPE[1:0]		EN11_GROUP[3:0]				7D
DIETEMPRSLTH	R	RSVD						DIETEMP[9:8]	RSVD	7E
DIETEMPRSLTL	R	DIETEMP[7:0]								7F
DIETEMPRSLTH	R	RSVD						VSYS[9:8]	RSVD	80
DIETEMPRSLTL	R	VSYS[7:0]								81
MODE	R/W	RSVD			CHG_STAT	RSVD	RSVD	TURNOFF_CRIT	RESET_CRIT	82
IOUT_H (DCD0)	R	RSVD						DCD0_IOUT[9:8]	RSVD	84
IOUT_L (DCD0)	R	DCD0_IOUT[7:0]								85
IOUT_H (DCD1)	R	RSVD						DCD1_IOUT[9:8]	RSVD	86
IOUT_L (DCD1)	R	DCD1_IOUT[7:0]								87
IOUT_H (DCD5)	R	RSVD						DCD5_IOUT[9:8]	RSVD	88
IOUT_L (DCD5)	R	DCD5_IOUT[7:0]								89
IOUT_H (DCD6)	R	RSVD						DCD6_IOUT[9:8]	RSVD	8A
IOUT_L (DCD6)	R	DCD6_IOUT[7:0]								8B
IOUT_H (DCD2)	R	RSVD						DCD2_IOUT[9:8]	RSVD	8C
IOUT_L (DCD2)	R	DCD2_IOUT[7:0]								8D
THRIMMONCTL	R/W	RSVD			MODE	TEMPFRQS	TEMPFRQA[1:0]		THRM_EN	8E
DCD_PG	R	RSVD	DCD_PG[6:0]	RSVD						8F
THRM_STAT_CFG	R/W	RSVD	PTC_ADC2	PTC_ADC1	PTC_ADC0	DIETEMP_EN	ADC2_EN	ADC1_EN	ADC0_EN	90
EXP2	R/W	RSVD						PMIC_ADR_CONFIG		92
ADC0_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	ADC0_ALRT_HYS[3:0]				ADC0_ALRT[9:8]		94
ADC0_THRMALRTL	R/W	ADC0_ALRT[7:0]								95
ADC0_THRMRESET	R/W	ADC0_RESET_EN	ADC0_RESET_OFS[6:0]							97
ADC1_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	ADC1_ALRT_HYS[3:0]				ADC1_ALRT[9:8]		99
ADC1_THRMALRTL	R/W	ADC1_ALRT[7:0]								9A

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
ADC1_THRMRESET	R/W	ADC1_RESET_EN	ADC1_RESET_OFS[6:0]							9C
LDOFI	R	LDO7_SC	LDO6_SC	LDO5_SC	LDO4_SC	LDO3_SC	LDO2_SC	LDO1_SC	LDO0_SC	9D
ADC2_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	ADC2_ALRT_HYS[3:0]				ADC2_ALRT[9:8]		9E
ADC2_THRMALRTL	R/W	ADC2_ALRT[7:0]								9F
DCD_ILIM	R/W	ILIM100US	DCD6_ILIM	DCD5_ILIM	RSVD		DCD2_ILIM	DCD1_ILIM	DCD0_ILIM	A0
ADC2_THRMRESET	R/W	ADC2_RESET_EN	ADC2_RESET_OFS[6:0]							A1
DCD3_VOUT	R/W	DCD3_RNG[1:0]		DCD3_VOUT[5:0]						A4
DCD4_VOUT	R/W	DCD4_RNG[1:0]		DCD4_VOUT[5:0]						A5
DCD5_VOUT	R/W	DCD5_RNG[1:0]		DCD5_VOUT[5:0]						A6
DCD6_VOUT	R/W	DCD6_RNG[1:0]		DCD6_VOUT[5:0]						A7
DCD0_SLEW	R/W	RSVD		FAST_RATE [1:0]	RSVD				SLOW_RATE	A8
DCD1_SLEW	R/W	RSVD		FAST_RATE [1:0]	RSVD				SLOW_RATE	A9
DCD2_SLEW	R/W	RSVD		FAST_RATE [1:0]	RSVD				SLOW_RATE	AA
S0Ix_EN	R/W	RSVD					S0Ix_DCD2	S0Ix_DCD1	S0Ix_DCD0	AB
S0Ix_ID	R/W	RSVD		S0Ix_ID_DCD2	RSVD	S0Ix_ID_DCD2	RSVD	S0Ix_ID_DCD2	RSVD	AC
FPWM	R/W	RSVD	DCD6_FPWM	DCD5_FPWM	DCD4_FPWM	DCD3_FPWM	DCD2_FPWM	DCD1_FPWM	DCD0_FPWM	AD
DCD_OC	R/W	RSVD	DCD6_OC	DCD5_OC	RSVD		DCD2_OC	DCD1_OC	DCD0_OC	AE
DIE_THRMALRTH	R/W	PROCHOT_EN	ALRT_EN	DIETEMP_HYS[3:0]				DIETEMP _ALRT[9:8]		AF
DIE_THRMALRTL	R/W	DIETEMP _ALRT[7:0]								B0
DIE_THRMWARNH	R/W	SALRT_EN	WARN_EN	DIETEMP_HYS[3:0]				DIETEMP _ALRT[9:8]		B1
DIE_THRMWARNL	R/W	DIETEMP _WARN[7:0]								B2
PROD_ID	R	PROD_ID [7:0]								B3
PROTOCOL_ID	R	PROTOCOL [7:0]								B4
CAPABILITY (DCD0)	R	CAPABILITY [7:0]								B5
STATUS_1	R	STATUS_1 [7:0]								B6
STATUS_2	R	STATUS_2 [7:0]								B7
STATUS2_PREV	R	STATUS2_PREV [7:0]								B8
ICC_MAX (DCD0)	R	ICC_MAX [7:0] (Default 05h: 5A) - Part configurations at power up based on the number of DPUs used								B9
SR_FAST (DCD0)	R	Reading this returns the slew rate from SetVID Fast in the DCD0SLEW register								BA
SR_SLOW (DCD0)	R	Reading this returns the slew rate from SetVID SLOW in the DCD0SLEW register								BB
VBOOT (DCD0)	R/W	VBOOT[7:1]							VBOOT[0]	BC
VOUT_ MAX (DCD0)	R/W	VOUT_MAX [7:0]								BD

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
VID (DCD0)	R/W	VID [7:1]							VID [0]	BE
PWR_ST (DCD0)	R/W	PWR_STATE[1:0]		RSVD						BF
VOFS (DCD0)	R/W	VOFS [7:0]								C0
MULTI_VR (DCD0)	R/W	RSVD						LCK_VID_PS	VRDY_0V	C1
SET_REG_ADR (DCD0)	R	SET_REG_ADR [7:0]								C2
SEQA_TIM	R/W	RSVD	DLY_GRP_OFF_A[2:0]			RSVD	DLY_GRP_ON_A[2:0]			C3
SEQU_TIM	R/W	RSVD	DLY_GRP_OFF_U[2:0]			RSVD	DLY_GRP_ON_U[2:0]			C4
CAPABILITY (DCD1)	R	CAPABILITY [7:0]								C5
STATUS_1	R	STATUS_1 [7:0]								C6
STATUS_2	R	STATUS_2 [7:0]								C7
STATUS2_PREV	R	STATUS2_PREV [7:0]								C8
ICC_MAX (DCD1)	R	ICC_MAX [7:0] (Default 05h: 5A) - Part configurations at power up based on the number of DPUs used								C9
SR_FAST (DCD1)	R	Reading this returns the slew rate from SetVID Fast in the DCD1SLEW register								CA
SR_SLOW (DCD1)	R	Reading this returns the slew rate from SetVID SLOW in the DCD1SLEW register								CB
VBOOT (DCD1)	R/W	VBOOT[7:1]							VBOOT[0]	CC
VOUT_ MAX (DCD1)	R/W	VOUT_ MAX [7:0]								CD
VID (DCD1)	R/W	VID [7:1]							VID [0]	CE
PWR_ST (DCD1)	R/W	PWR_STATE[1:0]		RSVD						CF
VOFS (DCD1)	R/W	VOFS [7:0]								D0
MULTI_VR (DCD1)	R/W	RSVD						LCK_VID_PS	VRDY_0V	D1
SET_REG_ADR (DCD1)	R	SET_REG_ADR [7:0]								D2
SEQS_TIM	R/W	RSVD	DLY_GRP_OFF_S[2:0]			RSVD	DLY_GRP_ON_S[2:0]			D3
SEQSX_TIM	R/W	RSVD	DLY_GRP_OFF_SX[2:0]			RSVD	DLY_GRP_ON_SX[2:0]			D4
CAPABILITY (DCD2)	R	CAPABILITY [7:0]								D5
STATUS_1	R	STATUS_1 [7:0]								D6
STATUS_2	R	STATUS_2 [7:0]								D7
STATUS2_PREV	R	STATUS2_PREV [7:0]								D8
ICC_MAX (DCD2)	R	ICC_MAX [7:0] (Default 05h: 5A) – Part configurations at power up based on the number of DPUs used								D9
SR_FAST (DCD2)	R	Reading this returns the slew rate from SetVID Fast in the DCD2SLEW register								DA
SR_SLOW (DCD2)	R	Reading this returns the slew rate from SetVID SLOW in the DCD2SLEW register								DB
VBOOT (DCD2)	R/W	VBOOT[7:1]							VBOOT[0]	DC
VOUT_ MAX (DCD2)	R/W	VOUT_ MAX [7:0]								DD
VID (DCD2)	R/W	VID [7:1]							VID [0]	DE
PWR_ST (DCD2)	R/W	PWR_STATE[1:0]		RSVD						DF
VOFS (DCD2)	R/W	VOFS [7:0]								E0
MULTI_VR (DCD2)	R/W	RSVD						LCK_VID_PS	VRDY_0V	E1

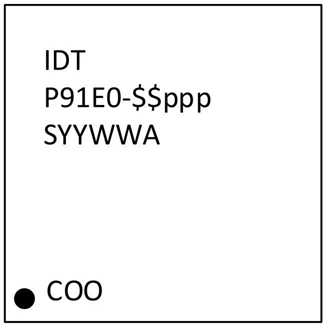
Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Address (HEX)
SET_REG_ADR (DCD2)	R	SET_REG_ADR [7:0]								E2
VRI_MODE	R/W	RSVD		VRI_TYPE[1:0]		RSVD				E3
THRM_MODE	R/W	RSVD		THRM_TYPE[1:0]		RSVD				E4
DCD0_GRP	R/W	DCD0_TYPE_EXIT[1:0]		DCD0_TYPE[1:0]		DCD0_GROUP[3:0]				E6
DCD1_GRP	R/W	DCD0_TYPE_EXIT[1:0]		DCD1_TYPE[1:0]		DCD1_GROUP[3:0]				E7
DCD2_GRP	R/W	RSVD		DCD2_TYPE[1:0]		DCD2_GROUP[3:0]				E8
DCD3_GRP	R/W	RSVD		DCD3_TYPE[1:0]		DCD3_GROUP[3:0]				E9
DCD4_GRP	R/W	RSVD		DCD4_TYPE[1:0]		DCD4_GROUP[3:0]				EA
DCD5_GRP	R/W	RSVD		DCD5_TYPE[1:0]		DCD5_GROUP[3:0]				EB
DCD6_GRP	R/W	RSVD		DCD6_TYPE[1:0]		DCD6_GROUP[3:0]				EC
LDO0_GRP	R/W	RSVD		LDO0_TYPE[1:0]		LDO0_GROUP[3:0]				ED
LDO1_GRP	R/W	RSVD		LDO1_TYPE[1:0]		LDO1_GROUP[3:0]				EE
LDO2_GRP	R/W	RSVD		LDO2_TYPE[1:0]		LDO2_GROUP[3:0]				EF
LDO3_GRP	R/W	RSVD		LDO3_TYPE[1:0]		LDO3_GROUP[3:0]				F0
LDO4_GRP	R/W	RSVD		LDO4_TYPE[1:0]		LDO4_GROUP[3:0]				F1
LDO5_GRP	R/W	RSVD		LDO5_TYPE[1:0]		LDO5_GROUP[3:0]				F2
LDO6_GRP	R/W	RSVD		LDO6_TYPE[1:0]		LDO6_GROUP[3:0]				F3
EN0_GRP	R/W	RSVD		EN0_TYPE[1:0]		EN0_GROUP[3:0]				F4
EN1_GRP	R/W	RSVD		EN1_TYPE[1:0]		EN1_GROUP[3:0]				F5
EN2_GRP	R/W	RSVD		EN2_TYPE[1:0]		EN2_GROUP[3:0]				F6
EN3_GRP	R/W	RSVD		EN3_TYPE[1:0]		EN3_GROUP[3:0]				F7
EN4_GRP	R/W	RSVD		EN4_TYPE[1:0]		EN4_GROUP[3:0]				F8
EN5_GRP	R/W	RSVD		EN5_TYPE[1:0]		EN5_GROUP[3:0]				F9
EN6_GRP	R/W	RSVD		EN6_TYPE[1:0]		EN6_GROUP[3:0]				FA
EN7_GRP	R/W	RSVD		EN7_TYPE[1:0]		EN7_GROUP[3:0]				FB
EN8_GRP	R/W	RSVD		EN8_TYPE[1:0]		EN8_GROUP[3:0]				FC
EN9_GRP	R/W	RSVD		EN9_TYPE[1:0]		EN9_GROUP[3:0]				FD
EN10_GRP	R/W	RSVD		EN10_TYPE[1:0]		EN10_GROUP[3:0]				FE

11. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/100-gqfn-package-outline-drawing-90-x-90-x-085-mm-body-epad-510-x-510-mm-05065mm-pitch-nhg100p1

12. Marking Diagram



Line 1: IDT

Line 2: Part number

- "-$$" = specific configuration
- "ppp" = package type

Line 3:

- "S" = device stepping
- "YYWW" is the last digit of the year and week that the part was assembled.
- "A" = assembly location

Line 4: COO denotes the lot number.

13. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
P91E0-I5NHGI	P91E0 IC packaged in a thermally-enhanced 9.0 × 9.0 × 0.85 mm 100-VFQFPN	3	Tray	-40°C to +85°C
P91E0-I5NHGI8	P91E0 IC packaged in a thermally-enhanced 9.0 × 9.0 × 0.85 mm 100-VFQFPN	3	Reel	-40°C to +85°C

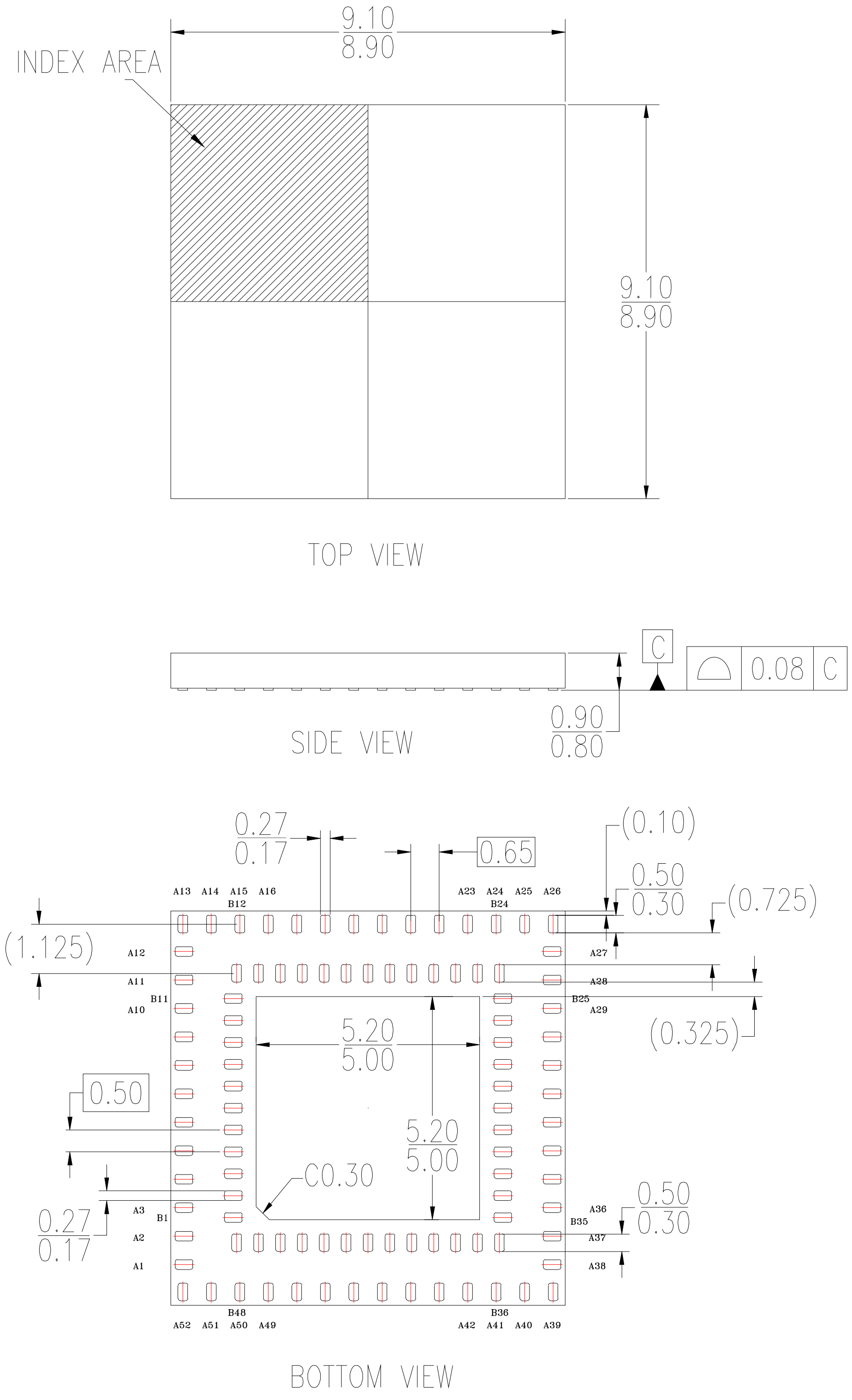
14. Revision History

Revision Date	Description of Change
November 2, 2018	▪ Corrections for Table 168. ▪ Minor edits
September 26, 2018	Initial release.

100-GQFN Package Outline Drawing

9.0 x 9.0 x 0.85 mm Body, Epad 5.10 x 5.10 mm, 0.50/65mm Pitch

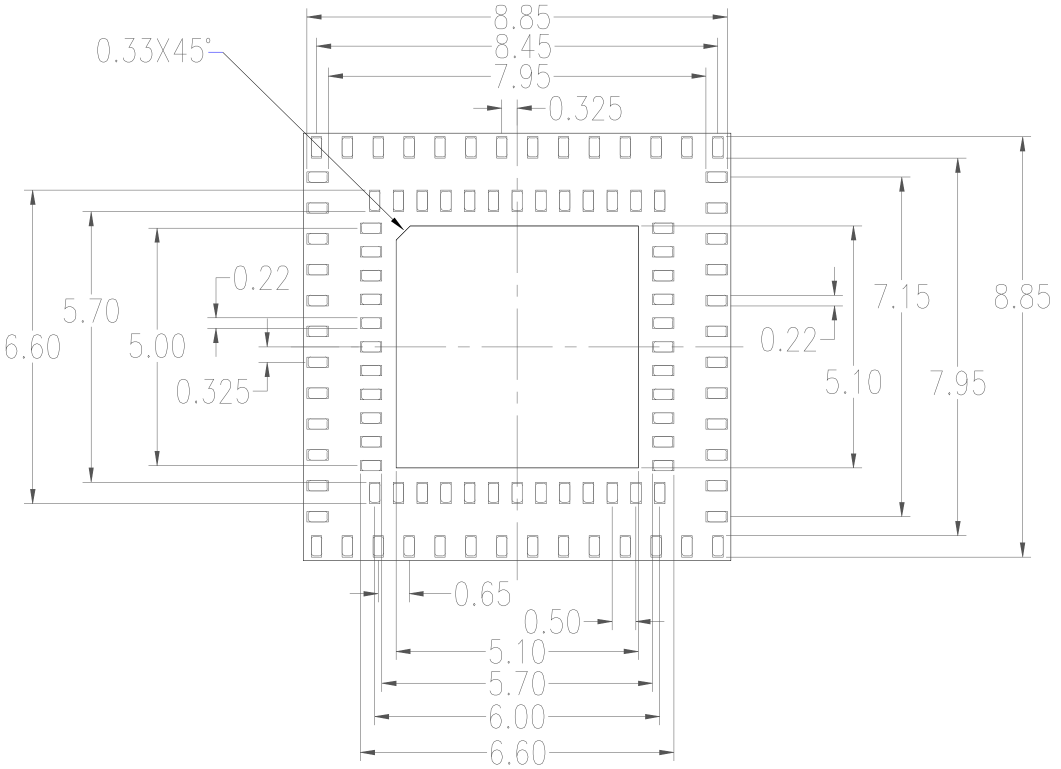
NHG100P1, PSC-4488-01, Rev 02, Page 1



NOTE: ALL DIMENSIONS IN MM.

100-GQFN Package Outline Drawing

9.0 x 9.0 x 0.85 mm Body, Epad 5.10 x 5.10 mm, 0.50/65mm Pitch
NHG100P1, PSC-4488-01, Rev 02, Page 2



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History

Date Created	Rev No.	Description
Sept 6, 2018	Rev 01	New Format, Add GQFN Package Category
March 17, 2020	Rev 02	Add Coplanarity Tolerance

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