

An Introduction to and Comparison of 74HCT TTL Compatible CMOS Logic

Fairchild Semiconductor
Application Note 368
March 1984



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The 54HC/74HC series of high speed CMOS logic is unique in that it has a sub-family of components, designated 54HCT/74HCT. Generally, when one encounters a 54/74 series number, the following letters designate some speed and power performance, usually determined by the technology used. Of course, the letters HC designate high speed CMOS with the same pinouts and functions as the 54LS/74LS series. The sub-family of HC, called HCT, is nearly identical to HC with the exception that its input levels are compatible with TTL logic levels.

This simple difference can, however, lead to some confusion as to why HCT is needed; how HCT should be used; how it is implemented; when it should be used; and how its performance compares to HC or LS. This paper will attempt to answer these questions.

It should also be noted that not all HCTs are the same. That is, HCTs from other vendors may have some characteristics that are different. Thus, when discussing general characteristics this paper will directly address Fairchild Semiconductor's 54HCT/74HCT which is compatible with JEDEC standard 7. Other vendors' ICs which also meet this standard will probably have similar characteristics.

WHY DOES HCT EXIST?

Ideally, when a designer sits down to design a low power high speed system, he would like to use 54HC/74HC, and CMOS LSI components. Unfortunately, due to system requirements he may have to use NMOS microprocessors and their NMOS or bipolar peripherals or bipolar logic (54S/74S,

54F/74F, 54ALS/74ALS, or 54AS/74AS) because either the specific function does not exist in CMOS or the CMOS device may not have adequate performance. Since the system designer still desires to use HC where possible, he will mix HC with these products. If these devices are specified to be TTL compatible, incompatibilities may result at the interface between the TTL, NMOS, etc. and HC.

More specifically, in the case of where a TTL or NMOS output may drive an HC input, a specification incompatibility results. Table 1 lists the output drive specifications of TTL compatible outputs with the input specifications of 54HC/74HC. Notice that the output high level of a TTL specified device will not be guaranteed to have a logic high output voltage level that will be guaranteed to be recognized as a valid logic high input level by HC. A TTL output will be equal to or greater than 2.4V, but an HCMOS input needs at least 3.15V. It should be noted that in an actual application the TTL output will pull-up probably to about V_{CC} minus 2 diode voltages, and HC will accept voltages as low as 3V as a valid one level so that in almost all cases there is no problem driving HC with TTL.

Even with the specified incompatibility, it is possible to improve the TTL-CMOS interface without using HCT. Figure 1 illustrates this solution. By merely tying a pull-up resistor from the TTL output to V_{CC} , this will force the output high voltage to go to V_{CC} . Thus, HC can be directly interfaced very easily to TTL. This works very well for systems with a few lines requiring pull-ups, but for many interfacing lines, HCT will be a better solution.

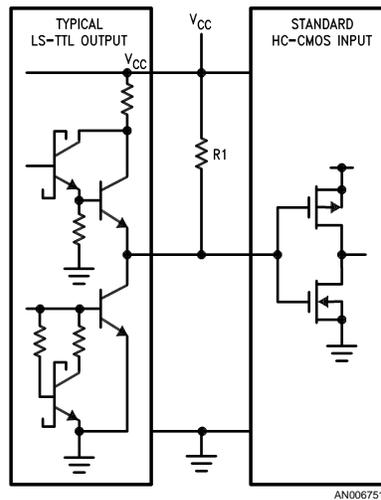


FIGURE 1. Interfacing LS-TTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor

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The input high logic level of HC is the only source of incompatibility. 54HC/74HC can drive TTL easily and its input low level is TTL compatible. Again referring to *Table 1*, the logic output of the TTL type device will be recognized to be a valid logic low (0) level, so there is no incompatibility here. *Table 2* shows that the specified output drive of HC is capable of driving many LS-TTL inputs, so there is no incompatibility here either (although one should be aware of possible fanout restrictions similar to that encountered when designing with TTL).

The question then arises: since only the input high level must be altered, why not design CMOS logic to be TTL compatible? 54HC/74HC was designed to optimize performance in all areas, and making a completely TTL compatible logic family would sacrifice significant performance. Most importantly, there is a large loss of AC noise immunity, and there are speed and/or die size penalties when trying to design for TTL input levels.

Thus, since it is obvious that there is a need to interface with TTL and TTL compatible logic, yet optimum performance would be sacrificed, a limited sub-family of HCT devices was created. It is completely TTL input compatible, which enables guaranteed direct connection of TTL outputs to its inputs. In addition, HCT still provides many of the other advantages of 54HC/74HC.

WHEN TO USE 54HCT/74HCT LOGIC

The 54HCT/74HCT devices are primarily intended to be used to provide an easy method of interfacing between TTL compatible microprocessor and associated peripherals and bipolar TTL logic to 54HC/74HC. There are essentially two application areas where a designer will want to perform this interface.

1. The first case is illustrated in *Figure 2*. In this case the system is a TTL compatible microprocessor. This figure shows an NS16XXX (any NMOS μ P may be substituted) that is in a typical system and therefore must be interfaced to 54HC/74HC. In this instance, the popular gate, buffer, decoder, and flip-flop functions provided in the 54HCT/74HCT sub-family can be used to interface the many lines that come from TTL compatible outputs. It is also easy to upgrade this configuration to an *all* CMOS system once the CMOS version of the microprocessor is available by replacing the HCT with HC.
2. A second application is, when in speed-critical situations a faster logic element than HC, probably ALS or AS, must be used in a predominantly 54HC/74HC system, or a specific logic function unique to TTL is placed into an HC design. This situation is illustrated in *Figure 3*. In this case, pull-up resistors on an HC input may be sufficient, but if not, then an HCT can be used to provide the guaranteed interface.

TABLE 1. Output Specifications for LS-TTL and NMOS LSI Compared to the Input Specifications for HCT and HC

	LS Output		NMOS Output		HC Inputs		HCT Input		
	V _{OUT}	I _{OUT}	V _{OUT}	I _{OUT}	V _{IN}	I _{IN}	V _{IN}	I _{IN}	
Output High	2.7V	400 μA	2.4V	400 μA	3.15V	1 μA	2.0V	1 μA	Input High
Output Low	0.5V	8.0 mA	0.4V	2.0 mA	0.9V	1 μA	0.8V	1 μA	Input Low

Note 1: V_{CC} = 4.5V

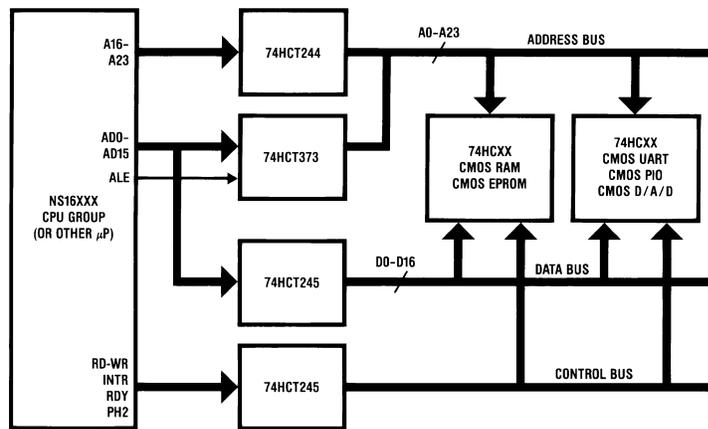
Note 2: Note the specified incompatibility between the output levels and HC input levels.

TABLE 2. 54HC/74HC and 54HCT/74HCT Output Specifications Compared to 54LS/74LS TTL Input Specifications and Showing Fanout

		HC Output		HCT Output		LS Inputs		Fanout
		V _{OUT}	I _{OUT}	V _{OUT}	I _{OUT}	V _{IN}	I _{IN}	
Standard Output	Output High	3.7V	4.0 mA	3.7V	4.0 mA	2.0V	40 μA	10
	Output Low	0.4V	4.0 mA	0.4V	4.0 mA	0.8V	400 μA	
Bus Output	Output High	3.7V	6.0 mA	3.7V	6.0 mA	2.0V	40 μA	15
	Output Low	0.4V	6.0 mA	0.4V	6.0 mA	0.8V	400 μA	

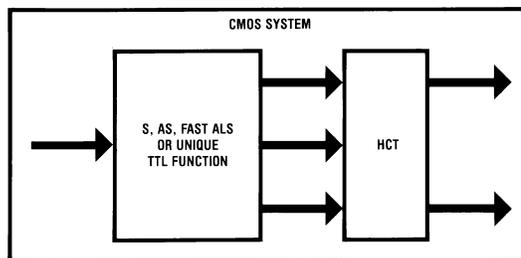
Note 3: V_{CC} = 4.5V

Note 4: Both HC and HCT output specifications are the same for the two sets of output types.



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FIGURE 2. Applications Where a TTL Compatible NMOS Microprocessor is Interfaced to a CMOS System



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FIGURE 3. A Conceptual Diagram Showing How HCT May Be Used to Interface a Faster ALS Part or Some Unique TTL Function in a CMOS System

The functions chosen for implementation in 54HCT/74HCT were chosen to avoid the undesirable situation where the designer is forced to add in an extra gate solely for the interface. A variety of HCT functions are provided to not only interface to HC, but to perform the desired logic function at the same time.

Although not the primary intention, a third use for 54HCT/74HCT is as a direct plug-in replacement for 54LS/74LS logic in already designed systems. If HCT is used to replace LS, power consumption can be greatly reduced, usually by a factor of 5 or so. This lower power consumption, and hence less heat dissipation, has the added advantage of increasing system reliability (in addition to the greater reliability of 54HC/74HC and 54HCT/74HCT). This is extremely useful in power-critical designs and may even offer the advantage of reduced power supply costs.

One note of caution: when plug-in replacing HCT for TTL, 54HCT/74HCT (as well as 54HC/74HC) does not have identical propagation delays to LS. Minor differences will occur, as would between any two vendors' LS products. To be safe, it is recommended that the designer verify that the performance of HCT is acceptable.

PERFORMANCE COMPARISON: HCT vs HC LS-TTL

To enable intelligent use of HCT in a design, both for the interface to NMOS or TTL and for TTL replacement applications, it is useful to compare the various performance parameters of HCT to those of HC and LS-TTL.

Input/Output Voltages and Currents

Table 3 tabulates the input voltages for LS-TTL and LS-TTL compatible ICs, HCT, and HC. Since HCT was designed to have TTL compatible inputs, its input voltage levels are the same. However, the input currents for HCT are the same as HC. This is an advantage over LS-TTL, since there are no fanout restrictions when driving into HCT as there are when driving into LS.

Referring to Table 2, the output voltage and current specifications for HC and HCT gates are shown. As can be seen, the output specifications of HCT are identical to HC. This was chosen since the primary purpose of HCT is to drive into HC as the interface from other logic.

There are some differences as to how LS-TTL, ALS-TTL and AS-TTL outputs are specified when compared to HCT (or HC), as shown in Table 4. The military parts are easy to compare. HC/HCT has the same I_{OL} as LS and much greater I_{OH} . At the commercial temperature range a direct comparison is difficult. LS has a higher output current, but also a higher output voltage and narrow operating temperature range. Taking these into account, the output drive of 74HC/HCT is roughly the same as LS.

In the HC family, there is a higher output drive specified for bus compatible devices. Again, HCT is identical. As can be

seen back in Table 2, the bus drive capability of both HC and HCT are identical, and both source and sink currents are symmetrical. This increased drive over standard devices provides better delay times when they are used in high load capacitance bus organized CMOS systems.

Both HC and HCT also have another voltage/current specification which is applicable to CMOS systems. This is the no load output voltage. In CMOS systems, usually the DC output drive for a device need not be greater than several μA since all CMOS inputs are very high impedance. For this reason, there is a 20 μA output voltage specification which says that 54HC/74HC and 54HCT/74HCT will pull to within 100 mV of the supplies.

NOISE MARGIN TRADEOFFS WITH HCT

The nominal trip point voltage for an HCT device has been designated to be around 1.4V, as compared to the 2.5V for a standard HC device. This will degrade the ground level noise margin for HCT by almost a volt. HC, on the other hand, has its trip point set to offer optimal noise margin for both V_{CC} and ground.

This may be a minor point since normally HCT is mixed with TTL and in this case the worst-case system noise margin is defined by the TTL circuits. If the HCT is being driven only by HC and not LS, then the worst-case V_{CC} margin is determined by the HC devices. This is not a normal usage, but may occur if, for example, some spare HCT logic can be utilized by HC to save chip count. Figure 4 graphs input noise margin for HC, HCT in an LS application and HCT being driven by HC. As one can see, the HC has a large V_{CC} and ground noise margin, the HCT interfacing from LS has a margin equal to LS, and the HCT interfacing from HC has a skewed margin.

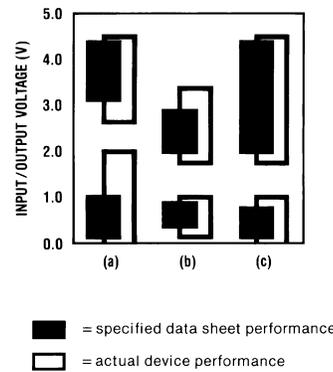


FIGURE 4. Guaranteed and Typical Noise Margins for a) HC; b) HCT in TTL System; c) HCT in HC System

TABLE 3. A Comparison of Input Specifications for 54LS/74LS, NMOS-LSI, 54HC/74HC, and 54HCT/74HCT

	LS Inputs		NMOS-LSI Input		HC Inputs		HCT Input	
	V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	V_{IN}	I_{IN}
Input High	2.0V	40 μA	2.0V	10 μA	3.15V	1 μA	2.0V	1 μA
Input Low	0.8V	400 μA	0.8V	10 μA	0.9V	1 μA	0.8V	1 μA

Note 5: $V_{CC} = 4.5V$

Note 6: The HCT specifications maintain the TTL compatible input voltage requirements and the HC input currents.

TABLE 4. This Compares the Output Drive of HC and HCT to LS for both the Military Temperature Range and the Commercial Temperature Range Devices at Rated Output Currents

	Military Temperature				Commercial Temperature*			
	HC/HCT Output		LS Output		HC/HCT Output		LS Output	
	V _{OUT}	I _{OUT}	V _{OUT}	I _{OUT}	V _{OUT}	I _{OUT}	V _{OUT}	I _{OUT}
Input High	3.7V	4.0 mA	2.5V	400 μA	3.84V	4.0 mA	2.7V	400 μA
Input Low	0.4V	4.0 mA	0.4V	4.0 mA	0.33V	4.0 mA	0.5V	8.0 mA

Note 7: V_{CC} = 4.5V

Note 8: *The commercial temperature range for HC/HCT is -40°C to +85°C, but for LS is 0°C to +70°C.

POWER CONSUMPTION OF HCT

In normal HC applications, power consumption is essentially zero in the quiescent state but is proportional to operating frequency when operating. In LS, large quiescent currents flow which overshadow (except at very high frequencies) other dynamic components. 54HCT/74HCT is a combination of these, depending on the application. Both quiescent and frequency-dependent power can be significant.

Referring back to Figure 1, this figure shows an LS-TTL output driving an HCT input. To see how quiescent current is drawn, notice that it is possible to have valid TTL voltages of 2.7V and 0.4V (ignoring the pull-up resistor). With 0.4V on the HCT input, we find the input N-channel transistor OFF and the P-channel ON. Thus, the output of this stage is high. Also, since one of the P- or N-channel transistors is OFF, no quiescent current flows. However, when the HCT input is high, 2.7V, the N-channel is ON and the P-channel is slightly ON. This will cause some current to flow through both the transistors, even in the static state.

Thus in a TTL application, HCT has the unusual characteristic that it will draw static current only when its inputs are driven by TTL (and TTL-like) outputs, and only when those outputs are high. Thus, to calculate total power, this quiescent power must be summed with the frequency-dependent component.

When HCT is driven by HC, as it possibly might be, the HC outputs will have high and low levels of V_{CC} and ground; never statically turning on both transistors simultaneously. Thus in this application, HCT will only dissipate frequency dependent power, and C_{PD} calculations can be made to determine power (see Fairchild Semiconductor Application Note, AN-303). In the latter application, HCT will dissipate the same amount of power as HC; in the first TTL application, the power dissipated will be more since there is also a DC component.

To show this, Figure 5 plots power versus frequency for an HCT00 being driven by HC, typical LS and worst-case LS. Notice that at the lower frequencies, the DC component for the TTL input is much greater; at higher frequencies, the two converge as the dynamic component becomes dominant.

SPEED/PROPAGATION DELAY PERFORMANCE

Of primary importance is the speed at which the components operate in a system. HCT was designed to have the same basic speeds as HC. This was accomplished in spite of the fact that HCT requires the addition of a TTL input translator, which will add to internal propagation delays. A second concern in the design was to maintain the required speeds while minimizing the possible power consumption of the input stage when driven to TTL high levels.

These requirements dictated designing HCT on a slightly more advanced 3μ N-well process, as well as increasing the

die to help compensate for speed loss. This process is slightly faster than the standard HC process, and this enables the HCT parts to have the same delays as their HC counterparts, while minimizing possible quiescent currents. Figure 6 shows a comparison of 74HCT240 and 74HC240 propagation delays, and they are identical.

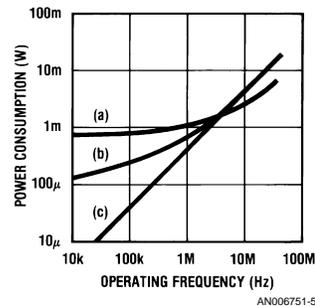


FIGURE 5. Power Consumption of 74HCT00 Being Driven by a) Worst-Case TTL Levels; b) Typical TTL Levels; c) CMOS Levels

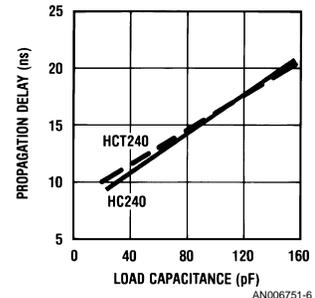


FIGURE 6. Typical propagation delay vs load for 74HC240 and 74HCT240 are virtually the same. Slight differences result from different design and processing.

One interesting point is that HCT and HC speed specifications are measured differently. One can compare the AC test waveforms in the HC databook and see that HC is measured with 0V–5V input waveforms and using 2.5V points on these waveforms. HCT, on the other hand, is tested like LS-TTL. HCT's input waveforms are 0V–3V and timing is measured using the 1.3V on both the input and the output waveforms.

The different test conditions for HCT result because HCT will be primarily used in LS-TTL applications. If HCT is used in HC systems, the actual speeds will be slightly different, but the differences will be small ($< 1 \text{ ns} - 2 \text{ ns}$).

HC and HCT speeds are not identical to LS-TTL. Some delays will be faster and some slightly slower. This is due to inherent differences in designing with CMOS versus bipolar logic. For an average system implemented in HC or LS-TTL, the same overall performance will result. On an individual part basis, some speeds will differ, so the designer should not blindly assume that HC or HCT will duplicate whatever a TTL IC does.

CMOS LATCH-UP AND ELECTROSTATIC DISCHARGE OF 54HCT/74HCT

These two phenomena are not strictly performance related in the same sense that speed or noise immunity are. Instead, latch-up and electrostatic discharge (ESD) immunity impact the ease of design, insusceptibility to spurious or transient signals causing a failure, and general reliability of 54HCT/74HCT.

Latch-up is a phenomenon that is a traditional problem with older CMOS families; however, as with 54HC/74HC, latch-up has been eliminated in 54HCT/74HCT circuits. In older CMOS, it is caused by forward biasing any protection diode on either an IC's input or output. If enough current flows through the diode (as low as 10 mA), then it is possible to trigger a parasitic SCR (four layer diode) within the IC that will cause the V_{CC} and ground pins to short out. Once shorted, the supply pins will remain so even after the trigger source is removed, and can only be stopped by removing power. Latch-up is described in much more detail in Fairchild Semiconductor Application Note AN-339, and, in particular, a set of performance criteria is discussed.

By a combination of process enhancements and some careful IC layout techniques, the latch-up condition cannot occur in 54HC/74HC or 54HCT/74HCT. If one attempts to cause latch-up by forcing current into the protection diodes, the IC will be overstressed in the same manner as overstressing a TTL circuit.

ESD has also been a concern with CMOS ICs. Primarily for historical reasons, MOS devices have always been considered to be sensitive to damage due to static discharges. However, process enhancements and careful input protection network design have actually improved 54HC/74HC and 54HCT/74HCT immunity to where it is actually better than bipolar logic. This includes 74ALS, 74LS, 74S, 74AS and 74F. ESD is measured using a standard military 38510 ESD test circuit, which zaps the test device by discharging a 100 pF capacitor through a 1.5 k Ω resistor into the test circuit. ESD test data is shown in Fairchild Semiconductor Reliability Report, PR-11.

CONCLUSION

HCT is a unique sub-family designation of HC. It is intended primarily for TTL level to HC interfacing, although it is far from restricted only to this application. HCT can be used as a pin-for-pin socket replacement of TTL, or can be mixed with HC logic.

54HCT/74HCT has the same speeds as HC and LS, the same noise immunity as TTL and a significantly lower power consumption than LS-TTL, although it is slightly greater than HC. Additionally, by providing latch-up immunity and low ESD sensitivity like the 54HC/74HC family, the overall system reliability and integrity is increased. All of these performance parameters enable HCT's use in a wide range of applications.

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