

74VHC157 Quad 2-Input Multiplexer

General Description

The VHC157 is an advanced high speed CMOS Quad 2-Channel Multiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and enable inputs. When the $\overline{\text{ENABLE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level. The SELECT decoding determines whether the I_{0x} or I_{1x} inputs get routed to their corresponding outputs.

An Input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply volt-

age. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

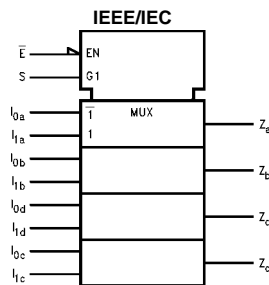
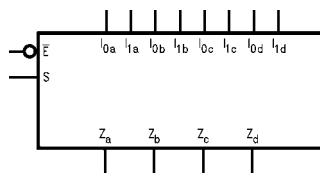
- High Speed: $t_{PD} = 4.1$ ns (typ) at $V_{CC} = 5V$
- Low power dissipation: $I_{CC} = 4$ μA (max.) at $T_A = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- Power down protection is provided on all inputs
- Low noise: $V_{OLP} = 0.8V$ (max.)
- Pin and function compatible with 74HC157

Ordering Code:

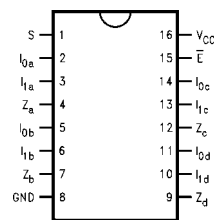
| Order Number | Package Number | Package Description |
|--------------|----------------|------------------------------------------------------------------------------|
| 74VHC157M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC157SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHC157MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHC157N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|-----------------|----------------------|
| $I_{0a}-I_{0d}$ | Source 0 Data Inputs |
| $I_{1a}-I_{1d}$ | Source 1 Data Inputs |
| \overline{E} | Enable Input |
| S | Select Input |
| Z_a-Z_d | Outputs |

Truth Table

| Inputs | | | | Outputs |
|-----------|---|----------------|----------------|---------|
| \bar{E} | S | I ₀ | I ₁ | Z |
| H | X | X | X | L |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Functional Description

The VHC157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The VHC157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

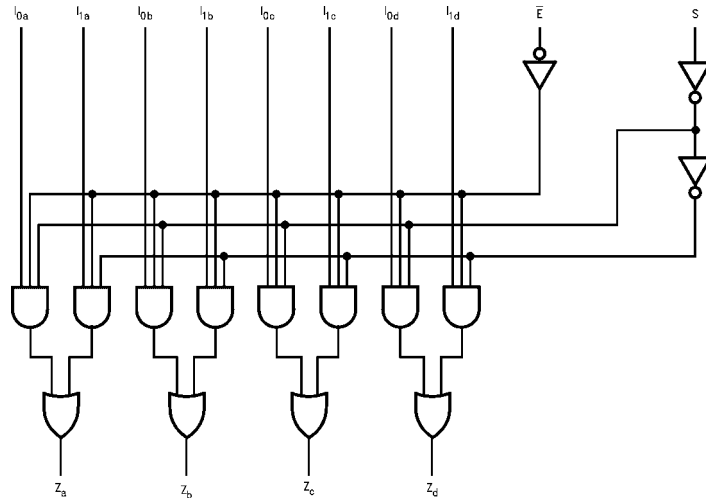
$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the VHC157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The VHC157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

| | |
|-------------------------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -0.5V to +7.0V |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| Input Diode Current (I_{IK}) | -20 mA |
| Output Diode Current (I_{OK}) | ± 20 mA |
| DC Output Current (I_{OUT}) | ± 25 mA |
| DC V_{CC} /GND Current (I_{CC}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Lead Temperature (T_L) (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|-----------------------------------------|----------------|
| Supply Voltage (V_{CC}) | 2.0V to +5.5V |
| Input Voltage (V_{IN}) | 0V to +5.5V |
| Output Voltage (V_{OUT}) | 0V to V_{CC} |
| Operating Temperature (T_{OPR}) | -40°C to +85°C |
| Input Rise and Fall Time (t_r, t_f) | |
| $V_{CC} = 3.3V \pm 0.3V$ | 0 ~ 100 ns/V |
| $V_{CC} = 5.0V \pm 0.5V$ | 0 ~ 20 ns/V |

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions | |
|----------|------------------------------|-----------------|--------------------------|--------------|-----|-------------------------------------------------|-----|---------------|----------------------------------|------------------------------------------------------|
| | | | Min | Typ | Max | Min | Max | | | |
| V_{IH} | HIGH Level | 2.0 | 1.50 | | | 1.50 | | V | | |
| | Input Voltage | 3.0 – 5.5 | $0.7 V_{CC}$ | | | $0.7 V_{CC}$ | | | | |
| V_{IL} | LOW Level | 2.0 | | 0.50 | | 0.50 | | V | | |
| | Input Voltage | 3.0 – 5.5 | | $0.3 V_{CC}$ | | $0.3 V_{CC}$ | | | | |
| V_{OH} | HIGH Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu\text{A}$ |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | | | |
| | | 3.0 | 2.58 | | | 2.48 | | | | |
| V_{OL} | LOW Level Output Voltage | 4.5 | 3.94 | | | 3.80 | | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ |
| | | 3.0 | 0.0 | 0.1 | | 0.1 | | | | |
| | | 4.5 | 0.0 | 0.1 | | 0.1 | | | | |
| | | 3.0 | | 0.36 | | 0.44 | | | | |
| I_{IN} | Input Leakage Current | 0 – 5.5 | | ± 0.1 | | ± 1.0 | | μA | $V_{IN} = 5.5V$ or GND | |
| | | 5.5 | | 4.0 | | 40.0 | | | | |
| I_{CC} | Quiescent Supply Current | 5.5 | | | | | | μA | $V_{IN} = V_{CC}$ or GND | |

Noise Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | Units | Conditions |
|-----------------------|---------------------------------------------|-----------------|--------------------------|--------|-------|-----------------------|
| | | | Typ | Limits | | |
| V_{OLP} (Note 3) | Quiet Output Maximum Dynamic V_{OL} | 5.0 | 0.3 | 0.8 | V | $C_L = 50 \text{ pF}$ |
| V_{OLV} (Note 3) | Quiet Output Minimum Dynamic V_{OL} | 5.0 | -0.3 | -0.8 | V | $C_L = 50 \text{ pF}$ |
| V_{IHD} (Note 3) | Minimum HIGH Level Dynamic Input Voltage | 5.0 | | 3.5 | V | $C_L = 50 \text{ pF}$ |
| V_{ILD} (Note 3) | Maximum LOW Level Dynamic Input Voltage | 5.0 | | 1.5 | V | $C_L = 50 \text{ pF}$ |

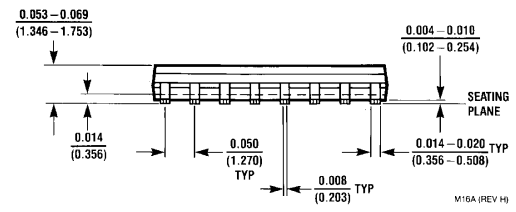
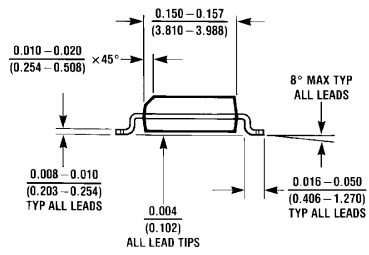
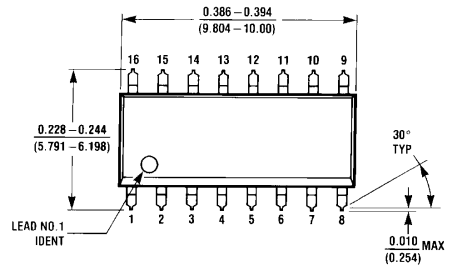
Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

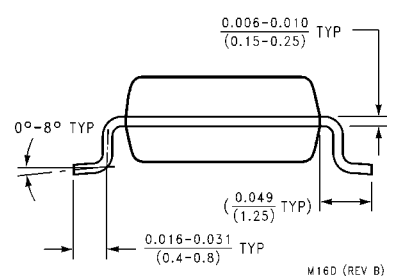
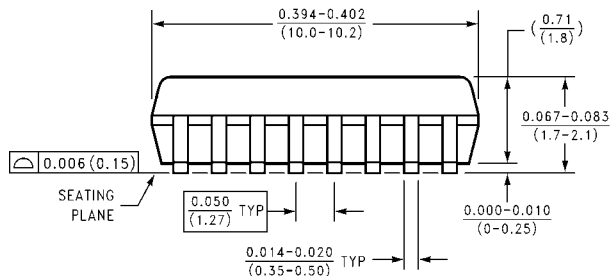
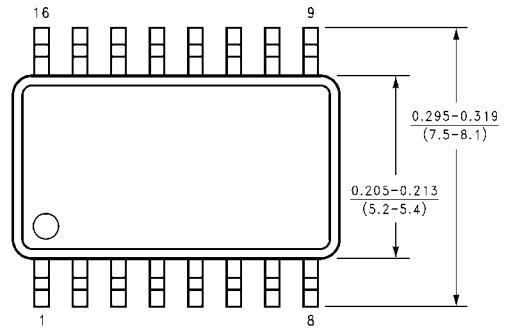
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | Conditions |
|------------------|-------------------------------------------------------|------------------------|-----------------------|------|-----|---------------------------------|-----|------------------------|------------|
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay I _n to Z _n | 3.3 ± 0.3 | 6.2 | 9.7 | 1.0 | 11.5 | ns | C _L = 15 pF | |
| t _{PHL} | | | 8.7 | 13.2 | 1.0 | 15.0 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 4.1 | 6.4 | 1.0 | 7.5 | ns | C _L = 15 pF | |
| | | | 5.6 | 8.4 | 1.0 | 9.5 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay S to Z _n | 3.3 ± 0.3 | 8.4 | 13.2 | 1.0 | 15.5 | ns | C _L = 15 pF | |
| t _{PHL} | | | 10.9 | 16.7 | 1.0 | 19.0 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 5.3 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 6.8 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay E to Z _n | 3.3 ± 0.3 | 8.7 | 13.6 | 1.0 | 16.0 | ns | C _L = 15 pF | |
| t _{PHL} | | | 11.2 | 17.1 | 1.0 | 19.5 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 5.6 | 8.6 | 1.0 | 10.0 | ns | C _L = 15 pF | |
| | | | 7.1 | 10.6 | 1.0 | 12.0 | | C _L = 50 pF | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF | V _{CC} = Open | |
| C _{PD} | Power Dissipation Capacitance | | 20 | | | | pF | (Note 4) | |

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC (opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

Physical Dimensions inches (millimeters) unless otherwise noted

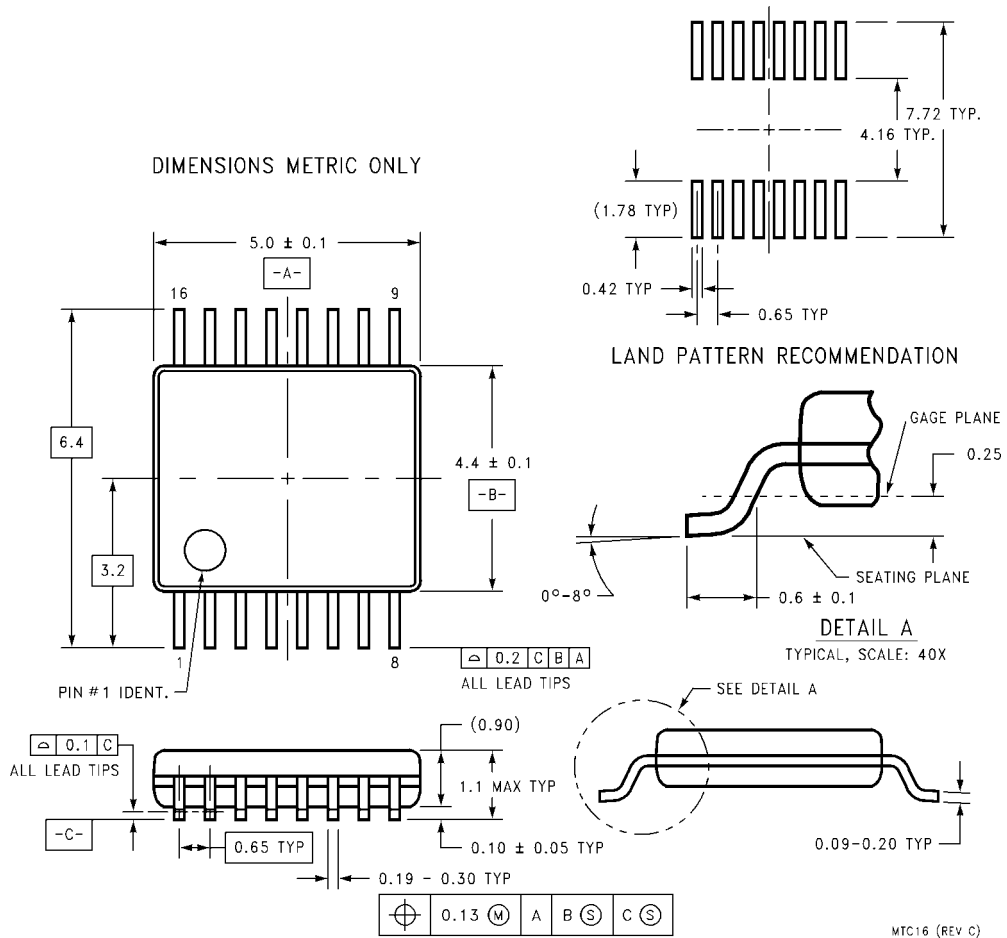


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

MTC16 (REV C)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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