NAND Flash Memory

Serial Peripheral Interface (SPI)

MT29F8G01ADBFD12

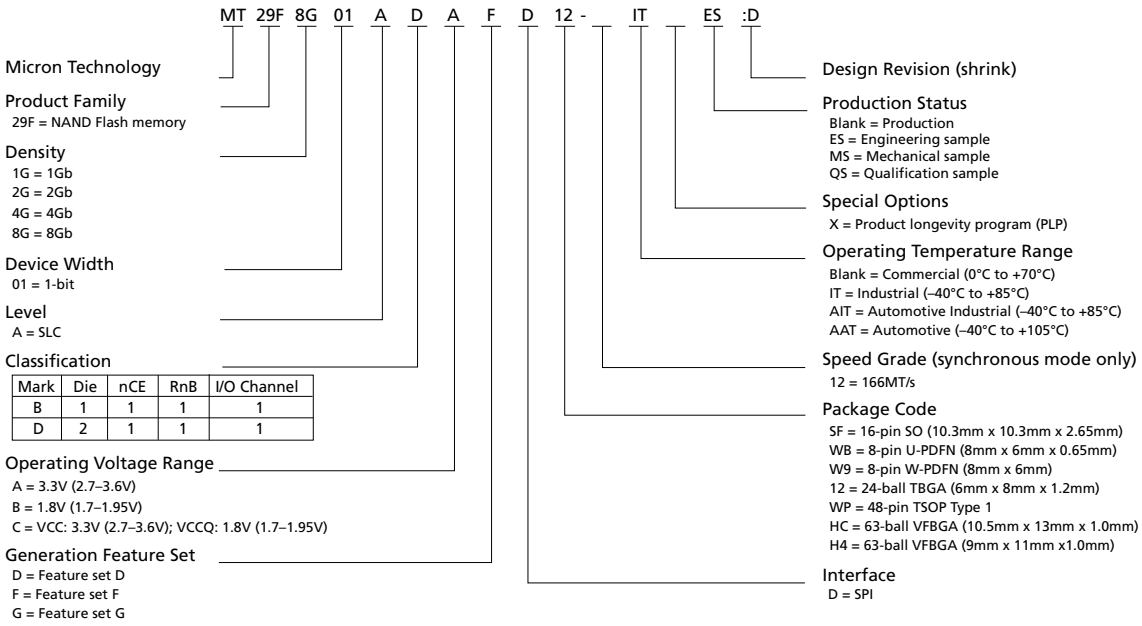
Features

- Single-level cell (SLC) technology
- 8Gb density dual die
- Organization
  - Page size ×1: 4352 bytes (4096 + 256 bytes)
  - Block size: 64 pages (256K + 16K bytes)
  - Device size: 8Gb (2 die × 2048 blocks)
- Standard and extended SPI-compatible serial bus interface
  - Instruction, address on 1 pin; data out on 1, 2, or 4 pins
  - Instruction on 1 pin; address, data out on 2 or 4 pins
  - Instruction, address on 1 pin; data in on 1 or 4 pins
  - Continuous read within block, boot-up ready or configure-able by feature register
- User-selectable internal ECC supported
  - 8 bits/sector
- Array performance
  - 83 MHz clock frequency (MAX)
  - Page read: 25µs (MAX) with on-die ECC disabled; 135µs (MAX) with on-die ECC enabled
  - Page program: 200µs (TYP) with on-die ECC disabled; 240µs (TYP) with on-die ECC enabled
  - Block erase: 2ms (TYP)
- Advanced features
  - Read page cache mode (×2, ×4, dual, quad, and random)
  - Read unique ID
  - Read parameter page
- Device initialization
  - Automatic device initialization after power-up
- Security
  - Blocks 7:0 for each die are valid when shipped from factory with ECC enabled
  - Software write protection with lock register
  - Hardware write protection to freeze BP bits
  - Lock tight to freeze BP bits during one power cycle
- Permanent block lock protection
  - OTP space: 10 pages per die one-time programmable NAND Flash memory area
- Operating voltage range
  - V_{CC} = 1.7–1.95V
- Operating temperature
  - Industrial: –40°C to +85°C
- Quality and reliability
  - Endurance: 100,000 PROGRAM/ERASE cycles
  - Data retention: JESD47H-compliant; see qualification report
  - Additional: Uncycled data retention: 10 years 24/7 @85°C
- Package
  - 24-ball T-PBGA, 05/6mm × 8mm (5 × 5 array) (package code: 12)

Part Numbering Information

All the permutations are not shown in the part number chart below. Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart



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General Description

Serial peripheral interface (SPI) NAND is an SLC NAND Flash memory device that provides a cost-effective nonvolatile memory storage solution where pin count must be kept to a minimum. It is also an alternative solution to SPI NOR, offering superior write performance and cost per bit over SPI NOR. The hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another and supports future upgrades to higher densities without board redesign.

The serial electrical interface follows the industry-standard serial peripheral interface. New command protocols and registers are defined for SPI operation. The command set resembles common SPI-NOR command sets, modified to handle NAND specific functions and additional new features.

New features include continuous read within a block for increased performance and to support boot-up functionality. SPI NAND Flash devices have six signal lines plus V_{CC} and ground (GND). The signal lines are SCK (serial clock), SI, SO (for command/response and data input/output), and control signals CS#, HOLD#, WP#. This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, supporting future upgrades to higher densities without board redesign.

Each block of the serial NAND Flash device is divided into 64 programmable pages, each page consisting of 4352 bytes. Each page is further divided into a 4096-byte data storage region and a 256-byte spare area. The spare area is typically used for memory and error management functions.

With internal ECC enabled as the default after power-on, ECC code is generated internally when a page is written to the memory core. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status. The internal ECC can be configured off after device initialization. Contact Micron representative if ECC is required to be default off after power on.

The first eight blocks are valid when shipped from factory. Security functions are also provided including software block protection: Lock tight and hardware protection modes avoid array data corruption.

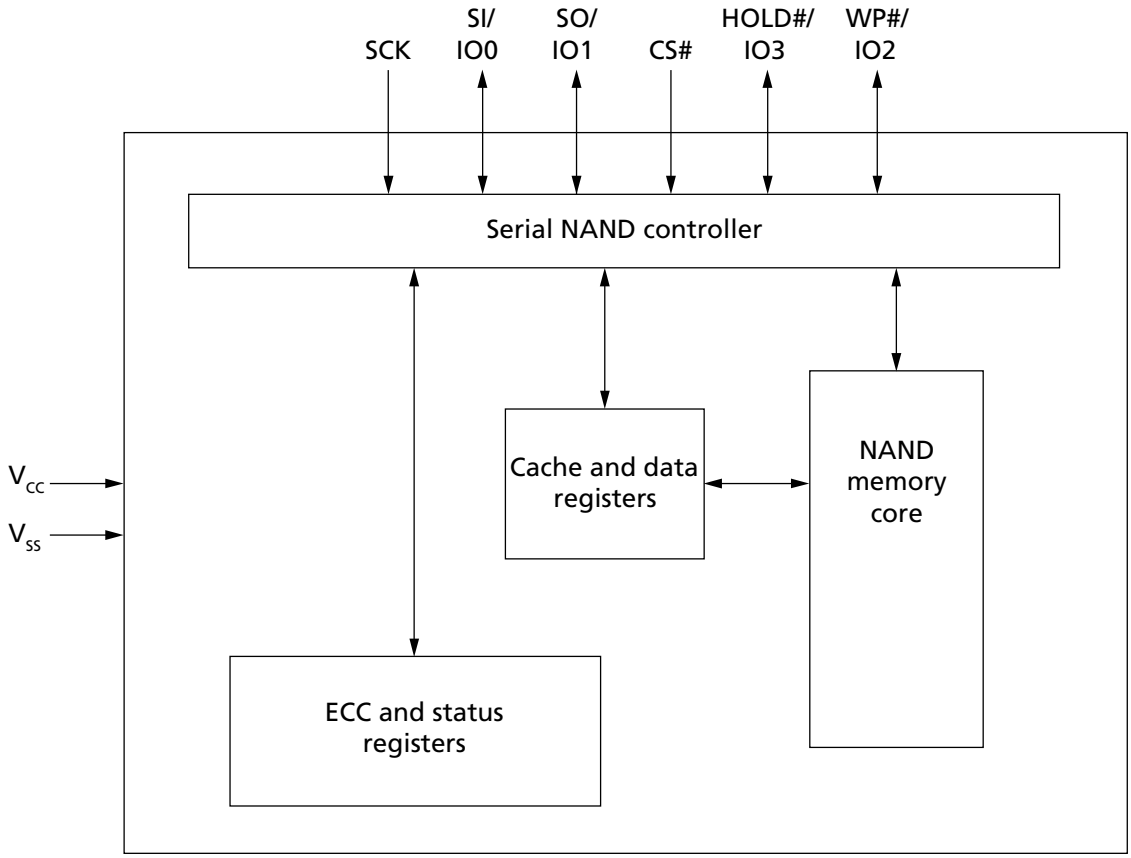
Architecture

The devices use an industry-standard NAND Flash memory core organized by page/block. The standard parallel NAND Flash electrical interface and I/O logic are replaced by an SPI interface. The new command protocol set is a modification of the SPI NOR command set available in the industry. The modifications are specifically to handle functions related to NAND Flash architecture. The interface supports page and random read/write and internal data move functions. The device also includes an internal ECC feature.

Data is transferred to or from the NAND Flash memory array, page-by-page, to a cache register and a data register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

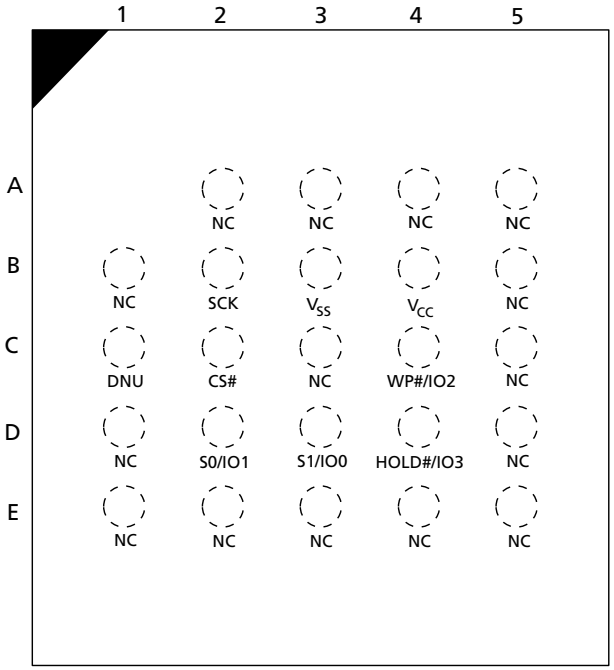
The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. The cache register functions as the buffer memory to enable random data READ/WRITE operations. These devices also use a new SPI status register that reports the status of device operation.

Figure 2: Functional Block Diagram



Pin Assignments

Figure 3: 24-Ball T-PBGA, 5 x 5 (Balls Down)



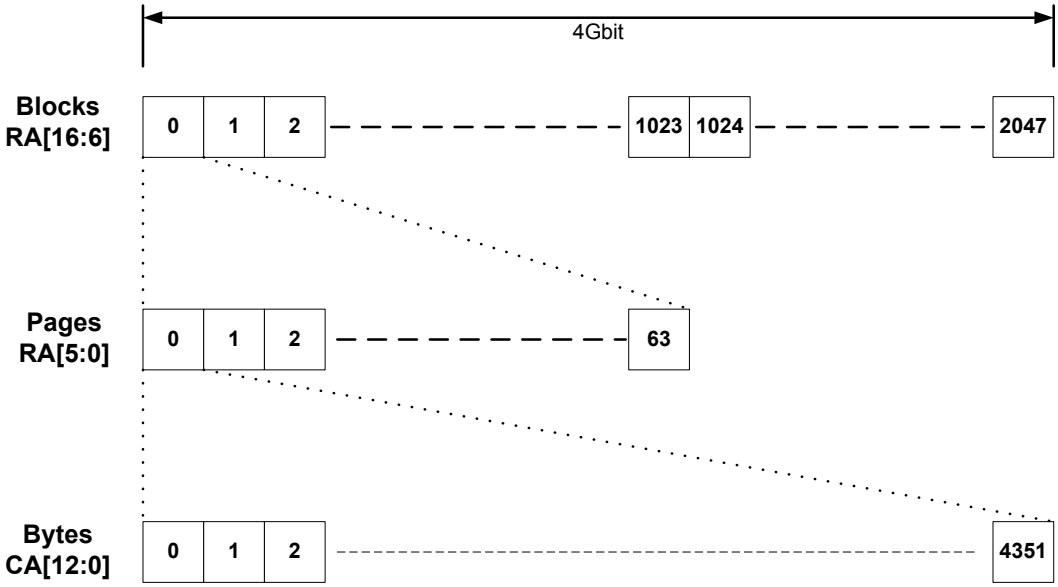
Pin Descriptions

Table 1: SPI Pin Descriptions

Symbol	Type	Description
CS#	Input	**Chip select:** Places the device in active power mode when driven LOW. Deselects the device and places SO at High-Z when HIGH. After power-up, the device requires a falling edge on CS# before any command can be written. The device goes into standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. In the case of write-type instructions, CS# must be driven HIGH after a whole sequence is completed. Single command and address sequences and array-based operations are registered on CS#.
SCK	Input	**Serial clock:** Provides serial interface timing. Latches commands, addresses, and data on SI on the rising edge of SCK. Triggers output on SO after the falling edge of SCK. While CS# is HIGH, keep SCK at V_{CC} or GND (determined by mode 0 or mode 3). Do not begin toggling SCK until after CS# is driven LOW.
WP#	Input	**Write protect:** When LOW, prevents overwriting block lock bits (BP[3:0] and TB) if the block register write disable (BRWD) bit is set. WP# must not be driven by the host during a x4 READ operation. If the device is deselected, this pin defaults as an input pin.
HOLD#	Input	**Hold:** Hold functionality is disabled by default except the special part numbers. Contact Micron Sales representatives for details. When enabled, the external pull-up resistor is necessary to avoid accidental operation being placed on hold. HOLD# pauses any serial communication with the device without deselecting it. To start the HOLD condition, the device must be selected, with CS# driven LOW. During HOLD status (HOLD# driven LOW), SO is High-Z and all inputs at SI and SCK are ignored. Hold mode starts at the falling edge of HOLD#, provided SCK is also LOW. If SCK is HIGH when HOLD# goes LOW, hold mode is kicked off at the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD#, provided SCK is also LOW. If SCK is HIGH, hold mode ends after the next falling edge of SCK. HOLD# must not be driven by the host during the x4 READ operation.
SI/IO0, SO/IO1, IO2, IO3	I/O	**Serial I/O:** The bidirectional I/O signals transfer address, data, and command information. The device latches commands, addresses, and data on the rising edge of SCK, and data is shifted out on the falling edge of the SCK. If the device is deselected, IO[0,2] defaults as an input pin and IO[1,3] defaults as an output pin. SI must not be driven by the host during x2 or x4 READ operations.
V_{CC}	Supply	**V_{CC}:** Supply voltage
V_{SS}	Supply	**V_{SS}:** Ground
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internal connection; can be driven or floated.

Memory Mapping

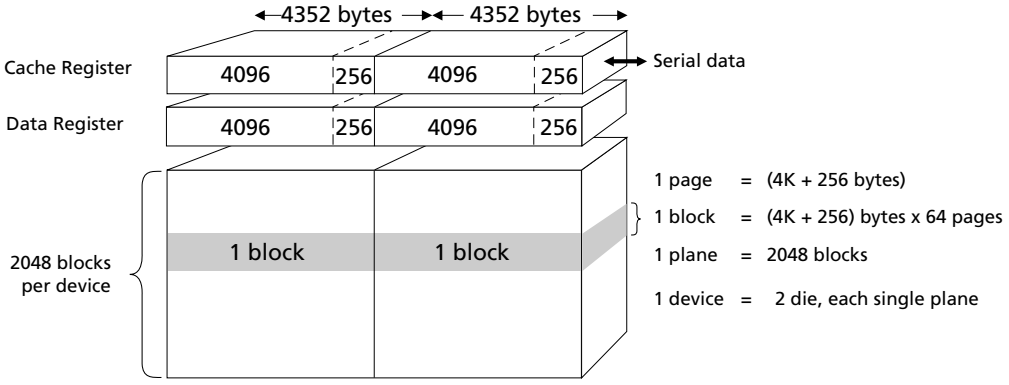
Figure 4: Memory Map



Note: 1. The 13-bit column address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4351 are valid. Bytes 4352 through 8191 of each page are "out of bounds", do not exist in the device, and cannot be addressed.

Array Organization

Figure 5: Array Organization



Bus Operation

SPI Modes

The device can be driven by a microcontroller with its SPI running in either of two modes depending on clock polarity (CPOL) and clock phase (CPHA) settings:

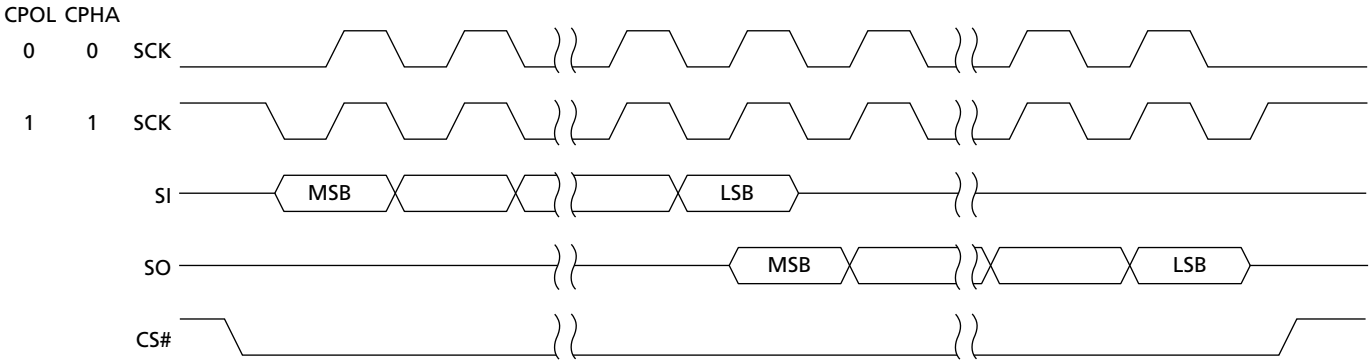
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

The difference between the two modes, shown here, is the clock polarity when the bus master is in standby mode and not transferring data.

- SCK remains at 0 for CPOL = 0, CPHA = 0 (Mode 0)
- SCK remains at 1 for CPOL = 1, CPHA = 1 (Mode 3)

Figure 6: SPI Modes Timing



Notes:
1. While CS# is HIGH, keep SCK at V_{CC} or GND (determined by mode 0 or mode 3). Do not begin toggling SCK until after CS# is driven LOW.
2. All timing diagrams shown in this data sheet are mode 0.

SPI Protocols

Standard SPI: Command, address, and data are transmitted on a single data line. Input on SI is latched in on the rising edge of SCK. Output on SO is available on the falling edge of SCK.

Extended SPI: An extension of the standard SPI protocol. Command and address are transmitted on a single data line through SI. Data are transmitted on two or four data lines, IO[3:0], depending on the command.

SPI NAND Command Definitions

Table 2: SPI NAND Command Set

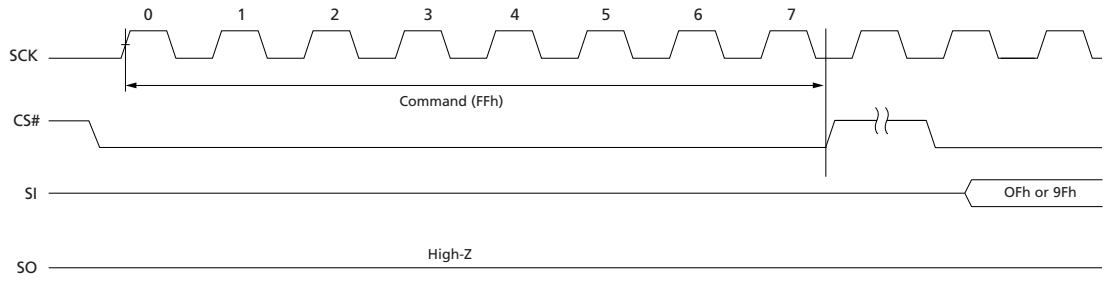
Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
RESET	FFh	0	0	0	Reset the device. It is accepted by all stacked die.
GET FEATURE	0Fh	1	0	1	Get features. It is accepted by all stacked die.
SET FEATURE	1Fh	1	0	1	Set features
READ ID	9Fh	0	1	2	Read device ID
PAGE READ	13h	3	0	0	Array read
READ PAGE CACHE RANDOM	30h	3	0	0	Cache read
READ PAGE CACHE LAST	3Fh	0	0	0	Ending of cache read
READ FROM CACHE ×1	03h, 0Bh	2	1	1 to 4352	Output cache data at column address
READ FROM CACHE ×2	3Bh	2	1	1 to 4352	Output cache data on IO[1:0]
READ FROM CACHE ×4	6Bh	2	1	1 to 4352	Output cache data on IO[3:0]
READ FROM CACHE Dual IO	BBh	2	1	1 to 4352	Input address/Output cache data on IO[1:0]
READ FROM CACHE Quad IO	EBh	2	2	1 to 4352	Input address/Output cache data on IO[3:0]
WRITE ENABLE	06h	0	0	0	Sets the WEL bit in the status register to 1; required to enable operations that change the content of the memory array
WRITE DISABLE	04h	0	0	0	Clears the WEL bit in the status register to 0; required to disable operations that change the content of the memory array
BLOCK ERASE	D8h	3	0	0	Block erase
PROGRAM EXECUTE	10h	3	0	0	Array program
PROGRAM LOAD ×1	02h	2	0	1 to 4352	Load program data into cache register on SI
PROGRAM LOAD ×2	A2h	2	0	1 to 4352	Load program data into cache register on SI[1:0]
PROGRAM LOAD RANDOM DATA ×2	44h	2	0	1 to 4352	Overwrite cache register with input data on SI[1:0]
PROGRAM LOAD ×4	32h	2	0	1 to 4352	Load program data into cache register on SI[3:0]
PROGRAM LOAD RANDOM DATA ×1	84h	2	0	1 to 4352	Overwrite cache register with input data on SI
PROGRAM LOAD RANDOM DATA ×4	34h	2	0	1 to 4352	Overwrite cache register with input data on SI[3:0]
PROTECT	2Ch	3	0	0	Permanently protect a specific group of blocks

RESET Operation

The RESET (FFh) command is used to put the memory device into a known condition and to abort the command sequence in progress. READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. Once the RESET command is issued to the device, it will take ^{t}RST to reset. During this period, the GET FEATURE command could be issued to monitor the status (OIP) except for the stacked devices. While the device is busy after sending the RESET Command, READ ID command can be issued to read the device ID. For the stacked devices, no command should be issued until ^{t}RST. The contents of the memory location being programmed or the block being erased are no longer valid. The first page data of block 0 is auto-loaded to the cache register. For dual die, Die 0 is selected as default and the first page of block 0 is loaded to the cache

All other status register bits will be cleared. The ECC status register bits will be updated after a reset. The configuration register bits CFG[2:0] will be cleared after a reset. All the other configuration register bits will not be reset. The block lock register bits will not be cleared after reset until the device is power cycled or is written to by SET FEATURE command.

Figure 7: RESET (FFh) Timing



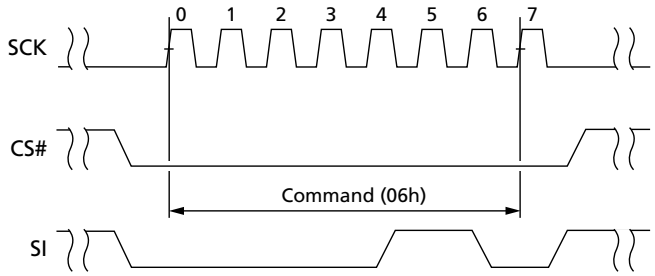
WRITE Operations

WRITE ENABLE (06h)

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. Write enable is required in the following operations that change the contents of the memory array:

- PAGE PROGRAM
- OTP AREA PROGRAM
- BLOCK ERASE

Figure 8: WRITE ENABLE (06h) Timing

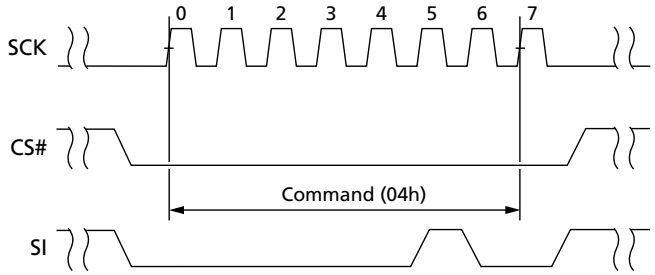


WRITE DISABLE (04h)

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0, disabling the following operations:

- PAGE PROGRAM
- OTP AREA PROGRAM
- BLOCK ERASE

Figure 9: WRITE DISABLE (04h) Timing



Continuous Read Operation

Description

The device provides a capability to read the whole block with a single command after power-up via a SET FEATURE command that enables the CONTINUOUS READ operation. Upon power-up, this mode is disabled by default (CONT_RD = 0). Continuous read mode can be enabled (CONT_RD = 1) using SET FEATURE command. With continuous read enabled (CONT_RD = 1), ECC is enabled automatically.

Table 3: Continuous Read Mode Matrix

CONTI_RD	ECC_ENABLE	Read Mode	ECC Status	Output
0	0	Cache read	N/A	4096 + 256
0	1	Cache read	Target page	4096 + 256[1]
1	0	Cache read	N/A	4096 + 256
1	1	Continuous read	Target block	4096

Note: 1. Refer to ECC Protection table.

Table 4: Continuous Read Mode MAX Clock Frequency

Command	Opcode	Max Clock Frequency	
		3.3V	1.8V
x1 Read	03h/0Bh	133 MHz	83 MHz
x2 Read	3Bh/BBh	100 MHz	60 MHz
x4 Read	6Bh/Ebh	50 MHz	30 MHz

Power-up Behaviour

The CONTINUOUS READ command doesn't require the starting column address. The device always output the data starting from the first column (byte 0) of the cache register, and once the end of the cache register is reached, the data output continues through the next page. With the continuous read mode, it is possible to read out the entire block using a single READ command, and once the end of the block is reached, the output pins become High-Z state. The data output can be terminated by de-selecting the CS#. If the continuous read is terminated by deselecting the CS# then the device remains busy for 6µs (OIP = 1), and all the data inside the data buffer are lost and unreliable to use. Below is the outline after the device comes out of power reset and ready to accept command:

- READ FROM CACHE (03h, 0Bh, 3Bh, 6Bh, BBh, or EBh) command sequence
- Read the data from address 0 until the end of the block or CS# is de-selected.

Read Operation With Continuous Mode On

The normal read mode requires PAGE READ (13h) command to specify which page of the block to read. After the device is not busy, READ FROM CACHE can be used to output the data continuously. At the end of the block, the output pins become High-Z state. The data output can be terminated anytime by de-selecting the CS#. If the continuous

read is terminated by deselecting the CS# then the device remains busy for 5µs (OIP = 1), and all the data inside the data buffer are lost and unreliable to use. Below is the outline of the sequence:

- PAGE READ (13h) command
- Wait until OIP bit of the status register is busy
- READ FROM CACHE (03h, 0Bh, 3Bh, 6Bh, BBh, or EBh) command sequence
- Read the data from address 0 until the end of the block or CS# is de-selected.

READ Operations

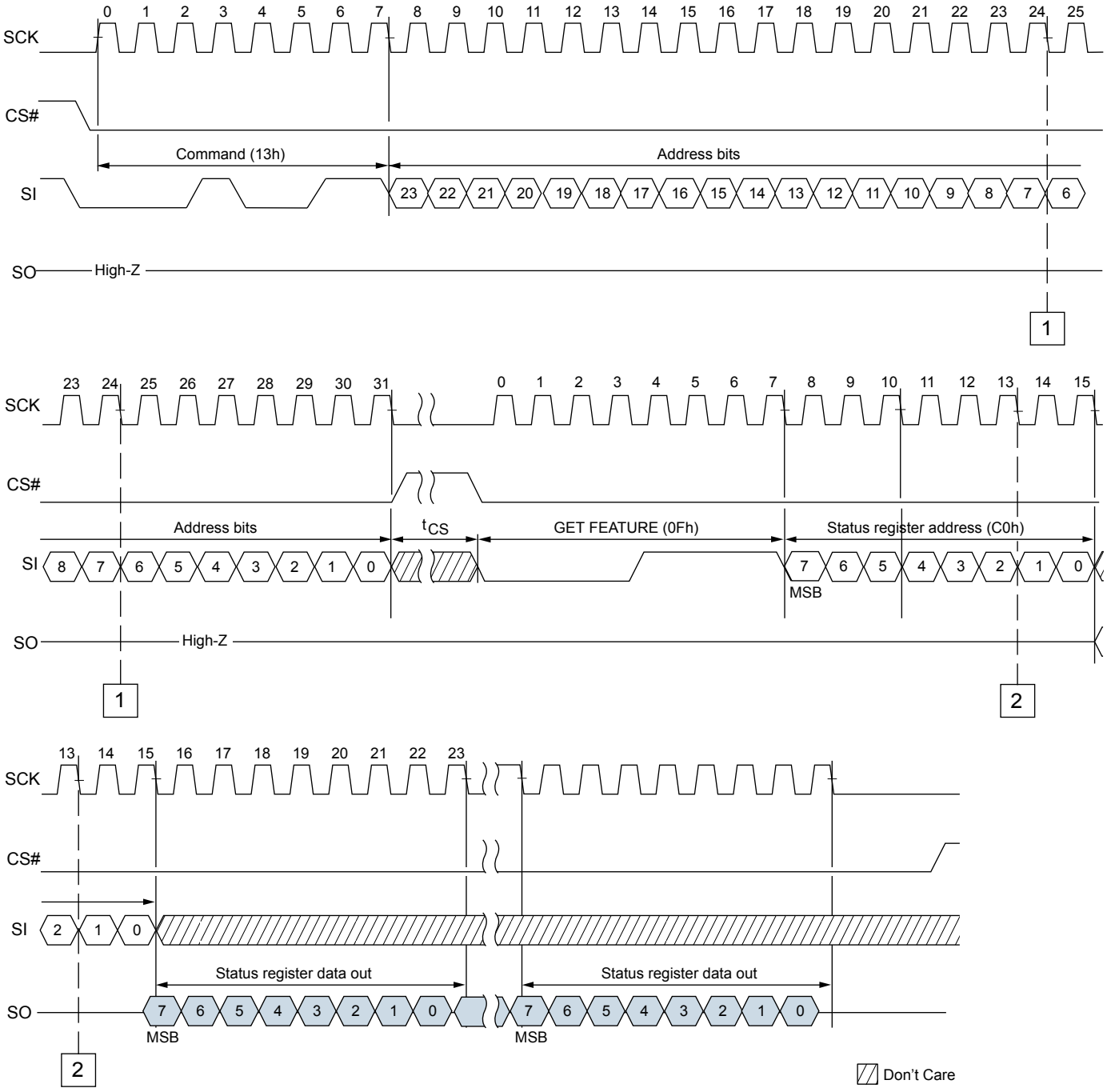
PAGE READ (13h)

The PAGE READ (13h) command transfers data from the NAND Flash array to the cache register. It requires a 24-bit address consisting of 7 dummy bits and a 17-bit block/page address. After the block/page address is registered, the device starts the transfer from the main array to the cache register. During this data transfer busy time of ^{t}RD, the GET FEATURE command can be issued to monitor the operation.

Following successful completion of PAGE READ, the READ FROM CACHE command must be issued to read data out of cache. The command sequence is as follows to transfer data from array to output:

- 13h (PAGE READ command to cache)
- 0Fh (GET FEATURE command to read the status)
- 03h or 0Bh (READ FROM CACHE)
- 3Bh (READ FROM CACHE ×2)
- 6Bh (READ FROM CACHE ×4)
- BBh (READ FROM CACHE Dual IO)
- EBh (READ FROM CACHE Quad IO)

Figure 10: PAGE READ (13h) Timing

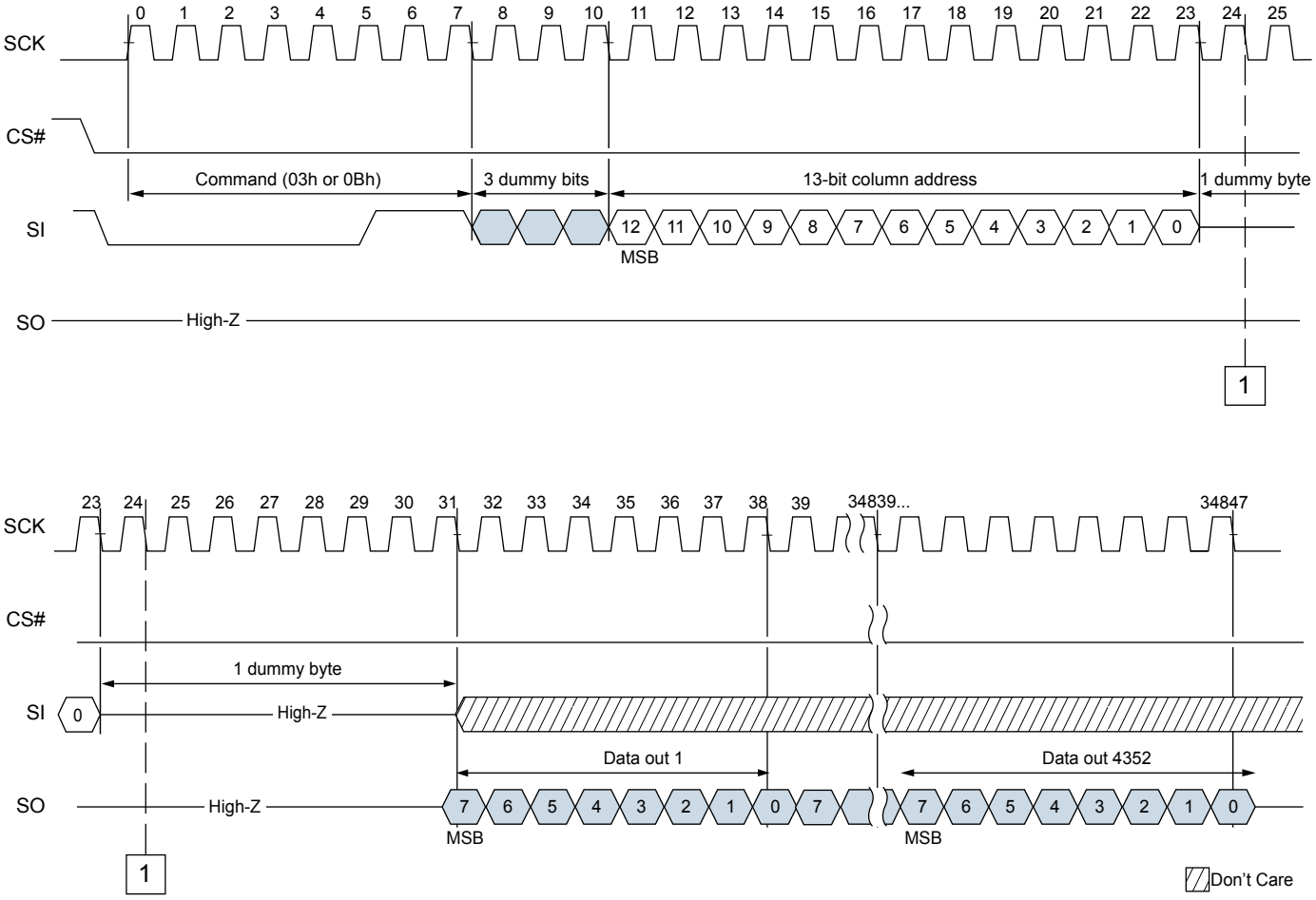


READ FROM CACHE ×1 (03h or 0Bh)

The READ FROM CACHE ×1 command enables sequentially reading one or more data bytes from the cache buffer. The command is initiated by driving CS# LOW, shifting in command opcode 03h/0Bh, followed by a 16-bit column address and 8-bit dummy clocks. Both the commands run at fast mode.

Data is returned from the addressed cache buffer, MSB first, on SO at the falling edge of SCK. The address is automatically incremented to the next higher address after each byte of data is shifted out, enabling a continuous stream of data. This command is completed by driving CS# HIGH.

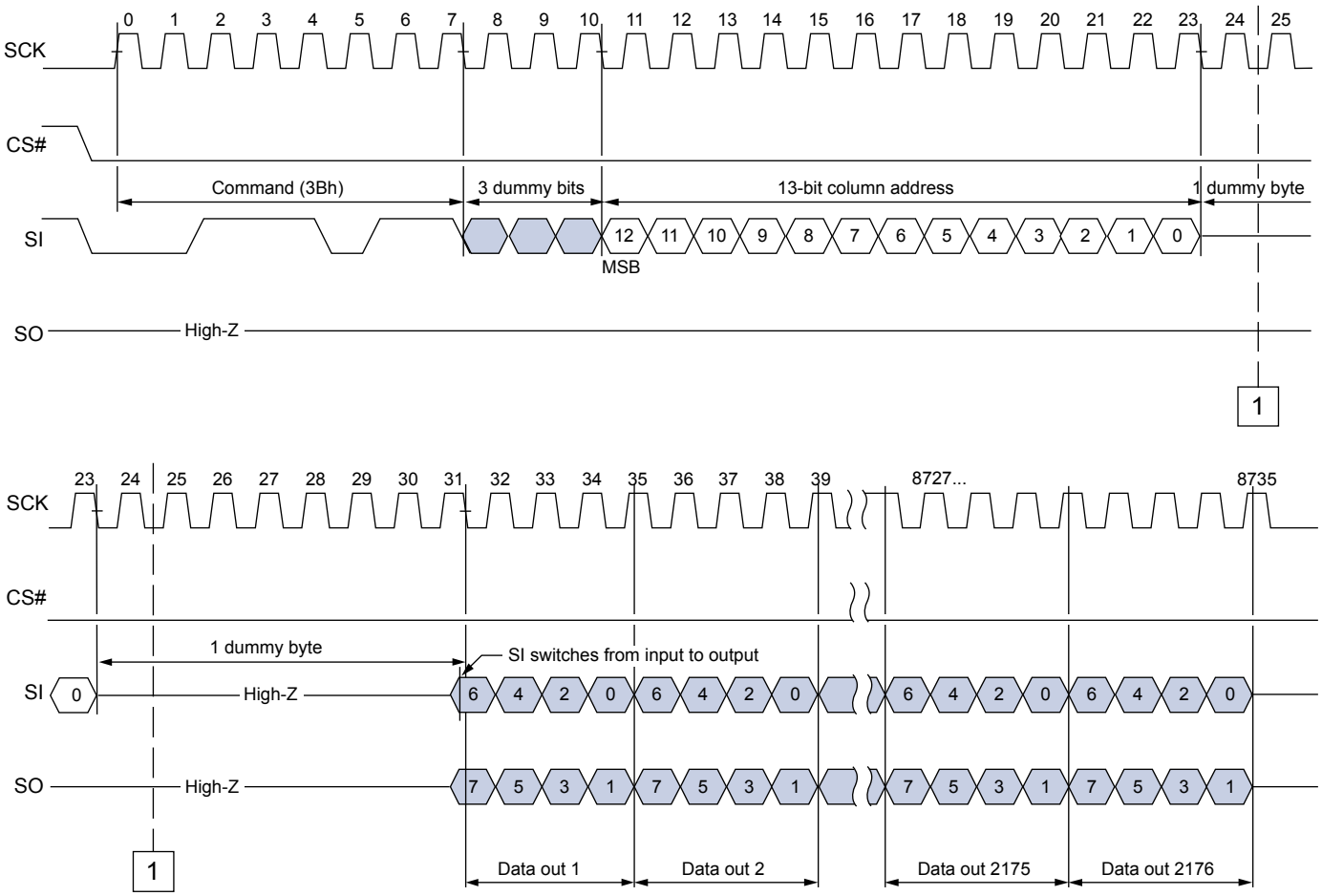
Figure 11: READ FROM CACHE (03h or 0Bh) Timing



READ FROM CACHE ×2 (3Bh)

The READ FROM CACHE ×2 (3Bh) command is similar to READ FROM CACHE ×1 (03h or 0Bh) except that data is output on the following two pins, enabling data transfer at twice the rate: IO0(SI) and IO1(SO).

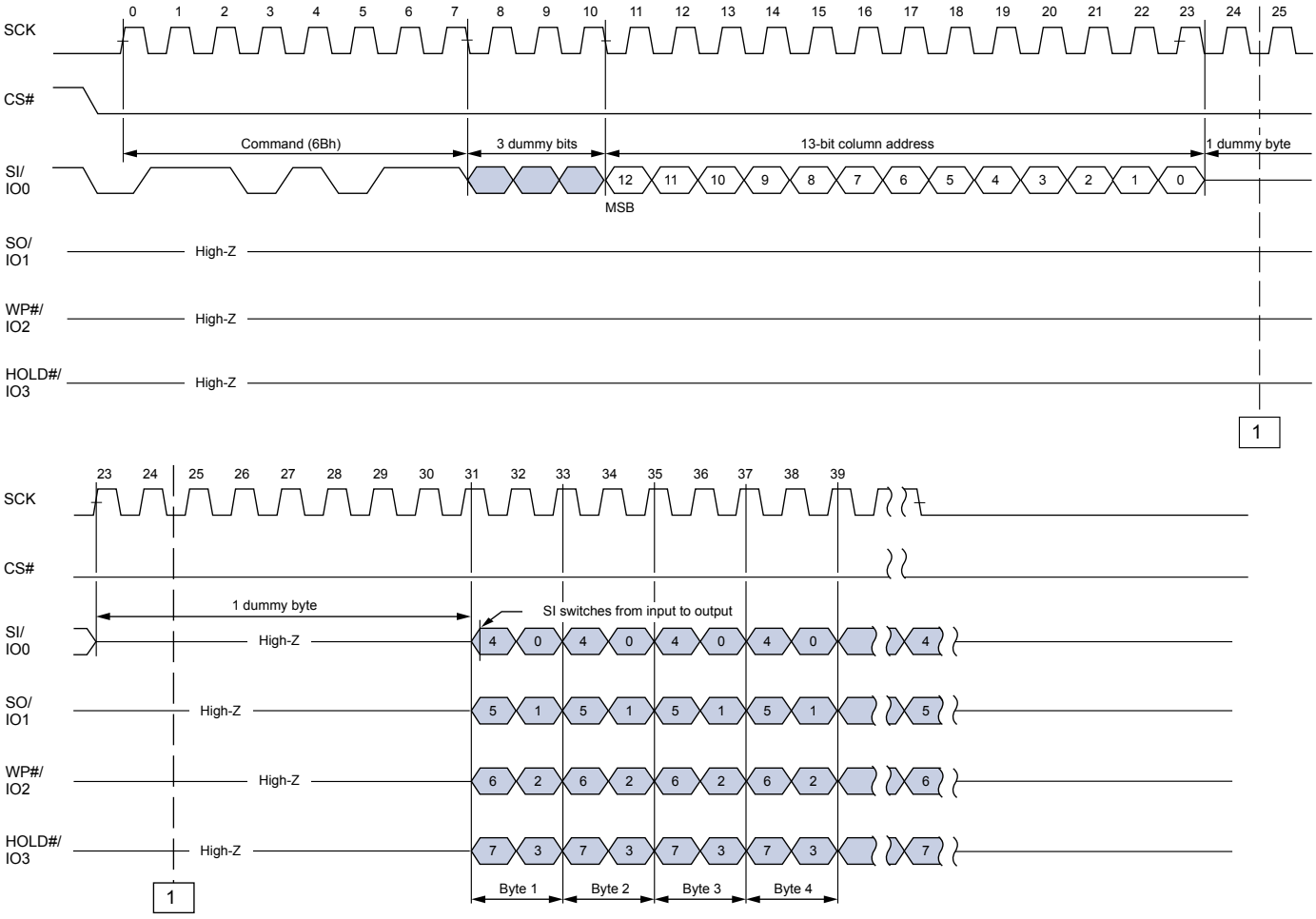
Figure 12: READ FROM CACHE ×2



READ FROM CACHE ×4 (6Bh)

The READ FROM CACHE ×4 (6Bh) command is similar to READ FROM CACHE ×1 command, but with the capability to output data across four data lines.

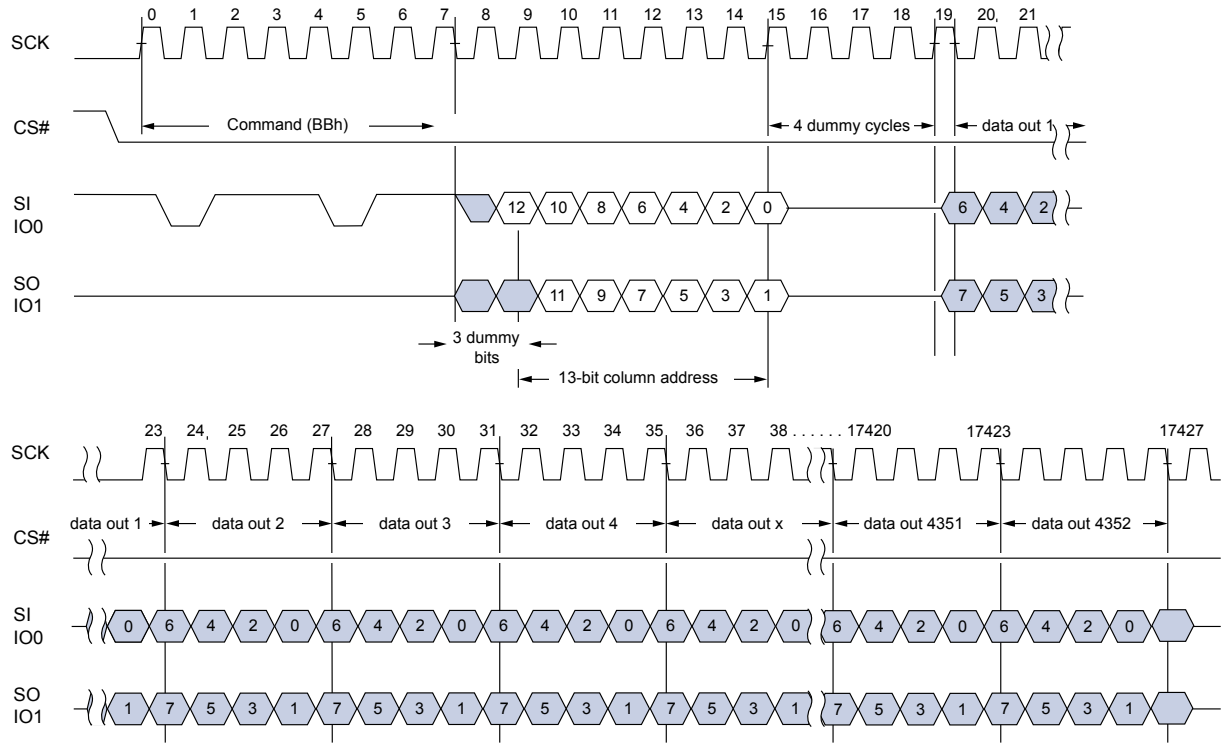
Figure 13: READ FROM CACHE ×4



READ FROM CACHE Dual IO (BBh)

The READ FROM CACHE Dual IO (BBh) command enables improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the READ FROM CACHE ×2 (3Bh) command but with capability to input either the column address or the dummy clocks two bits per clock, thereby reducing command overhead. Refer to the Electrical Specifications for the supported frequency.

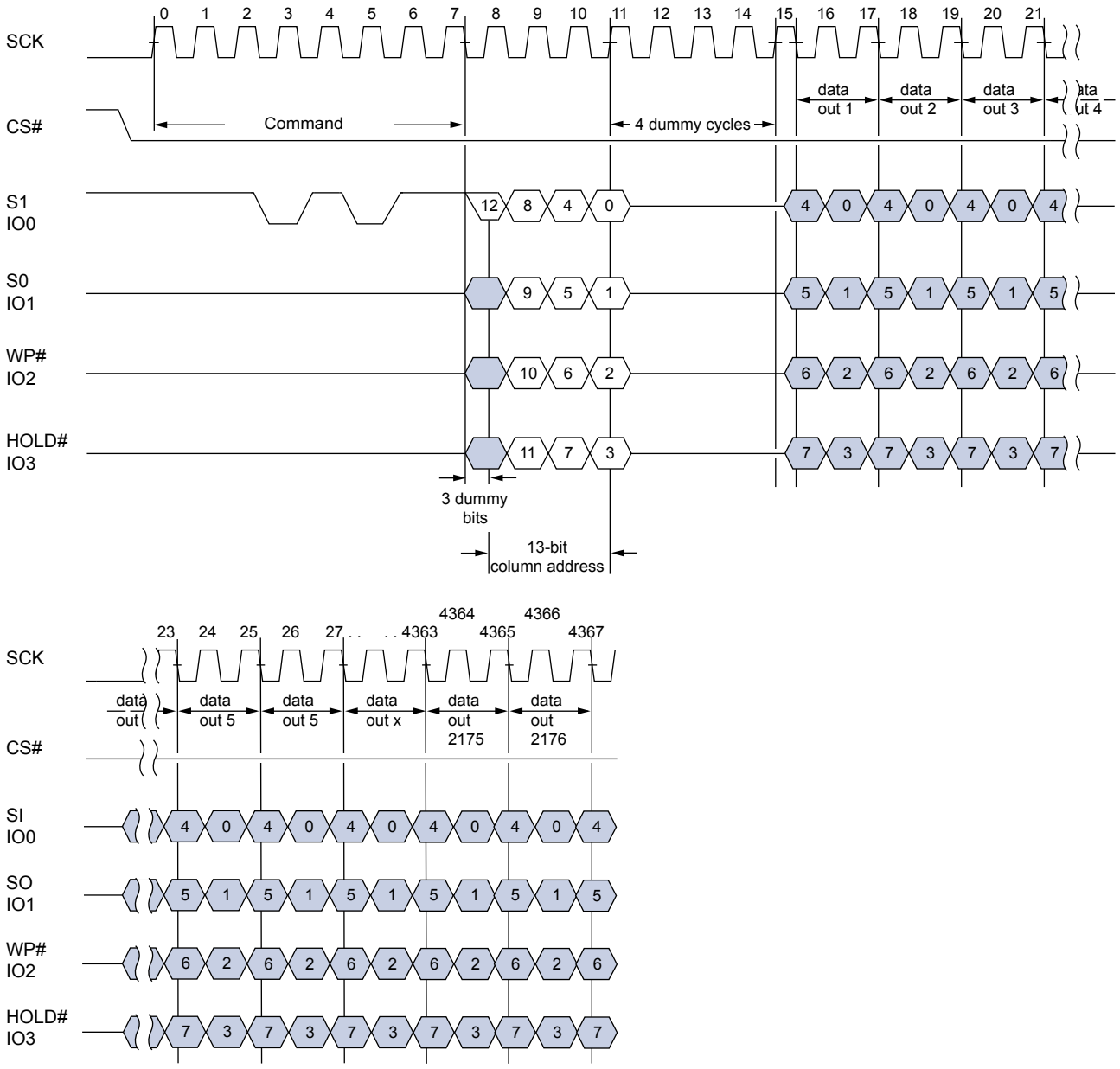
Figure 14: READ FROM CACHE Dual IO



READ FROM CACHE Quad IO (EBh)

The READ FROM CACHE Quad IO (EBh) command is similar to the READ FROM CACHE Dual IO (BBh) command except that address and data bits are input and output through four pins: IO0, IO1, IO2, and IO3. The quad IO dramatically reduces command overhead, enabling faster random access to the cache buffer. Refer to the Electrical Specifications for the supported frequency.

Figure 15: READ FROM CACHE Quad IO



READ PAGE CACHE RANDOM (30h)

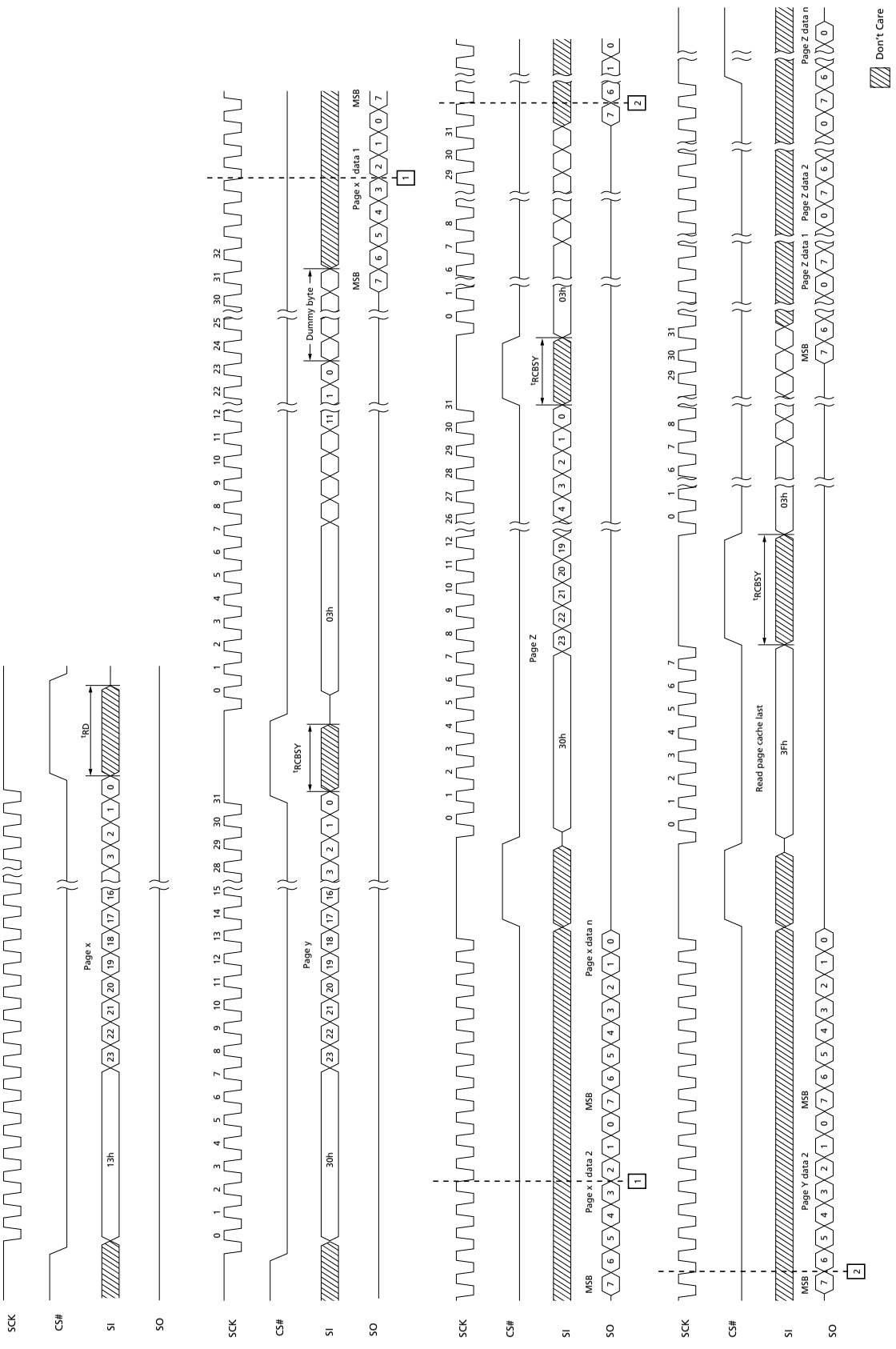
This mode is not available when continuous mode is enabled. The READ PAGE CACHE RANDOM (30h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die when it is ready (OIP = 0, CRBSY = 0). This command is used to improve the read throughput as follows:

1. 13h – PAGE READ to cache
2. 0Fh – GET FEATURE command to the read status until OIP status bit is changed from 1 to 0
3. 30h – READ PAGE CACHE RANDOM command to transfer data from data register to cache register and kick off the next page transfer from array to data register
4. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0
5. 03h, 0Bh, 3Bh, 6Bh, BBh, or EBh – READ FROM CACHE to output command
6. 0Fh – GET FEATURE command to read the status until CRBSY = 0
7. Repeat step 3 to step 6 to read out all expected pages until last page
8. 3Fh – READ PAGE CACHE LAST command to end the read page cache sequence and copy a last page from the data register to the cache register
9. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0
10. 03h, 0Bh, 3Bh, 6Bh, BBh, or EBh – READ FROM CACHE TO OUTPUT command to read out last page from cache register to output

The READ PAGE CACHE RANDOM command requires a 24-bit address consisting of 7 dummy bits followed by a 17-bit block/page address. After the block/page addresses are registered, the device starts to transfer data from data register to cache register for ^{t}RCBSY. After ^{t}RCBSY, OIP bit (through GET FEATURE command to check this status bit) goes to 0 from 1, indicating that the cache register is available and that the specified page in the READ PAGE CACHE RANDOM command is copying from the Flash array to the data register. At this point, data can be output from the cache register beginning at the column address specified by READ FROM CACHE commands. The status register CRBSY bit value remains at 1, indicating that the specified page in READ PAGE CACHE RANDOM command is copying from the Flash array to the data register; CRBSY returns to 0 to indicating the copying from array is completed. During ^{t}RCBSY, the error check and correction is also performed.

Note: With an on-die ECC-enabled die, ECC is executed after data is transferred from the data register to the cache register; therefore, ^{t}RCBSY includes this ECC time, which must be factored in when checking the OIP status.

Figure 16: READ PAGE CACHE RANDOM Sequence



READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the READ PAGE CACHE RANDOM sequence and copies a page from the data register to the cache register. This command is accepted by the die when it is ready (OIP = 0, CRBSY = 0). After this command is issued, the status register bit OIP goes HIGH and the device is busy (CRBSY = 0, OIP = 1) for ^{t}RCBSY. Address is not applied in this command sequence. When data is completely copied to cache register, OIP goes LOW and READ FROM CACHE commands could be issued to output data.

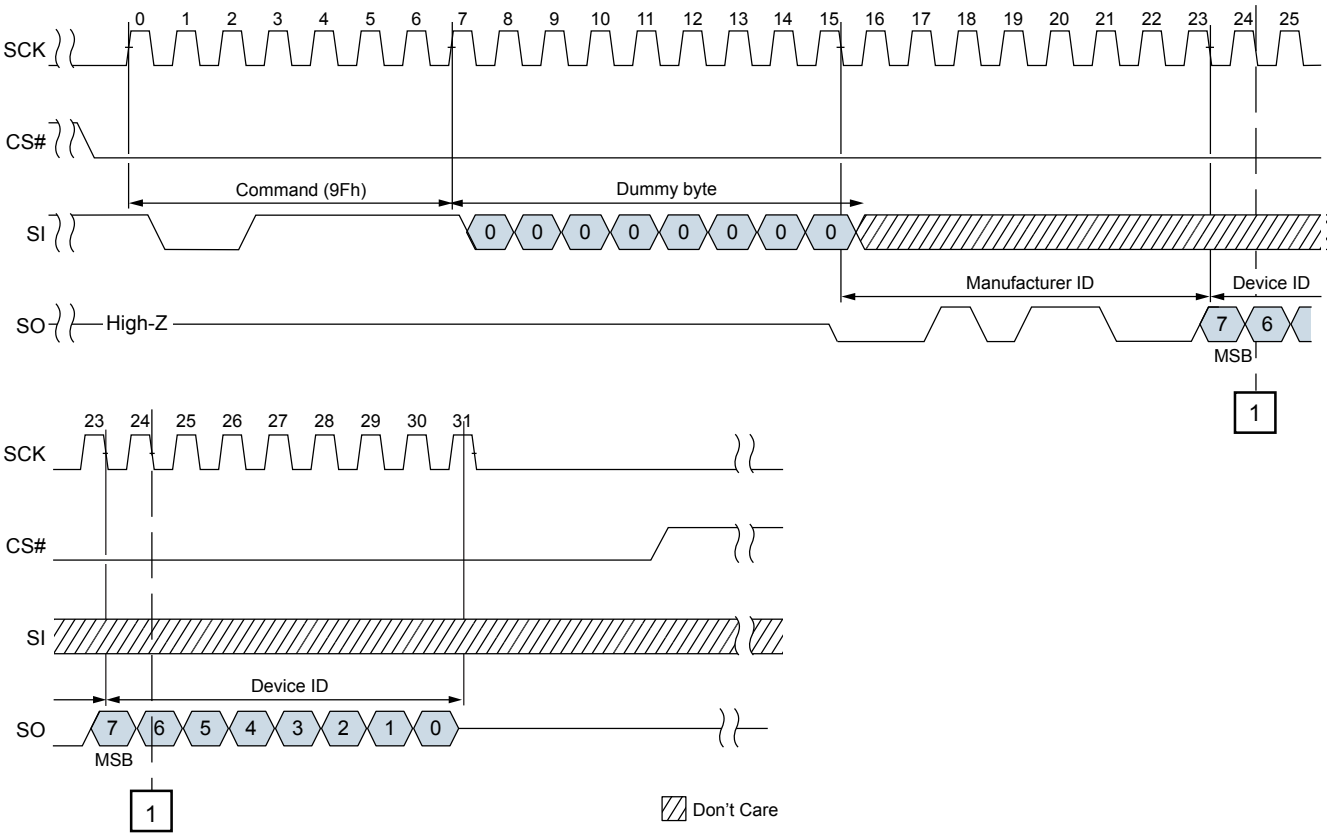
READ ID (9Fh)

READ ID reads the 2-byte identifier code programmed into the device, which includes ID and device configuration data as shown in the table below.

Table 5: READ ID Table

Byte	Description	7	6	5	4	3	2	1	0	Value
Byte 0	Manufacturer ID (Micron)	0	0	1	0	1	1	0	0	2Ch
Byte 1	8Gb 3.3V Device ID	0	1	0	0	0	1	1	0	46h
Byte 1	8Gb 1.8V Device ID	0	1	0	0	0	1	1	1	47h

Figure 17: READ ID (9Fh) Timing



Parameter Page

The following command flow must be issued by the memory controller to access the parameter page contained within Micron SPI devices:

1. 1Fh – SET FEATURE command with a feature address of B0h and data value for CFG[2:0] = 010b (to access OTP/Parameter/Unique ID pages).
2. 13h – PAGE READ command with a block/page address of 0x01h, and then check the status of the read completion using the GET FEATUR ES (0Fh) command with a feature address of C0h.
3. 03h – READ FROM CACHE command with an address of 0x00h to read the data out of the NAND device (see the following Parameter Page Data Structure table for a description of the contents of the parameter page).
4. 1Fh – SET FEATURE command with a feature address of B0h and data value of 00h to exit the parameter page reading.

Parameter Page Data Structure Table

Table 6: Parameter Table

Byte	Description	Value (hex)
0–3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4–5	Revision number	00h
6–7	Feature support	00h
8–9	Optional commands support	06h, 00h
10–31	Reserved	00h
32–43	Device manufacturer	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model: MT29F8G01ADBFD12	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 31h, 41h, 44h, 42h, 46h, 44h, 31h, 32h, 20h, 20h, 20h, 20h
64	Manufacturer ID	2Ch
65–66	Date code	00h
67–79	Reserved	00h
80–83	Number of data bytes per page	00h, 10h, 00h, 00h
84–85	Number of spare bytes per page	00h, 01h
86–89	Number of data bytes per partial page	00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page	40h, 00h
92–95	Number of pages per block	40h, 00h, 00h, 00h
96–99	Number of blocks per unit	00h, 08h, 00h, 00h
100	Number of logical units	02h
101	Number of address cycles	00h
102	Number of bits per cell	01h
103–104	Bad blocks maximum per unit	28h, 00h
105–106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	08h

Table 6: Parameter Table (Continued)

Byte	Description	Value (hex)
108–109	Block endurance for guaranteed valid blocks	00h
110	Number of programs per page	04h
111	Partial programming attributes	00h
112	Number of ECC bits	08h
113	Number of interleaved address bits	00h
114	Interleaved operation attributes	00h
115–127	Reserved	00h
128	I/O pin capacitance	09h
129–130	Timing mode support	00h
131–132	Program cache timing	00h
133–134	^{t}PROG maximum page program time	58h, 02h
135–136	^{t}ERS maximum block erase time	10h, 27h
137–138	^{t}R maximum page read time	9Bh, 00h
139–140	^{t}CCS minimum	00h
141–163	Reserved	00h
164–165	Vendor-specific revision number	00h
166–179	Vendor specific	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 02h, 02h, B0h, 0Ah, B0h
180–247	Reserved	00h
248	ECC maximum correct ability	08h
249	Die select feature	01h
250–253	Reserved	00h
254–255	Integrity CRC	
256–512	2nd copy of the parameter table	
513–768	3rd copy of the parameter table	
769–2048	Additional redundant parameter pages	

Unique ID Page

The following command flow must be issued by the memory controller to access the unique ID page contained within the device:

1. Issue a SET FEATURE (1Fh) command on a feature address of B0h and data value of 40h (Access to OTP, Parameter, Unique ID pages, ECC disable).
2. Issue a PAGE READ (13h) command on a block/page address of 0x00h, and then poll the status register OIP bit until device ready using the GET FEATURE (0Fh) command issued on a feature address of C0h.
3. Issue a READ FROM CACHE (03h) command on an address of 0x00h to read the unique ID data out of the NAND device.

4. To exit reading the unique ID page, issue a SET FEATURE (1Fh) command with a feature address of B0h and data value of 10h or 00h (main array READ, ECC enable/disable).

The device stores 16 copies of the unique ID data. Each copy is 32 bytes: the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, that copy of the unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data.

Program Operations

PAGE PROGRAM (02h/10h)

A PAGE PROGRAM operation sequence enables the host to input 1 byte to 4352 bytes of data within a page to a cache register, and moves the data from the cache register to the specified block and page address in the array. If more than 4352 bytes are loaded, then those additional bytes are ignored by the cache register.

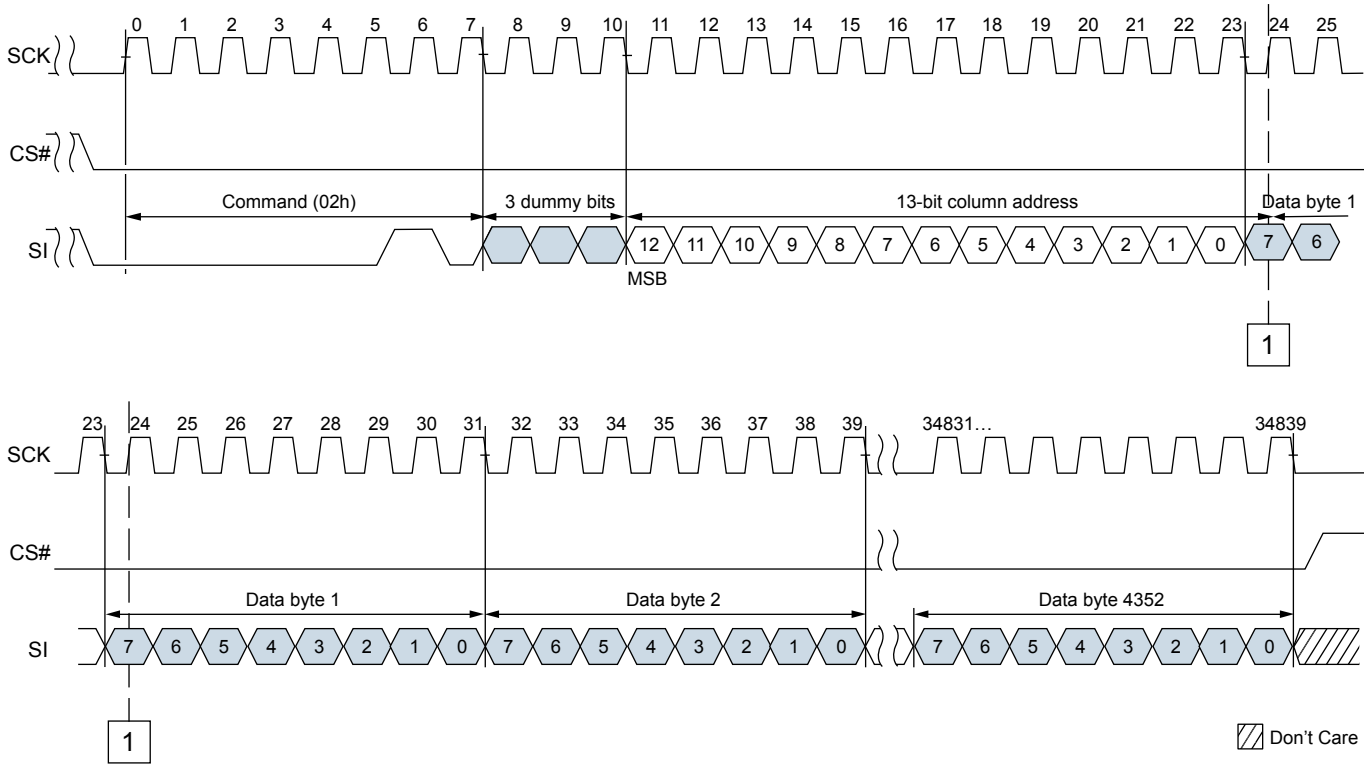
The page program sequence is as follows:

- 06h (WRITE ENABLE command)
- 02h (PROGRAM LOAD command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURE command to read the status)

PROGRAM LOAD ×1 (02h)

Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. WRITE ENABLE is followed by a PROGRAM LOAD (02h) command. The PROGRAM LOAD command consists of an 8-bit op code, followed by 3 dummy bits and a 13-bit column address, and then the data bytes to be programmed. The data bytes are loaded into a cache register that is 4352 bytes long. Only four partial-page programs are allowed on a single page. If more than 4352 bytes are loaded, those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH.

Figure 18: PROGRAM LOAD (02h) Timing

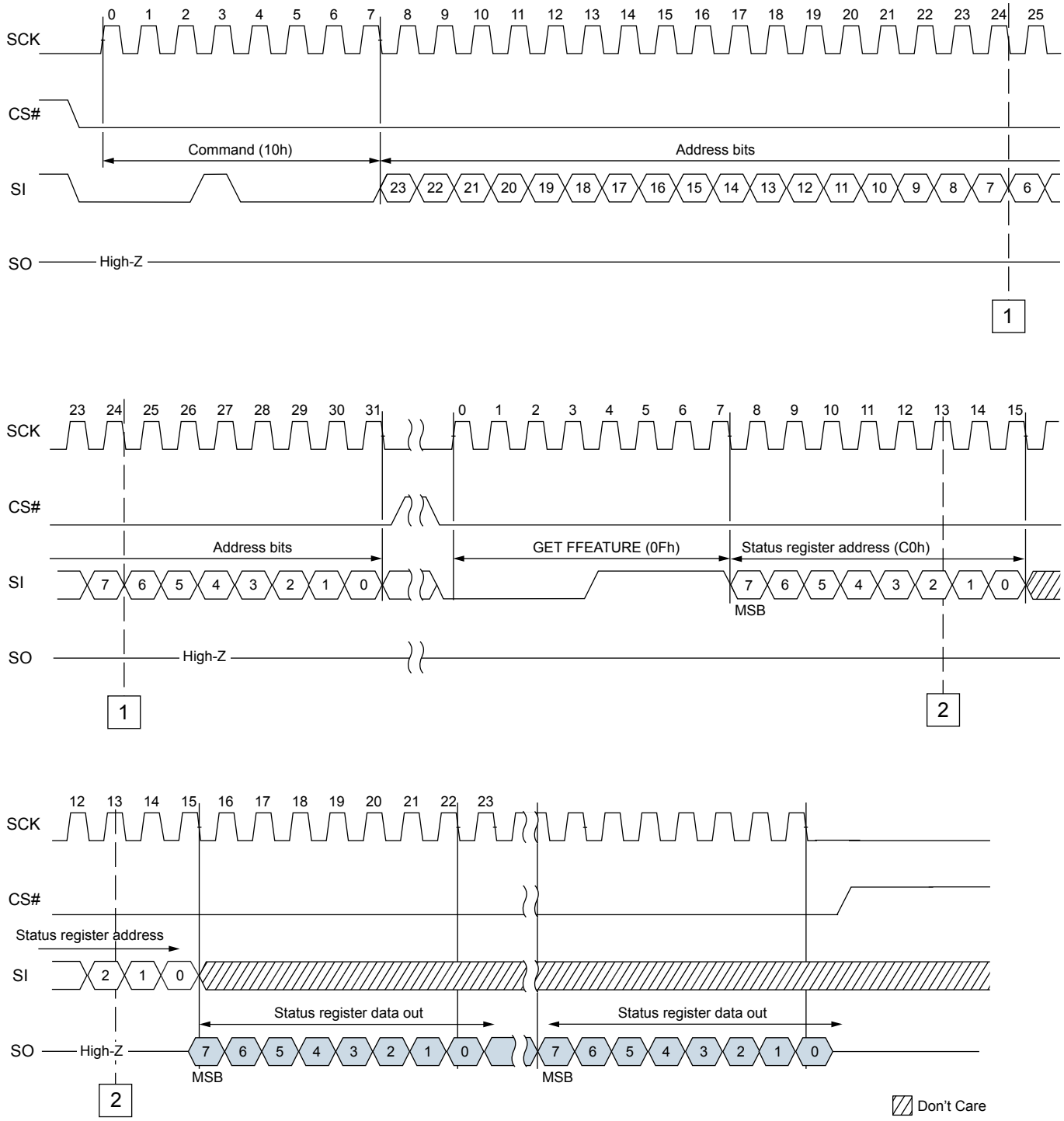


Note: 1. WRITE ENABLE (06h) and PROGRAM LOAD (02h) are required before PROGRAM EXECUTE (10h) command.

PROGRAM EXECUTE (10h)

The PROGRAM EXECUTE command consists of an 8-bit op code, followed by a 24-bit address. After the page/block address is registered, the device starts the transfer from the cache register to the main array and is busy for ^{t}PROG time. During this busy time, the status register can be polled to monitor the status of the operation (refer to the status register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure 19: PROGRAM EXECUTE (10h) Timing



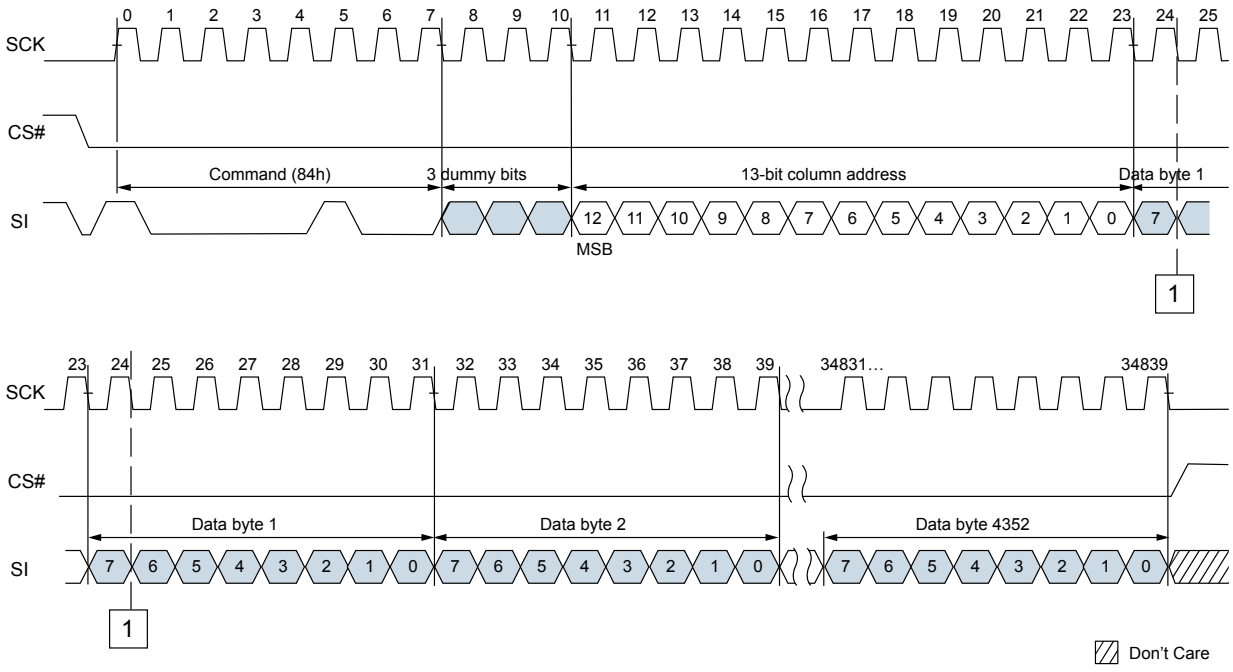
RANDOM DATA PROGRAM ×1 (84h)

The RANDOM DATA PROGRAM operation programs or replaces data in a page with existing data. The random data program sequence is as follows:

- 06h (WRITE ENABLE command)
- 84h (PROGRAM LOAD RANDOM DATA command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURE command to read the status)

The PROGRAM LOAD RANDOM DATA ×1 (84h) operation is similar to PROGRAM LOAD ×1 (02h). The difference is that PROGRAM LOAD ×1 command will reset the cache buffer to an all FFh value, while PROGRAM LOAD RANDOM DATA ×1 command will only update the data bytes that are specified by the command input sequence, and the rest of data in the cache buffer will remain unchanged. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA ×1 (84h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Figure 20: PROGRAM LOAD RANDOM DATA (84h) Timing



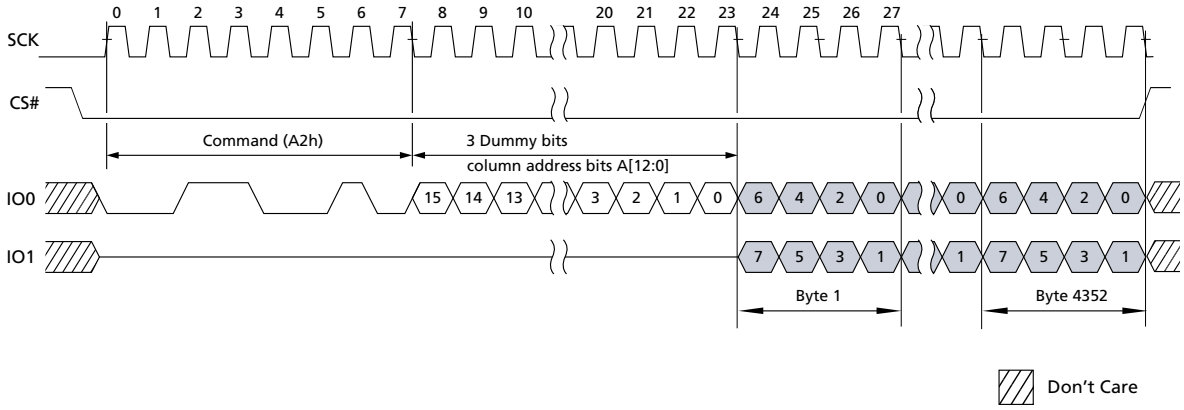
PROGRAM LOAD ×2 (A2h)/PROGRAM LOAD RANDOM DATA ×2 (44h)

The PROGRAM LOAD ×2 and PROGRAM LOAD RANDOM DATA ×2 instructions are similar to the PROGRAM LOAD and PROGRAM LOAD RANDOM DATA in terms of operation sequence and functionality. The only difference is that ×2 instructions will input the data bytes from 2 I/O pins instead of the single SI pin.

Both PROGRAM LOAD ×2 and PROGRAM LOAD RANDOM DATA ×2 instructions are the same command sequence. The difference is that PROGRAM LOAD ×2 instruction will

reset the cache buffer to all FFh value, while PROGRAM LOAD RANDOM DATA ×2 instruction will only update the data bytes that are specified by the command input sequence and the rest of data in the cache buffer will remain unchanged.

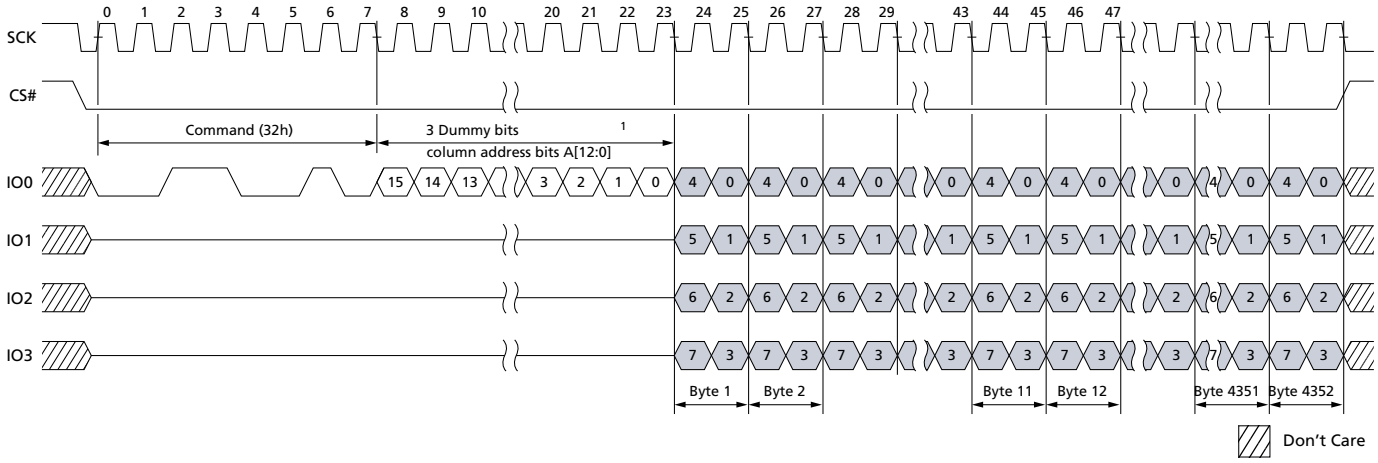
Figure 21: PROGRAM LOAD ×2 (A2h) Timing



PROGRAM LOAD ×4 (32h) and PROGRAM LOAD RANDOM DATA ×4 (34h)

The PROGRAM LOAD ×4 (32h) and RANDOM DATA ×4 (34h) are similar to PROGRAM LOAD ×1 (02h) command and RANDOM DATA ×1 (84h), but with the capability to input the data across four data lines.

Figure 22: PROGRAM LOAD ×4 (32h) Timing



INTERNAL DATA MOVE

The INTERNAL DATA MOVE command programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13h (PAGE READ command to cache)

- 06h (WRITE ENABLE command)
- 84h (PROGRAM LOAD RANDOM DATA command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURE command to read the status)

Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. This is done by issuing a PAGE READ (13h) command. The PAGE READ command must be followed with a WRITE ENABLE (06h) command in order to change the contents of memory array. After the WRITE ENABLE command is issued, the PROGRAM LOAD RANDOM DATA (84h) command, PROGRAM LOAD RANDOM DATA ×2 (44h) command, or PROGRAM LOAD RANDOM DATA ×4 (34h) can be issued. This command consists of an 8-bit Op code, followed by 3 dummy bits, a 13-bit column address and the new data to be loaded. If the random data is not sequential, another PROGRAM LOAD RANDOM command must be issued with the new column address. After all data are loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation. It is not possible to use the INTERNAL DATA MOVE operation to move data from one die (LUN) to another.

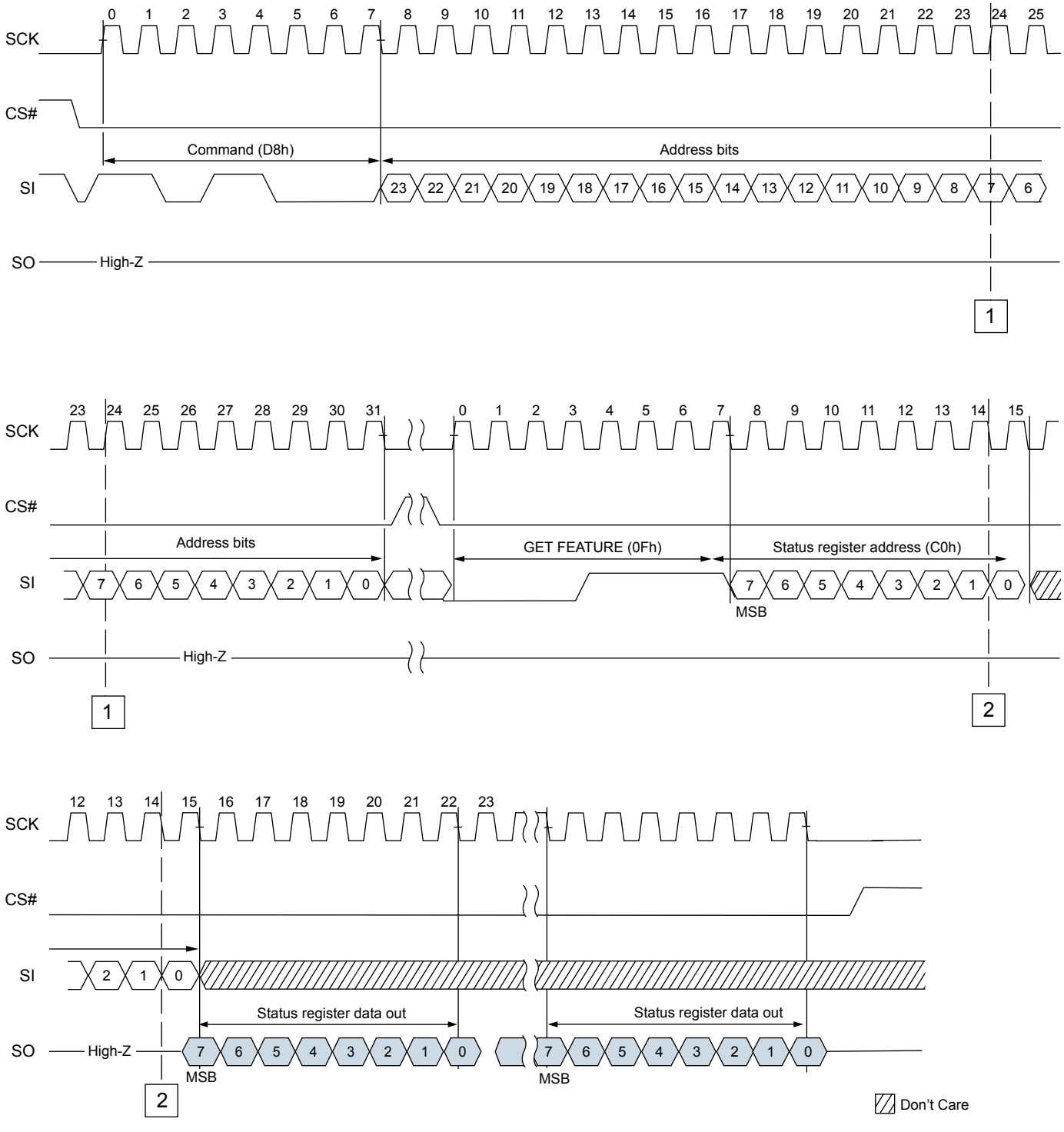
Block Erase Operations

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block. The BLOCK ERASE (D8h) command operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENABLE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURE command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of dummy bits followed by a valid block address. After the address is registered, the control logic automatically controls timing and ERASE and VERIFY operations. The device is busy for ^{t}ERS time during the BLOCK ERASE operation. The GET FEATURE (0Fh) command can be used to monitor the status of the operation. (See the following figure.)

Figure 23: BLOCK ERASE (D8h) Timing



Features Operations

GET FEATURE (0Fh) and SET FEATURE (1Fh)

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands either monitor the device status or alter the device configuration from the default at power-on. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP protect, block locking, SPI NOR like protocol configuration, and ECC correction can be managed by setting specific bits in feature addresses. Typically, the status register at feature address C0h is read to check the device status, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless specified otherwise, when the device is set, it remains set even if a RESET (FFh) command is issued. CFG[2:0] will be cleared to 000 after a reset and the device is back to normal operation.

Figure 24: GET FEATURE (0Fh) Timing

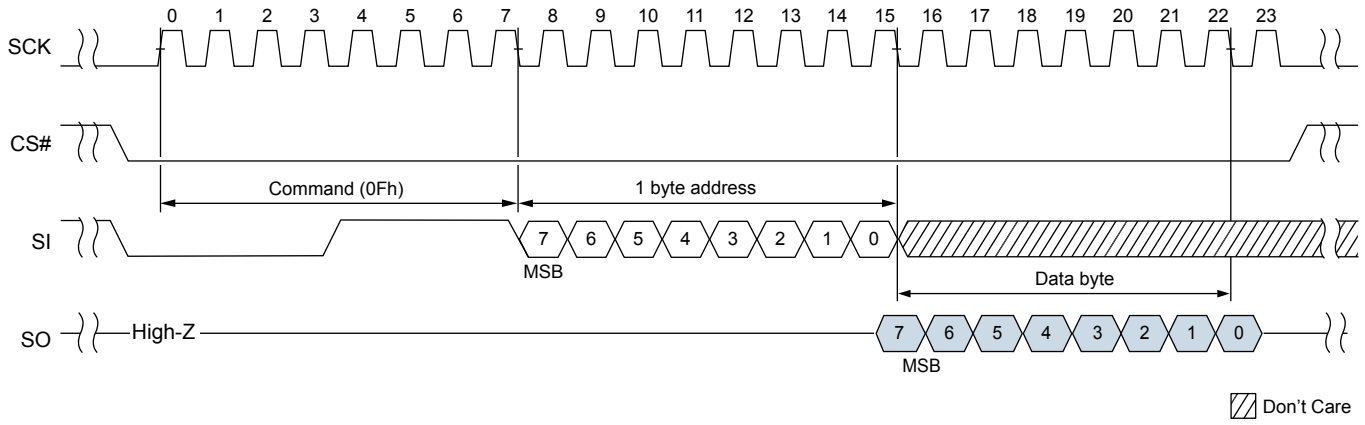
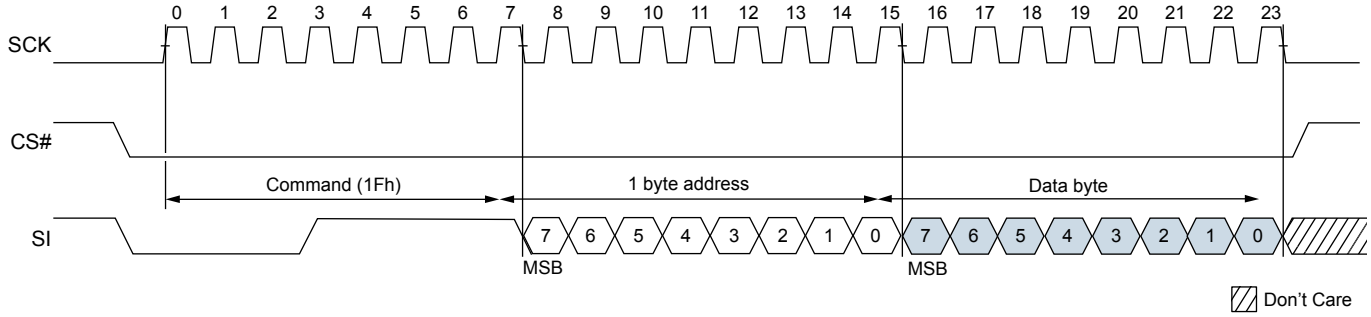


Figure 25: SET FEATURE (1Fh) Timing



Feature Settings

Table 7: Feature Address Settings and Data Bits

Register	Feature Address	Feature Data Bits								Notes
		7	6	5	4	3	2	1	0	
Block lock	Address = A0h; Access = R/W	BRWD	BP3	BP2	BP1	BP0	TB	WP#/ HOLD# Disable	–	1
Configuration	Address = B0h; Access = R/W	CFG2	CFG1	LOT_EN	ECC_EN	DS_S1	DS_S0	CFG0	CONTI_RD	2
Status	Address = C0h; Access = R	CRBSY	ECCS2	ECCS1	ECCS0	P_Fail	E_Fail	WEL	OIP	1
Die select	Address = D0h; Access = R/W	–	DS0	–	–	–	–	–	–	3

Notes:
1. When the WP#/HOLD# disable bit is at the default value of 0, and with BRWD set to 1 and WP# LOW, block lock registers [7:2] cannot be changed.
2. DS_Sx are used to adjust the driver strength and CONTI_RD provides capability to enable/disable continuous read.
3. Die Select only available in stacked die devices .

Driver Strength Configuration (DS_S1/DS_S0)

The driver strength configuration bits (DS_S1/DS_S0) are default at 00 after power-up, when these bits are updated with SET FEATURE command, they remain active even if a RESET command is issued, until the device is power cycled or these bits are updated again.

Table 8: Driver Strength Register Bits Descriptions

DS_S1	DS_S0	Drive Strength (%)[1]
0	0	100
0	1	75
1	0	50
1	1	25

Note:
1. POR frequency is guaranteed only at 100% drive strength.

Die Selection

Dual Die Behaviour During Power-on

After power-up or RESET, die 0 is the default die selected. For instance, the host can use the SET FEATURE (1Fh) command with D0h address and data 40h to select die 1. RESET and SET FEATURE commands are listened by both the die simultaneously. Do not use GET FEATURE command to detect device status during initialization or RESET. Wait ^{t}POR or ^{t}RST after power-up before issuing any commands. SET FEATURE is also not allowed when any LUN is in busy state to avoid addressing the wrong LUN. The rest of the command sets are listened only by the selected die.

Table 9: Die Selection

Dual Die Stack	SET FEATURE Command Address	SET FEATURE Command Data
Die 0	D0h	0h
Die 1	D0h	40h

Security – Volatile Block Protection

The block lock feature protects the entire device or ranges of device blocks from the PROGRAM and ERASE operations. The SET FEATURE command must be issued to alter the state of block protection. After power-up, the device is in the locked state by default; block lock register bits BP[3:0] and TB are 1. Reset will not modify the block protection state. When a PROGRAM/ERASE command is issued to a locked block, a status register P_Fail bit or E_Fail bit will be set to indicate the operation failure.

The following command sequence unlocks all blocks after power-up: The SET FEATURE REGISTER WRITE (1Fh) operation is issued, followed by the feature address (A0h). Then, 00h is issued on data bits to unlock all blocks.

Security – Block Protection Bits

Table 10: Block Lock Register Block Protection Bits

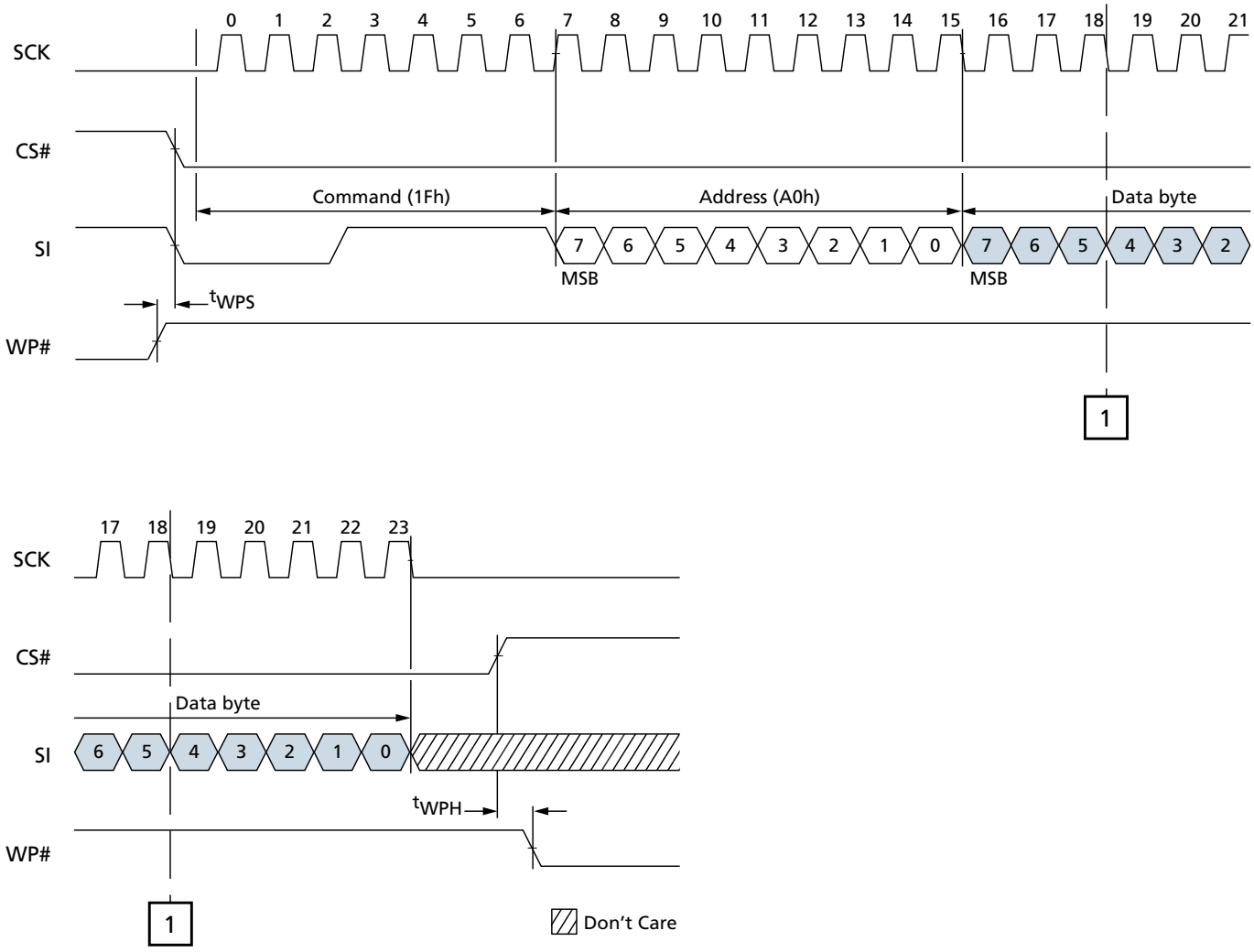
TB	BP3	BP2	BP1	BP0	Protected Portion	Protected Blocks
0	0	0	0	0	None – all unlocked	None
0	0	0	0	1	Upper 1/1024 locked	4092:4095
0	0	0	1	0	Upper 1/512 locked	4088:4095
0	0	0	1	1	Upper 1/256 locked	4080:4095
0	0	1	0	0	Upper 1/128 locked	4064:4095
0	0	1	0	1	Upper 1/64 locked	4032:4095
0	0	1	1	0	Upper 1/32 locked	3968:4095
0	0	1	1	1	Upper 1/16 locked	3840:4095
0	1	0	0	0	Upper 1/8 locked	3584:4095
0	1	0	0	1	Upper 1/4 locked	3072:4095
0	1	0	1	0	Upper 1/2 locked	2048:4095
1	0	0	0	0	All unlocked	None
All others					All locked	0:4095
1	0	0	0	1	Lower 1/1024 locked	0:3
1	0	0	1	0	Lower 1/512 locked	0:7
1	0	0	1	1	Lower 1/256 locked	0:15
1	0	1	0	0	Lower 1/128 locked	0:31
1	0	1	0	1	Lower 1/64 locked	0:63
1	0	1	1	0	Lower 1/32 locked	0:127
1	0	1	1	1	Lower 1/16 locked	0:255
1	1	0	0	0	Upper 1/8 locked	0:511
1	1	0	0	1	Lower 1/4 locked	0:1023
1	1	0	1	0	Lower 1/2 locked	0:2047
1	1	1	1	1	All locked (default)	0:4095

Security – Hardware Write Protection

Hardware write protection prevents the block protection state from hardware modifications. In order to utilize this feature, SET FEATURE command is issued on the feature address A0h and WP#/HOLD# disable bit state is set to 0.

The BRWD bit is operated in conjunction with WP#/HOLD# disable bit. When BRWD is set to 1 and WP# is LOW, none of the other block lock register bits [7:2] can be set. The block lock state cannot be changed, regardless of what is unlocked or locked. Also, when the WP#/HOLD# disable bit is set to 1, the hardware protected mode is disabled. The default value of BRWD and WP#/HOLD# disable bits = 0 after power up.

Figure 26: WP# Timing



Security – Device Lock Tight

The lock tight (LOT) mode prevents the block protection state from software modifications. After it is enabled, this mode cannot be disabled by a software command. Also,

BP, TB, and BRWD bits are protected from further software changes. Only another power cycle can disable the lock tight mode.

The following command sequence enables the lock tight mode: The SET FEATURE REGISTER WRITE (1Fh) operation is issued, followed by the feature address (B0h). Then, data bits are set to enable LOT (LOT_EN bit = 1).

When the hardware write protection mode is disabled during quad or ×4 mode, lock tight can be used to prevent a block protection state change.

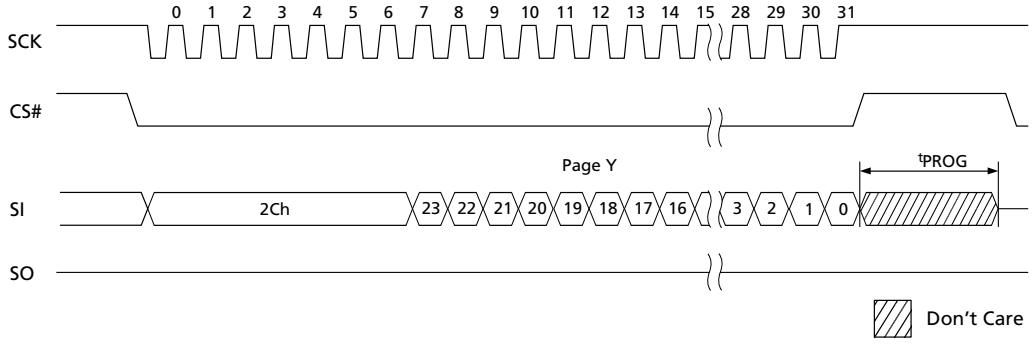
Permanent Block Lock Protection

48 blocks per die (0 to 47) can be permanently locked using PROTECT command. The PROTECT command provides nonvolatile, irreversible protection of up to twelve groups (48 blocks). Implementation of the protection is group-based, which means that a minimum of one group (4 blocks) is protected when the PROTECT command is issued. Because block protection is nonvolatile, a power-on or power-off sequence does not affect the block status after the PROTECT command is issued. The device is shipped from the factory with no blocks protected so that users can program or erase the blocks before issuing the PROTECT command. Block protection is also irreversible in that when protection is enabled by issuing the PROTECT command, the protected blocks can no longer be programmed or erased. If permanent lock is disabled, PROTECT command would be ignored. As with any command that changes the memory contents, the WRITE ENABLE must be executed. If this command is not issued, then the PROTECT command is ignored. WRITE ENABLE must be followed by a PROTECT (2Ch) command.

The following protect sequence is used:

- 06h (WRITE ENABLE)
- 2Ch (PROTECT)
- 24-bit address (see the PROTECT Command Details)
- After ^{t}PROG time, use GET FEATURE (0Fh) command with feature address C0h to verify P_Fail bit

Figure 27: PROTECT Command Cycle



PROTECT (2Ch) Command Details

To enable protection, the PROTECT command consists of an 8-bit command code, followed by a 24-bit address (7 dummy bits and 17-bit page/block address). Row address

bits 11, 10, 9, 8 (named as Y) input the targeted block group information. Where Y defines the group of blocks to be protected. There are 12 Groups Y where Y = 0000b–1011b:

- Y = 0000 protects Group0 = blks 0, 1, 2, 3.
- Y = 0001 protects Group1 = blks 4, 5, 6, 7.
- .....
- Y = 1011 protects Group11 = blks 44, 45, 46, 47.

After ^{t}PROG, the targeted block groups are protected. Upon PROTECT operation failure, the status register reports a value of 08h (P_FAIL = 1 and WEL = 0). Upon PROTECT operation success, the status register reports a value of 00h.

Permanent Block Lock Protection Disable Mode

This mode disables the ability to accept the PROTECT command. Running this command sequence ensures no more groups can ever be permanently locked.

The following disable protect sequence should be used on each die (for dual die device):

- Select the die using SET FEATURE command
- SET FEATURE (1Fh) command with B0h mode and data value C2h
- 06h (WRITE ENABLE)
- 10h (Execute with block/page address as "0")
- After ^{t}PROG time, use GET FEATURE (0Fh) command with feature address C0h to verify P_Fail bit.

Permanent Block Protection Status Read

The permanent block protection status is accessible while the permanent block protection status read mode is enabled. To enable this mode, issue the SET FEATURE (1Fh) command to feature address B0h and data value with OTP_CFG[2:0] = 001b. When the device is in permanent block protection status read mode, all subsequent PAGE READ commands will return with the block protection status. To read block protection status, issue the PAGE READ (13h) command sequence with the target block address.

To determine whether the device is busy getting the block protection status, use GET FEATURE command at address C0h to check OIP bit. Once ready, any READ FROM CACHE command could be used to check the target block's protection status, reading out all "0" indicate the target block is permanently protected; all "1" indicates target block is not permanently protected.

To exit from permanent block protection status read mode and return to normal array operation mode, issue the SET FEATURE (1Fh) command to feature address B0h and data value with OTP_CFG[2:0] = 000b.

If the RESET (FFh) command is issued while in permanent block protection status read mode, the device will exit this mode and enter normal operation mode.

Security – One Time Programmable

This device offers a protected, one-time programmable NAND Flash memory area. Ten full pages per die are available, and the entire range is guaranteed. Users can choose how to use the one time programmable (OTP) area, such as programming serial numbers or other data for permanent storage. The OTP area can't be erased. When ECC is enabled, data written in the OTP area is ECC protected. Besides some additional configuration bits are described in this section.

Enable OTP Access

OTP access needs to be enabled in order to read and write to the OTP region. When the die is in OTP operation mode, all subsequent PAGE PROGRAM or PAGE READ commands are applied to the OTP area. SET FEATURE (1Fh) command with feature address B0h and data 50h (OTP operation mode with ECC enabled) or 40h (OTP operation mode with ECC disabled) are used to enable the OTP access.

After OTP access is enabled, the following sequence is used to program one or more pages:

- WRITE ENABLE (06h) command
- PROGRAM EXECUTE (10h) command with the row address of page (OTP page address range 02h-0Bh)
- Verify until OIP bit not busy using GET FEATURE (0Fh) command with feature address C0h
- Using GET FEATURE (0Fh) command with feature address C0h, verify if P_FAIL bit is 0 for the successful operation

After OTP access is enabled, the following sequence is used to read one or more pages:

- PAGE READ (13h) command with the page address (02h-0Bh)
- Verify until OIP bit is not busy using GET FEATURE (0Fh) command with feature address C0h
- Page data using READ FROM CACHE (03h) command

OTP Configuration States

To check the status of OTP data protect, SPI NOR read enable, or permanent block Lock protection, the following sequence is used:

- SET FEATURE (1Fh) command with feature address B0h and data (C0h for OTP data protect bit, 82h for NOR read protocol enable bit, C2h for permanent block lock disable bit)
- PAGE READ (13h) command with address 0
- Verify until OIP bit not busy using GET FEATURE (0Fh) command with feature address C0h
- READ FROM CACHE (03h) command with address 0
- Expect the read from cache data all 1 for the mode disabled or all "0" for enabled.

Note: Configuration status of CFG[2:0] can be read using GET FEATURE (0Fh) command with feature address B0h.

OTP Protection and Program Prevention

This mode is used to prevent further programming of the pages in the OTP area. To protect and prevent programming the OTP area, the following sequence is used:

- SET FEATURE (1Fh) command with feature address B0h and data C0h (CFG[2:0] = 110b)
- WRITE ENABLE (06h) command
- PROGRAM EXECUTE (10h) command with the row address 00h
- Verify until OIP bit not busy and P_FAIL bit 0 using GET FEATURE (0Fh) command with status register address C0h.

Exit OTP

To exit from OTP operation mode and return the device to normal array operation mode, the SET FEATURE (1Fh) command is issued. This is followed by setting the feature address = B0h and data CFG[2:0] = 000b. Last, the RESET (FFh) command is issued.

Table 11: Configuration Registers for Security

CFG2	CFG1	CFG0	State
0	0	0	Normal operation
0	0	1	Access to permanent block protect status read mode
0	1	0	Access OTP area/Parameter/Unique ID
1	1	0	Access to OTP data protection bit to lock OTP area
1	0	1	Access to SPI NOR read protocol enable mode
1	1	1	Access to permanent block lock protection disable mode

Status Register

The device has an 8-bit status register that software can read during the device operation. All bits are read-only register except WEL, which could be changed by WRITE DISABLE (04h) and WRITE ENABLE (06h) commands. None of bits can be changed by SET FEATURE (1Fh) command. The status register can be read by issuing the GET FEATURE (0Fh) command, followed by the feature address (C0h). The status register will output the status of the operation.

Table 12: Status Register Bit Descriptions

Bit	Bit Name	Description
7	Cache read busy (CRBSY)	This bit is set (CRBSY = 1) when READ PAGE CACHE RANDOM command is executing; this bit remains a 1 until the page specified at READ PAGE CACHE RANDOM command is transferred from array to data register. When the bit is 0, the device is in the ready state and background READ PAGE CACHE operation is completed. RESET command is acceptable during CRBSY = 1 and could halt background READ PAGE CACHE operation and download first page at block 0 into cache register at default.
6	ECC status register (ECCS2)	See ECC Protection for the ECC status definition. ECC status is set to 000b either following a RESET or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC status is invalid if ECC is disabled (via a SET FEATURE command to get access the configuration register). After a power-up RESET, ECC status is set to reflect the contents of block 0, page 0.
5	ECC status register (ECCS1)	
4	ECC status register (ECCS0)	
3	Program fail (P_Fail)	Indicates that a program failure has occurred (P_Fail = 1). This bit will also be set if the user attempts to program a locked or protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_Fail = 0).
2	Erase fail (E_Fail)	Indicates that an erase failure has occurred (E_Fail = 1). This bit will also be set if the user attempts to erase a locked region or if the ERASE operation fails. This bit is cleared (E_Fail = 0) at the start of the BLOCK ERASE command sequence or a RESET command.
1	Write enable latch (WEL)	Indicates the current status of the write enable latch (WEL) and must be set (WEL = 1) prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be cleared (WEL = 0) by issuing the WRITE DISABLE command or a successful PROGRAM/ERASE operation.
0	Operation in progress (OIP)	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, READ PAGE CACHE LAST, BLOCK ERASE, READ PAGE CACHE RANDOM (within ^{t}RCBSY to wait for cache register readiness), RESET command, or a power-up initialization is executing; the device is busy. When the bit is 0, the interface is in the ready state.

ECC Protection

The device offers an 8-bit data corruption protection by offering internal ECC to obtain the data integrity. The internal ECC can be enabled or disabled by setting the ECC_EN bit in the configuration register. ECC is enabled after device power-up by default. The READ and PROGRAM commands operate with internal ECC by default. Reset will not change the existing configuration. To enable/disable ECC after power-on, perform the following command sequence:

- Issue the SET FEATURE (1Fh) command
- Issue configuration register address (B0h)
- Then: To enable ECC, set bit 4 (ECC enable) to 1; To disable ECC, clear bit 4 (ECC enable) to 0

During a PROGRAM operation, the device calculates an expected ECC code on the ECC-protected bytes in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the expected ECC code value read from the array. If a 1–8-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status register bit indicates whether or not the error correction is successful. The table below describes the ECC protection scheme used throughout a page.

Note: The unique ID and parameter page are not ECC-protected areas. Multiple copies are provided for parameter page to obtain the data integrity. XOR method is provided for unique ID to verify the data.

With internal ECC, users must accommodate the following (details provided in table below):

- Spare area definitions
- WRITEs are supported for main and spare areas (user meta data I and II). WRITEs to the ECC area are prohibited

When using partial-page programming, the following conditions must both be met:

- In the main user area and user meta data area I, SINGLE PARTIAL-PAGE PROGRAMMING operations must be used
- Within a page, a maximum of four PARTIAL-PAGE PROGRAMMING operations can be performed

Table 13: ECC Status Register Bit Descriptions

Bit 2	Bit 1	Bit 0	Description
0	0	0	No errors
0	0	1	1–3 bit errors detected and corrected
0	1	0	Bit errors greater than 8 bits detected and not corrected
0	1	1	4–6 bit errors detected and corrected. Indicates data refreshment might be taken
1	0	1	7–8 bit errors detected and corrected. Indicates data refreshment must be taken to guarantee data retention
Others			Reserved

Table 14: ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
9FFh	800h	Yes	Main 4	User data 4
BFFh	A00h	Yes	Main 5	User data 5
DFFh	C00h	Yes	Main 6	User data 6
FFFh	E00h	Yes	Main 7	User data 7
1003h	1000h	No	Spare 0	Reserved (bad block data)
1007h	1004h	No	Spare 1	Reserved or meta data II
100Bh	1008h	No	Spare 2	Reserved or meta data II
100Fh	100Ch	No	Spare 3	Reserved or meta data II
1013h	1010h	No	Spare 4	Reserved or meta data II
1017h	1014h	No	Spare 5	Reserved or meta data II
101Bh	1018h	No	Spare 6	Reserved or meta data II
101Fh	101Ch	No	Spare 7	Reserved or meta data II
1023h	1020h	No	Spare 0	Reserved or meta data II
1027h	1024h	No	Spare 1	Reserved or meta data II
102Bh	1028h	No	Spare 2	Reserved or meta data II
102Fh	102Ch	No	Spare 3	Reserved or meta data II
1033h	1030h	No	Spare 4	Reserved or meta data II
1037h	1034h	No	Spare 5	Reserved or meta data II
103Bh	1038h	No	Spare 6	Reserved or meta data II
103Fh	103Ch	No	Spare 7	Reserved or meta data II
1047h	1040h	Yes	Spare 0	Reserved or meta data I
104Fh	1048h	Yes	Spare 1	Reserved or meta data I
1057h	1050h	Yes	Spare 2	Reserved or meta data I
105Fh	1058h	Yes	Spare 3	Reserved or meta data I
1067h	1060h	Yes	Spare 4	Reserved or meta data I
106Fh	1068h	Yes	Spare 5	Reserved or meta data I
1077h	1070h	Yes	Spare 6	Reserved or meta data I
107Fh	1078h	Yes	Spare 7	Reserved or meta data I
108Fh	1080h	Yes	Spare 0	ECC for main/spare 0
109Fh	1090h	Yes	Spare 1	ECC for main/spare 1
10AFh	10A0h	Yes	Spare 2	ECC for main/spare 2
10BFh	10B0h	Yes	Spare 3	ECC for main/spare 3
10CFh	10C0h	Yes	Spare 4	ECC for main/spare 4

Table 14: ECC Protection (Continued)

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
10DFh	10D0h	Yes	Spare 5	ECC for main/spare 5
10EFh	10E0h	Yes	Spare 6	ECC for main/spare 6
10FFh	10F0h	Yes	Spare 7	ECC for main/spare 7

Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (N_{VB}) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 15: Error Management Details

Description	Requirement
Minimum number of total valid blocks (N_{VB})	4016
Total available blocks per device	4096
Total available blocks per die	2048
First spare area location in the first page of each block	Byte 4096
Value programmed for bad block at the first byte of spare area	00h
Minimum required ECC	8-bit ECC per sector (544) bytes of data

Table 15: Error Management Details (Continued)

Description	Requirement
Minimum ECC with internal ECC enabled	8-bit ECC per 512 bytes (user data) + 8 bytes (Spare) + 16 bytes (ECC data)

SPI NOR Read Configuration

Some chipset vendors may have already designed in SPI NOR IP to support system boot; address allocation on clock cycle in SPI NAND read from cache protocol will cause incompatibility. To be drop-in compatible to SPI NOR read protocol, this device offers an alternative solution to implement 03h/0Bh commands, as are done with SPI NOR. Refer to the Electrical Specifications for detail timing requirement. This solution would be enabled using the following command sequence:

- SET FEATURE (1Fh) command with feature address B0h and CFG bits[2:0] = 101b (access SPI NOR read protocol enable mode)
- WRITE ENABLE (06h) command
- PROGRAM EXECUTE (10h) command with block/page address all 0
- GET FEATURE (0Fh) command with status register address C0h to check until device is ready (OIP bit clear) and verify that P_FAIL bit is not set
- SET FEATURE (1Fh) command with feature address B0h and CFG bits[2:0] = 000b (return to normal operation mode)
- GET FEATURE (0Fh) command at address B0h and CFG bits[2:0] = 101b to verify all 0; all 1 indicates SPI NOR mode not enabled.

It is a nonvolatile configuration setting and power cycle will not recover it back to SPI NAND default mode. The rest of the SPI NAND commands still work in this configuration.

Figure 28: Read from Cache (03h)

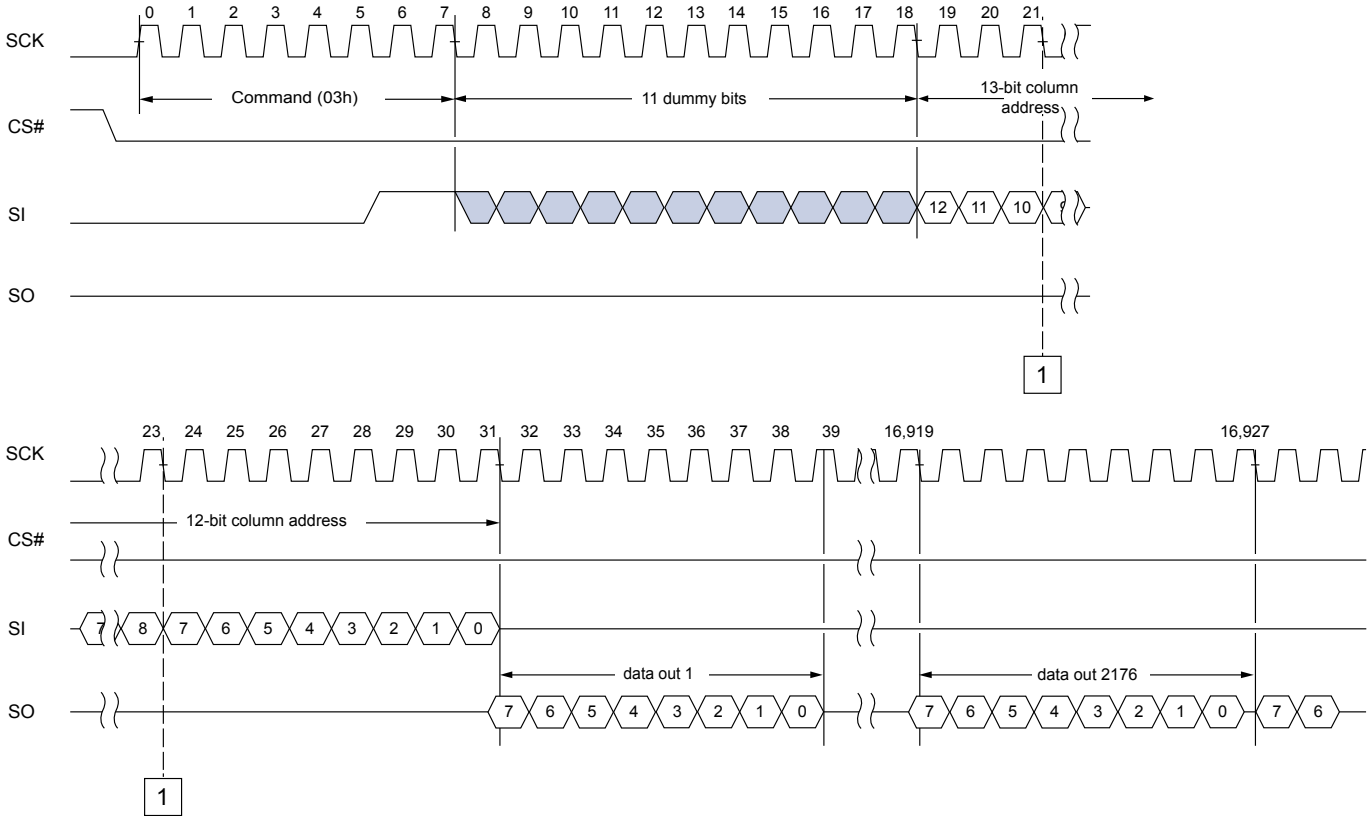
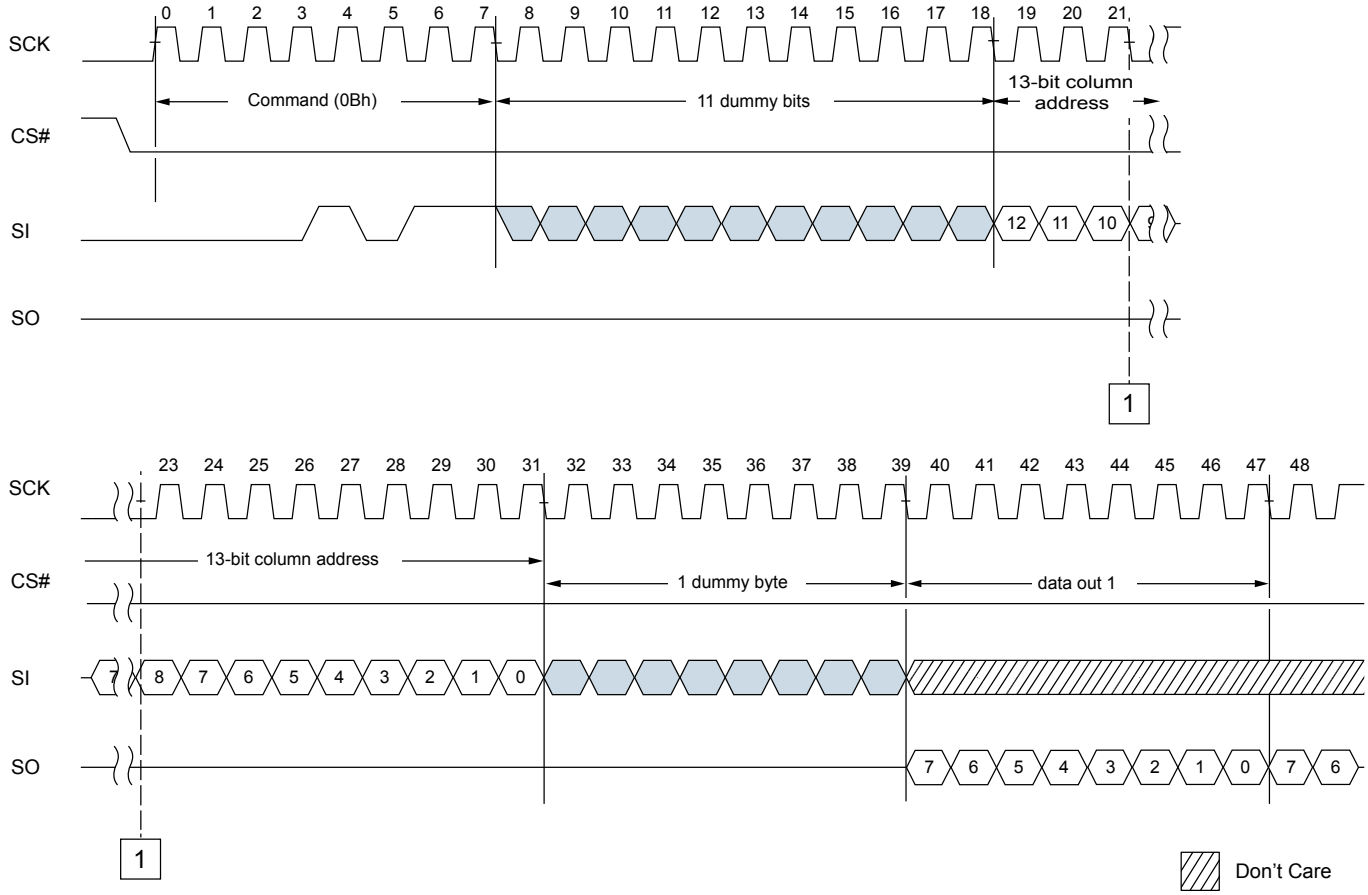


Figure 29: Fast Read from Cache (0Bh)

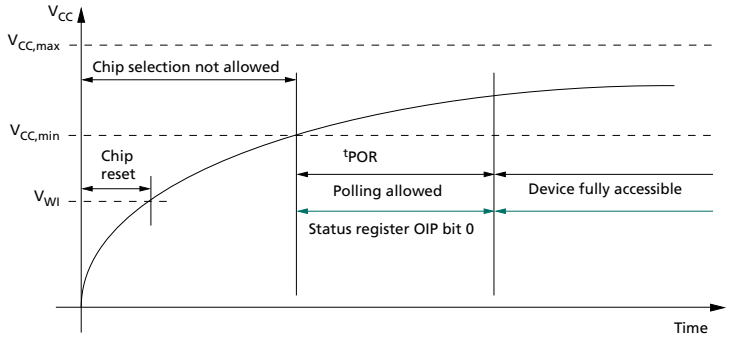


Power-Up and Power-Down

During the power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on V_{CC} until V_{CC} reaches the correct values: $V_{CC, min}$ at power-up and V_{SS} at power-down. Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. After the device V_{CC} has reached the $V_{CC, min}$, GET FEATURE command can be issued to poll the status register (OIP) before the first access. Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor (recommended 4.7µF + 0.1µF) close to the package pins.

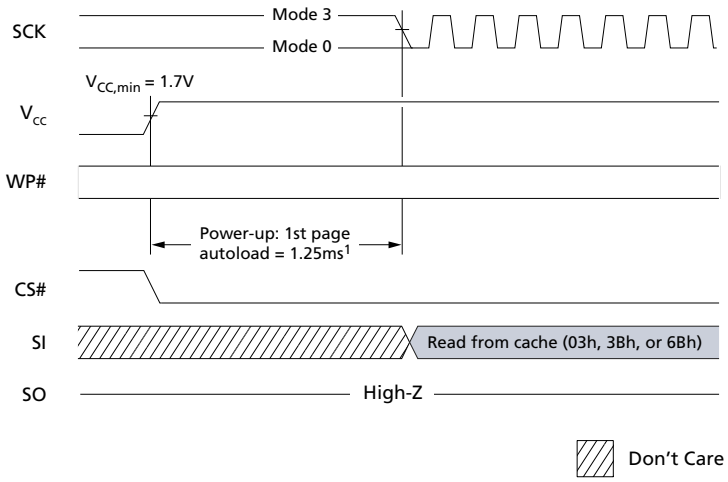
Note: For power cycle testing, the system must not initiate the power-up sequence until V_{CC} drops down to 0V.

Figure 30: SPI Power-Up



This device supports default device initialization that does not require RESET (FFh) command. When device V_{CC} has reached the write inhibit voltage, the device automatically starts the initialization. At default setting, first page data is automatically loaded into cache register. During the initialization, GET FEATURE command can be issued to poll the status register (OIP) before the first access; Or, the first access can occur 1.25ms (for 3.3V) or 2ms (for 1.8V) after V_{CC} reaches $V_{CC,min}$.

Figure 31: Automatic Device Initialization



Notes:
1. A = 1.25ms for 3.3V, 2ms for 1.8V.
2. B = 2.7V for 3.3V, 1.7V for 1.8V.

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above values in this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 16: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage (SPI)	V_{CC}	–0.6	2.4	V
I/O voltage	V_{CC}	–0.6	2.4	V
Operating temperature (ambient)	T_A	–40	85	°C
Storage temperature	T_S	–65	150	°C

Note: 1. During infrequent, nonperiodic transitions and for periods less than 20ns, voltage potential between V_{SS} and V_{CC} may undershoot to –2.0V or overshoot to $V_{CC,max}$ + 2.0V.

Table 17: Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	1.7	1.8	1.95	V
Ambient operating temperature (industrial)	T_A	–40	25	85	°C

Table 18: AC Measurement Conditions

Parameter	Symbol	Min	Max	Unit
Load capacitance	C_L	30/10		pF
Input rise and fall time	–	–	5	ns
Input rise and fall times (for ≥80 MHz)[1, 2]	–	–	2.1	ns
Input pulse voltage[1]	–	0.2 V_{CC}	0.8 V_{CC}	V
Input timing reference voltages	–	0.3 V_{CC}	0.7 V_{CC}	V
Output timing reference voltages	–	$V_{CC}/2$		V

Notes: 1. Applicable to 20 MHz or 66 MHz.
2. 20% of clock period.

Figure 32: AC Measurement I/O Waveform

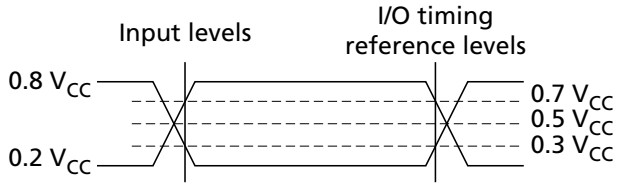


Table 19: Capacitance

Description	Symbol	Test Conditions	Min	Max	Unit
Input/output capacitance (IO0, IO1, IO2, IO3)	C_{IN}	V_{OUT} = 0V	–	18	pF
Input capacitance (other pins)	C_{IN}	V_{IN} = 0V	–	18	pF

Notes:
1. These parameters are verified in device characterization and are not 100% tested.
2. The value includes the silicon and package together.

Table 20: DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}	–	0.7 × V_{CC}	–	V_{CC} + 0.4	V
Input low voltage	V_{IL}	–	–0.5	–	0.3 × V_{CC}	V
Output high voltage	V_{OH}	I_{OH} = –100µA	V_{CC} - 0.2	–	–	V
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
Input leakage current	I_{LI}	–	–	–	±10	µA
Output leakage current	I_{LO}	–	–	–	±10	µA
Page read current x1: Continuous Read on[3, 4]	I_{CC2}	SCK = 0.1V_{CC}/0.9V_{CC} at 83 MHz	–	33	43	mA
Page read current	I_{CC3}	CE# = V_{CC}	–	33	43	mA
Program current	I_{CC4}	CE# = V_{CC}	–	28	33	mA
Erase current	I_{CC5}	CE# = V_{CC}	–	23	33	mA
Standby current	I_{CC1}	CE# = V_{CC}; V_{IN} = V_{SS} or V_{CC}	–	35	70	µA

Notes:
1. Typical values are given for T_A = 25 °C.
2. These parameters are verified in device characterization and are not 100% tested.
3. All read currents are average current measured over a page of continuous reads.
4. Continuous read currents is average current measured over any complete block read.

Table 21: AC Characteristics

Parameter	Symbol	Min	Max	Unit
Clock frequency[1, 2]	^{f}C	–	83	MHz
Clock LOW time	^{t}WL	5.4	–	ns
Clock HIGH time	^{t}WH	5.4	–	ns
Clock LOW time (SPI NOR read 03h mode at 5 MHz)	^{t}WL	90	–	ns
Clock HIGH time (SPI NOR read 03h mode at 5 MHz)	^{t}WH	90	–	ns
Clock rise time	^{t}CRT	0.5	–	V/ns
Clock fall time	^{t}CFT	0.5	–	V/ns
Command deselect time	^{t}CS	50	–	ns
CS# active setup time relative to SCK	^{t}CSS	4.5	–	ns
CS# non-active hold time relative to SCK	^{t}CSH	3	–	ns

Table 21: AC Characteristics (Continued)

Parameter	Symbol	Min	Max	Unit
Output disable time	^{t}DIS	–	7	ns
Data input setup time	^{t}SUDAT	4	–	ns
Data input hold time	^{t}HDDAT	2	–	ns
Clock LOW to output valid (30pF)	^{t}V	–	8	ns
Clock LOW to output valid (10pF)	^{t}V	–	7	ns
Clock LOW to output valid (similar to SPI NOR 5 MHz read 30pF)	^{t}V	–	30	ns
Clock LOW to output valid (similar to SPI NOR 5 MHz read 10pF)	^{t}V	–	28	ns
Output hold time (30pF)	^{t}HO	2.5	–	ns
Output hold time (10pF)	^{t}HO	2	–	ns
Output hold time (SPI NOR similar to 5 MHz read 30pF)	^{t}HO	0	–	ns
Output hold time (SPI NOR similar to 5 MHz read 10pF)	^{t}HO	0	–	ns
WP# hold time	^{t}WPH	100	–	ns
WP# setup time	^{t}WPS	20	–	ns

Notes:
1. When read protocol similar to SPI NOR is enabled, READ FROM CACHE 03h command can run up to 5 MHz, while READ FROM CACHE 0Bh command can run up to 83 MHz.
2. READ FROM CACHE x2, Dual IO (3Bh, BBh) can run up to 74 MHz and x4, Quad IO (6Bh, EBh) up to 37 MHz.

Table 22: PROGRAM/READ/ERASE Characteristics

Parameter	Symbol	Typ	Max	Unit
BLOCK ERASE operation time (128KB)	^{t}ERS	2	10	ms
PROGRAM PAGE operation time (ECC disabled)	^{t}PROG	200	600	µs
PROGRAM PAGE operation time (ECC enabled)		240	600	
Page read time (ECC disabled, CONTI_RD off)	^{t}RD	–	25	µs
Page read time (ECC enabled, CONTI_RD on)		90	170	
Data transfer time from data register to cache register (internal ECC disabled)	^{t}RCBSY	–	5	µs
Data transfer time from data register to cache register (internal ECC enabled)		90	170	µs
Power-on reset time (device initialization) from $V_{CC,min}$	^{t}POR	–	2	ms
Write inhibit voltage	V_{WI}	–	1.5	V
Reset time for READ, PROGRAM, and ERASE operations (internal ECC disabled, CONTI_RD off)	^{t}RST	–	30/35/525	µs
Reset time for READ, PROGRAM, and ERASE operations (internal ECC enabled, CONTI_RD on)		–	140/145/635	µs
Number of partial-page programming operations supported	NOP[1]	–	4	–

Note:
1. In the main user area and in user meta data area I, single partial-page programming operations must be used. Within a page, the user can perform a maximum of four partial-page programming operations.

Figure 33: Serial Input Timing

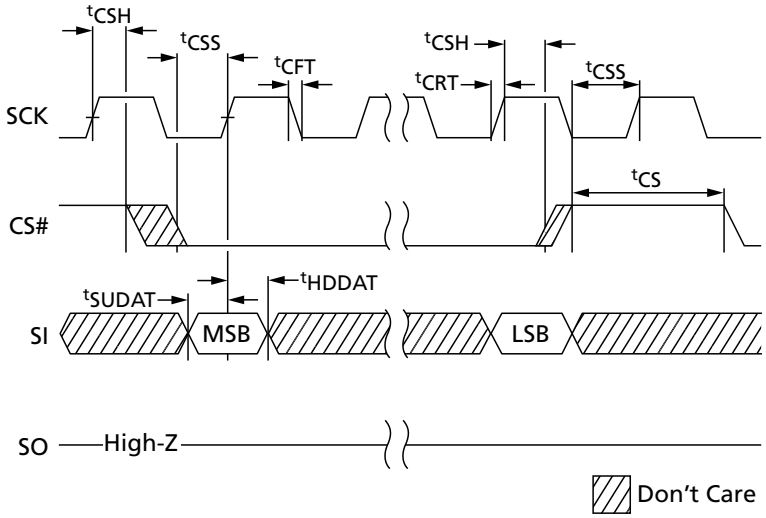
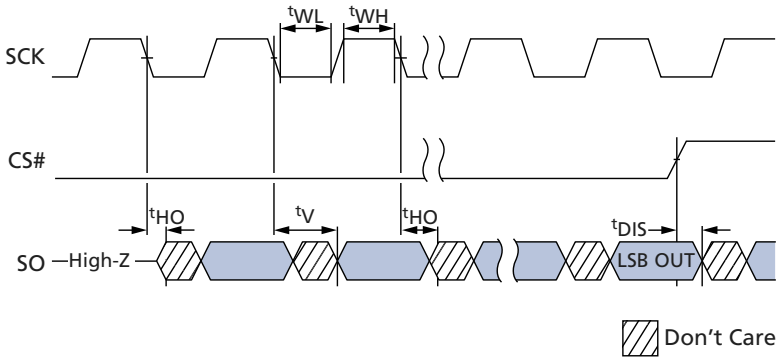
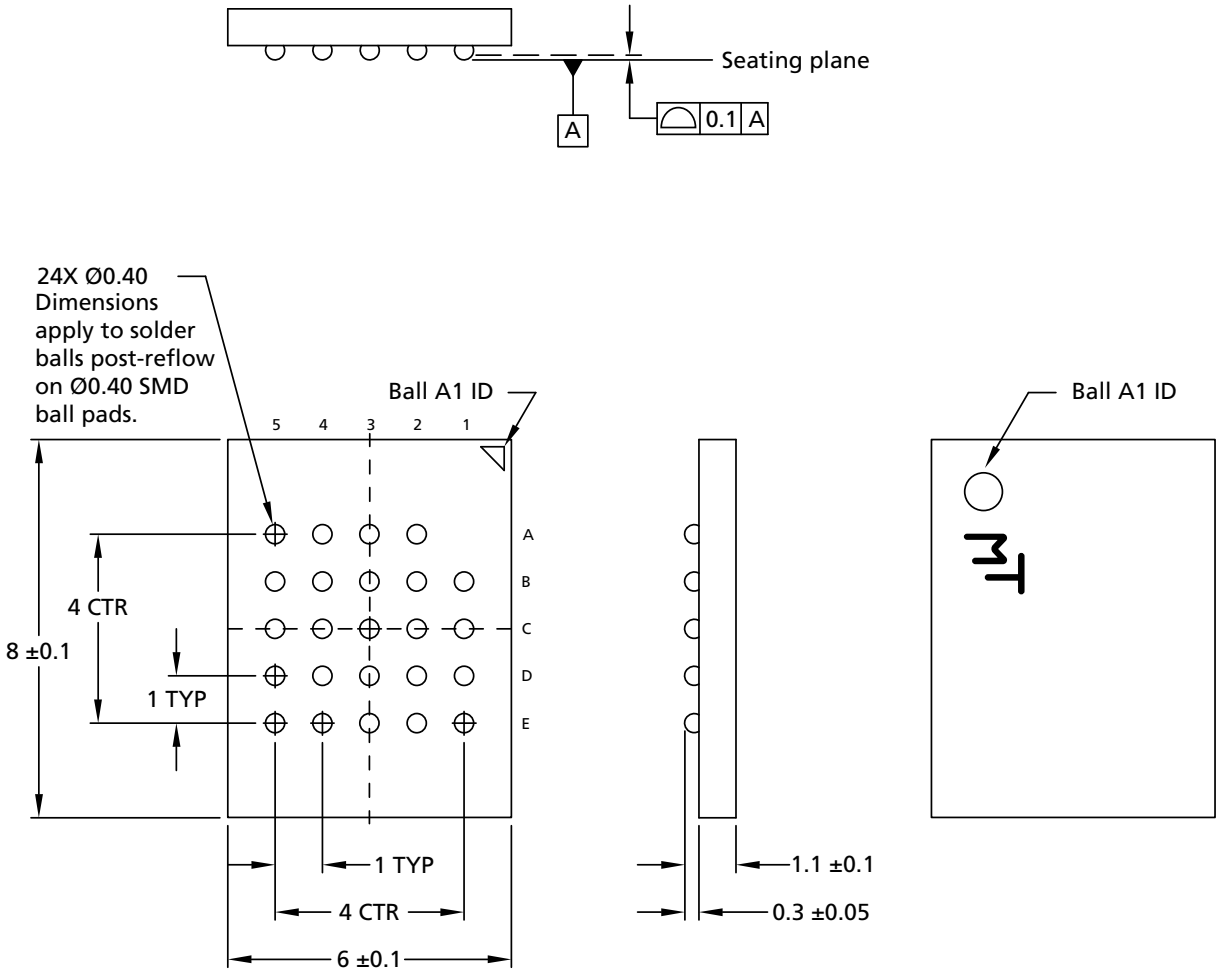


Figure 34: Serial Output Timing



Package Dimensions

Figure 35: 24-Pin T-PBGA (5 × 5 Ball Grid Array) 6mm × 8mm – Package Code: 12



Note: 1. All dimensions are in millimeters.

Revision History

Rev. C – 8/19

- Changed value in Parameter Table: Byte 112 from 00h to 08h to reflect 8 bit ECC
- Updated Continuous Read Operation: Updated Description; Updated Continuous Read Mode Matrix table

Rev. B – 4/19

- Updated legal status to Production
- Specified values in Electrical Specifications section

Rev. A – 7/17

- Initial release