1.35V DDR3L-RS SDRAM

MT41K256M8 – 32 Meg x 8 x 8 banks

MT41K128M16 – 16 Meg x 16 x 8 banks

Description

DDR3L-RS SDRAM (1.35V) is a low current self refresh version, via a TCSR feature, of the DDR3L SDRAM (1.35V) device. Unless stated otherwise, the DDR3L-RS SDRAM meets the functional and timing specifications listed in the equivalent density standard or automotive DDR3L SDRAM data sheets located on www.micron.com.

Features

- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.45V)
- Backward-compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Write leveling
- Output driver calibration
- Multipurpose register
- T_C of 0°C to +95°C
  - 64ms, 8192-cycle refresh at 0°C to +85°C
  - 32ms at +85°C to +95°C; See (SRT)
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Temperature-compensated self refresh (TCSR) mode
- Very low current self refresh mode when at room temperature

Options	Marking
• Configuration	
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. M, K	DA
• FBGA package (Pb-free) – x16	
– 96-ball FBGA (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.875ns @ CL = 7 (DDR3-1066)	-187E
• Temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
• Power Saving	
– TCSR	M
• Revision	:M /:K

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5

Table 1: Key Timing Parameters (Continued)

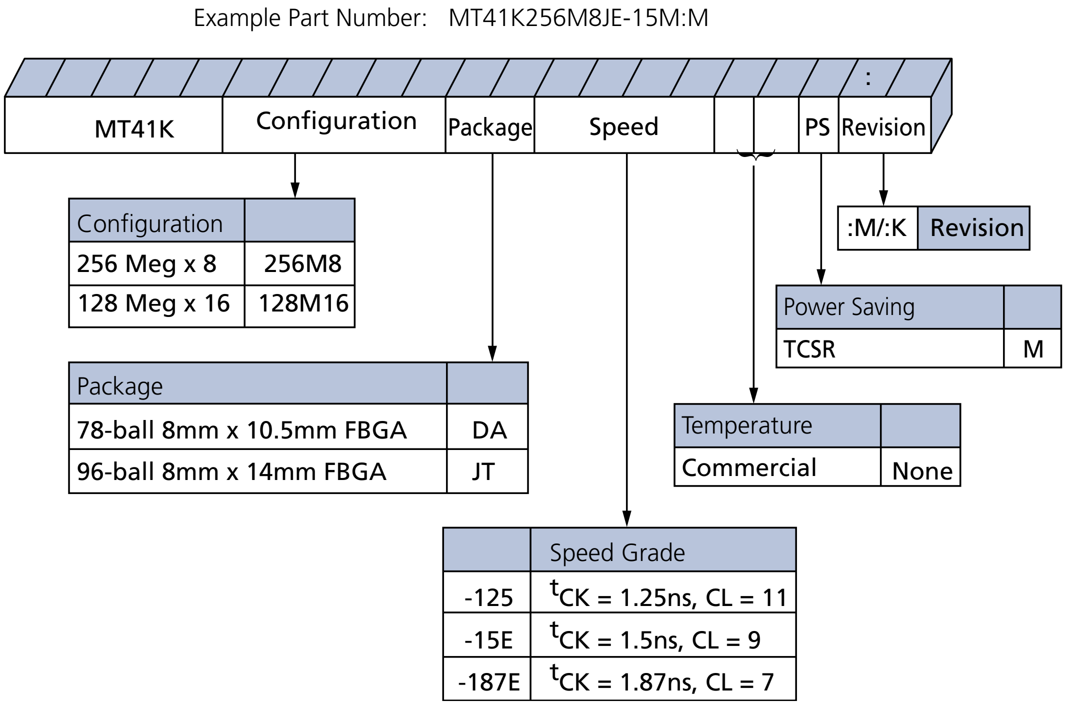
Speed Grade	Data Rate (MT/s)	Target ^tRCD-^tRP-CL	^tRCD (ns)	^tRP (ns)	CL (ns)
-187E	1066	7-7-7	13.1	13.1	13.1

Notes:
1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).

Table 2: Addressing

Parameter	256 Meg x 8	128 Meg x 16
Configuration	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K
Row address	32K A[14:0]	16K A[13:0]
Bank address	8 BA[2:0]	8 BA[2:0]
Column address	1K A[9:0]	1K A[9:0]

Figure 1: DDR3L-RS Part Numbers



Configuration	
256 Meg x 8	256M8
128 Meg x 16	128M16

Package	
78-ball 8mm x 10.5mm FBGA	DA
96-ball 8mm x 14mm FBGA	JT

	Speed Grade
-125	^{t}CK = 1.25ns, CL = 11
-15E	^{t}CK = 1.5ns, CL = 9
-187E	^{t}CK = 1.87ns, CL = 7

Temperature	
Commercial	None

Power Saving	
TCSR	M

:M/:K	Revision

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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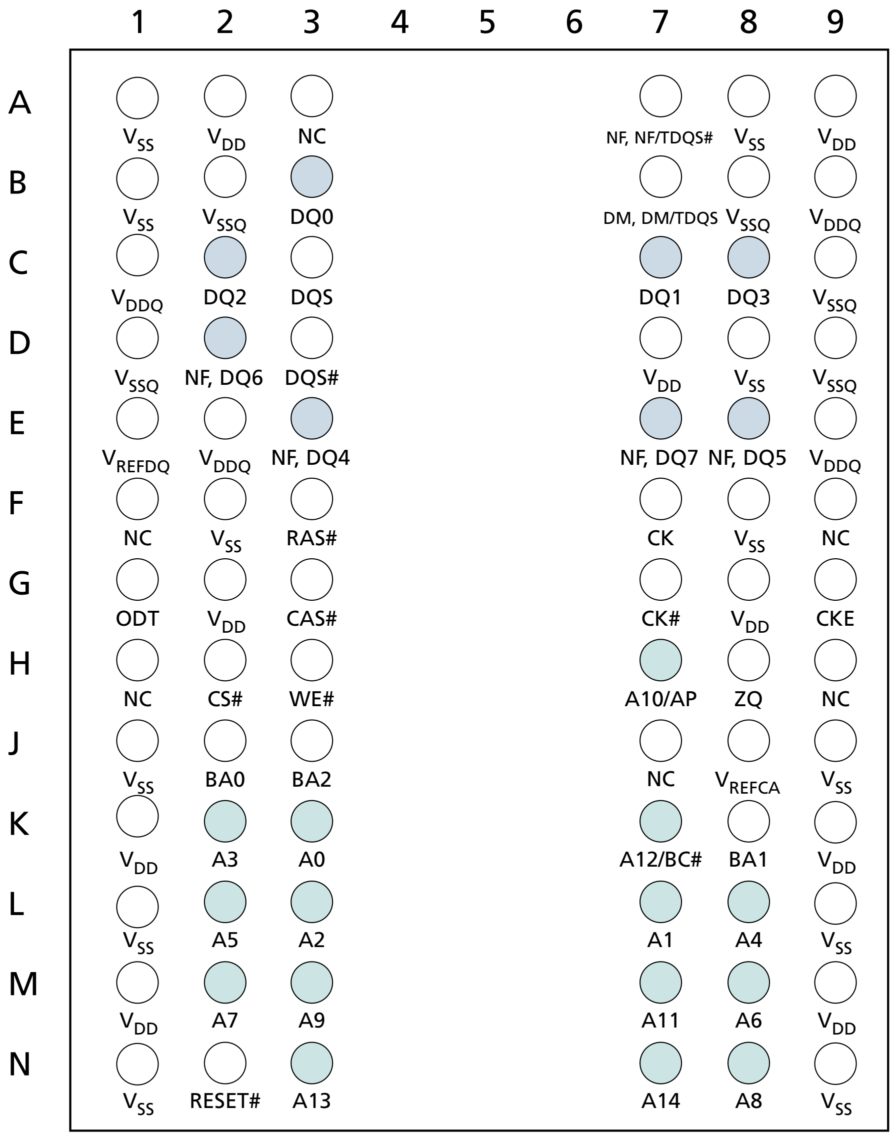
Ball Assignments and Descriptions

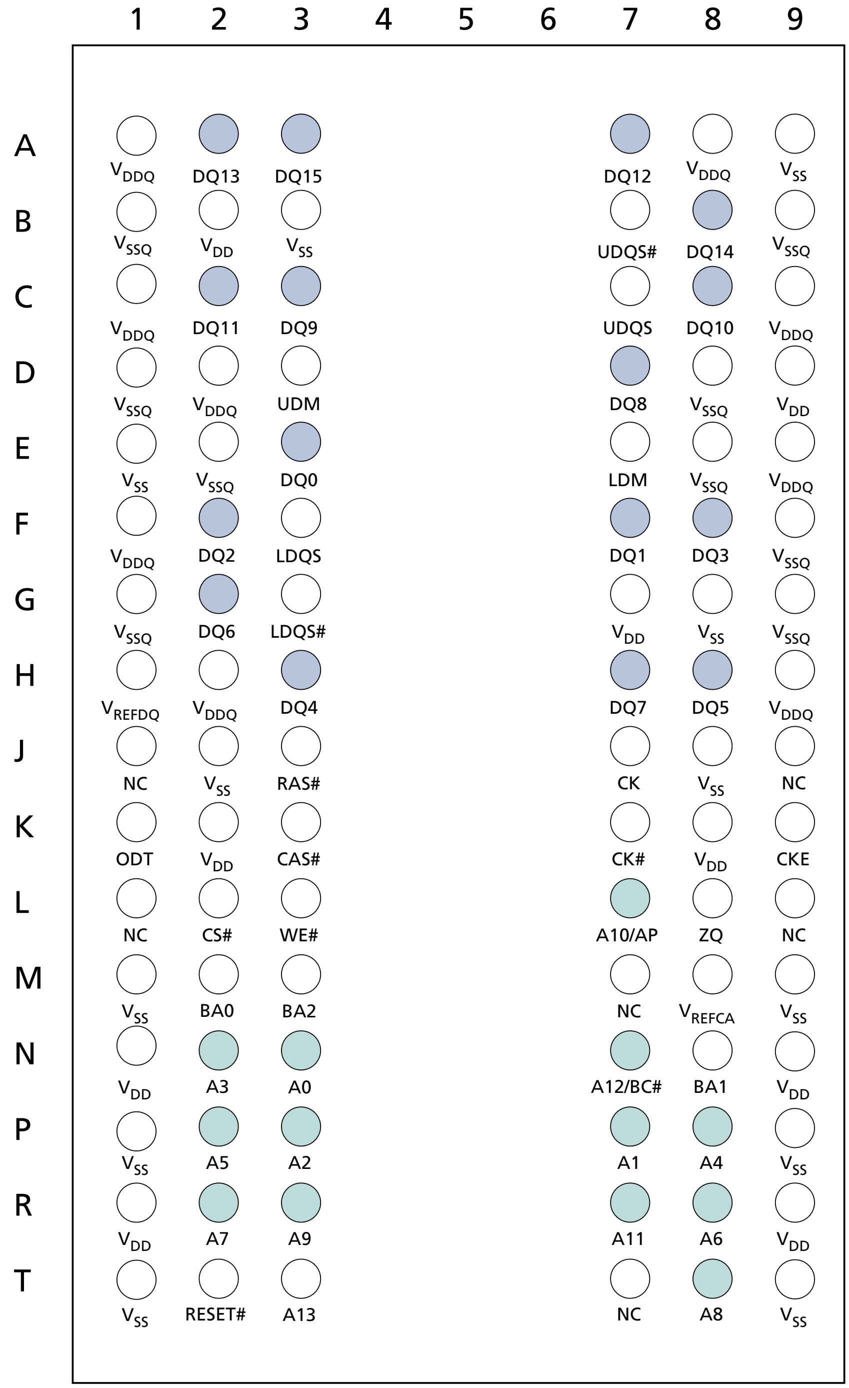
Figure 2: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)



	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DD}	NC				NF, NF/TDQS#	V_{SS}	V_{DD}
B	V_{SS}	V_{SSQ}	DQ0				DM, DM/TDQS	V_{SSQ}	V_{DDQ}
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}
D	V_{SSQ}	NF, DQ6	DQS#				V_{DD}	V_{SS}	V_{SSQ}
E	V_{REFDQ}	V_{DDQ}	NF, DQ4				NF, DQ7	NF, DQ5	V_{DDQ}
F	NC	V_{SS}	RAS#				CK	V_{SS}	NC
G	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}
K	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
L	V_{SS}	A5	A2				A1	A4	V_{SS}
M	V_{DD}	A7	A9				A11	A6	V_{DD}
N	V_{SS}	RESET#	A13				A14	A8	V_{SS}

Notes:
1. Ball descriptions listed in Table 3 (page 7) are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function. Example: D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

Figure 3: 96-Ball FBGA – x16 Ball Assignments (Top View)



	1	2	3	4	5	6	7	8	9
A	V_{DDQ}	DQ13	DQ15				DQ12	V_{DDQ}	V_{SS}
B	V_{SSQ}	V_{DD}	V_{SS}				UDQS#	DQ14	V_{SSQ}
C	V_{DDQ}	DQ11	DQ9				UDQS	DQ10	V_{DDQ}
D	V_{SSQ}	V_{DDQ}	UDM				DQ8	V_{SSQ}	V_{DD}
E	V_{SS}	V_{SSQ}	DQ0				LDM	V_{SSQ}	V_{DDQ}
F	V_{DDQ}	DQ2	LDQS				DQ1	DQ3	V_{SSQ}
G	V_{SSQ}	DQ6	LDQS#				V_{DD}	V_{SS}	V_{SSQ}
H	V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}
J	NC	V_{SS}	RAS#				CK	V_{SS}	NC
K	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
L	NC	CS#	WE#				A10/AP	ZQ	NC
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}
N	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
P	V_{SS}	A5	A2				A1	A4	V_{SS}
R	V_{DD}	A7	A9				A11	A6	V_{DD}
T	V_{SS}	RESET#	A13				NC	A8	V_{SS}

Notes:
1. Ball descriptions listed in Table 4 (page 9) are listed as "x16."
2. A comma separates the configuration; a slash defines a selectable function.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Truth Table - Command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8 device.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DDQ} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and deassertion are asynchronous.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ}.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	I/O	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (R_{ZQ}), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Table 4: 96-Ball FBGA – x16 Ball Descriptions

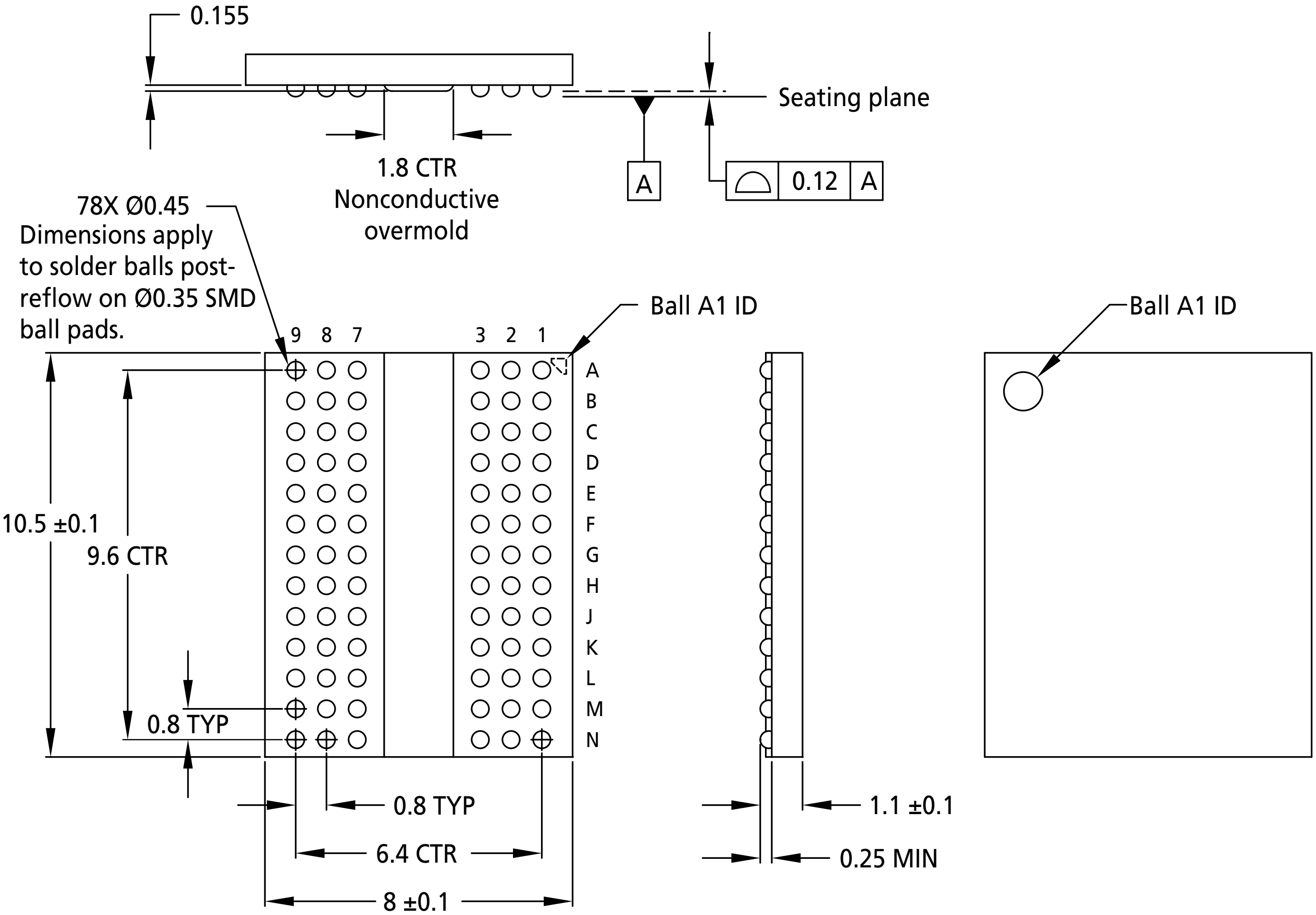
Symbol	Type	Description
A13, A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Truth Table - Command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (LDQS, LDQS#, UDQS, UDQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and LDQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DDQ} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and deassertion are asynchronous.

Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with the input data during a write access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and UDQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. LDQS is center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. UDQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (R_{ZQ}), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

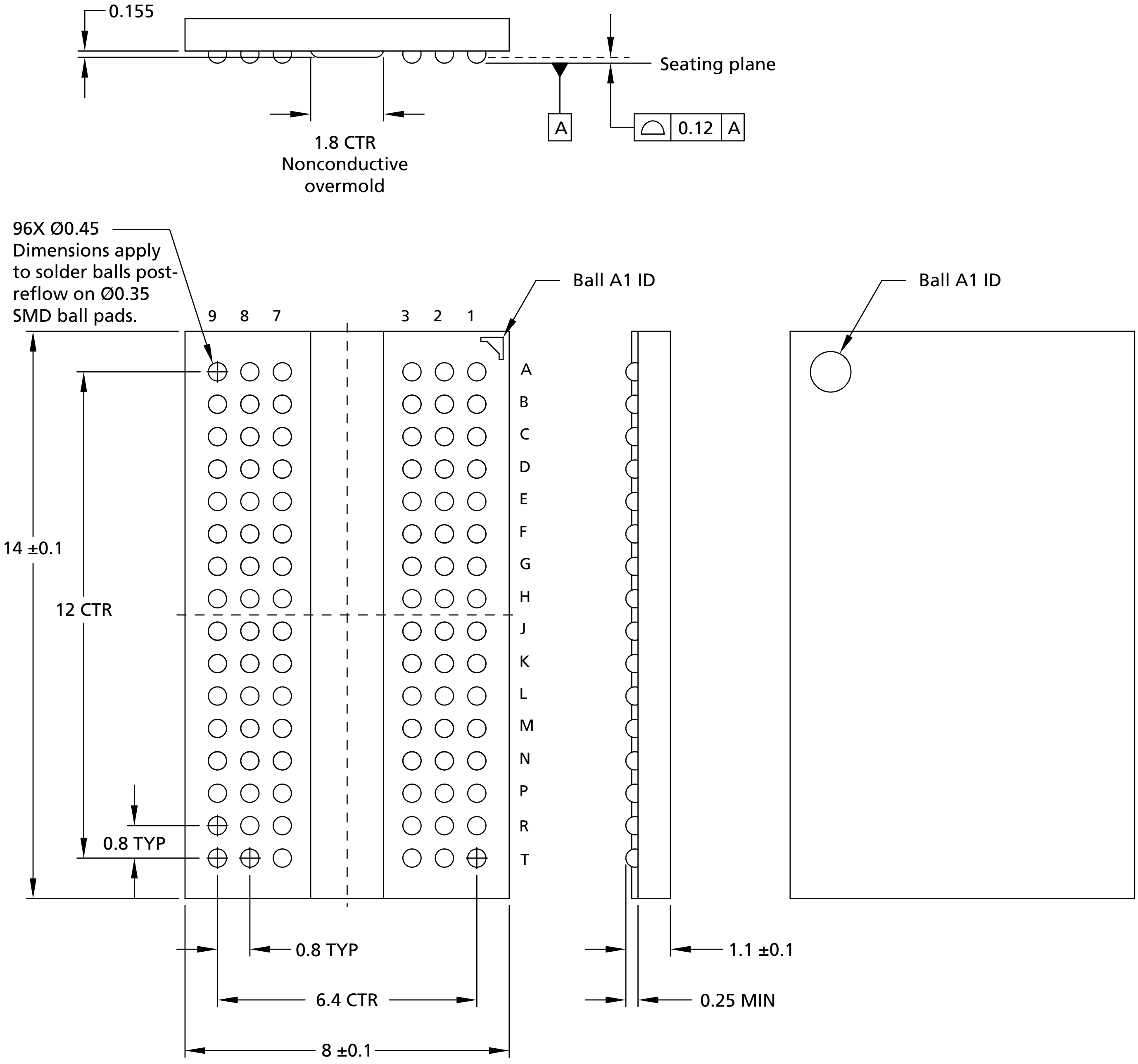
Package Dimensions

Figure 4: 78-Ball FBGA – x4, x8; Die Rev. M, K (DA)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 5: 96-Ball FBGA – x16; Die Rev. K (JT)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Electrical Characteristics – I_{DD} Specifications

Table 5: I_{DD} Maximum Limits – Die Rev. M

Speed Bin			DDR3L-RS -1066	DDR3L-RS -1333	DDR3L-RS -1600	Unit	Notes
Parameter	**Symbol**	**Width**					
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	x8	50	55	60	mA	1
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	x8	65	70	75	mA	1
Precharge power-down current: Slow exit	I_{DD2P0}	x8	8	8	12	mA	1
Precharge power-down current: Fast exit	I_{DD2P1}	x8	23	28	33	mA	1
Precharge quiet standby current	I_{DD2Q}	x8	23	28	33	mA	1
Precharge standby current	I_{DD2N}	x8	25	30	35	mA	1
Precharge standby ODT current	I_{DD2NT}	x8	30	35	40	mA	1
Active power-down current	I_{DD3P}	x8	37	42	47	mA	1
Active standby current	I_{DD3N}	x8	42	47	52	mA	1
Burst read operating current	I_{DD4R}	x8	110	125	140	mA	1
Burst write operating current	I_{DD4W}	x8	95	110	125	mA	1
Burst refresh current	I_{DD5B}	x8	180	185	190	mA	1
Room temperature self refresh	I_{DD6}	x8	2.8	2.8	2.8	mA	2
+45°C temperature self refresh	I_{DD6}	x8	3.0	3.0	3.0	mA	3
Elevated temperature self refresh	I_{DD6}	x8	5	5	5	mA	4
	I_{DD6}	x8	6	6	6	mA	5
Extended temperature self refresh	I_{DD6ET}	x8	8	8	8	mA	6
	I_{DD6ET}	x8	9	9	9	mA	7
All banks interleaved read current	I_{DD7}	x8	190	205	220	mA	1
Reset current	I_{DD8}	x8	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	mA	1

Notes:
1. T_C = +85°C; SRT is disabled, ASR is disabled. Value is maximum.
2. $T_C \leq$ Room Temperature; SRT is disabled, ASR is enabled. Value is typical.
3. $T_C \leq$ +45°C; SRT is disabled, ASR is enabled. Value is typical.
4. T_C = +80°C; SRT is disabled, ASR is enabled. Value is typical.
5. +45°C < $T_C \leq$ +80°C; SRT is disabled, ASR is enabled. Value is maximum.
6. T_C = +95°C; SRT is disabled, ASR is enabled. Value is typical.
7. +85°C < $T_C \leq$ +95°C; SRT is disabled, ASR is enabled. Value is maximum.

Table 6: I_{DD} Maximum Limits – Die Rev. K

Speed Bin			DDR3L-RS -1066	DDR3L-RS -1333	DDR3L-RS -1600	DDR3L-RS -1866	Unit	Notes
Parameter	**Symbol**	**Width**						
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	x8	32	34	35	36	mA	1
		x16	39	41	42	44	mA	1
Operating current 1: One bank ACTIVATE-to-READ-to-PRE-CHARGE	I_{DD1}	x8	41	45	47	49	mA	1
		x16	52	57	59	62	mA	1
Precharge power-down current: Slow exit	I_{DD2P0}	All	7	7	7	7	mA	1
Precharge power-down current: Fast exit	I_{DD2P1}	All	11	11	11	11	mA	1
Precharge quiet standby current	I_{DD2Q}	All	16	16	16	16	mA	1
Precharge standby current	I_{DD2N}	All	17	17	17	17	mA	1
Precharge standby ODT current	I_{DD2NT}	x8	21	24	26	28	mA	1
		x16	24	27	28	30	mA	1
Active power-down current	I_{DD3P}	All	19	19	19	19	mA	1
Active standby current	I_{DD3N}	x8	24	26	28	30	mA	1
		x16	24	26	28	30	mA	1
Burst read operating current	I_{DD4R}	x8	60	74	86	96	mA	1
		x16	78	98	118	138	mA	1
Burst write operating current	I_{DD4W}	x8	64	76	88	99	mA	1
		x16	87	107	126	144	mA	1
Burst refresh current	I_{DD5B}	All	175	177	178	180	mA	1
Room temperature self refresh	I_{DD6}	All	2.5	2.5	2.5	2.5	mA	2
+45°C temperature self refresh	I_{DD6}	All	2.7	2.7	2.7	2.7	mA	3
Elevated temperature self refresh	I_{DD6}	All	5	5	5	5	mA	4
		All	6	6	6	6	mA	5
Extended temperature self refresh	I_{DD6ET}	All	8	8	8	8	mA	6
		All	9	9	9	9	mA	7
All banks interleaved read current	I_{DD7}	x8	111	140	146	154	mA	1
		x16	142	162	185	209	mA	1
Reset current	I_{DD8}	all	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	mA	1

Notes:
1. T_C = +85°C; SRT is disabled, ASR is disabled. Value is maximum.
2. $T_C \leq$ Room Temperature; SRT is disabled, ASR is enabled. Value is typical.
3. $T_C \leq +45°C$; SRT is disabled, ASR is enabled. Value is typical.
4. T_C = +80°C; SRT is disabled, ASR is enabled. Value is typical.
5. $+45°C < T_C \leq +80°C$; SRT is disabled, ASR is enabled. Value is maximum.
6. T_C = +95°C; SRT is disabled, ASR is enabled. Value is typical.
7. $+85°C < T_C \leq +95°C$; SRT is disabled, ASR is enabled. Value is maximum.

Temperature-Compensated Self Refresh (TCSR)

The temperature-compensated self refresh (TCSR) feature substantially reduces the self refresh current (I_{DD6}). TCSR takes effect when T_C is less than 45°C and the auto self refresh (ASR) function is enabled. ASR is required to utilize the TCSR feature and is enabled manually via mode register 2 (MR2[6]). See Figure 6 (page 15).

Enabling ASR also automatically changes the DRAM self refresh rate from 1x to 2x when the case temperature exceeds 85°C. This allows the user to operate the DRAM beyond the standard 85°C limit, up to the optional extended temperature range of 95°C while in self refresh mode.

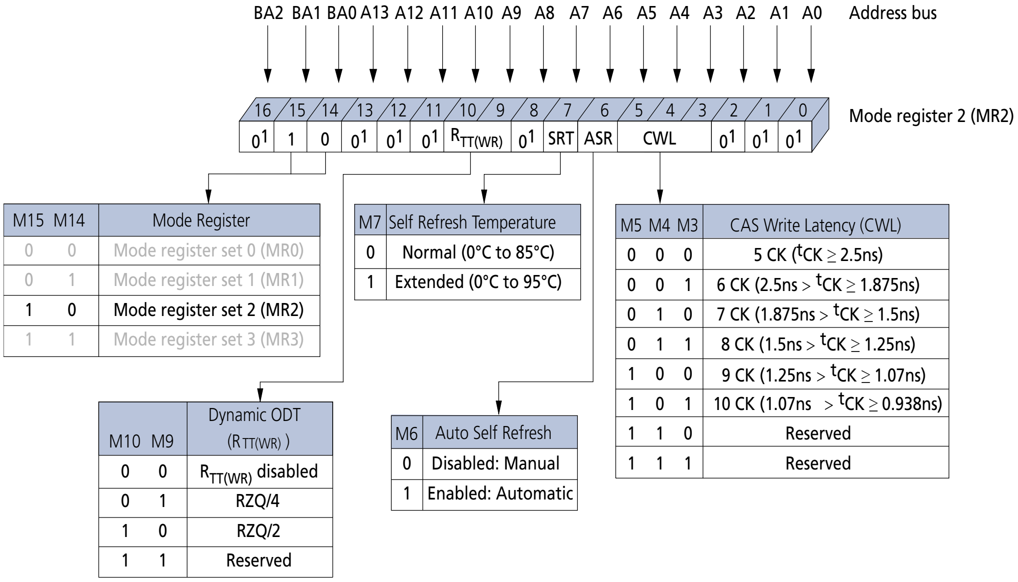
When ASR is disabled and T_C is 0°C to 85°C, the self refresh mode refresh rate is assumed to be at the normal rate (sometimes referred to as 1x refresh rate). Also, if ASR is disabled and T_C is 85°C to 95°C, the user must select the SRT extended temperature self refresh rate (sometimes referred to as 2x refresh rate). SRT is selected via mode register 2 (MR2[7]) register. See Figure 6 (page 15).

SPD settings should always support 05h (101 binary) in byte 31.

Mode Register 2 (MRS)

Mode register 2 (MR2) controls additional functions and features not available in the other mode registers. The ASR function is of particular interest for the DDR3L-RS SDRAM because the Micron DDR3L-RS SDRAM goes into TCSR mode when ASR has been enabled. This function is controlled via the bits shown in the figure below.

Figure 6: Mode Register 2 Definition



M15	M14	Mode Register
0	0	Mode register set 0 (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M7	Self Refresh Temperature
0	Normal (0°C to 85°C)
1	Extended (0°C to 95°C)

M5	M4	M3	CAS Write Latency (CWL)
0	0	0	5 CK (^{t}CK ≥ 2.5ns)
0	0	1	6 CK (2.5ns > ^{t}CK ≥ 1.875ns)
0	1	0	7 CK (1.875ns > ^{t}CK ≥ 1.5ns)
0	1	1	8 CK (1.5ns > ^{t}CK ≥ 1.25ns)
1	0	0	9 CK (1.25ns > ^{t}CK ≥ 1.07ns)
1	0	1	10 CK (1.07ns > ^{t}CK ≥ 0.938ns)
1	1	0	Reserved
1	1	1	Reserved

M10	M9	Dynamic ODT ($R_{TT(WR)}$)
0	0	$R_{TT(WR)}$ disabled
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

M6	Auto Self Refresh
0	Disabled: Manual
1	Enabled: Automatic

Note: 1. MR2[17, 14:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

Electrical Specifications

Table 7: Input/Output Capacitance

Capacitance Parameters	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-end I/O: DQ, DM	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Inputs (CTRL, CMD,ADDR)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF

Table 8: DC Electrical Characteristics and Operating Conditions – 1.35V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1, 2, 3, 4
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1, 2, 3, 4

Notes:
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (for example, 1 sec).
2. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specification.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see Figure 7 (page 29)).

Table 9: DC Electrical Characteristics and Operating Conditions – 1.5V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2, 3
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2, 3

Notes:
1. If the minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3L operation (see Figure 7 (page 29)).

Table 10: Input Switching Conditions – Command and Address

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}{}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}{}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC125)min}{}^1$	–	–	125	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}{}^1$	–	–	–125	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}{}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}{}^1$	–160	–160	–	mV

Note: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDRL-800, the address/command inputs must use either $V_{IH(AC160),min}$ with ^{t}IS(AC160) of 215ps or $V_{IH(AC135),min}$ with ^{t}IS(AC135) of 365ps; independently, the data inputs may use either $V_{IH(AC160),min}$ or $V_{IH(AC135),min}$.

Table 11: Input Switching Conditions – DQ and DM

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}{}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}{}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC130)min}{}^1$	–	–	130	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC130)min}{}^1$	–	–	–130	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}{}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}{}^1$	–160	–160	–	mV

Note: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDRL-800, the data inputs must use either $V_{IH(AC160),min}$ with ^{t}IS(AC160) of 90ps or $V_{IH(AC135),min}$ with ^{t}IS(AC135) of 140ps; independently, the address/command inputs may use either $V_{IH(AC160),min}$ or $V_{IH(AC135),min}$.

Table 12: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	–180	mV
Differential input logic high	$V_{IH,diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	V_{DD}/V_{DDQ}	mV
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	2 × ($V_{IL(AC)}$ - V_{REF})	mV
Single-ended high level for strobes	V_{SEH}	V_{DDQ}/2 + 160	V_{DDQ}	mV
Single-ended high level for CK, CK#		V_{DD}/2 + 160	V_{DD}	mV
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	V_{DDQ}/2 - 160	mV
Single-ended low level for CK, CK#		V_{SS}	V_{DD}/2 - 160	mV

Table 13: Minimum Required Time ^{t}DVAC for CK/CK#, DQS/DQS# Differential for AC Ringback

	DDR3L-800/1066/1333/1600		DDR3L-1866		
Slew Rate (V/ns)	^{t}DVAC at 320mV (ps)	^{t}DVAC at 270mV (ps)	^{t}DVAC at 270mV (ps)	^{t}DVAC at 250mV (ps)	^{t}DVAC at 260mV (ps)
>4.0	189	201	163	168	176
4.0	189	201	163	168	176
3.0	162	179	140	147	154
2.0	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	55
1.2	Note1	44	5	22	24
1.0	Note1	Note1	Note1	Note1	Note1
<1.0	Note1	Note1	Note1	Note1	Note1

Note: 1. Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.

Table 14: R_{TT} Effective Impedance

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	$R_{TT,120PD240}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/1
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/1
			$0.8 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/1
		$R_{TT,120PU240}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/1
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/1
			$0.8 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/1
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	$R_{TT,60PD120}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/2
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/2
			$0.8 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/2
		$R_{TT,60PU120}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/2
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/2
			$0.8 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/2
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	$R_{TT,40PD80}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/3
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/3
			$0.8 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/3
		$R_{TT,40PU80}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/3
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/3
			$0.8 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/3
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	$R_{TT,30PD60}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/4
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/4
			$0.8 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/4
		$R_{TT,30PU60}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/4
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/4
			$0.8 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/4
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/8
1, 0, 0	20Ω	$R_{TT,20PD40}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/6
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/6
			$0.8 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/6
		$R_{TT,20PU40}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/6
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/6
			$0.8 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/6
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/12

Table 15: Reference Settings for ODT Timing Measurements

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
^tAON	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tAOF	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tAONPD	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tAOFPD	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tADC	RZQ/12 (20Ω)	RZQ/2 (20Ω)	200mV	250mV

Table 16: 34Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max[1]	Units
0, 1	34.3Ω	$R_{ON,34PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/7
		$R_{ON,34PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 17: 40Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max[1]	Units
0, 0	40Ω	$R_{ON,40PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
		$R_{ON,40PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 18: Single-Ended Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	SRQ_{se}	1.75	6	V/ns

Table 19: Differential Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.18 \times V_{DDQ}$ and $V_{OH,diff(AC)} = 0.18 \times V_{DDQ}$	SRQ_{diff}	3.5	12	V/ns
Output differential crosspoint voltage	$V_{OX(AC)}$	V_{REF} - 135	V_{REF} + 135	mV

Table 20: Electrical Characteristics and AC Operating Conditions

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQ Input Timing													
Data setup time to DQS, DQS#	Base (specification)	^tDS (AC160)	90	–	40	–	N/A	–	N/A	–	N/A	–	ps
	V_{REF} @ 1 V/ns		250	–	200	–	N/A	–	N/A	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	^tDS (AC135)	140	–	90	–	45	–	25	–	N/A	–	ps
	V_{REF} @ 1 V/ns		275	–	225	–	180	–	160	–	N/A	–	ps
Data hold time from DQS, DQS#	Base (specification)	^tDH (DC90)	160	–	110	–	75	–	55	–	N/A	–	ps
	V_{REF} @ 1 V/ns		250	–	200	–	165	–	145	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	^tDS (AC130)	N/A	–	N/A	–	N/A	–	N/A	–	70	–	ps
	V_{REF} @ 2 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	135	–	ps
Data hold time from DQS, DQS#	Base (specification)	^tDH (DC90)	N/A	–	N/A	–	N/A	–	N/A	–	75	–	ps
	V_{REF} @ 2 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	110	–	ps
Command and Address Timing													
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^tIS (AC160)	215	–	140	–	80	–	60	–	N/A	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	N/A	–	ps

Table 20: Electrical Characteristics and AC Operating Conditions (Continued)

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^{t}IS (AC135)	365	–	290	–	205	–	185	–	65	–	ps
	V_{REF} @ 1 V/ns		500	–	425	–	340	–	320	–	200	–	ps
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^{t}IS (AC125)	N/A	–	N/A	–	N/A	–	N/A	–	150	–	ps
	V_{REF} @ 1 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	275	–	ps
CTRL, CMD, ADDR hold from CK, CK#	Base (specification)	^{t}IH (DC90)	285	–	210	–	150	–	130	–	110	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	200	–	ps

Notes:

1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

   For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC160),min}$ with ^{t}IS(AC160) of 215ps or $V_{IH(AC135),min}$ with ^{t}IS(AC135) of 365ps; independently, the data inputs must use either $V_{IH(AC160),min}$ with ^{t}DS(AC160) of 90ps or $V_{IH(AC135),min}$ with ^{t}DS(AC135) of 140ps.
2. When DQ single-ended slew rate is 1V/ns, the DQS differential slew rate is 2V/ns; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns;

Table 21: Derating Values for ^{t}IS/^{t}IH – AC160/DC90-Based

Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5

Table 22: Derating Values for ^{t}IS/^{t}IH – AC135/DC90-Based

CMD/ADDR Slew Rate V/ns	Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based															
	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–3	2	–3	2	–3	10	5	18	13	26	21	34	31	42	47
0.8	3	–8	3	–8	3	–8	11	1	19	9	27	17	35	27	43	43
0.7	6	–13	6	–13	6	–13	14	–5	22	3	30	11	38	21	46	37
0.6	9	–20	9	–20	9	–20	17	–12	25	–4	33	4	41	14	49	30
0.5	5	–30	5	–30	5	–30	13	–22	21	–14	29	–6	37	4	45	20
0.4	–3	–45	–3	–45	–3	–45	6	–37	14	–29	22	–21	30	–11	38	5

Table 23: Derating Values for ^{t}IS/^{t}IH – AC125/DC90-Based

CMD/ADDR Slew Rate V/ns	Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based															
	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	3	–3	3	–3	3	–3	11	5	19	13	27	21	35	31	43	47
0.8	6	–8	6	–8	6	–8	14	1	22	9	30	17	38	27	46	43
0.7	10	–13	10	–13	10	–13	18	–5	26	3	34	11	42	21	50	37
0.6	16	–20	16	–20	16	–20	24	–12	32	–4	40	4	48	14	56	30
0.5	15	–30	15	–30	15	–30	23	–22	31	–14	39	–6	47	4	55	20
0.4	13	–45	13	–45	13	–45	21	–37	29	–29	37	–21	45	–11	53	5

Table 24: Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866	
	^{t}VAC at 160mV (ps)	^{t}VAC at 135mV (ps)	^{t}VAC at 135mV (ps)	^{t}VAC at 125mV (ps)
>2.0	200	213	200	205
2.0	200	213	200	205
1.5	173	190	178	184
1.0	120	145	133	143
0.9	102	130	118	129
0.8	80	111	99	111
0.7	51	87	75	89
0.6	13	55	43	59
0.5	Note 1	10	Note 1	18
<0.5	Note 1	10	Note 1	18

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Table 25: Derating Values for ^{t}DS/^{t}DH – AC160/DC90-Based

Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–1	–3	–1	–3	7	5	15	13	23	21				
0.8					–3	–8	5	1	13	9	21	17	29	27		
0.7							–3	–5	11	3	19	11	27	21	35	37
0.6									8	–4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													–8	–11	0	5

Table 26: Derating Values for ^{t}DS/^{t}DH – AC135/DC90-Based

Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–3	2	–3	10	5	18	13	26	21				
0.8					3	–8	11	1	19	9	27	17	35	27		
0.7							14	–5	22	3	30	11	38	21	46	37
0.6									25	–4	33	4	41	14	49	30
0.5											39	–6	37	4	45	20
0.4													30	–11	38	5

Table 27: Derating Values for ^{t}DS/^{t}DH – AC130/DC100-Based at 2V/ns

Shaded cells indicate slew rate combinations not supported

DQ Slew Rate V/ns	Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based – DQS, DQS# Differential Slew Rate: 8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH
4.0	33	23	33	23	33	23																		
3.5	28	19	28	19	28	19	28	19																
3.0	22	15	22	15	22	15	22	15	22	15														
2.5			13	9	13	9	13	9	13	9	13	9												
2.0					0	0	0	0	0	0	0	0	0	0										
1.5							–22	–15	–22	–15	–22	–15	–22	–15	–14	–7								
1.0									–65	–45	–65	–45	–65	–45	–57	–37	–49	–29						
0.9											–62	–48	–62	–48	–54	–40	–46	–32	–38	–24				
0.8													–61	–53	–53	–45	–45	–37	–37	–29	–29	–19		
0.7															-49	–50	–41	-42	–33	–34	–25	–24	–17	-8
0.6																	–37	-49	–29	–41	–21	–31	–13	–15
0.5																			–31	–51	–23	–41	–15	–25
0.4																					–28	–56	–20	–40

Table 28: Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition

Slew Rate (V/ns)	^{t}VAC at 160mV (ps)	^{t}VAC at 135mV (ps)	^{t}VAC at 130mV (ps)
>2.0	165	113	95
2.0	165	113	95
1.5	138	90	73
1.0	85	45	30
0.9	67	30	16
0.8	45	11	Note1
0.7	16	Note1	–
0.6	Note1	Note1	–
0.5	Note1	Note1	–
<0.5	Note1	Note1	–

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Voltage Initialization/Change

If the SDRAM is powered up and initialized for the 1.35V operating voltage range, voltage can be increased to the 1.5V operating range provided the following conditions are met (See Figure 7 (page 29)):

- Just prior to increasing the 1.35V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.5V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.5V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. ^{t}ZQinit must be satisfied after the 1.5V operating voltages are stable and prior to any READ command.

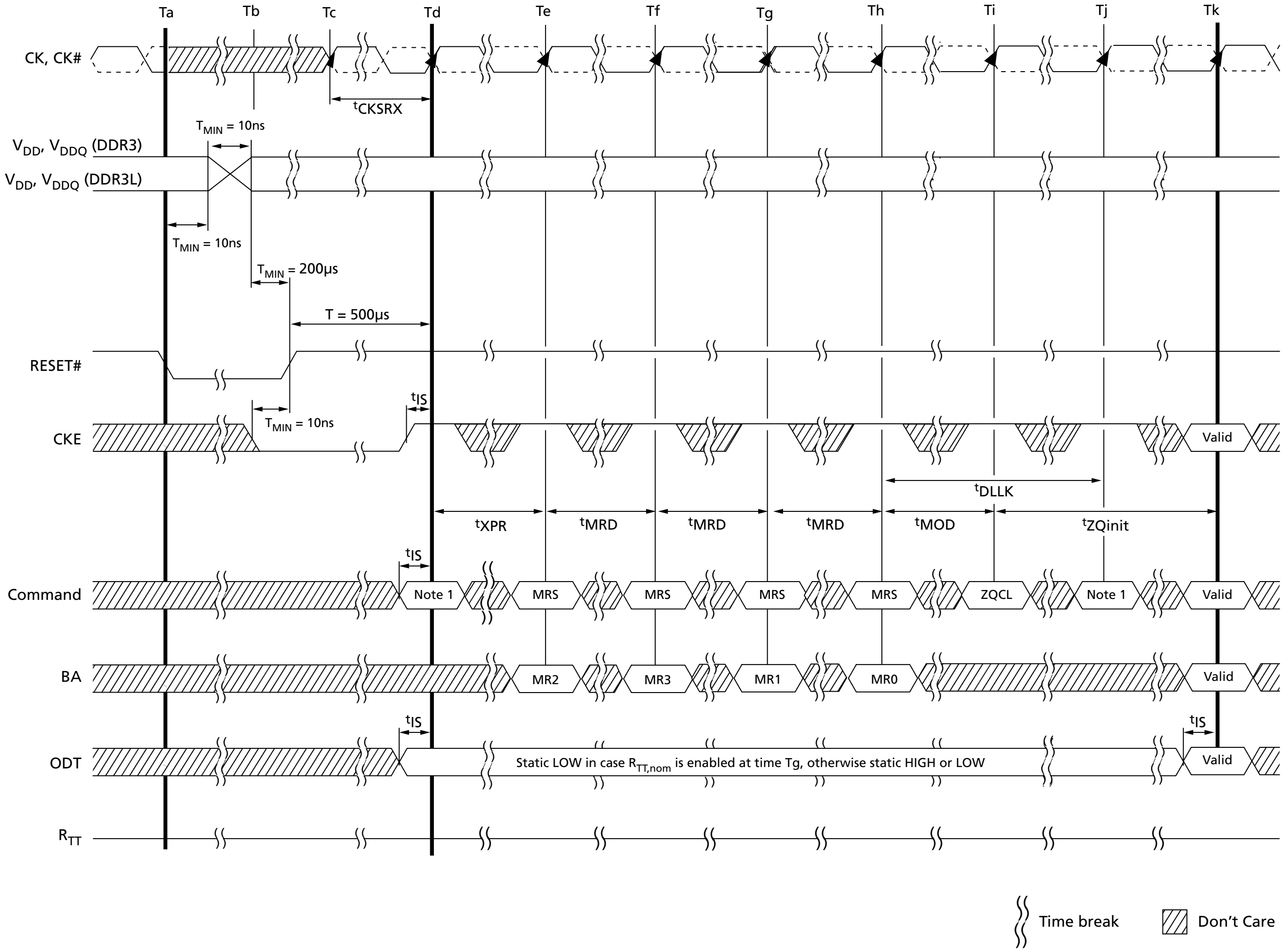
If the SDRAM is powered up and initialized for the 1.5V operating voltage range, voltage can be reduced to the 1.35V operation range provided the following conditions are met (See Figure 7 (page 29)) :

- Just prior to reducing the 1.5V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.35V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.35V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. ^{t}ZQinit must be satisfied after the 1.35V operating voltages are stable and prior to any READ command.

V_{DD} Voltage Switching

After the DDR3L DRAM is powered up and initialized, the power supply can be altered between the DDR3L and DDR3 levels, provided the sequence in Figure 7 is maintained.

Figure 7: V_{DD} Voltage Switching



Note: 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.