Product Change Notification / SYST-18TZLF179

Date:

24-Aug-2020

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18F27/47/57Q43 Silicon Errata and Datasheet Clarifications

Affected CPNs:

SYST-18TZLF179_Affected_CPN_08242020.pdf
SYST-18TZLF179_Affected_CPN_08242020.csv

Notification Text:

SYST-18TZLF179

Microchip has released a new Product Documents for the PIC18F27/47/57Q43 Silicon Errata and Datasheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18F27/47/57Q43 Silicon Errata and Datasheet Clarifications.

Notification Status: Final

Description of Change: Adding silicon revision B2.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Aug 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18F27/47/57Q43 Silicon Errata and Datasheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F27Q43-E/ML
PIC18F27Q43-E/SO
PIC18F27Q43-E/SP
PIC18F27Q43-E/SS
PIC18F27Q43-E/STX
PIC18F27Q43-I/ML
PIC18F27Q43-I/SO
PIC18F27Q43-I/SP
PIC18F27Q43-I/SS
PIC18F27Q43-I/STX
PIC18F27Q43T-I/ML
PIC18F27Q43T-I/SO
PIC18F27Q43T-I/SS
PIC18F27Q43T-I/STX
PIC18F47Q43-E/ML
PIC18F47Q43-E/MP
PIC18F47Q43-E/P
PIC18F47Q43-E/PT
PIC18F47Q43-I/ML
PIC18F47Q43-I/MP
PIC18F47Q43-I/P
PIC18F47Q43-I/PT
PIC18F47Q43T-I/ML
PIC18F47Q43T-I/MP
PIC18F47Q43T-I/PT
PIC18F57Q43-E/6LX
PIC18F57Q43-E/PT
PIC18F57Q43-I/6LX
PIC18F57Q43-I/PT
PIC18F57Q43T-I/6LX
PIC18F57Q43T-I/PT

PIC18F27/47/57Q43

PIC18F27/47/57Q43 Silicon Errata and Data Sheet Clarifications

The PIC18F27/47/57Q43 devices you have received conform functionally to the current device data sheet (DS40002147D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q43 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		B0	B2
PIC18F27Q43	0x7480	0xA040	0xA042
PIC18F47Q43	0x74A0	0xA040	0xA042
PIC18F57Q43	0x74C0	0xA040	0xA042

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ43 Family Programming Specification"** (DS40002079) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				B0	B2
ADCC	Capacitive Voltage Divider	1.1.1	CVD is only functional on PORTA[2:0] and PORTB[4:0]	X	
Oscillator	XT mode	1.2.1	Maximum clock frequency limited to 2 MHz for XT mode	X	X
I^2C	I^2C	1.3.1	I2CxADR0/1/2/3 registers have incorrect Reset value	X	X
SRAM	SRAM Read-Back	1.4.1	SRAM read-back can be incorrect	X	

Note: Only those issues indicated in the last column apply to the current silicon revision.

Table of Contents

1. Silicon Errata Issues

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Capacitive Voltage Divider (CVD)

The CVD feature is only functional on PORTA[2:0] and PORTB[4:0]. This feature is not recommended for use on any other pins.

Work around

None.

Affected Silicon Revisions

B0	B2
X	

1.2 Module: Oscillator

1.2.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

B0	B2
X	X

1.3 Module: I^2C

1.3.1 I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/1/2/3 registers reset to 0xFF when the I2CxMD is enabled instead of 0x00.

Work around

None.

Affected Silicon Revisions

B0	B2
X	X

1.4 Module: SRAM

1.4.1 SRAM Read-Back

Following a device power-up sequence, there is a possibility that some SRAM locations will not return the expected written value but will read back '00' instead.

Work around

None. The device can only recover by power cycling.

This erroneous condition can be detected by running the following code that writes non-zero values to SRAM and then verifies that the returned read values are not '00'. If a returned value is '00', the application code has to be put into a safe state until a POR event occurs. This code has to be executed immediately after power-up. If the test passes, the device operation will be normal.

```
// SRAM test

FSR0 = 0xcff;         // Write data into RAM address for devices up to 2K RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 2K of SRAM, add the following code
FSR0 = 0x14ff;        // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 4K of SRAM, add the following code
FSR0 = 0x24ff;        // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to Safe state
}
```

Affected Silicon Revisions

B0	B2
X	

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002147D):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
F	08/2020	Adding silicon revision B2.
E	06/2020	Adding silicon erratum item 1.4.1.
D	06/2020	Adding silicon erratum item 1.3.1.
C	04/2020	Adding XT mode erratum and Temperature Indicator data sheet clarification.
B	02/2020	Add working pins for CVD.
A	12/2019	Initial document release.

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