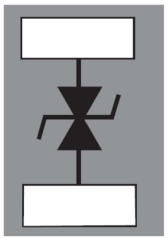
ESDZX051-1BF4

Datasheet

10 V ultra-low clamping single line high speed bidirectional ESD protection

0201 package



Product status link
ESDZX051-1BF4

Features

- Ultra-low clamping voltage: 10 V TLP at 16 A I_{pp}
- Bidirectional protection diode
- Very high bandwidth: 24 GHz
- Very low dynamic resistance: 0.5 Ω
- Suitable for RF antenna application with very low harmonic:
  - H3 < -50 dBm at 20 dBm power:
    - 710 MHz, 824 MHz and 2.4 GHz
- ST0201 package
- ECOPACK2 compliant component
- Exceeds IEC 61000-4-2 level 4:
  - ±12 kV (contact discharge)
  - ±20 kV (air discharge)

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- USB 3.2 Gen 1 and Gen 2
- RF antenna
- Ethernet 1000 BASE-T
- Ethernet 10G BASE-T
- Display port
- LVDS

Description

The ESDZX051-1BF4 is a bidirectional single line TVS diode designed to protect the data lines or other I/O ESD transients. Thanks to extra low capacitance, ESDZX051-1BF4 can protect high speed differential lines with no impact on signal integrity.

With an extremely low clamping voltage, ESDZX051-1BF4 is able to protect the most sensitive, submicron technology circuits.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	±12 ±20	kV
P_{pp}	Peak pulse power (8/20 µs)		20	W
I_{pp}	Peak pulse current (8/20 µs)		4	A
T_j	Operating junction temperature range		-55 to 150	°C
T_{stg}	Storage junction temperature range		-65 to 150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics (definitions)

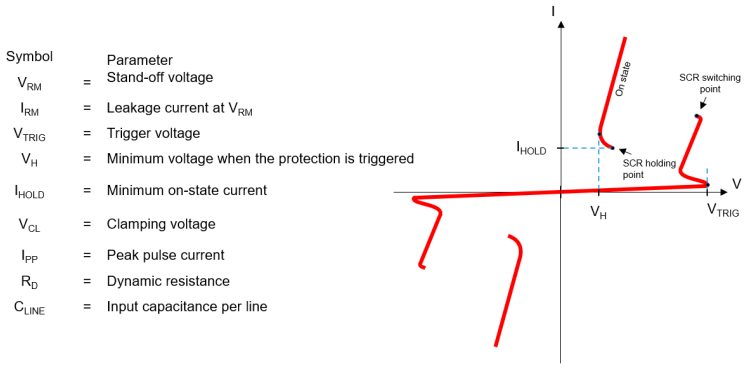


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{TRIG}	Maximum off-state voltage				9.6	10.5	V
V_H	Lower voltage than V_H guarantees the protection turn-off			1.4	1.7		V
I_{HOLD}	Minimum on-state current				35		mA
V_{RM}	Reverse working voltage					3.6	V
I_{RM}	Leakage current	V_{RM} = 3.6 V				100	nA
V_{CL}	Clamping voltage	I_{pp} = 4 A - 8/20µs			4	5	V
		8 kV contact discharge after 30 ns, IEC 61000-4-2			11		V
		TLP measurement (pulse duration 100 ns)	I_{PP} = 16 A		10		V
			I_{PP} = 4 A		4		
R_D	Dynamic resistance, TLP pulse duration 100 ns (from 4 A to 16 A I_{pp})				0.5		Ω
f_C	Cut-off frequency		-3dB		24		GHz
C_{LINE}	Line capacitance	V_{LINE} = 0 V, F = 3 GHz			0.28	0.35	pF
		V_{LINE} = 0 V, F = 10 GHz			0.25	0.33	

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature (typical values)

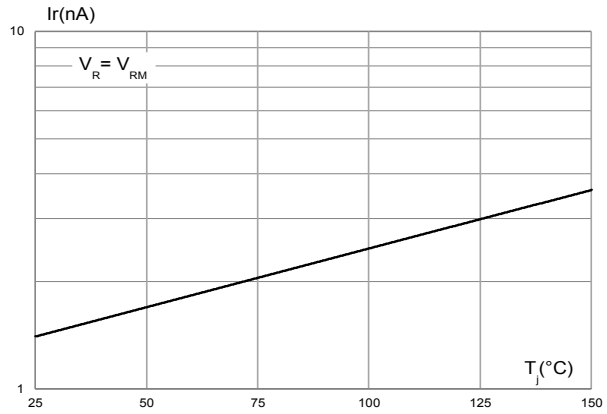
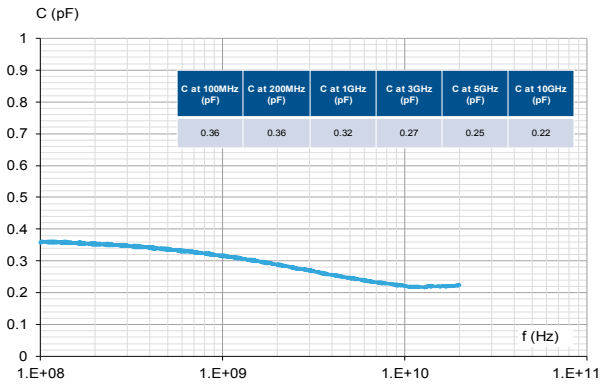


Figure 3. Junction capacitance versus frequency (typical values)



C at 100MHz (pF)	C at 200MHz (pF)	C at 1GHz (pF)	C at 3GHz (pF)	C at 5GHz (pF)	C at 10GHz (pF)
0.36	0.36	0.32	0.27	0.25	0.22

Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

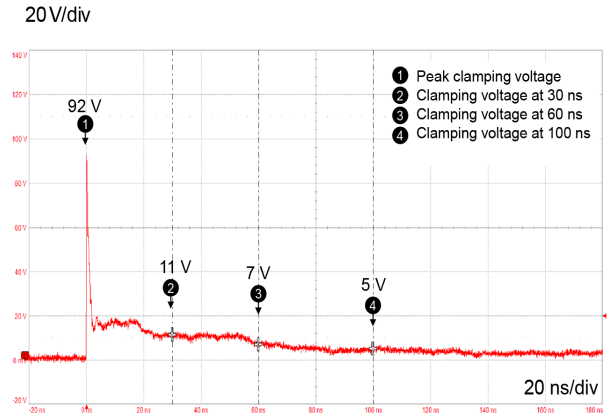


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

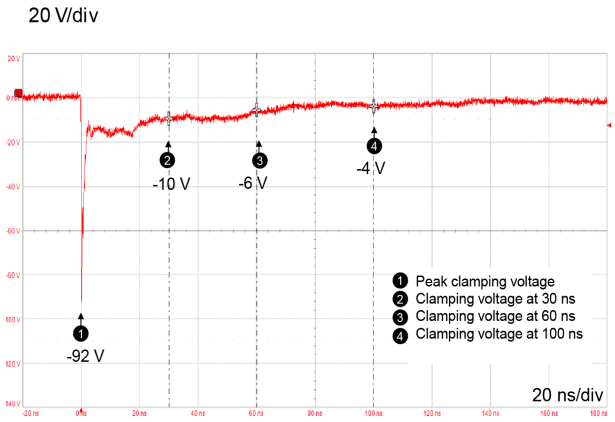


Figure 6. S21 attenuation measurement results

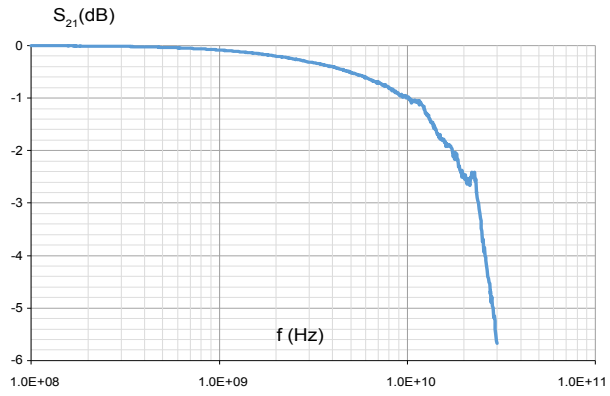


Figure 7. TLP measurement

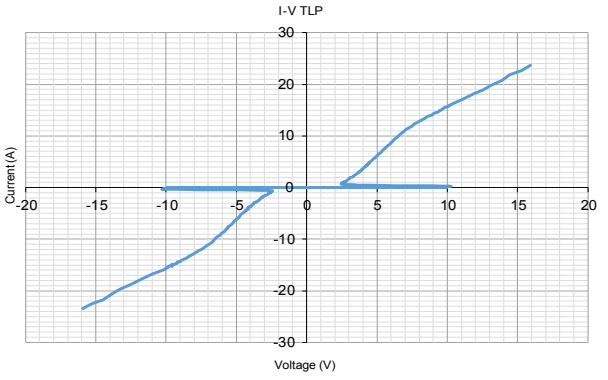


Figure 8. Harmonic measurement at 710 MHz : H2

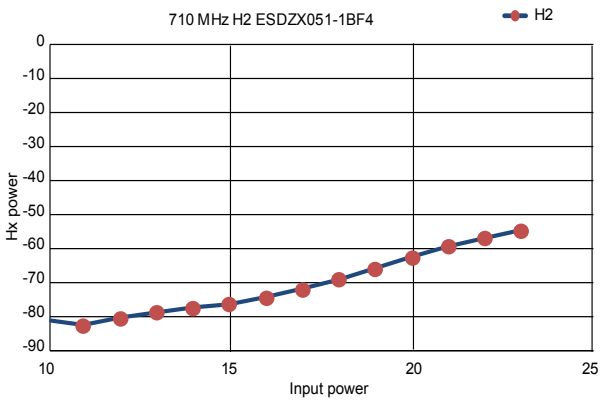


Figure 9. Harmonic measurement at 710 MHz : H3

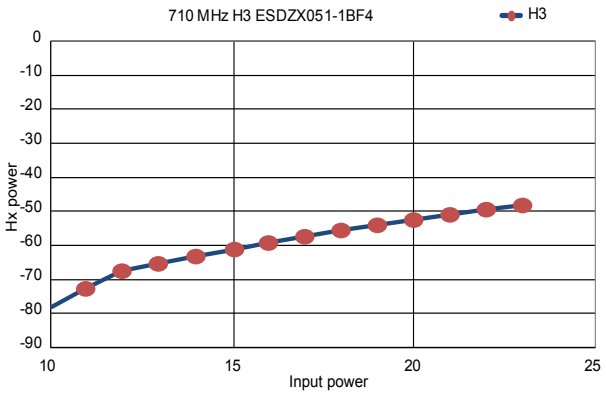


Figure 10. Harmonic measurement at 824 MHz : H2

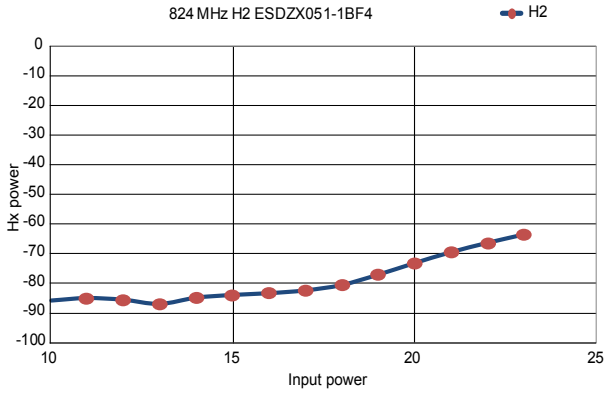


Figure 11. Harmonic measurement at 824 MHz : H3

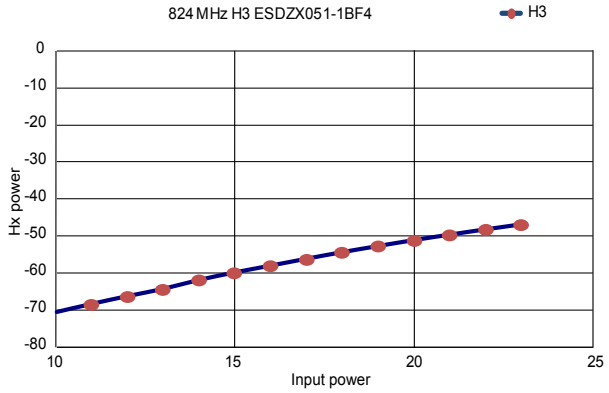


Figure 12. Harmonic measurement at 2.4 GHz : H2

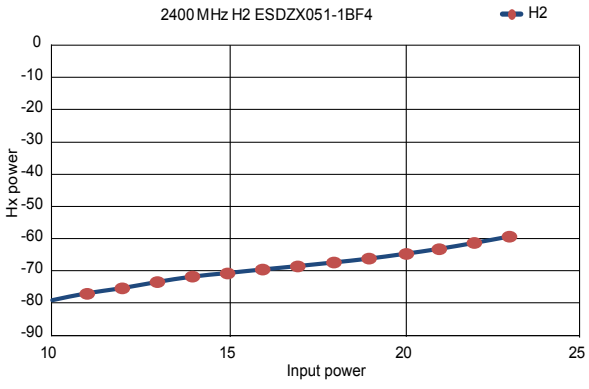
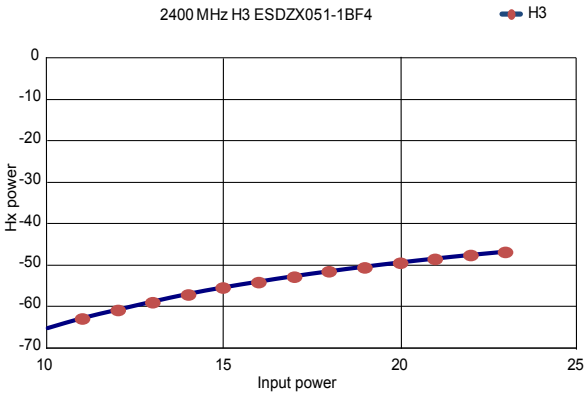


Figure 13. Harmonic measurement at 2.4 GHz : H3



2 Application information

2.1 Latch-up consideration

There is a potential risk of latch-up using SCR based ESD protection if the working voltage V_{RM} is higher than V_H voltage.

To ensure a latch-up free state, the current injected in the protection must be lower than the holding current I_{HOLD} when the voltage across the protection device is equal to V_{HOLD}. The following equation gives the latch-up free condition.

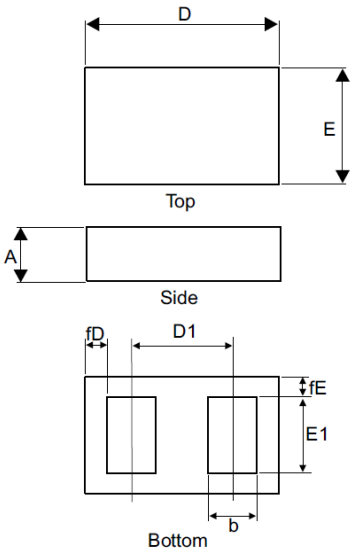
$$I_{HOLD} > \frac{V_{SOURCE\max} - V_{HOLD}}{R_{SOURCE\min}}$$

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 ST0201 package information

Figure 14. ST0201 package outline

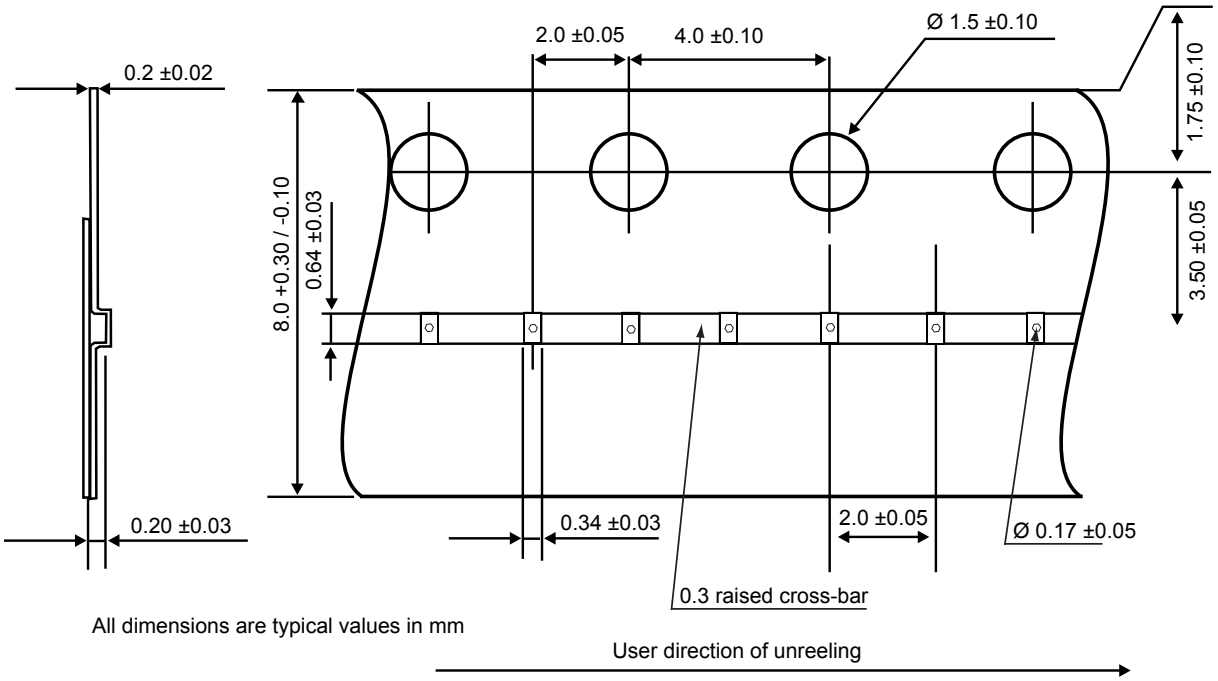


Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Table 3. 0201 package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.130	0.150	0.170
b	0.1675	0.1875	0.2075
D	0.560	0.580	0.600
D1		0.3375	
E	0.260	0.280	0.300
E1	0.205	0.225	0.245
fD		0.0275	
fE		0.0275	

Figure 15. Tape and reel specification (in mm)

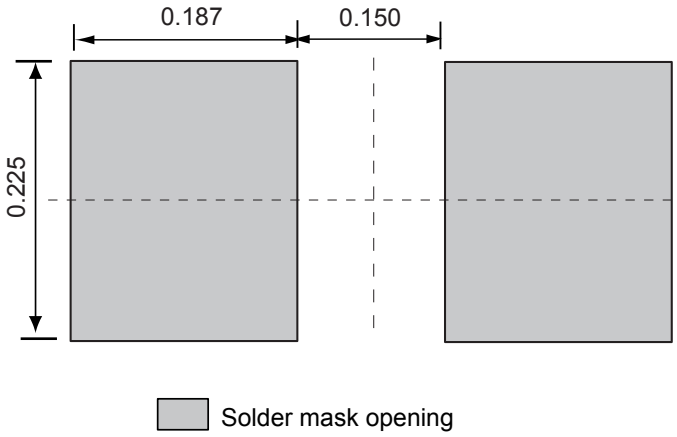


4 Recommendation on PCB assembly

4.1 Footprint

1. SMD footprint design is recommended

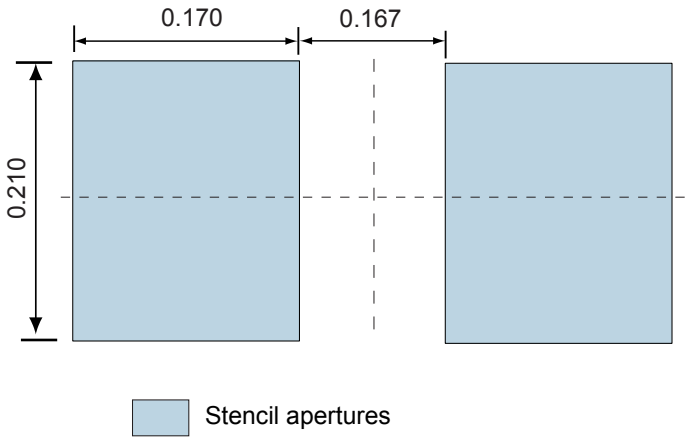
Figure 16. Footprint in mm



4.2 Stencil opening design

1. Recommended design reference
   a. Stencil opening dimensions: 75 µm / 3 mils
   b. Stencil aperture ratio : 100%

Figure 17. Stencil opening recommendations



4.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

4.4 Placement

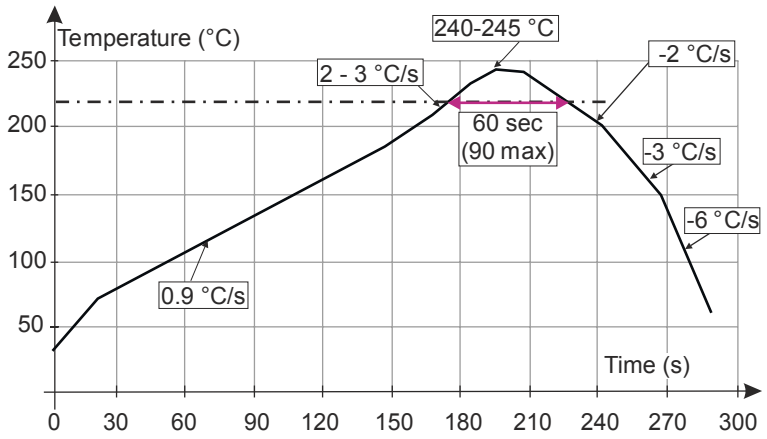
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

4.6 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 19. **Ordering information scheme**

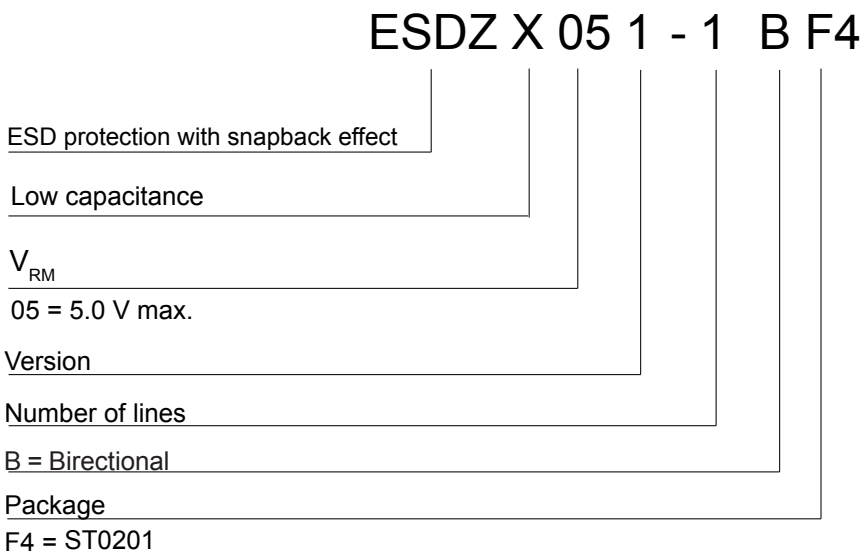


Table 4. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
ESDZX051-1BF4	N	ST0201	0.116 mg	15000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assemble location.*

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
27-Jan-2020	1	First issue.
30-Mar-2020	2	Updated Table 2.

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