



## Product Change Notification - SYST-17AIFA028

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**Date:**

23 Jun 2020

**Product Category:**

16-Bit - Microcontrollers and Digital Signal Controllers

**Affected CPNs:****Notification subject:**

ERRATA - dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X Errata

**Notification text:**

SYST-17AIFA028

Microchip has released a new Product Documents for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X Errata of devices. If you are using one of these devices please read the document located at [dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X Errata](#).

**Notification Status:** Final

**Description of Change:**

- 1) Updated all Affected Families and Silicon Revision tables to a new format
- 2) Removed silicon issue 29 (JTAG) since it no longer applies.
- 3) Removed all data sheet clarifications because the issues were corrected in the latest data sheet revision.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 23 Jun 2020

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachment(s):**

[dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X Errata](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33EP512GP502-E/MM  
DSPIC33EP512MC202-E/MM  
DSPIC33EP512MC502-E/MM  
DSPIC33EP512GP502-E/SP  
DSPIC33EP512MC202-E/SP  
DSPIC33EP512MC502-E/SP  
DSPIC33EP512MC502-E/SO  
DSPIC33EP512GP506-E/MR  
DSPIC33EP512MC206-E/MR  
DSPIC33EP512MC506-E/MR  
DSPIC33EP512GP504-E/MV  
DSPIC33EP512MC204-E/MV  
DSPIC33EP512MC504-E/MV  
DSPIC33EP512GP504-E/ML  
DSPIC33EP512MC204-E/ML  
DSPIC33EP512MC504-E/ML  
DSPIC33EP512GP504-E/PT  
DSPIC33EP512MC504-E/PT  
DSPIC33EP512GP506-E/PT  
DSPIC33EP512MC206-E/PT  
DSPIC33EP512MC506-E/PT  
DSPIC33EP512GP506-E/PTVAO  
DSPIC33EP512GP502-I/MM  
DSPIC33EP512MC202-I/MM  
DSPIC33EP512MC502-I/MM  
DSPIC33EP512GP502-I/SP  
DSPIC33EP512MC202-I/SP  
DSPIC33EP512MC502-I/SP  
DSPIC33EP512GP502-I/SO  
DSPIC33EP512MC202-I/SO  
DSPIC33EP512MC502-I/SO  
DSPIC33EP512GP506-I/MR  
DSPIC33EP512MC206-I/MR  
DSPIC33EP512MC506-I/MR  
DSPIC33EP512GP504-I/MV  
DSPIC33EP512MC204-I/MV  
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DSPIC33EP512MC204-I/ML  
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DSPIC33EP512MC204-I/PT  
DSPIC33EP512MC504-I/PT  
DSPIC33EP512GP506-I/PT  
DSPIC33EP512MC206-I/PT  
DSPIC33EP512MC506-I/PT

DSPIC33EP512GP504T-H/TL  
DSPIC33EP512MC204T-H/TL  
DSPIC33EP512MC504T-H/TL  
DSPIC33EP512GP502T-H/MM  
DSPIC33EP512MC202T-H/MM  
DSPIC33EP512MC502T-H/MM  
DSPIC33EP512GP506T-H/MR  
DSPIC33EP512MC206T-H/MR  
DSPIC33EP512MC506T-H/MR  
DSPIC33EP512GP504T-H/MV  
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DSPIC33EP512GP502T-I/MM  
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DSPIC33EP512GP506T-I/MR  
DSPIC33EP512MC206T-I/MR  
DSPIC33EP512MC506T-I/MR

DSPIC33EP512GP504T-I/MV  
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DSPIC33EP512MC504T-I/MV  
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DSPIC33EP512GP502T-E/MM  
DSPIC33EP512MC502T-E/MM  
DSPIC33EP512GP506T-E/MR  
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DSPIC33EP512MC506T-E/MR  
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DSPIC33EP512MC504T-E/ML  
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DSPIC33EP64MC202-E/SP  
DSPIC33EP64MC502-E/SP  
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DSPIC33EP64GP503-E/M5  
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DSPIC33EP64GP504-E/PT  
DSPIC33EP64MC204-E/PT  
DSPIC33EP64MC504-E/PT  
DSPIC33EP64MC204-E/PTV02  
DSPIC33EP64MC504-E/PTVAO  
DSPIC33EP64MC204-E/PTVAO  
DSPIC33EP64GP506-E/PT  
DSPIC33EP64MC206-E/PT  
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DSPIC33EP64MC503-I/TL  
DSPIC33EP64GP502-I/MM  
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DSPIC33EP64GP502-I/SO  
DSPIC33EP64MC202-I/SO  
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DSPIC33EP64MC504-I/PT  
DSPIC33EP64GP504-I/PTVAO

DSPIC33EP64MC206-I/PTA3  
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DSPIC33EP64MC506-I/PT  
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DSPIC33EP64MC502-H/SP  
DSPIC33EP64MC202-H/SSV11  
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DSPIC33EP64MC506-H/MR  
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DSPIC33EP64MC504-H/ML  
DSPIC33EP64MC204-H/MLVAO  
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DSPIC33EP64MC204-H/PTV01  
DSPIC33EP64MC204-H/PTV09  
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DSPIC33EP64MC502T-I/MM  
DSPIC33EP64GP502T-I/SS  
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DSPIC33EP64GP502T-E/MM  
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DSPIC33EP64MC502T-E/MM  
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DSPIC33EP64MC202T-E/SSC05  
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DSPIC33EP64MC502T-E/SO  
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DSPIC33EP64MC206T-E/MR

DSPIC33EP64MC506T-E/MR  
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DSPIC33EP64MC504T-E/MV  
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DSPIC33EP64MC504T-E/ML  
DSPIC33EP64MC204T-E/MLVAO  
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DSPIC33EP64MC504T-E/PT  
DSPIC33EP64MC204T-E/PTV02  
DSPIC33EP64MC504T-E/PTVAO  
DSPIC33EP64MC204T-E/PTVAO  
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DSPIC33EP64MC506T-E/PT  
DSPIC33EP64MC206T-E/PTV08  
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DSPIC33EP128MC504-E/TL  
DSPIC33EP128MC202-E/MM  
DSPIC33EP128GP502-E/MMVAO  
DSPIC33EP128GP502-E/SS  
DSPIC33EP128MC502-E/SS  
DSPIC33EP128MC202-E/SO  
DSPIC33EP128GP506-E/MR  
DSPIC33EP128MC206-E/MR  
DSPIC33EP128MC506-E/MR  
DSPIC33EP128GP504-E/MV  
DSPIC33EP128MC204-E/MV  
DSPIC33EP128MC504-E/MV  
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DSPIC33EP128MC504-E/PT  
DSPIC33EP128GP504-E/PTVAO  
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DSPIC33EP128MC506-E/PT  
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DSPIC33EP128MC502-I/SO  
DSPIC33EP128GP506-I/MRA3  
DSPIC33EP128MC206-I/MRA3  
DSPIC33EP128MC506-I/MRA3  
DSPIC33EP128GP506-I/MR  
DSPIC33EP128MC206-I/MR  
DSPIC33EP128MC506-I/MR  
DSPIC33EP128GP504-I/MV  
DSPIC33EP128MC204-I/MV  
DSPIC33EP128MC504-I/MV  
DSPIC33EP128GP504-I/ML  
DSPIC33EP128MC204-I/ML  
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DSPIC33EP128GP504-I/PT  
DSPIC33EP128MC204-I/PT  
DSPIC33EP128MC504-I/PT  
DSPIC33EP128MC206-I/PTA3  
DSPIC33EP128GP506-I/PT  
DSPIC33EP128MC206-I/PT  
DSPIC33EP128MC506-I/PT  
DSPIC33EP128MC206T-H/MR  
DSPIC33EP128MC206T-H/MRV10  
DSPIC33EP128MC206T-H/MRVAO  
DSPIC33EP128MC506T-H/MRVAO  
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DSPIC33EP128MC204T-H/MV  
DSPIC33EP128MC504T-H/MV  
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DSPIC33EP128MC204T-H/MLV11  
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DSPIC33EP128MC504-H/PTVAO  
DSPIC33EP128GP506-H/PT  
DSPIC33EP128MC206-H/PT  
DSPIC33EP128MC506-H/PT  
DSPIC33EP128MC204T-I/TL  
DSPIC33EP128MC504T-I/TL  
DSPIC33EP128GP502T-I/MM  
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DSPIC33EP128GP502T-I/MMV09  
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DSPIC33EP128MC204T-I/MV  
DSPIC33EP128MC504T-I/MV  
DSPIC33EP128GP504T-I/ML  
DSPIC33EP128MC204T-I/ML  
DSPIC33EP128MC504T-I/ML  
DSPIC33EP128MC204T-I/PTA3  
DSPIC33EP128MC204T-I/PT  
DSPIC33EP128MC206T-I/PTA3  
DSPIC33EP128GP506T-I/PT  
DSPIC33EP128MC206T-I/PT  
DSPIC33EP128MC506T-I/PT  
DSPIC33EP128MC502T-E/MM  
DSPIC33EP128MC202T-E/MM  
DSPIC33EP128MC202T-E/MMVAO  
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DSPIC33EP128GP506T-E/PTV03  
DSPIC33EP128GP506T-E/PTV06  
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DSPIC33EP256GP502-E/MM  
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DSPIC33EP256MC502-E/MM  
DSPIC33EP256GP502-E/MMVAO  
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DSPIC33EP256MC202-E/SP  
DSPIC33EP256MC502-E/SP  
DSPIC33EP256GP502-E/SS  
DSPIC33EP256MC202-E/SS  
DSPIC33EP256MC502-E/SS  
DSPIC33EP256GP502-E/SO  
DSPIC33EP256MC202-E/SO  
DSPIC33EP256MC502-E/SO  
DSPIC33EP256GP506-E/MR  
DSPIC33EP256MC206-E/MR  
DSPIC33EP256MC506-E/MR  
DSPIC33EP256MC206-E/MRRA3  
DSPIC33EP256GP504-E/MV  
DSPIC33EP256MC204-E/MV  
DSPIC33EP256MC504-E/MV  
DSPIC33EP256GP504-E/ML  
DSPIC33EP256MC204-E/ML  
DSPIC33EP256MC504-E/ML  
DSPIC33EP256GP504-E/PT  
DSPIC33EP256MC204-E/PT  
DSPIC33EP256MC504-E/PTVAO  
DSPIC33EP256MC206-E/PT  
DSPIC33EP256MC506-E/PT  
DSPIC33EP256GP506-E/PTV02  
DSPIC33EP256GP506-E/PTV07  
DSPIC33EP256MC206-E/PTVAO  
DSPIC33EP256MC506-E/PTVAO  
DSPIC33EP256GP504-I/TL  
DSPIC33EP256MC204-I/TL  
DSPIC33EP256MC504-I/TL  
DSPIC33EP256GP502-I/MM  
DSPIC33EP256MC202-I/MM  
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PIC24EP256GP202T-I/MMV05

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PIC24EP256MC202T-I/SS  
PIC24EP256GP202T-I/SO  
PIC24EP256MC202T-I/SO  
PIC24EP256GP206T-I/MR  
PIC24EP256MC206T-I/MR  
PIC24EP256GP204T-I/MV  
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PIC24EP256MC204T-I/ML  
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PIC24EP256GP206T-I/PTV06  
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PIC24EP256MC202T-E/SS  
PIC24EP256GP202T-E/SO  
PIC24EP256MC202T-E/SO  
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PIC24EP256MC204T-E/MV  
PIC24EP256GP204T-E/ML  
PIC24EP256MC204T-E/ML  
PIC24EP256GP204T-E/PTVAO  
PIC24EP256GP206T-E/PT  
PIC24EP32MC202-E/MM021  
PIC24EP32GP202-E/MM  
PIC24EP32MC202-E/MM  
PIC24EP32GP202-E/SP  
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PIC24EP32GP202-E/SO  
PIC24EP32MC202-E/SO  
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PIC24EP32MC204-E/MV  
PIC24EP32GP203-E/M5  
PIC24EP32MC203-E/M5  
PIC24EP32GP204-E/ML  
PIC24EP32MC204-E/ML  
PIC24EP32GP204-E/PT  
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PIC24EP32MC202-I/MM  
PIC24EP32GP202-I/SP  
PIC24EP32MC202-I/SP

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PIC24EP32MC202-I/SO  
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PIC24EP32MC204-I/MV  
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PIC24EP32GP204-H/MV  
PIC24EP32MC204-H/MV  
PIC24EP32GP203-H/M5  
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PIC24EP32MC204-H/ML  
PIC24EP32GP204-H/PT  
PIC24EP32MC204-H/PT  
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PIC24EP32GP202T-I/SS  
PIC24EP32GP202T-I/SO  
PIC24EP32GP204T-I/MV  
PIC24EP32MC204T-I/MV  
PIC24EP32GP204T-I/ML  
PIC24EP32MC204T-I/ML  
PIC24EP32GP204T-I/PT  
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PIC24EP32GP202T-E/MM  
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PIC24EP32GP202T-E/SO  
PIC24EP32GP204T-E/MV  
PIC24EP32MC204T-E/MV  
PIC24EP32GP204T-E/ML  
PIC24EP32MC204T-E/ML  
PIC24EP32GP204T-E/PT



SYST-17AIFA028 - ERRATA - dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND  
PIC24EPXXXGP/MC20X Errata

Affected Catalog Part Numbers(CPN)

DSPIC33EP512GP502-E/MM  
DSPIC33EP512MC202-E/MM  
DSPIC33EP512MC502-E/MM  
DSPIC33EP512GP502-E/SP  
DSPIC33EP512MC202-E/SP  
DSPIC33EP512MC502-E/SP  
DSPIC33EP512MC502-E/SO  
DSPIC33EP512GP506-E/MR  
DSPIC33EP512MC206-E/MR  
DSPIC33EP512MC506-E/MR  
DSPIC33EP512GP504-E/MV  
DSPIC33EP512MC204-E/MV  
DSPIC33EP512MC504-E/MV  
DSPIC33EP512GP504-E/ML  
DSPIC33EP512MC204-E/ML  
DSPIC33EP512MC504-E/ML  
DSPIC33EP512GP504-E/PT  
DSPIC33EP512MC504-E/PT  
DSPIC33EP512GP506-E/PT  
DSPIC33EP512MC206-E/PT  
DSPIC33EP512MC506-E/PT  
DSPIC33EP512GP506-E/PTVAO  
DSPIC33EP512GP502-I/MM  
DSPIC33EP512MC202-I/MM  
DSPIC33EP512MC502-I/MM  
DSPIC33EP512GP502-I/SP  
DSPIC33EP512MC202-I/SP  
DSPIC33EP512MC502-I/SP  
DSPIC33EP512GP502-I/SO  
DSPIC33EP512MC202-I/SO  
DSPIC33EP512MC502-I/SO  
DSPIC33EP512GP506-I/MR  
DSPIC33EP512MC206-I/MR  
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DSPIC33EP512GP504T-H/TL  
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DSPIC33EP512MC202T-H/MM  
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DSPIC33EP512MC206-H/PT  
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DSPIC33EP512GP502T-I/SO  
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DSPIC33EP512MC506T-I/MR  
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DSPIC33EP512MC204T-I/MV  
DSPIC33EP512MC504T-I/MV  
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DSPIC33EP512MC504T-E/ML  
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DSPIC33EP64MC506-E/MR  
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DSPIC33EP64MC504-E/PT  
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DSPIC33EP64MC504-E/PTVAO  
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DSPIC33EP128MC202-E/MM  
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DSPIC33EP128MC502-E/SS  
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DSPIC33EP128MC206T-I/PTA3  
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PIC24EP128GP206T-I/PTV08  
PIC24EP128GP206T-I/PTVAO  
PIC24EP128GP202T-E/SS  
PIC24EP128GP204T-E/MV  
PIC24EP128MC204T-E/MV  
PIC24EP128GP204T-E/PTVAO  
PIC24EP256GP204-E/TL  
PIC24EP256GP202-E/MM  
PIC24EP256MC202-E/MM  
PIC24EP256GP202-E/SP  
PIC24EP256MC202-E/SP  
PIC24EP256GP202-E/SS  
PIC24EP256MC202-E/SS  
PIC24EP256GP202-E/SO  
PIC24EP256MC202-E/SO  
PIC24EP256GP206-E/MR  
PIC24EP256GP204-E/MV  
PIC24EP256MC204-E/MV  
PIC24EP256GP204-E/ML  
PIC24EP256MC204-E/ML  
PIC24EP256GP204-E/PT  
PIC24EP256MC204-E/PT  
PIC24EP256GP204-E/PTVAO  
PIC24EP256GP206-E/PT  
PIC24EP256GP204-I/TL  
PIC24EP256MC204-I/TL  
PIC24EP256GP202-I/MM

PIC24EP256MC202-I/MM  
PIC24EP256GP202-I/SP  
PIC24EP256MC202-I/SP  
PIC24EP256GP202-I/SS  
PIC24EP256MC202-I/SS  
PIC24EP256GP202-I/SO  
PIC24EP256MC202-I/SO  
PIC24EP256GP206-I/MR  
PIC24EP256MC206-I/MR  
PIC24EP256GP204-I/MV  
PIC24EP256MC204-I/MV  
PIC24EP256GP204-I/ML  
PIC24EP256MC204-I/ML  
PIC24EP256GP204-I/PT  
PIC24EP256MC204-I/PT  
PIC24EP256GP206-I/PT  
PIC24EP256MC206-I/PT  
PIC24EP256GP202T-H/MM  
PIC24EP256MC202T-H/MM  
PIC24EP256GP202T-H/SS  
PIC24EP256MC202T-H/SS  
PIC24EP256GP202T-H/SO  
PIC24EP256MC202T-H/SO  
PIC24EP256GP204T-H/MV  
PIC24EP256MC204T-H/MV  
PIC24EP256GP204T-H/ML  
PIC24EP256MC204T-H/ML  
PIC24EP256GP204T-H/PT  
PIC24EP256MC204T-H/PT  
PIC24EP256GP202-H/MM  
PIC24EP256MC202-H/MM  
PIC24EP256GP202-H/SP  
PIC24EP256MC202-H/SP  
PIC24EP256GP202-H/SS  
PIC24EP256MC202-H/SS  
PIC24EP256GP202-H/SO  
PIC24EP256MC202-H/SO  
PIC24EP256GP204-H/MV  
PIC24EP256MC204-H/MV  
PIC24EP256GP204-H/ML  
PIC24EP256MC204-H/ML  
PIC24EP256GP202T-I/MM  
PIC24EP256MC202T-I/MM  
PIC24EP256GP202T-I/MMV01  
PIC24EP256GP202T-I/MMV05  
PIC24EP256GP202T-I/SS  
PIC24EP256MC202T-I/SS

PIC24EP256GP202T-I/SO  
PIC24EP256MC202T-I/SO  
PIC24EP256GP206T-I/MR  
PIC24EP256MC206T-I/MR  
PIC24EP256GP204T-I/MV  
PIC24EP256MC204T-I/MV  
PIC24EP256GP204T-I/ML029  
PIC24EP256GP204T-I/ML  
PIC24EP256MC204T-I/ML  
PIC24EP256GP204T-I/PT  
PIC24EP256MC204T-I/PT  
PIC24EP256GP206T-I/PT  
PIC24EP256MC206T-I/PT  
PIC24EP256GP206T-I/PTV03  
PIC24EP256GP206T-I/PTV06  
PIC24EP256GP202T-E/MM  
PIC24EP256MC202T-E/MM  
PIC24EP256GP202T-E/SS  
PIC24EP256MC202T-E/SS  
PIC24EP256GP202T-E/SO  
PIC24EP256MC202T-E/SO  
PIC24EP256GP204T-E/MV  
PIC24EP256MC204T-E/MV  
PIC24EP256GP204T-E/ML  
PIC24EP256MC204T-E/ML  
PIC24EP256GP204T-E/PTVAO  
PIC24EP256GP206T-E/PT  
PIC24EP32MC202-E/MM021  
PIC24EP32GP202-E/MM  
PIC24EP32MC202-E/MM  
PIC24EP32GP202-E/SP  
PIC24EP32MC202-E/SP  
PIC24EP32GP202-E/SS  
PIC24EP32MC202-E/SS  
PIC24EP32GP202-E/SO  
PIC24EP32MC202-E/SO  
PIC24EP32GP204-E/MV  
PIC24EP32MC204-E/MV  
PIC24EP32GP203-E/M5  
PIC24EP32MC203-E/M5  
PIC24EP32GP204-E/ML  
PIC24EP32MC204-E/ML  
PIC24EP32GP204-E/PT  
PIC24EP32GP202-I/MM  
PIC24EP32MC202-I/MM  
PIC24EP32GP202-I/SP  
PIC24EP32MC202-I/SP

PIC24EP32GP202-I/SS  
PIC24EP32MC202-I/SS  
PIC24EP32GP202-I/SO  
PIC24EP32MC202-I/SO  
PIC24EP32GP204-I/MV  
PIC24EP32MC204-I/MV  
PIC24EP32GP203-I/M5  
PIC24EP32MC203-I/M5  
PIC24EP32GP204-I/ML  
PIC24EP32MC204-I/ML  
PIC24EP32GP204-I/PT  
PIC24EP32MC204-I/PT  
PIC24EP32GP204T-H/MV  
PIC24EP32MC204T-H/MV  
PIC24EP32GP204T-H/ML  
PIC24EP32MC204T-H/ML  
PIC24EP32GP204T-H/PT  
PIC24EP32MC204T-H/PT  
PIC24EP32GP204-H/MV  
PIC24EP32MC204-H/MV  
PIC24EP32GP203-H/M5  
PIC24EP32MC203-H/M5  
PIC24EP32GP204-H/ML  
PIC24EP32MC204-H/ML  
PIC24EP32GP204-H/PT  
PIC24EP32MC204-H/PT  
PIC24EP32GP202T-I/MM  
PIC24EP32GP202T-I/SS  
PIC24EP32GP202T-I/SO  
PIC24EP32GP204T-I/MV  
PIC24EP32MC204T-I/MV  
PIC24EP32GP204T-I/ML  
PIC24EP32MC204T-I/ML  
PIC24EP32GP204T-I/PT  
PIC24EP32MC202T-E/MM021  
PIC24EP32GP202T-E/MM  
PIC24EP32GP202T-E/SS  
PIC24EP32MC202T-E/SS  
PIC24EP32GP202T-E/SO  
PIC24EP32GP204T-E/MV  
PIC24EP32MC204T-E/MV  
PIC24EP32GP204T-E/ML  
PIC24EP32MC204T-E/ML  
PIC24EP32GP204T-E/PT





# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Family Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family devices that you have received conform functionally to the current Device Data Sheet (DS70000657J), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X silicon.

**Note:** This document summarizes all silicon errata issues from the revisions of silicon, previous as well as current. The released silicon revision levels are:

dsPIC33/PIC24EP32	A3, A8
dsPIC33/PIC24EP64	A2, A3, A8
dsPIC33/PIC24EP128	A3, A8
dsPIC33/PIC24EP256	A3, A8, A9
dsPIC33/PIC24EP512	A7

**Note:** The current silicon revision levels are identified by shaded columns:

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64					
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512					

Data Sheet clarifications and corrections start on [Page 27](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website ([www.microchip.com](http://www.microchip.com)).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICKIT™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICKIT 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various silicon revisions are shown in [Table 1](#).

**TABLE 1: SILICON DEVREV VALUES**

Part Number	Device ID <sup>(1)</sup>	Silicon Revision/Device ID <sup>(2)</sup>			
PIC24EP32GP202	0x1C19	—	A3 0x4003	A8 0x4008	—
PIC24EP32GP203	0x1C1A				
PIC24EP32GP204	0x1C18				
dsPIC33EP32GP502	0x1C0D				
dsPIC33EP32GP503	0x1C0E				
dsPIC33EP32GP504	0x1C0C				
PIC24EP32MC202	0x1C11				
PIC24EP32MC203	0x1C12				
PIC24EP32MC204	0x1C10				
dsPIC33EP32MC202	0x1C01				
dsPIC33EP32MC203	0x1C02				
dsPIC33EP32MC204	0x1C00				
dsPIC33EP32MC502	0x1C05				
dsPIC33EP32MC503	0x1C06				
dsPIC33EP32MC504	0x1C04				
dsPIC33EP32MC506	0x1D27				
PIC24EP64GP202	0x1D39				
PIC24EP64GP203	0x1D3A				
PIC24EP64GP204	0x1D38				
PIC24EP64GP206	0x1D3B				
dsPIC33EP64GP502	0x1D2D				
dsPIC33EP64GP503	0x1D2E				
dsPIC33EP64GP504	0x1D2C				
dsPIC33EP64GP506	0x1D2F				
PIC24EP64MC202	0x1D31				
PIC24EP64MC203	0x1D32				
PIC24EP64MC204	0x1D30				
PIC24EP64MC206	0x1D33				
dsPIC33EP64MC202	0x1D21				
dsPIC33EP64MC203	0x1D22				
dsPIC33EP64MC204	0x1D20				
dsPIC33EP64MC206	0x1D23				
dsPIC33EP64MC502	0x1D25				
dsPIC33EP64MC503	0x1D26				
dsPIC33EP64MC504	0x1D24				
dsPIC33EP64MC506	0x1D27				

**Note 1:** The Device and Revision IDs (DEVVID and DEVREV) are located at the last two implemented addresses in program memory.

**2:** Refer to the “dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits” (DS70663) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID <sup>(1)</sup>	Silicon Revision/Device ID <sup>(2)</sup>			
PIC24EP128GP202	0x1E59	—	A3 0x4003	A8 0x4008	—
PIC24EP128GP204	0x1E58				
PIC24EP128GP206	0x1E5B				
dsPIC33EP128GP502	0x1E4D				
dsPIC33EP128GP504	0x1E4C				
dsPIC33EP128GP506	0x1E4F				
PIC24EP128MC202	0x1E51				
PIC24EP128MC204	0x1E50				
PIC24EP128MC206	0x1E53				
dsPIC33EP128MC202	0x1E41				
dsPIC33EP128MC204	0x1E40				
dsPIC33EP128MC206	0x1E43				
dsPIC33EP128MC502	0x1E45				
dsPIC33EP128MC504	0x1E44				
dsPIC33EP128MC506	0x1E47				
PIC24EP256GP202	0x1F79				
PIC24EP256GP204	0x1F78				
PIC24EP256GP206	0x1F7B				
dsPIC33EP256GP502	0x1F6D				
dsPIC33EP256GP504	0x1F6C				
dsPIC33EP256GP506	0x1F6F				
PIC24EP256MC202	0x1F71				
PIC24EP256MC204	0x1F70				
PIC24EP256MC206	0x1F73				
dsPIC33EP256MC202	0x1F61				
dsPIC33EP256MC204	0x1F60				
dsPIC33EP256MC206	0x1F63				
dsPIC33EP256MC502	0x1F65				
dsPIC33EP256MC504	0x1F64				
dsPIC33EP256MC506	0x1F67				

**Note 1:** The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

**2:** Refer to the “dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits” (DS70663) for detailed information on Device and Revision IDs for your specific device.

**TABLE 1: SILICON DEVREV VALUES (CONTINUED)**

Part Number	Device ID <sup>(1)</sup>	Silicon Revision/Device ID <sup>(2)</sup>			
PIC24EP512GP202	0x1799	—	A7 0x4007	—	—
PIC24EP512GP204	0x1798				
PIC24EP512GP206	0x179B				
dsPIC33EP512GP502	0x178D				
dsPIC33EP512GP504	0x178C				
dsPIC33EP512GP506	0x178F				
PIC24EP512MC202	0x1791				
PIC24EP512MC204	0x1790				
PIC24EP512MC206	0x1793				
dsPIC33EP512MC202	0x1781				
dsPIC33EP512MC204	0x1780				
dsPIC33EP512MC206	0x1783				
dsPIC33EP512MC502	0x1785				
dsPIC33EP512MC504	0x1784				
dsPIC33EP512MC506	0x1787				

- Note 1:** The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.
- 2:** Refer to the “*dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits*” (DS70663) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary
CPU	div.sd	1.	When using the <code>div.sd</code> instruction, the Overflow bit is not getting set when an overflow occurs.
CPU	DO Loop	2.	PSV access, including Table Reads or Writes in the first or last instruction of a DO loop, is not allowed.
SPI	Frame Sync Pulse	3.	Frame Sync pulse is not generated in Master mode when <code>FRMPOL = 0</code> .
SPI	Frame Sync Pulse	4.	When in SPI Slave mode, with the Frame Sync pulse set as an input, <code>FRMDLY</code> must be set to '0'.
UART	TX Interrupt	5.	A Transmit (TX) interrupt may occur before the data transmission is complete.
Power System	Flash Regulator	6.	The <code>VREGSF (RCON[11])</code> bit always reads back as '0'.
ADC	DONE bit	7.	The ADC Conversion Status bit (DONE) does not work when an external interrupt is selected as the ADC trigger source.
PTG	Strobe Output	8.	Strobe output pulse width is incorrectly dependent on the <code>PTGPWD[3:0] (PTGCON[7:4])</code> bits setting.
Op Amp	Enabling Op Amp mode	9.	When using any of these op amp modules, or Analog Channels AN0, AN3 or AN6, to sample external signals, bit 11 of the <code>CMxCON</code> register must be set to '1'.
Op Amp	AC/DC Electrical Characteristics	10.	The AC/DC electrical characteristics for the op amp module (and the related ADC specifications) are not within the specifications published in the current data sheet.
PWM	Dead-Time Compensation	11.	Dead-time compensation is not enabled for Center-Aligned PWM mode.
Flash	Flash Programming	12.	The Stall mechanism may not function properly when erasing or programming Flash memory.
QEI	Index Counter	13.	The QEI Index Counter does not count correctly in Quadrature Detector mode.
QEI	Modulo Mode	14.	Modulo mode functionality is incorrect when the count polarity bit is set.
PWM	Master Time Base Mode	15.	In Master Time Base mode, writing to the period register and any other timing parameter of the <code>PWMx</code> module, will cause the update of the other timing parameter to take effect one PWM cycle after the period update is effective.
ADC	1.1 Msps Sampling	16.	Selecting the same <code>ANx</code> input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.
ADC	Channel Scan	17.	Channel scanning is limited to AN0 through AN15.
Output Compare	Interrupt	18.	Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag ( <code>OCxIF</code> ) bit to become set prior to the Change-of-State (COS) of the <code>OCx</code> pin.
CAN	DMA	19.	Write collisions on a DMA-enabled CAN module does not generate <code>DMAC</code> error traps.
PWM	Immediate Update	20.	Dead time is not asserted when <code>PDCx</code> is updated to cause an immediate transition on the <code>PWMxH</code> and <code>PWMxL</code> outputs.
PWM	Center-Aligned Mode	21.	<code>PWMxH</code> is asserted for 100% of the PWM period in Complementary mode under certain circumstances.
PWM	Complementary Mode	22.	With dead time greater than zero, 0% and 100% duty cycle cannot be obtained on <code>PWMxL</code> and <code>PWMxH</code> outputs.

**TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)**

Module	Feature	Item Number	Issue Summary
CPU	Program Memory	23.	Address error trap may occur while accessing certain program memory locations.
PWM	Center-Aligned Mode	24.	Updates to active MDC/PDCx/ALTDTRx/PHASEx registers occur only once every two PWM periods.
PWM	Independent Time Base Mode	25.	Under certain circumstances, updates to the OVRENH and OVRENH bits may be ignored by the PWMx module.
PWM	Center-Aligned Mode	26.	PHASEx register updates are delayed.
CTMU	ADC Operation	27.	CTMU does not work with the ADC Converter in 12-bit mode.
Input Capture	External Synchronization	28.	Input capture and output compare modules cannot be synchronized.
JTAG	—	29.	—
I/O	Pin Functions that are Not 5V Tolerant	30.	Select pins are not 5V tolerant.
JTAG	I/O	31.	Active-high logic pulse on the I/O pin with TMS function at POR.
QE1	Velocity Counter	32.	Under certain circumstances, the Velocity Counter 1 register (VEL1CNT) misses count pulses.
QE1	Position Capture	33.	Under certain conditions, the captured position may be off by $\pm 1$ count.
QE1	Position Capture	34.	Position count captured at the rising edge of the HOME signal and not the INDEX signal.
PWM	Center-Aligned Mode	35.	Under certain conditions, PWMxH and PWMxL are deasserted.
PWM	Current Reset Mode	36.	When the PWM generator is configured to operate in Current Reset mode, the PWM Reset will happen only in every alternate PWM cycle.
Op Amp/Comparator	External Reference	37.	Op Amp/Comparator Voltage Reference fails when the voltage on VREF+ is less than 1.33V.
PWM	PWM Override	38.	Glitch on PWMxH or PWMxL pins when override is turned off.
PWM	PWM SWAP	39.	When in Complementary mode, PWM SWAP feature does not function properly.
PWM	PWM Override	40.	PWM override feature is not functional.
CAN	Receive Buffer	41.	Read-Modify-Write operation on a CxRXFULx register may not update it correctly.
PWM	Edge-Aligned Mode	42.	Missing dead time under certain conditions.
PWM	Output Modes	43.	Output glitch pulse.
PWM	Complementary Output Mode	44.	Missing dead time between complementary outputs under certain conditions.
PWM	PWM SWAP	45.	In Center-Aligned mode, there is missing dead time when SWAP is disabled.
PWM	Center-Aligned Mode	46.	Updates to the PHASEx registers occur only at the middle of the Center-Aligned PWM cycle.
CPU	Data Flash Reads	47.	Given a specific set of preconditions, when two or more data Flash read instructions (via Program Space Visibility (PSV) read or Table Read) are executed back-to-back, one or more subsequent instructions will be misexecuted.

**Silicon Errata Issues**

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The **Affected Families and Silicon Revisions** tables display an X when a silicon revision is affected by the silicon errata issue. If a cell is empty, the corresponding silicon revision either is not available or is not affected by the errata.

**1. Module: CPU**

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

**Work around**

Test for and handle overflow conditions outside of the `div.sd` instruction.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**2. Module: CPU**

Table Write (`TBLWTx`), Table Read (`TBLRDx`) and PSV Flash read instructions should not be used in the first or last instruction locations of a `DO` loop.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**3. Module: SPI**

When using the Frame Sync pulse output feature (FRMEN bit (`SPIxCON2[15]`) = 1) in Master mode (SPIFSD bit (`SPIxCON2[14]`) = 0), the Frame Sync pulse is not being generated with an active-low pulse (FRMPOL bit (`SPIxCON2[13]`) = 0).

**Work around**

The `SSx` pin is used as the Frame Sync pulse when the Frame Sync pulse output feature is used. Mapping the `SSx` input function and output function to the same pad, by using the Peripheral Pin Select (PPS) feature, resolves this issue.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**4. Module: SPI**

When in SPI Slave mode (MSTEN bit (`SPIxCON1[5]`) = 0) and using the Frame Sync pulse output feature (FRMEN bit (`SPIxCON2[15]`) = 1) in Slave mode (SPIFSD bit (`SPIxCON2[14]`) = 1), the Frame Sync Pulse Edge Select bit must be set to '0' (FRMDLY bit (`SPIxCON2[1]`) = 0).

**Work around**

There is no work around. The Frame Sync Pulse Edge Select bit, FRMDLY, cannot be set to produce a Frame Sync pulse that coincides with the first bit clock.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**5. Module: UART**

When using UTXISEL[1:0] = 01 (interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register (TSR), the Transmit (TX) interrupt may occur before the final bit is shifted out.

**Work around**

If it is critical that the interrupt processing occurs only when all transmit operations are complete. Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**6. Module: Power System**

The VREGSF bit functions as documented, but will always read back as '0'. Because of the Read-Modify-Write process, any BSET or BCLR instruction of the RCON register will also write a '0' to the VREGSF bit.

**Work around**

If the VREGSF bit is intended to be set to '1', the user software must also write a '1' to the VREGSF bit when setting or clearing any other bit in the RCON register.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**7. Module: ADC**

The ADC Conversion Status (DONE) bit (ADxCON1[0]) does not indicate completion of conversion when an external interrupt is selected as the ADC trigger source (SSRC[2:0] bits (AD1CON1[7:5]) = 0x1).

**Work around**

Use an ADC interrupt or poll the ADxIF bit in the IFSx registers to determine the completion of conversion.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**8. Module: PTG**

When using the strobe output Step commands ('PTGCTRL 0b1110', 'PTGCTRL 0b1100' and 'PTGCTRL 0b1101') to write to the AD1CHS0 register, the PTGPWD[3:0] bits (PTGCON[7:4]) determine the number of times the PTG module will write to the AD1CHS0 register.

**Work around**

Set the PTGPWD[3:0] bits to '0000' so that the PTG module does not write to the AD1CHS0 register multiple times.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		



### 9. Module: Op Amp

When using any of these op amp modules or analog channels, AN0, AN3 or AN6, to sample external signals, bit 11 of the CMxCON register must be set to '1'.

If Using This Feature:	These Conditions Must be Met:	
	OPMODE (CMxCON[10])	CMxCON[11]
AN0	OPMODE (CM2CON[10]) = 0	CM2CON[11] = 1
AN3	OPMODE (CM1CON[10]) = 0	CM1CON[11] = 1
AN6	OPMODE (CM3CON[10]) = 0	CM3CON[11] = 1
Op Amp 1	OPMODE (CM1CON[10]) = 1	CM1CON[11] = 1
Op Amp 2	OPMODE (CM2CON[10]) = 1	CM2CON[11] = 1
Op Amp 3	OPMODE (CM3CON[10]) = 1	CM3CON[11] = 1

#### Work around

None.

#### Affected Families and Silicon Revisions

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64	X				
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512					

### 10. Module: Op Amp

The AC/DC electrical characteristics for the op amp module (and the related ADC module specifications) differ from the specifications in the published data sheet. Refer to [Table 3](#) and [Table 4](#) (below) for the A2 revision silicon specifications.

#### Work around

None.

#### Affected Families and Silicon Revisions

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64	X				
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512					

TABLE 3: AC/DC CHARACTERISTICS: OP AMP

Param. No.	Symbol	Minimum	Typical	Maximum	Units	Conditions
CM21a	PM	—	40	—	Degree	—
CM21b	PM	—	30	—	Degree	—
CM23a	GBW	—	7	—	MHz	—
CM23b	GBW	—	2	—	MHz	—
CM49a	VOADC	AVSS + 0.350 AVSS + 0.500	— —	AVDD – 0.350 AVDD – 0.500	V V	IOUT = 390 µA, Op Amp 1 and 2 IOUT = 390 µA, Op Amp 3
CM49b	VOUT	AVSS + 0.375 AVSS + 0.525	— —	AVDD – 0.375 AVDD – 0.525	V V	IOUT = 390 µA, Op Amp 1 and 2 IOUT = 390 µA, Op Amp 3
CM51a	RINT1	351	468	613	Ω	—

TABLE 4: AC/DC CHARACTERISTICS: ADC

Parameter No.	Symbol	Minimum	Typical	Maximum	Units	Conditions
AD57b	TSAMP	5 TAD	—	—	—	Op Amp 1 and 2, 12-bit mode, Configuration B
		5 TAD	—	—	—	Op Amp 3, 10-bit mode, Configuration B
		7 TAD	—	—	—	Op Amp 3, 12-bit mode, Configuration B

**11. Module: PWM**

When dead-time compensation is enabled (DTC[1:0] (PWMCONx[7:6]) = 11) in Center-Aligned mode (CAM (PWMCONx[2]) = 1), the dead time, as specified in the ALTDTRx register, is not being applied to the PWMxH output. The leading and trailing edges of the PWMxL output are extended by one-half the value of the ALTDTRx register, but the PWMxH leading and trailing edges are unaffected.

**Work around**

Using the values from “High-Speed PWM” (DS70645) in the “dsPIC33/PIC24 Family Reference Manual”, adjust the PWM parameters as follows:

- Subtract one-half of the ALTDTR dead time from PDCx
- Use twice the value for ALTDTR. For example:
  - Frequency of 60 kHz, duty cycle of 50%
  - Desired dead time of 833 ns and dead-time compensation of 833 ns

Using the specified values from “High-Speed PWM” (DS70645):

- PHASEx = 1000
- PDCx = 500
- ALTDTRx = 833 ns/8.33 ns = 100
- DTRx = (833 ns/8.33 ns)/2 = 50

Applying the work around:

- ALTDTRx = 2 \* 100 = 200
- PDCx = PDCx – 25 = 475

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**12. Module: Flash**

The processor stalls while performing Run-Time Self-Programming (RTSP) erase and write operations on the same Flash segment (General or Auxiliary) from which code is being executed. The Stall mechanism does not always function properly and can cause unexpected behavior.

**Work around**

Two options are available to avoid this issue:

1. If you are required to execute code, including an Interrupt Service Routine (ISR), from the same segment (either General or Auxiliary) that you are performing RTSP operations on, you must disable global interrupts until the erase or programming operation is complete (see Example 1).
2. If possible, structure your project such that RTSP operations are performed on a segment from which no code is being executed. For example, place all of your executable code in the General Segment and all reprogrammable data in the Auxiliary Segment, or vice versa. This solution has the added advantage that no CPU Stalls occur since the programming operation is not being performed on the same segment that is executing the code.

**EXAMPLE 1: WORK AROUND CODE**

```

; Load write latches if programming ...
; Setup NVMCON register to erase or program
as required ...
; Disable interrupts
PUSH W0
PUSH W1
MOV INTCON2, W1
BCLR INTCON2, #15
; Write the KEY sequence
MOV #0x55, W0
MOV W0, NVMKEY
MOV #0xAA, W0
MOV W0, NVMKEY
; Start the programming sequence
BSET NVMCON, #15
; Insert two NOPs after programming
NOP
NOP
; Wait for operation to complete
prog_wait:
BTSC NVMCON, #15
BRA prog_wait
; Re-enable interrupts,
BTSC W1, #15
BSET INTCON2, #15
POP W1
POP W0
    
```

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512					

**13. Module: QEI**

In Quadrature Encoder mode (CCM[1:0] (QEIXCON[1:0]) = 00), the Index Counter registers (INDXxCNTH and INDXxCNTL) cannot be relied upon to increment when the last known direction was positive and an index pulse occurs. The Index Counter register can decrement even if the last known direction was positive. This does not apply to the External Clock or Internal Timer QEI modes.

**Work around**

The index event can be used to implement a software counter. The direction could be determined by comparing the current POSxCNT value to that of the previous Index Event.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**14. Module: QEI**

When Modulo Count mode (Mode 6) is selected for the position counter (PIMOD[2:0] (QEIXCON[12:10]) = 110), and the counter direction is set to negative (CNTPOL (QEIXCON[3]) = 1), the functions of the QEIXLEC and QEIXGEC registers are reversed.

**Work around**

When using Modulo Count mode in conjunction with a negative count direction (polarity), use the QEIXLEC register as the upper count limit and the QEIXGEC as the lower count limit.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**15. Module: PWM**

The PWMx module can operate with variable period, duty cycle, dead-time and phase values. The master period and other timing parameters can be updated in the same PWM cycle. With immediate updates disabled, the new values should take effect at the start of the next PWM cycle.

As a result of this issue, the updated master period takes effect on the next PWM cycle, while the update of the additional timing parameter is delayed by one PWM cycle. The parameters affected by this erratum are as follows:

Master Period Registers – Update effective on the next PWM cycle (PTPER).

Additional PWM Timing Parameters – Update effective one PWM cycle after master period update:

- Duty Cycle – PDCx and MDC registers
- Phase – PHASEx register
- Dead Time – DTRx and ALTDTRx registers and dead-time compensation signals
- Clearing of current-limit and Fault conditions, and application of External Period Reset signal

**Work around**

If the application requires the master period and other parameters to be updated at the same time, enable both immediate updates:

- EIPU (PTCON[10]) = 1 – To enable immediate period updates
- IUE (PWMCONx[0]) = 1 – To enable immediate updates of additional parameters listed above

Enabling immediate updates will allow updates to the master period and the other parameter to take effect immediately after writing to the respective registers.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**16. Module: ADC**

Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.

**Work around**

Bring the analog signal into the device using both AN0 and AN3, connect externally, and then assign one input to CH0 and the other to CH1.

If selecting AN0 on CH1 (CH123Sx = 0), select AN3 on CH0 (CH0Sx = 3). Conversely, if selecting AN3 on CH1 (CH123Sx = 1), select AN0 on CH0 (CH0Sx = 0).

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**17. Module: ADC**

Selection of channels for channel scan operation is limited to those available in the AD1CSSL register (AN0 through AN15). Selections in the AD1CSSH register, (OA1 through OA3, CTMU TEMP and CTMU Open) are not available.

**Work around**

There is no work around of the CTMU TEMP and CTMU Open selections. OA1 through OA3 can be scanned using AN3, AN0 and AN6 for Op Amp 1, Op Amp 2 and Op Amp 3, respectively.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**18. Module: Output Compare**

Under certain circumstances, an output compare match may cause the Output Compare Interrupt Flag (OCxIF) to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM[2:0] = 001, 010 or 100);
- One of the timer modules is being used as the time base; and
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing OCM[2:0] after the One-Shot compare, the OCx pin may not be driven as expected.

**Work around**

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing OCM[2:0]. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**19. Module: CAN**

When DMA is used with the CAN module, and the CPU and DMA write to an CAN Special Function Register (SFR) at the same time, the DMAC error trap is not occurring. In addition, neither the PWCOL[3:0] bits of the DMAPWC SFR or the DMACERR bit of the INTCON1 SFR are being set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

**Work around**

There is no work around; however, under normal circumstances, this situation should not arise. When DMA is used with the CAN module, the application should not be writing to the CAN SFRs.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**20. Module: PWM**

The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

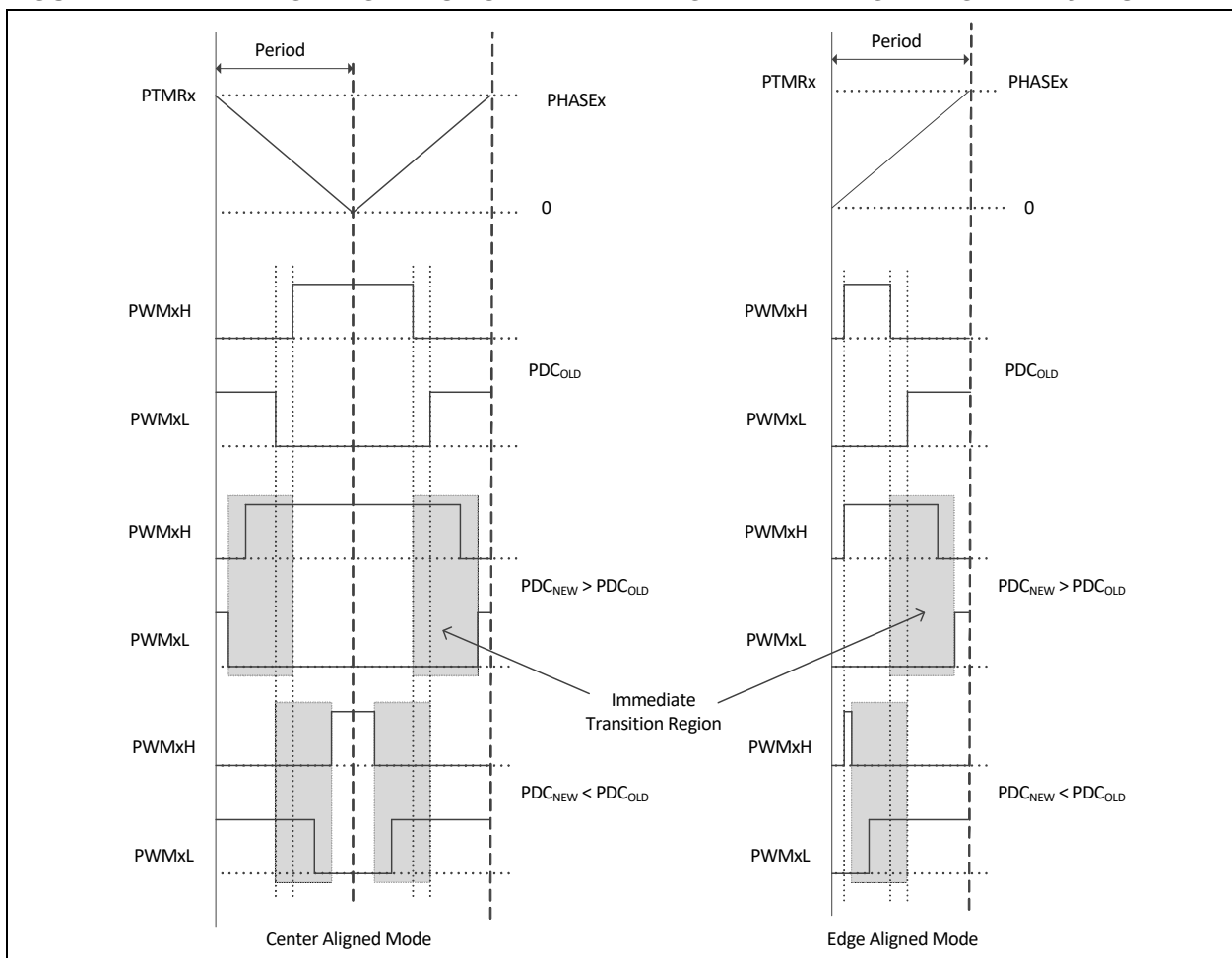
- The PWM generator is configured to operate in Complementary mode with Independent Time Base (ITB) or master time base;
- Immediate update is enabled; and
- The value in the PDC register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDC<sub>OLD</sub>, newly calculated duty cycle, PDC<sub>NEW</sub>, and the point at which a write to the Duty Cycle register occurs within the PWM

time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDC<sub>NEW</sub>, at a point of time when the PWM time base is counting a value that is in between PDC<sub>NEW</sub> and PDC<sub>OLD</sub>. Additionally, writing to the Duty Cycle register, close to the instant of time where dead time is being applied, may result in a reduced dead time effective on the PWMxH and PWMxL transition edges.

In Figure 1, if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

**FIGURE 1: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES**



**Work around**

None.

However, in most applications the duty cycle update timing can be controlled using the TRIGx trigger, or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**21. Module: PWM**

In Center-Aligned Complementary mode with Independent Time Base, the PWM generator may assert the PWMxH output for 100% of the duty cycle. This has been observed when the value in its PDCx register is less than one-half the value in its ALTDTRx register.

**Work around**

Include a software routine to check that the duty cycle value written to the PDCx register is always at least one-half of the value in ALTDTRx.

**Example 2** shows one way of doing this, with PDCtemp representing the value to be written to the PDCx register.

**EXAMPLE 2: WORK AROUND CODE**

```

Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
    PDCx = Altdtr_by2;
}
else
{
    PDCx = PDCtemp;
}
    
```

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512					

**22. Module: PWM**

This issue is applicable when a PWM generator is configured to operate in Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, PWMxL is not asserted for 100% of the time when PDCx is zero. Similarly, when dead time is non-zero, PWMxH is not asserted for 100% of the time when PDCx is equal to PHASEx. This issue applies to Master Time Base mode as well.

**Work around**

In Center-Aligned mode:

- To obtain 0% duty cycle, first zero out the ALTDTRx register, then write zero to the PDCx register.
- To obtain 100% duty cycle, first zero out the ALTDTRx register, then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, first zero out the registers, DTRx and ALTDTRx, then write zero to the PDCx register.
- To obtain 100% duty cycle, first zero out the registers, DTRx and ALTDTRx, then write (PHASEx + 1) to the PDCx register.

Alternatively, in both Center-Aligned and Edge-Aligned PWM modes, 0% and 100% duty cycle can be obtained by enabling the PWM override (IOCONx[9:8] = 0b11) with the Output Override Synchronization bit (IOCONx[0]) set as '1':

- For 0% duty cycle, set the Override Data bits (IOCONx[7:6]) for PWMxH and PWMxL as '0b01'
- For 100% duty cycle, set the Override Data bits (IOCONx[7:6]) for PWMxH and PWMxL as '0b10'

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**23. Module: CPU**

An unexpected address error trap may occur during accesses to program memory addresses, 0x001 through 0x200. This has been observed when one or more interrupt requests are asserted while reading or writing program memory addresses, using TBLRDx, TBLWTx or PSV-based instructions.

**Work around**

Before executing instructions that read or write program memory addresses, 0x001 through 0x200, disable interrupts using the DISI instruction.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**24. Module: PWM**

In Center-Aligned mode, updates to active MDC/PDCx/ALTDTRx/PHASEx registers occur only once every two PWM periods; that is, when the PWM timer matches the PHASEx register. In other words, the double update feature is not available. Figure 2 illustrates this relationship.

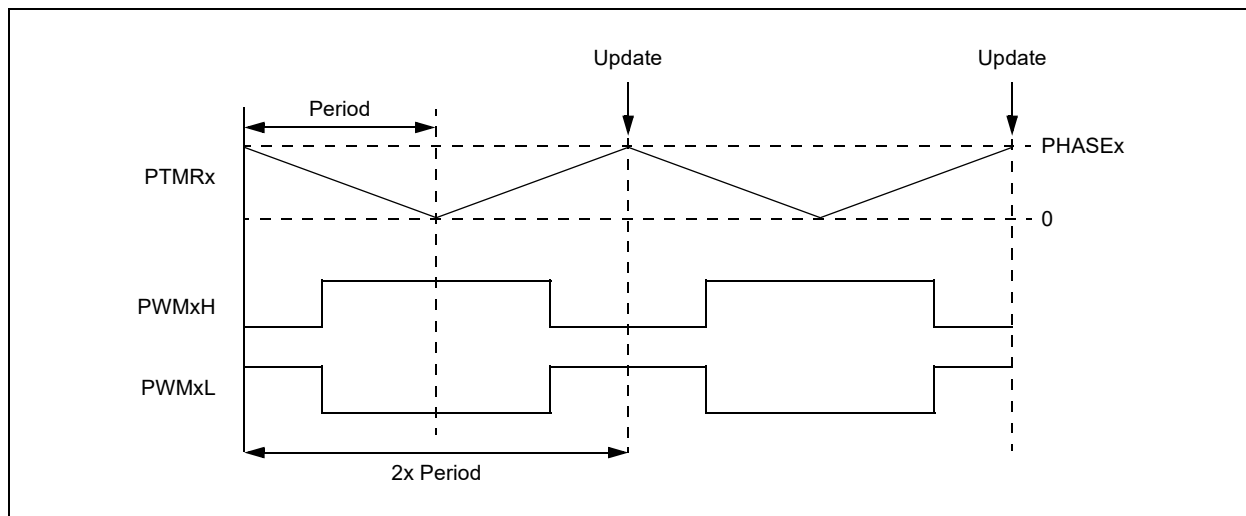
**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512					

**FIGURE 2: PWM TIMING DIAGRAM**



**25. Module: PWM**

Under certain circumstances, an update to the IOCONx register to turn off the override will be ignored by the PWMx module. The issue has been observed to occur when the IOCONx update to turn off the override occurs close to the time when dead time is being applied.

**Work around**

1. Turn off the PWM dead time.
2. Alternatively, turn off the PWM override with the following procedure:
  - a) Disable the PWMx module (PTEN = 0)
  - b) Clear the Override Enable bits (OVRENH = 0 and OVRENL = 0)
  - c) Enable the PWMx module (PTEN = 1)

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512	See Silicon Issue <a href="#">40</a> .				

**26. Module: PWM**

In Center-Aligned Complementary mode with Independent Time Base, updates to the PHASEx register take effect after a delay of two PWM periods.

This occurs only when the Immediate Update feature is disabled (IUE = 0). If Immediate Update is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512					

**27. Module: CTMU**

The CTMU cannot be used with the A/D Converter when the converter is operating in 12-bit mode.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**28. Module: Input Capture**

When an input capture module is selected as the Sync source for either an output compare module or another input capture module, synchronization may fail.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**29. Module: JTAG**

This is no longer an issue to any silicon revisions and has been removed.

**Work around**

No work around necessary.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64					
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512					



**30. Module: I/O**

On all packages, pins with the following functions are not 5V tolerant:

- RC3
- RC4
- RC5
- RA9

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512					

**31. Module: JTAG**

At a Power-on Reset (POR), when JTAG is disabled in the Configuration bits, the I/O pin with TMS function produces an active-high logic pulse with a pulse width in the order of milliseconds.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512					

**32. Module: QEI**

The Velocity Counter x (VELxCNT) register is a 16-bit wide register that increments or decrements based on the signal from the quadrature decoder logic. Reading this register results in a Counter Reset. Typically, the user application should read the Velocity Counter at a rate of 1-4 kHz.

As a result of this issue, the Velocity Counter may miss a count if the user application reads the Velocity Counter 1 register at the same time as a (+1 or -1) count increment occurs.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

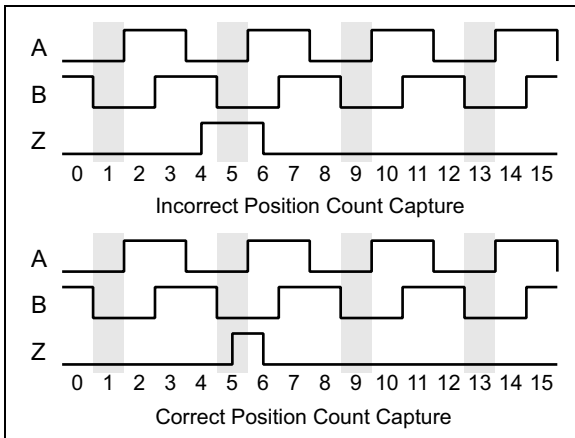
**33. Module: QEI**

When index count position capture is being used (QEIXIOC.QCAPEN = 1), the position count may be one more or one less than the correct value, depending on the direction of the count.

This is only observed when the leading edge of the index pulse occurs prior to the leading edge of the index match event. When the index pulse starts after the leading edge of the index match event, the position count is captured correctly.

Figure 3 shows how this occurs. In these cases, Encoder Signals A, B and (index) Z are shown, with the module being configured for index match when A and B are '0'. The effects of a correct and incorrect capture are shown side by side (shaded area indicates the index match event); the position count is shown along the bottom.

**FIGURE 3: CORRECT AND INCORRECT POSITION COUNT CAPTURES**



**Work around**

There are two different work arounds depending on the encoder type.

For encoder signals with timing that ensures the index pulse always starts prior to the start of the index match event (i.e., encoders with a non-gated index pulse), measure the direction of the encoder motion. If the encoder is counting up, add one to the captured position count; if the encoder is counting down, subtract one from the captured position count.

For encoder signals where the index pulse leading edge approximately coincides with the start of the index match event (i.e., encoders with a gated index pulse), a small delay can be added to the index pulse, for instance, by using a simple R-C filter.

If the encoder does not meet either of these criteria, no work around is available.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64					
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512			X		

**34. Module: QEI**

When QCAPEN (QEIXIOC[15]) is enabled, the position count is captured at the rising edge of the HOME signal, instead of the index match event as indicated by the data sheet.

**Work around**

None.

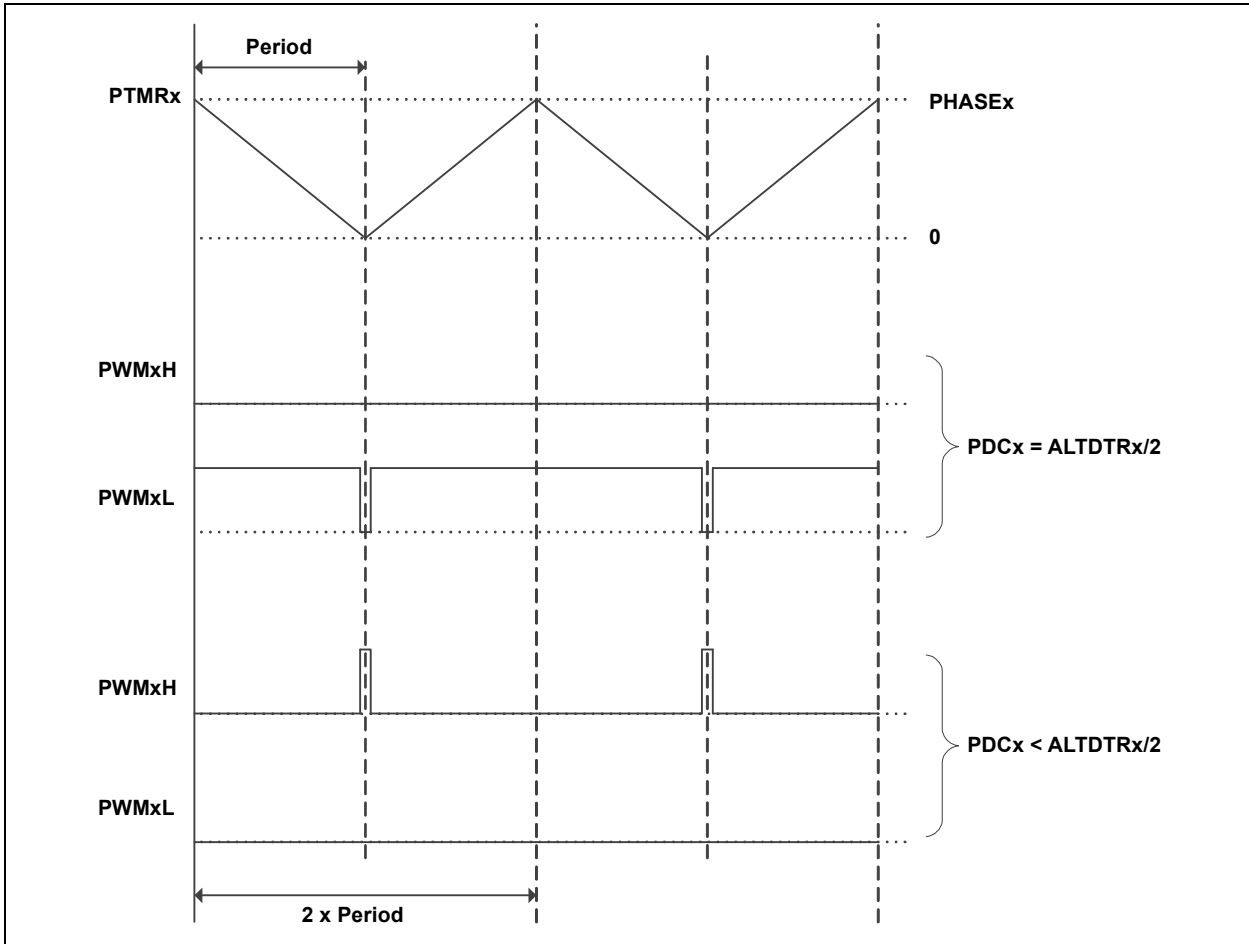
**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512					

35. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, if the value in the PDCx register is less than one-half the value in the ALTDTRx register, the PWM generator will force the PWMxL to low, and on the PWMxH, generate pulses of width less than twice the dead time, as shown in Figure 4.

FIGURE 4: PWM GENERATOR TIMING DIAGRAM



**Work around**

Include a software routine to ensure that the duty cycle value written to the PDCx register is always at least one-half of the value in ALTDTRx. [Example 3](#) shows one method, with PDCtemp representing the variable which has the value to be written to the PDCx register. Alternatively, for duty cycle values less than half the desired dead-time value, zero out the ALTDTRx register or dynamically reduce the value in the ALTDTRx register, such that ALTDTRx is always equal to 2 \* PDCx, as shown in [Example 4](#).

**EXAMPLE 3: WORK AROUND CODE**

```
Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
PDCx = Altdtr_by2;
}
else
{
PDCx = PDCtemp;
}
```

**EXAMPLE 4: WORK AROUND CODE**

```
#define DESIRED_DEADTIME 100
if (PDCtemp < (DESIRED_DEADTIME/2))
{
ALTDTRx = PDCtemp * 2;
PDCx = PDCtemp;
}
else
{
ALTDTRx = DESIRED_DEADTIME;
PDCx = PDCtemp;
}
```

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32				X	
dsPIC33/PIC24EP64				X	
dsPIC33/PIC24EP128				X	
dsPIC33/PIC24EP256				X	X
dsPIC33/PIC24EP512			X		

**36. Module: PWM**

When the PWM generator is configured to operate in Current Reset mode (XPRES (PWMCONx[1]) = 1 with Independent Time Base mode (ITB (PWMCONx[9]) = 1), the PWM Reset will happen only in every alternate PWM cycle.

**Work around**

1. Generate an interrupt when the comparator state changes. This interrupt should be high priority and could be either a comparator interrupt or PWM Fault interrupt. The current-limit interrupt does not function in this mode. Inside the interrupt, update PHASEx (period value) with a value less than the programmed duty cycle and then immediately update the PHASEx register with the value, as required by the application (PWM\_period), shown in [Example 5](#).

**EXAMPLE 5: WORK AROUND CODE**

```
PWMx_ISR:
{
PHASEx = PDCx - 100;
PHASEx = PWM_period;
PWMxIF = 0;
}
```

2. When the External Current Reset signal is applied to the PWM generator (configured using Current-Limit Signal Source Select bits (CLSRC[4:0]) in the PWMx Fault Current-Limit Control registers (FCLCONx[14:10]), depending on the PWM resolution selected, PCLKDIV[2:0] (PTCON2[2:0]), the maximum pulse width of the External Current Reset signal is to be restricted to less than the values, as shown in [Table 5](#).

**TABLE 5: MAXIMUM EXTERNAL CURRENT RESET SIGNAL WIDTH**

PCLKDIV[2:0]	Max. External Current Reset Signal Width (in nS)
000	20
001	40
010	80
011	160
100	320
101	640
110	1280

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512			X		

**37. Module: Op Amp/Comparator**

Op amp/comparator voltage reference can choose its source either from VREF+ or AVDD, depending on the CVRSS bit (CVRCON[4]) setting.

If the CVRSS bit is set to '1', the comparator voltage reference source will be CVRSRC = (VREF+) – (AVSS). Due to this issue, if the CVRSS bit is set to '1' and the voltage on VREF+ is less than 1.33V, the op amp/comparator voltage reference will malfunction.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**38. Module: PWM**

In Complementary mode after the PWMx module is enabled (PTEN = 1), if the PWM override is turned off, a 1 T<sub>osc</sub> glitch will be present on the rising edge of either PWMxH or PWMxL, whichever occurs first, as shown in Figure 5. The glitch will be present on PWMxH/PWMxL every time the override state is changed from enabled to disabled. The width of this glitch is equal to 1 T<sub>osc</sub> when PCLKDIV[2:0] = 000; increasing the PWM input clock prescaler setting will increase the width of the glitch accordingly.

Since the width of the glitch is just 1 T<sub>osc</sub> at higher values of F<sub>osc</sub>, the glitch may not be visible on the PWMxH/PWMxL pins due to pin and PCB trace capacitances.

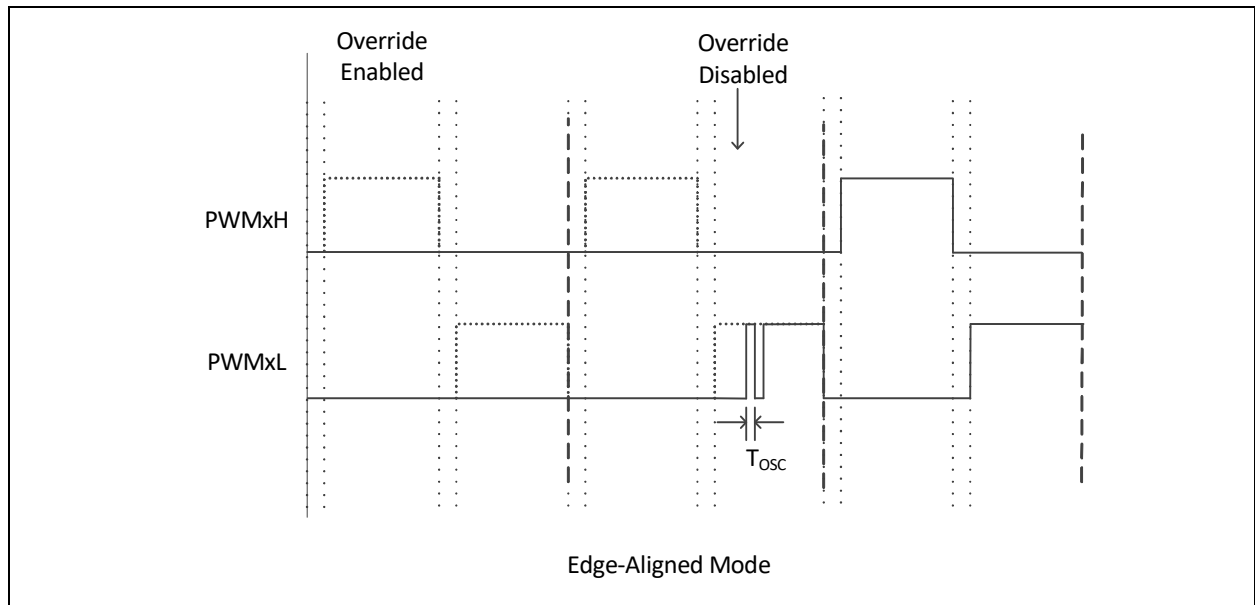
**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32				X	
dsPIC33/PIC24EP64				X	
dsPIC33/PIC24EP128				X	
dsPIC33/PIC24EP256				X	X
dsPIC33/PIC24EP512					

**FIGURE 5: ILLUSTRATION OF 1 T<sub>osc</sub> GLITCH WHEN PWM OVERRIDE IS TURNED OFF**



**39. Module: PWM**

In Complementary mode, if SWAP (IOCONx[1]) is set from '0' to '1' after enabling the PWMx module (PTEN (PTCON[15]) = 1), either PWMxH or PWMxL may stop functioning until SWAP is set back to '0'.

**Work around**

Disable dead time.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X			
dsPIC33/PIC24EP64	X	X			
dsPIC33/PIC24EP128		X			
dsPIC33/PIC24EP256		X			
dsPIC33/PIC24EP512			X		

**40. Module: PWM**

PWM override feature is not functional.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32					
dsPIC33/PIC24EP64					
dsPIC33/PIC24EP128					
dsPIC33/PIC24EP256					
dsPIC33/PIC24EP512			X		

**41. Module: CAN**

When the DMA controller is copying the received CAN message into an appropriate message buffer in the user-defined device RAM area, any Read-Modify-Write operation on a CxRXFULx (C1RXFUL1, C1RXFUL2, C2RXFUL1 and C2RXFUL2) register may not update the CxRXFULx register properly. The CPU can only clear a bit in the CxRXFULx register. A Read-Modify-Write operation successfully clears the intended bit, but it may incorrectly clear the bit set by the CAN module after a successful transfer of a message into RAM by the DMA.

**Work around**

Avoid Read-Modify-Write operations on C1RXFUL1, C1RXFUL2, C2RXFUL1 and C2RXFUL2 registers. See [Example 6](#) to clear any bit in the C1RXFUL1, C1RXFUL2, C2RXFUL1 and C2RXFUL2 registers while developing code in C:

**EXAMPLE 6: WORK AROUND CODE**

```

if (C1FIFObits.FNRB <= 15)
{
    C1RXFUL1 = ~(0x001 << C1FIFObits.FNRB);
}
else
{
    C1RXFUL2 = ~(0x001 << (C1FIFObits.FNRB - 16));
}
    
```

The CPU can only clear a bit in the CxRXFULx registers, but the CPU cannot set any bit in any of the CxRXFULx registers. Therefore, in the work around ([Example 6](#)):

- If the FNRB[5:0] (C1FIFO[5:0]) bits value is less than or equal to 15, only one bit of the C1RXFUL1 register will be cleared depending on the FNRB[5:0] bits value.
- If the FNRB[5:0] bits value is greater than 15, only one bit of the C1RXFUL2 register will be cleared depending on the FNRB[5:0] bits value.

This same method should be adopted for the C2RXFUL1 and C2RXFUL2 registers.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**42. Module: PWM**

In Edge-Aligned Complementary mode, changes to the PHASEx register under certain circumstances will result in missing dead time at the PWMxH-to-PWMxL transition. This has been observed only when all of the following are true:

- Master Time Base mode is enabled (PWMCONx[9] = 0);
- PHASEx is changed after the PWMx module is enabled; and
- The PHASEx register value is changed, so that either PHASEx < DTRx or PHASEx > PDCx.

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

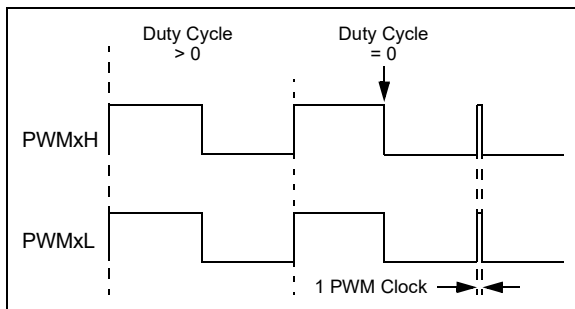
**43. Module: PWM**

In certain output modes, the PWMx module produces a pulse glitch of one PWM clock in width (Figure 6). This has been observed only when all of the following are true:

- Either Redundant or Push-Pull Output mode is selected (IOCONx[11:10] = 10 or 01);
- Immediate Update is disabled (PWMCONx[0] = 0); and
- The value of the current Duty Cycle register (either the PDCx or MDC register, as determined by PWMCONx[8]) is updated to zero from any non-zero value.

The pulse glitch has been observed to occur at the beginning of the following PWM boundary period.

**FIGURE 6:**



**Work around**

If the application requires a duty cycle of zero, two possible work arounds are available.

1. Use the PWM overrides to force the output to a low state, instead of writing a '0' to the Duty Cycle register. When using this method, the PWM override must be disabled when the duty cycle is a non-zero value. If output override synchronization is configured to occur on CPU clock boundaries (IOCONx[0] = 0), enabling and disabling the override must be timed to occur as closely as possible to the PWM period boundary.
2. Configure the module for Immediate Update (PWMCONx[0] = 1) before enabling the module. In this mode, writes to the Duty Cycle register have an immediate effect on the output. As with the previous work around, writes to the Duty Cycle register must be timed to occur as close to the PWM period boundary as possible in order to avoid distortion of the output.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

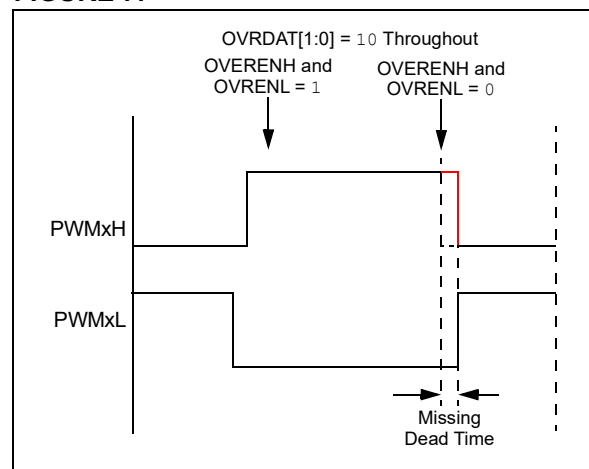
**44. Module: PWM**

In Complementary Output mode, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when the following occurs:

- Output override synchronization is configured to occur on the CPU clock boundary (IOCONx[0] = 0);
- Both PWMxH and PWMxL overrides are enabled prior to the event (OVRENH and OVRENL are both '1'), and
- Both overrides are disabled (OVRENH and OVRENL are both '0') at the instant the dead time should be asserted (Figure 7).

This has been observed in both Center-Aligned and Edge-Aligned modes.

**FIGURE 7:**



**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**45. Module: PWM**

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP is disabled under the following conditions:

- PWMx module is enabled (PTEN = 1)
- SWAP is enabled prior to this event

**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

**46. Module: PWM**

In Center-Aligned Complementary mode with Independent Time Base, updates to the PHASEx register take effect in the middle of a center-aligned PWM cycle, as shown in Figure 8. This occurs only when the Immediate Update feature is disabled (IUE = 0). If Immediate Update is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

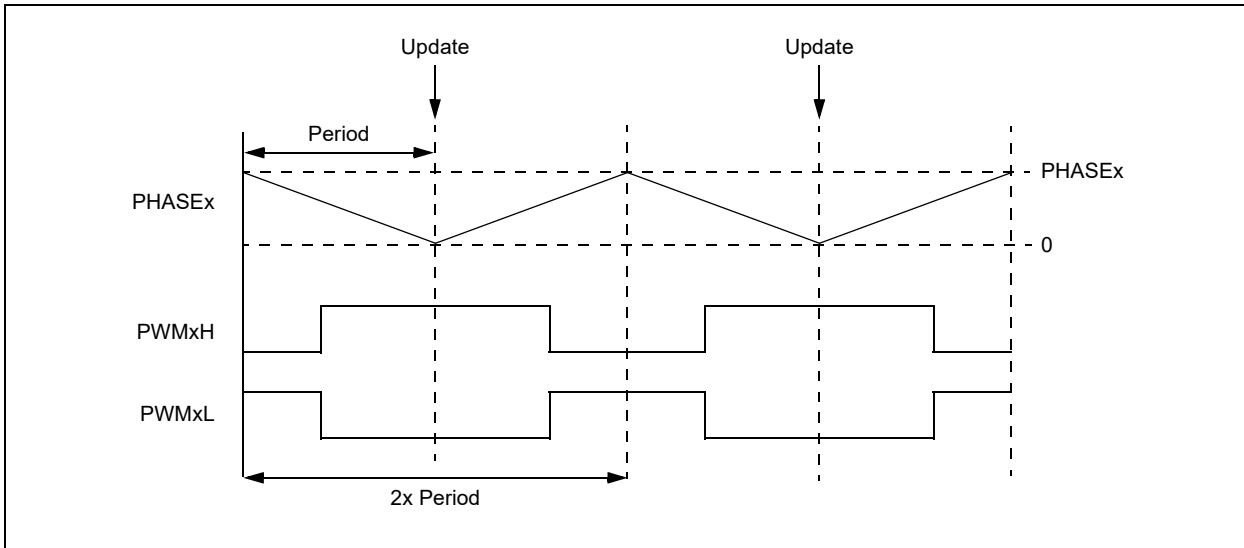
**Work around**

None.

**Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32				X	
dsPIC33/PIC24EP64				X	
dsPIC33/PIC24EP128				X	
dsPIC33/PIC24EP256				X	X
dsPIC33/PIC24EP512			X		

**FIGURE 8:**





47. Module: CPU

**Note:** This issue is deterministic based on the instruction sequence executed, and is not sensitive to manufacturing process, temperature, voltage or other application operating conditions that do not affect the instruction sequence.

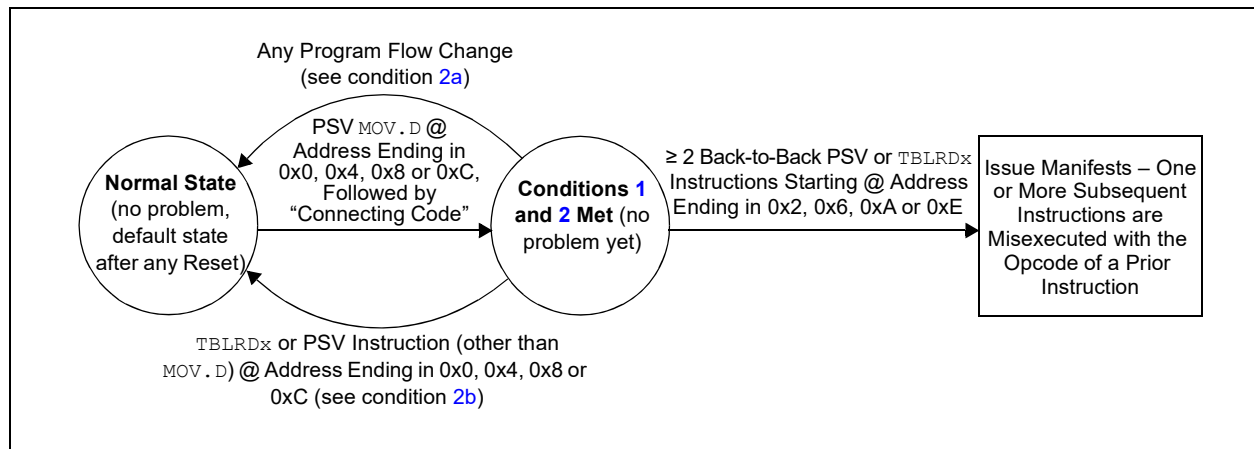
When two or more data Flash read instructions (via Program Space Visibility (PSV) read or table read) are executed back-to-back, one or more subsequent instructions can be misexecuted when all of the conditions in Table 6 occur.

**TABLE 6: REQUIRED CONDITIONS**

1.	A PSV <code>MOV.D</code> instruction is executed, with opcode at address ending in 0x0, 0x4, 0x8 or 0xC; and
2.	Some “connecting code” is executed (following the <code>MOV.D</code> of condition 1), with the properties: <ul style="list-style-type: none"> <li>a) The connecting code does not include any program flow changes, including: taken branch instructions (including all versions of <code>BRA</code>, <code>CPBEQ</code>, <code>CPBGT</code>, <code>CPBLT</code>, <code>CPBNE</code>), <code>CALL</code>, <code>CALL.L</code>, <code>GOTO</code>, <code>GOTO.L</code>, <code>RCALL</code>, <code>RETLW</code>, <code>RETURN</code>, vectoring to an ISR, returning from an interrupt (<code>RETFIE</code>) and certain debug operations, such as <code>break</code> and <code>one-step</code>; and</li> <li>b) The connecting code does not include a <code>TBLRDx</code> or non-<code>MOV.D</code> PSV instruction, located at a Flash memory address ending in 0x0, 0x4, 0x8 or 0xC; and</li> <li>c) The connecting code is at least two instruction words in length; and</li> <li>d) The connecting code does not end with a <code>REPEAT</code> instruction, with <code>count &gt; 0</code>; and</li> </ul>
3.	$\geq 2$ back-to-back PSV or <code>TBLRDx</code> instructions are executed (following the code of condition 2), where the first of the back-to-back instructions is located at an address ending in 0x2, 0x6, 0xA or 0xE.

Figure 9 provides an example of the effective behavior.

**FIGURE 9: SIMPLIFIED BEHAVIOR**



## **Work around**

The issue can be avoided by ensuring any one or more of the requirements are not met. For example:

1. All instances of PSV `MOV.D` can be replaced with two PSV `MOV` instructions instead. Non-PSV `MOV.D` instructions acting on RAM/SFRs do not need to be modified; or
2. If not already present, a program flow change instruction (such as `BRA $+2`) can be inserted above back-to-back data Flash read sequences; or
3. Back-to-back data Flash read instruction sequences can be broken up by inserting a non-Flash read instruction (such as a `NOB`) in between the Flash read instructions; or
4. The alignment of the code can be shifted to avoid the required opcode location addresses.

C code built with MPLAB® XC16 Compiler, Version 1.32, or later, implements the work around by default. However, if the application uses Assembly language routines, these should be manually modified to implement the work around. Additionally, if precompiled libraries are used, these should be built with XC16 Version 1.32 or later. For additional information, please visit: [www.microchip.com/erratum\\_psrds\\_psrds](http://www.microchip.com/erratum_psrds_psrds).

## **Affected Families and Silicon Revisions**

Device	A2	A3	A7	A8	A9
dsPIC33/PIC24EP32		X		X	
dsPIC33/PIC24EP64	X	X		X	
dsPIC33/PIC24EP128		X		X	
dsPIC33/PIC24EP256		X		X	X
dsPIC33/PIC24EP512			X		

### **Data Sheet Clarifications**

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000657J):

<p><b>Note:</b> Corrections are shown in <b>bold</b>. Where possible, the original bold text formatting has been removed for clarity.</p>
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None.

## APPENDIX A: REVISION HISTORY

### Rev A Document (11/2011)

Initial release of this document; issued for revision A2 silicon.

Includes silicon issues 1 (CPU), 2 (CPU) 3 (SPI), 4 (SPI), 5 (UART), 6 (Power System), 7 (ADC), 8 (PTG), 9 (Op Amp), 10 (Op Amp), 11 (PWM), 12 (Flash), 13 (QEI), 14 (QEI) and 15 (PWM).

### Rev B Document (4/2012)

Updated silicon issues 9 (Op Amp), 10 (Op Amp), and 12 (Flash).

Added silicon issues 16 (ADC), 17 (ADC), 18 (Output Compare), and 19 (CAN).

### Rev C Document (6/2012)

Updated document to include all related device families (program memory sizes of 32, 128, 256 and 512 Kbytes) in this superfamily. In the process, revised the document format to accommodate the different silicon revision levels across the different families.

Added silicon issues 20, 21 and 22 (PWM), and 23 (CPU) to all device families.

Added data sheet clarification 1 (Packaging).

### Rev D Document (8/2012)

Updated Table 1 to include both A2 and A3 silicon revision device IDs and removed PIC24EP512/dsPIC32EP512 (A4). Updated all Affected Families and Silicon Revisions tables.

Added silicon issues 24 (PWM) and 25 (PWM).

Added data sheet clarification 2 (High-Speed PWM Module).

### Rev E Document (3/2013)

Adds silicon revision A2 for all 64 Kbyte devices to all existing silicon issues, except 9 and 10 (Op Amp).

Revises issue 24 (PWM) with a figure to illustrate the timing of the issue.

Revises issue 25 (PWM) to clarify conditions, and add work around options.

Added new silicon issues 26 (PWM), 27 (CTMU), 28 (Input Capture), 29 (JTAG), 30 (I/O), 31 (JTAG) and 32 (QEI) to silicon revision A3 for all device families, and revision A2 for 64 Kbyte device families only.

Updates data sheet revision level to "G". Removes previous data sheet clarifications, which have been addressed in the new revision; adds new data sheet clarification 1 (Revision History).

### Rev F Document (6/2013)

Updates document to include 512 Kbytes memory. Adds silicon issues 33 (QEI), 34 (QEI), 35 (PWM), 36 (PWM) and 37 (Op Amp/Comparator). Revises silicon issue 15 (PWM) description. Revises silicon issue 20 (PWM) with new figure and text. Revises issue 25 (PWM). Removes data sheet clarification 1 (Pin Diagrams) since this is now addressed in the current data sheet revision.

### Rev G Document (9/2013)

Updates document to include revision A8 silicon.

Adds silicon issues 38-40 (PWM).

Modifies the Affected Families and Silicon Revisions table for issue 25 (PWM) with respect to the dsPIC33/PIC24EP512 devices. Updated Figure 1, relevant to issue 20 (PWM).

### Rev H Document (02/2014)

Updates document to include silicon revision A8 for 128-Kbyte devices. All references to "ECAN" in this document are now changed to "CAN".

Added silicon issue 41 (CAN).

Updated Table 2, relevant to issue 41 (CAN). Modifies the Affected Families and Silicon Revisions table for issue 26 (PWM) and issue 36 (PWM).

### Rev J Document (3/2014)

Updates document to include silicon revision A8 for 32-Kbyte devices.

Adds data sheet clarifications 1 (Electrical Characteristics), 2 (DC and AC Device Characteristics Graphs), 3 (Electrical Characteristics), 4 (Electrical Characteristics), 5 (Electrical Characteristics) and 6 (High-Temperature Electrical Characteristics).

### Rev K Document (7/2014)

Updates document to add silicon revision A8 to all 256 Kbyte devices. Adds all existing silicon issues affecting silicon revision A8 for 64 Kbyte devices to revision A8 for 256 Kbyte devices.

Adds new silicon issues 42, 43 and 44 (PWM).

Amends silicon issue 4 (SPI) by correcting the state of the SPIFSD bit to '0'. (The text of the issue is otherwise unaffected and the issue is unchanged.)

Amends silicon issue 8 (PTG) by correcting the base prefix of the affected commands to '0b' instead of '0h'. (The text of the issue is otherwise unaffected and the issue is unchanged.)

Amends Table 5 in the work around for silicon issue 36 (PWM) by deleting the row corresponding to PCLKDIV[2:0] = 111, since this is a reserved setting. The basic issue is unchanged.

Amends silicon issue 38 (PWM) by adding additional text to the first paragraph to clarify the nature of the observed glitch. The basic issue is unchanged.

Adds data sheet clarifications 7 (I/O Ports), 8 (10/12-Bit Analog-to-Digital Converter (ADC)) and 9-10 (Comparator/Op Amp).

### Rev L Document (12/2014)

Adds silicon revision A9 to dsPIC33EP256MC506. Adds silicon issues 45 (PWM) and 46 (PWM). Adds data sheet clarification 11 (Electrical Characteristics), 12 (High-Temperature Electrical Characteristics) and 13 (Power-Saving Features).

### Rev M Document (8/2017)

Updates silicon issue 2 (CPU).

Adds silicon issue 47 (CPU).

## Rev N Document (5/2018)

Adds 36-pin UQFN package related data sheet clarifications: 14 ([Introduction](#)), 15 ([Introduction](#)), 16 ([Packaging Information](#)), 17 ([Packaging Information](#)), 18 ([Electrical Characteristics](#)) and 19 ([Product Identification System](#)).

## Rev P Document (8/2019)

Adds data sheet clarification 20 ([High-Temperature Electrical Characteristics](#)).

## Rev Q Document (10/2019)

Updated silicon issue 12 ([Flash](#)).

## Rev R Document (6/2020)

Updated all Affected Families and Silicon Revision tables to a new format.

Removed silicon issue 29 ([JTAG](#)) since it no longer applies.

Removed all data sheet clarifications because the issues were corrected in the latest data sheet revision.

NOTES:

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