

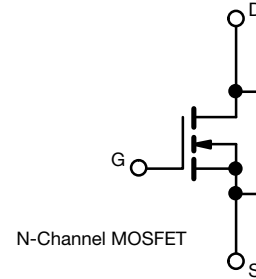
Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE


RoHS
 COMPLIANT
 HALOGEN
FREE


PRODUCT SUMMARY	
V _{DS} (V)	40
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0050
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.0075
I _D (A)	123
Configuration	Single
Package	PowerPAK SO-8L

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	40	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current	T _C = 25 °C	I _D	123	A
	T _C = 125 °C		71	
Continuous source current (diode conduction)		I _S	124	
Pulsed drain current ^a		I _{DM}	168	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	14	
Single pulse avalanche energy		E _{AS}	9.8	
Maximum power dissipation ^a	T _C = 25 °C	P _D	136	W
	T _C = 125 °C		45	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^b	R _{thJA}	42	°C/W
Junction-to-case (drain)		R _{thJC}	1.1	

Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.2	1.7	2.2	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$	-	0.004	0.0050	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0085	
		$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0100	
		$V_{GS} = 4.5\text{ V}$	$I_D = 15\text{ A}$	-	0.0055	0.0075	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		-	69	-	S
Dynamic ^b							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	1166	1633	μF
Output capacitance	C_{oss}			-	412	577	
Reverse transfer capacitance	C_{rss}			-	57	80	
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 15\text{ A}$	-	22.5	34	nC
Gate-source charge ^c	Q_{gs}			-	4	-	
Gate-drain charge ^c	Q_{gd}			-	4.3	-	
Gate resistance	R_g	f = 1 MHz		3.5	5.9	9.4	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1.33\text{ }\Omega$ $I_D \cong 15\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	9.6	13.5	ns
Rise time ^c	t_r			-	4.3	6.1	
Turn-off delay time ^c	$t_{d(off)}$			-	25	35	
Fall time ^c	t_f			-	8.5	12	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I_{SM}			-	-	168	A
Forward voltage	V_{SD}	$I_F = 15\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		-	28	42	ns
Body diode reverse recovery charge	Q_{rr}			-	12	18	nC
Reverse recovery fall time	t_a			-	10	14	ns
Reverse recovery rise time	t_b			-	16	28	
Body diode peak reverse recovery current	$I_{RM(REC)}$					-	0.8

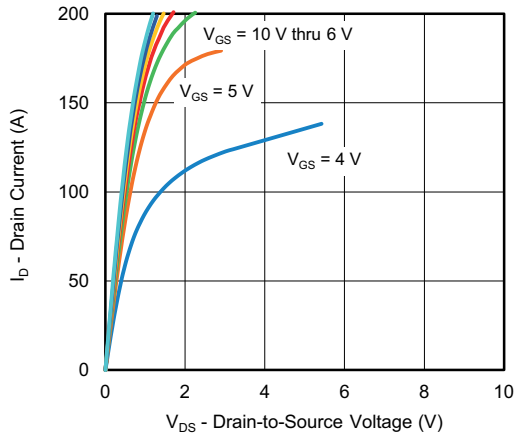
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

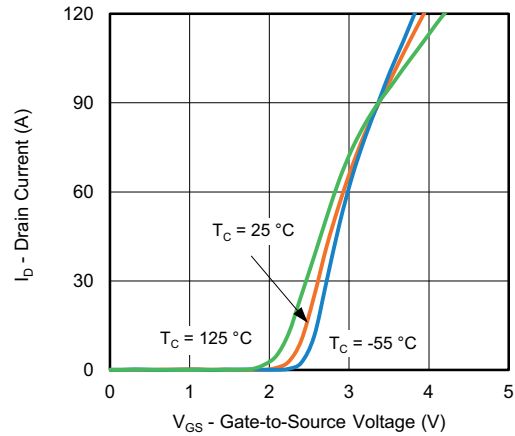
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



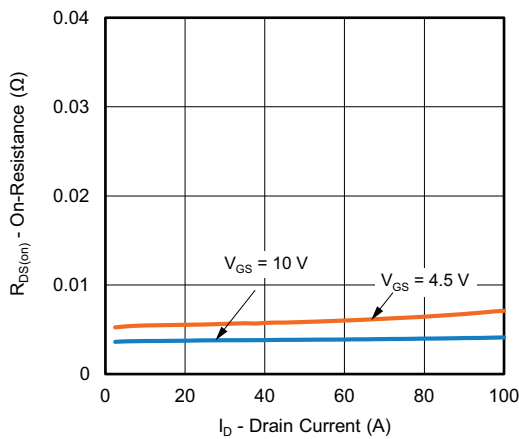
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



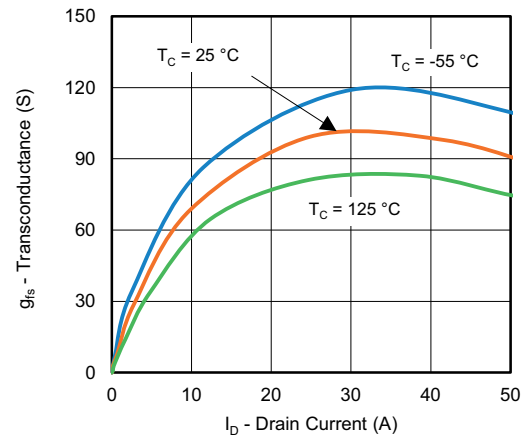
Output Characteristics



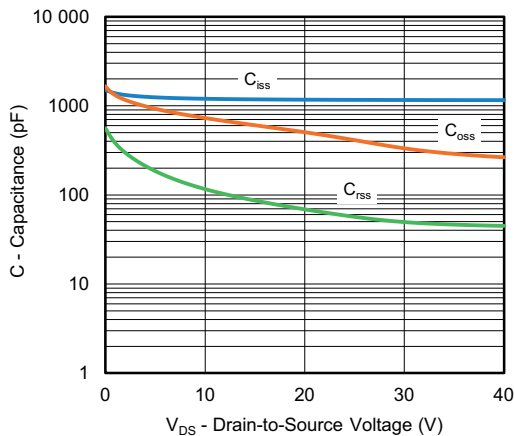
Transfer Characteristics



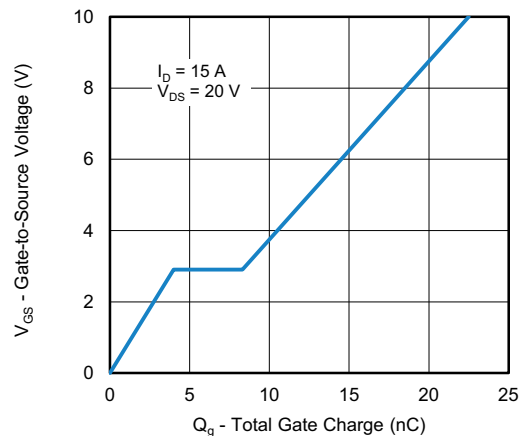
On-Resistance vs. Drain Current



Transconductance

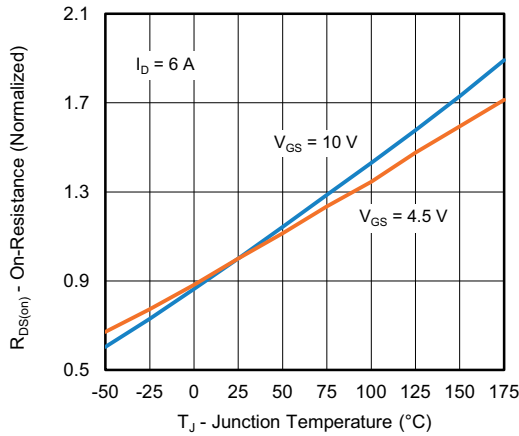


Capacitance

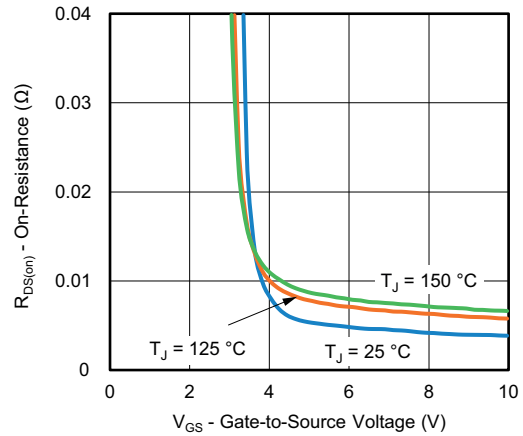


Gate Charge

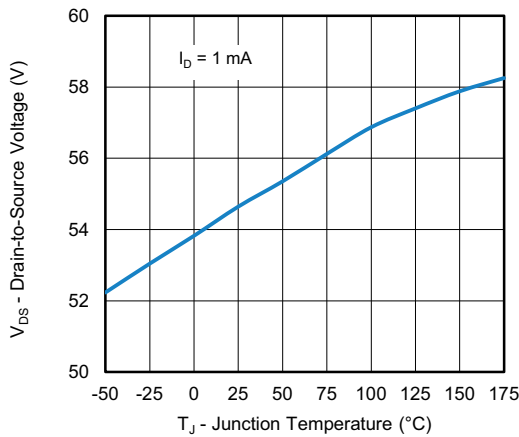
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



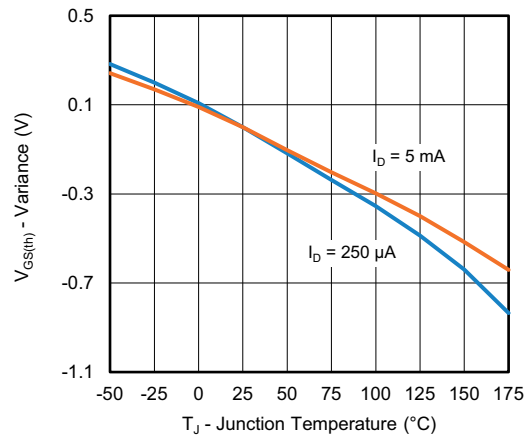
On-Resistance vs. Junction Temperature



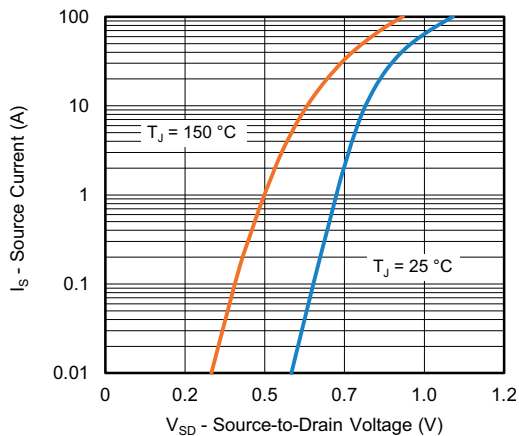
On-Resistance vs. Gate-to Source Voltage



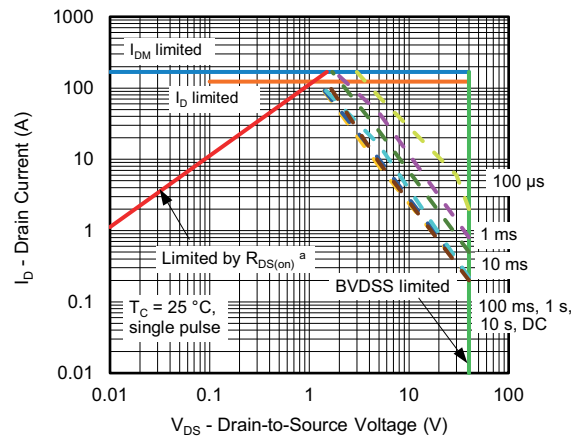
Drain Source Breakdown vs. Junction Temperature



Threshold Voltage



Source Drain Diode Forward Voltage



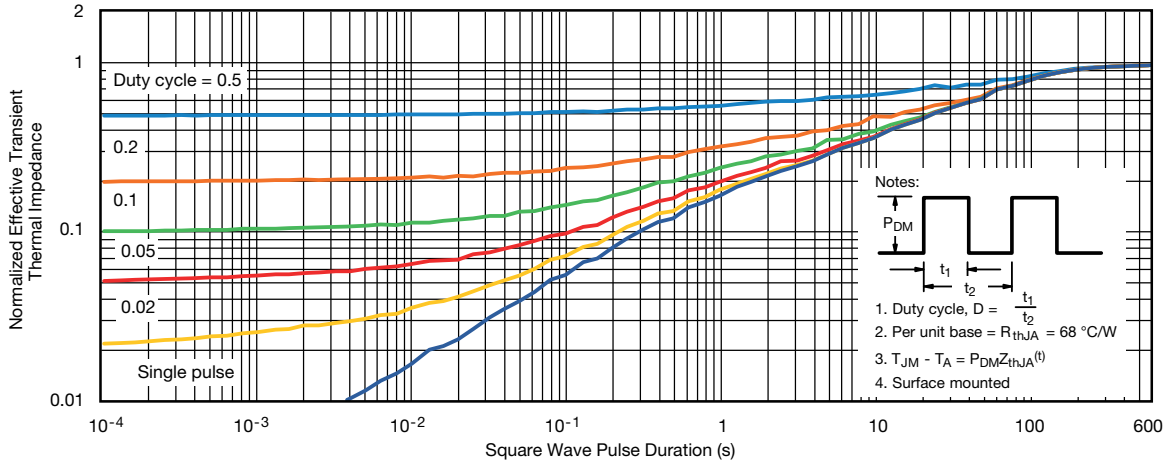
Safe Operating Area

Note

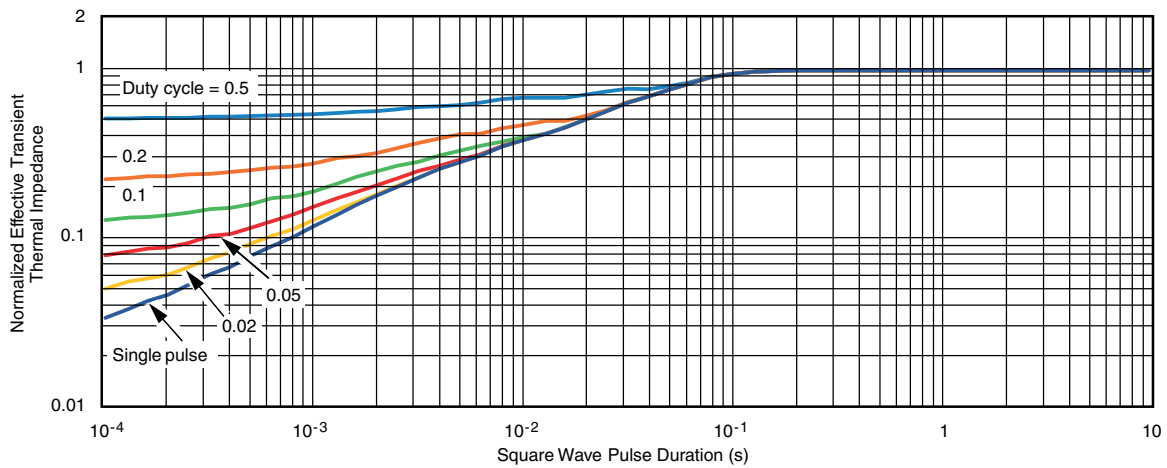
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

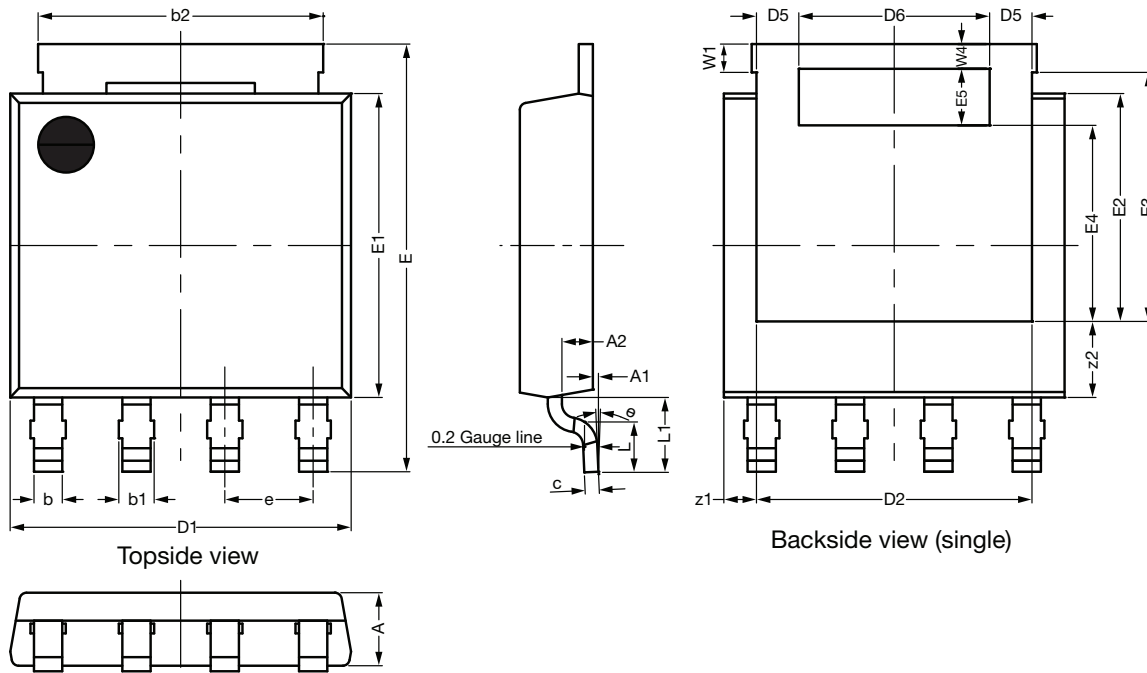
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79684.



PowerPAK® SO-8L Case Outline 3



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	---	0.127	0.000	---	0.005
A2	0.40	0.45	0.50	0.016	0.018	0.020
b	0.33	0.41	0.49	0.013	0.016	0.019
b1	0.43	0.51	0.59	0.017	0.020	0.023
b2	4.00	4.10	4.20	0.157	0.161	0.165
c	0.15	0.20	0.25	0.006	0.008	0.010
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D5	0.51	0.61	0.71	0.020	0.024	0.028
D6	2.64	2.74	2.84	0.104	0.108	0.112
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
E3	3.48	3.58	3.68	0.137	0.141	0.145
E4	2.72	2.82	2.92	0.107	0.111	0.115
E5	0.71	0.81	0.91	0.028	0.032	0.036
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
W1	0.31	0.41	0.51	0.012	0.016	0.020
W4	0.31	0.36	0.41	0.012	0.014	0.016
z1	0.37	0.47	0.57	0.015	0.019	0.022
z2	0.99	1.09	1.19	0.039	0.043	0.047
θ	0°	---	5°	0°	---	5°

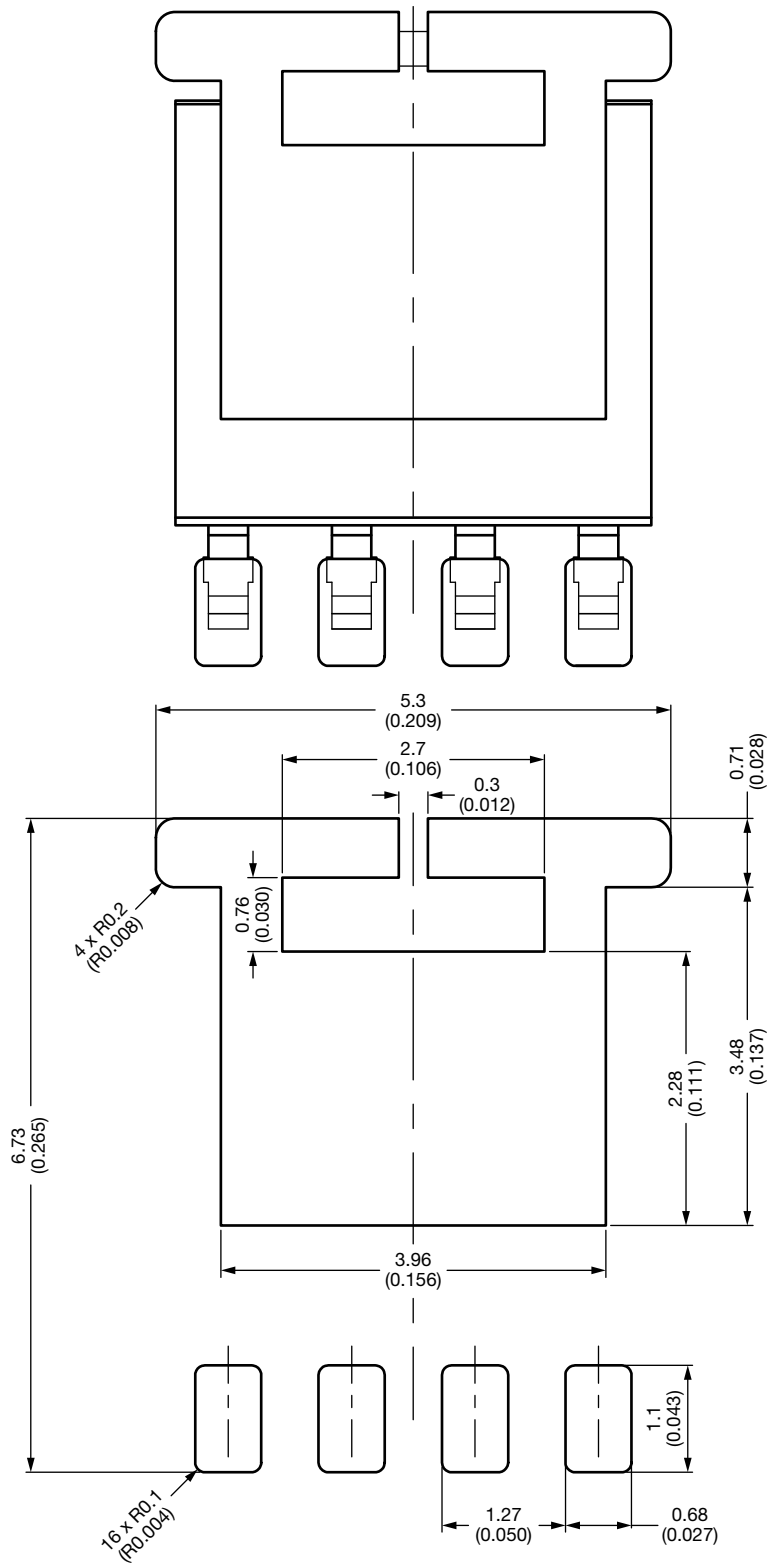
ECN: S19-0643-Rev. B, 05-Aug-2019
 DWG: 6067

Note

- Millimeter will govern



Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)



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