



Final Product Change Notification

202008044F01

Issue Date: 13-Sep-2020

Effective Date: 11-Dec-2020

Dear *Gordon Love*,

Here's your personalized quality information concerning products Premier Farnell PLC purchased from NXP.

For detailed information we invite you to [view this notification online](#)

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Management Summary

The LPC175x and LPC176x will be upgraded to revision C and Powerchip will be added as a second source wafer fab for product in LQFP80 and TFBGA100 packages.

Change Category

<input type="checkbox"/> Wafer Fab Process	<input type="checkbox"/> Assembly Process	<input type="checkbox"/> Product Marking	<input type="checkbox"/> Test Location	<input checked="" type="checkbox"/> Design
<input type="checkbox"/> Wafer Fab Materials	<input checked="" type="checkbox"/> Assembly Materials	<input type="checkbox"/> Mechanical Specification	<input type="checkbox"/> Test Process	<input checked="" type="checkbox"/> Errata
<input checked="" type="checkbox"/> Wafer Fab Location	<input type="checkbox"/> Assembly Location	<input type="checkbox"/> Packing/Shipping/Labeling	<input type="checkbox"/> Test Equipment	<input type="checkbox"/> Electrical spec./Test coverage
<input type="checkbox"/> Firmware	<input type="checkbox"/> Other			

LPC175x/6x Revision
Change to Rev C and
Addition of 2nd Source
Wafer Fab for Product in
LQFP80 and TFBGA100
Packages

Description of Change

The silicon wafers are currently produced in SSMC. Powerchip (PTCF12) has been qualified as a 2nd source wafer fab for LPC175x and LPC176x products in the LQFP80 and TFBGA100 packages.

- No change in ordering part number / 12NC.
- Assembly location and final test location remains unchanged at NXP Assembly and Test Kaohsiung (ATKH).
- No changes in datasheet parameters. New device revisions have been added to updated datasheets.

The die revision will be changed from Rev A to Rev C which includes design changes to fix the following errata: ADC.1, GPIO.2, I2S.1, PLL0.1 and USB.1.

Updated errata sheets and data sheets are available on the NXP website:

https://www.nxp.com/docs/en/errata/ES_LPC176X.pdf.

https://www.nxp.com/docs/en/errata/ES_LPC175X.pdf.

https://www.nxp.com/docs/en/data-sheet/LPC1759_58_56_54_52_51.pdf

https://www.nxp.com/docs/en/data-sheet/LPC1769_68_67_66_65_64_63.pdf

For existing product in TFBGA100 packages, the bond wire changes from Au to Cu and the mold compound changes from CEL-9750HF10F to CEL-9750HF10CH.

Samples of the following superset part numbers are available:

LPC1759FBD80

LPC1768FET100

Reason for Change

To ensure wafer supply with increased capacity and to resolve errata issues.

Identification of Affected Products

Top side marking

Product version is incremented from "A" to "C". See marking details in attached Self Qualification Report (SQR) document.

Product Availability

Sample Information

Samples are available from 11-Sep-2020

Production

Planned first shipment 09-Dec-2020

Anticipated Impact on Form, Fit, Function, Reliability or Quality

The product marking changes and errata issues are resolved as identified above.

Data Sheet Revision

A new datasheet will be issued

Disposition of Old Products

Existing inventory will be shipped until depleted

Additional information

Affected products and sales history information: see attached file

Self qualification: [view online](#)

Additional documents: [view online](#)

Timing and Logistics

In compliance with JEDEC J-STD-046, your acknowledgement of this change is expected by 13-Oct-2020.

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please [contact NXP "Global Quality Support Team"](#).

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

Name Tim Camenzind

Position Quality Manager, LPC Microcontroller Products

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NXP Quality Management Team.

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