

# NXS0102

Dual supply translating transceiver; open drain;  
auto direction sensing

Rev. 2 — 23 September 2020

Product data sheet

## 1. General description

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The NXS0102 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied at any voltage between 1.65 V and 3.6 V and  $V_{CC(B)}$  can be supplied at any voltage between 2.3 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to  $V_{CC(A)}$  and pins Bn are referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

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- Wide supply voltage range:
  - $V_{CC(A)}$ : 1.65 V to 3.6 V and  $V_{CC(B)}$ : 2.3 V to 5.5 V
- Maximum data rates:
  - Push-pull: 24 Mbps
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2.5 kV for A port
  - HBM: ANSI/ESDA/Jedec JS-001 Class 3B exceeds 8 kV for B port
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1.5 kV
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Applications

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- Desktop PC
- Handset
- Smartphone
- Tablet

## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NXS0102DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
NXS0102GT <sup>[1]</sup>	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

[1] This product is in development.

## 5. Marking

Table 2. Marking

Type number	Marking code
NXS0102DC	m2
NXS0102GT	m2

## 6. Functional diagram

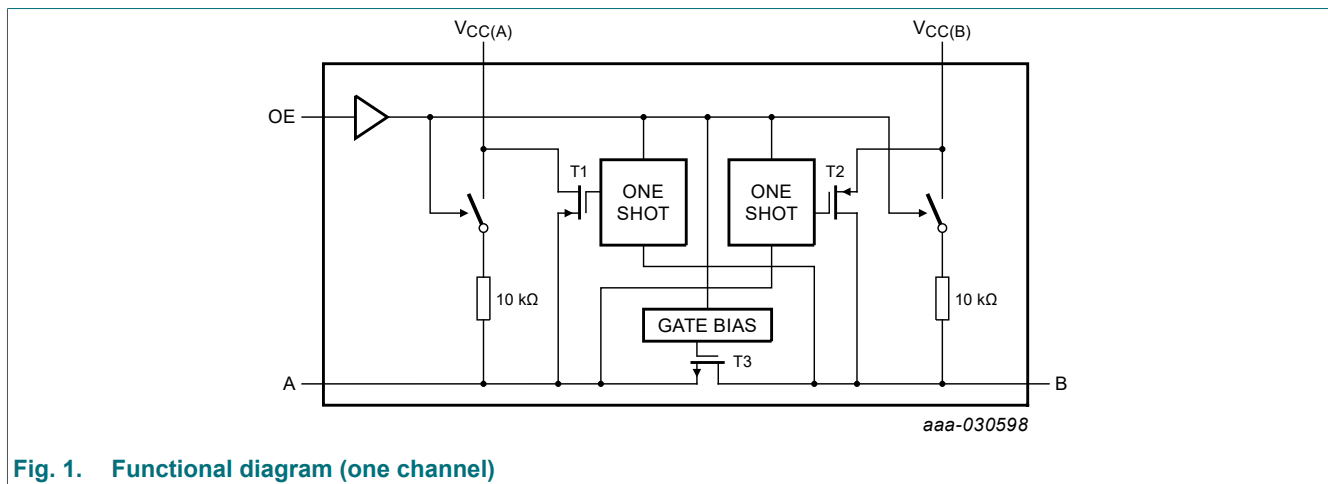


Fig. 1. Functional diagram (one channel)

## 7. Pinning information

### 7.1. Pinning

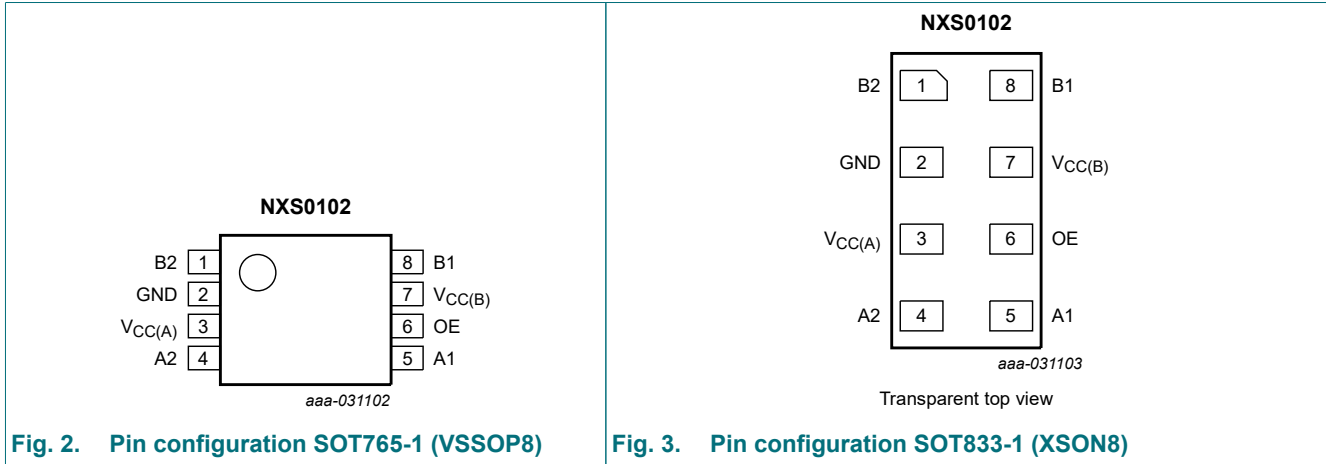


Fig. 2. Pin configuration SOT765-1 (VSSOP8)

Fig. 3. Pin configuration SOT833-1 (XSON8)

### 7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B2, B1	1, 8	data input or output (referenced to V <sub>CC(B)</sub> )
GND	2	ground (0 V)
V <sub>CC(A)</sub>	3	supply voltage A
A2, A1	4, 5	data input or output (referenced to V <sub>CC(A)</sub> )
OE	6	output enable input (active HIGH; referenced to V <sub>CC(A)</sub> )
V <sub>CC(B)</sub>	7	supply voltage B

## 8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage		Input	Input/output	
V <sub>CC(A)</sub> [1]	V <sub>CC(B)</sub>	OE	An	Bn
1.65 V to 3.6 V	2.3 V to 5.5 V	L	Z	Z
1.65 V to 3.6 V	2.3 V to 5.5 V	H	input or output	output or input
GND	2.3 V to 5.5 V	X	Z	Z
1.65 V to 3.6 V	GND	X	Z	Z

[1] V<sub>CC(A)</sub> must be less than or equal to V<sub>CC(B)</sub>.

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
$V_I$	input voltage	OE [1]	-0.5	+6.5	V
		Power-down or 3-state mode			
		A, B [1]	-0.5	+6.5	V
		Active mode			
$V_O$	output voltage	Power-down or 3-state mode			
		A, B [1]	-0.5	+6.5	V
		Active mode			
		A, B [1] [3] [4]	-0.5	$V_{CC1} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$ [4]	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [5]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CC1}$  is the supply voltage associated with the input.

[3]  $V_{CC1} + 0.5$  V or  $V_{CCO} + 0.5$  V should not exceed 6.5 V.

[4]  $V_{CCO}$  is the supply voltage associated with the output.

[5] For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) package:  $P_{tot}$  derates linearly with 3.1 mW/K above 68 °C.

## 10. Recommended operating conditions

Table 6. Recommended operating conditions [1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
$V_I$	input voltage	OE	0	5.5	V
		Power-down or 3-state mode			
		A	0	3.6	V
		B	0	5.5	V
		Active mode A, B [3]	0	$V_{CCI}$	V
$V_O$	output voltage	Power-down or 3-state mode			
		A	0	3.6	V
		B	0	5.5	V
		Active mode A, B [4]	0	$V_{CCO}$	V
		$T_{amb}$	ambient temperature		-40
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	10	ns/V
		OE input			
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at  $V_{CCI}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

[3]  $V_{CCI}$  is the supply voltage associated with the input.

[4]  $V_{CCO}$  is the supply voltage associated with the output.

## 11. Static characteristics

**Table 7. Typical static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ . [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_I$	input leakage current	OE input; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ ; $OE = 0\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
		B port; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$				
		enabled	-	10	-	pF
		disabled	-	4	-	pF
		B port; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$				
		enabled	-	10	-	pF
	disabled	-	7	-	pF	

[1]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

**Table 8. Typical supply current**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	$\mu\text{A}$
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	$\mu\text{A}$
3.3 V	-	-	0.1	0.1	0.1	2.8	$\mu\text{A}$

## Dual supply translating transceiver; open drain; auto direction sensing

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	A port					
		V <sub>CC(A)</sub> = 1.65 V to 1.95 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	V <sub>CC(A)</sub> - 0.2	V <sub>CC(A)</sub>	V <sub>CC(A)</sub> - 0.2	V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 2.3 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	V <sub>CC(A)</sub> - 0.4	V <sub>CC(A)</sub>	V <sub>CC(A)</sub> - 0.4	V <sub>CC(A)</sub>	V
		B port					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	V <sub>CC(B)</sub> - 0.4	V <sub>CC(B)</sub>	V <sub>CC(B)</sub> - 0.4	V <sub>CC(B)</sub>	V
		OE input					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0.65V <sub>CC(A)</sub>	V <sub>CC(A)</sub>	0.65V <sub>CC(A)</sub>	V <sub>CC(A)</sub>	V
V <sub>IL</sub>	LOW-level input voltage	A or B port					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0	0.15	0	0.15	V
		OE input					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0	0.35V <sub>CC(A)</sub>	0	0.35V <sub>CC(A)</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	A port; I <sub>O</sub> = -20 μA; V <sub>I</sub> ≥ V <sub>CC(B)</sub> - 0.4 V					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0.67V <sub>CC(A)</sub>	-	0.67V <sub>CC(A)</sub>	-	V
		B port; I <sub>O</sub> = -20 μA; V <sub>I</sub> ≥ V <sub>CC(A)</sub> - 0.2 V					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0.67V <sub>CC(B)</sub>	-	0.67V <sub>CC(B)</sub>	-	V
V <sub>OL</sub>	LOW-level output voltage	A or B port; I <sub>O</sub> = 1 mA; V <sub>I</sub> ≤ 0.15 V					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.4	-	0.4	V
I <sub>I</sub>	input leakage current	OE input; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	±2	-	±12	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	±2	-	±12	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0 V to 5.5 V	-	±2	-	±12	μA
		B port; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0 V to 3.6 V	-	±2	-	±12	μA

## Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	OE = 0 V or V <sub>CC(A)</sub> ; An, Bn open					
		I <sub>CC(A)</sub>					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	2.4	-	15	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	2.2	-	15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	-1	-	-8	μA
		I <sub>CC(B)</sub>					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	12	-	30	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	-1	-	-5	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	1	-	6	μA
		I <sub>CC(A)</sub> + I <sub>CC(B)</sub>					
V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	14.4	-	30	μA		

[1] V<sub>CC(A)</sub> must be less than or equal to V<sub>CC(B)</sub> and V<sub>CC(A)</sub> must not exceed 3.6 V.

## 12. Dynamic characteristics

**Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 4 to Fig. 6.

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.8 V ± 0.15 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	5.3	-	5.4	-	6.8	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	7.1	-	7.1	-	7.5	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	4.4	-	4.5	-	4.7	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	5.3	-	4.5	-	0.5	ns
t <sub>en</sub>	enable time	OE to A, B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A, B; no external load [1] [2]	-	35	-	35	-	35	ns
		OE to A	-	230	-	230	-	230	ns
		OE to B	-	200	-	200	-	200	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.9	2.8	10.5	ns
t <sub>sk(o)</sub>	output skew time	between channels [3]	-	0.7	-	0.7	-	0.7	ns
t <sub>W</sub>	pulse width	data inputs	41	-	41	-	41	-	ns
f <sub>data</sub>	data rate		-	24	-	24	-	24	Mbps



## Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	3.2	-	3.7	-	3.8	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	3.5	-	4.4	-	4.6	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	3.0	-	3.6	-	4.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	2.5	-	1.6	-	1.0	ns
$t_{en}$	enable time	OE to A, B	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	35	-	35	-	35	ns
		OE to A	-	200	-	200	-	200	ns
		OE to B	-	200	-	200	-	200	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	2.8	7.5	2.6	6.6	1.8	6.5	ns
		B port	3.2	8.5	2.9	7.9	2.4	6.8	ns
$t_{THL}$	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.9	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.7	-	0.7	-	0.7	ns
$t_W$	pulse width	data inputs	41	-	41	-	41	-	ns
$f_{data}$	data rate		-	24	-	24	-	24	Mbps
<b><math>V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	2.4	-	3.1	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	4.2	-	4.4	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	2.5	-	3.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	2.5	-	2.6	ns
$t_{en}$	enable time	OE to A, B	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	-	-	35	-	35	ns
		OE to A	-	-	-	260	-	260	ns
		OE to B	-	-	-	200	-	200	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	2.3	6.2	1.9	6.3	ns
		B port	-	-	2.5	6.9	2.1	7.4	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	2.0	5.4	1.9	5.0	ns
		B port	-	-	2.3	7.4	2.4	7.6	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.7	-	0.7	ns
$t_W$	pulse width	data inputs	-	-	41	-	41	-	ns
$f_{data}$	data rate		-	-	-	24	-	24	Mbps

[1]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[2] The disable time with no external load indicates the delay between when OE goes LOW and when outputs actually become disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

## Dual supply translating transceiver; open drain; auto direction sensing

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 4 to Fig. 6.

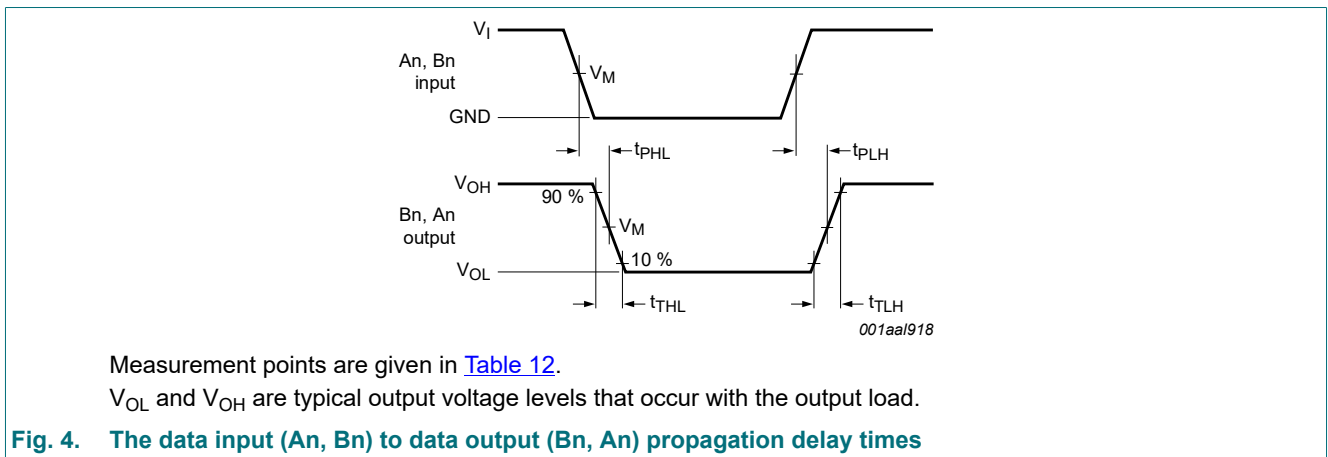
Symbol	Parameter	Conditions	V <sub>CC(B)</sub>						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.8 V ± 0.15 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	0.7	ns
t <sub>en</sub>	enable time	OE to A, B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A, B; no external load [1] [2]	-	45	-	45	-	45	ns
		OE to A	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
t <sub>sk(o)</sub>	output skew time	between channels [3]	-	0.8	-	0.8	-	0.8	ns
t <sub>W</sub>	pulse width	data inputs	50	-	41	-	41	-	ns
f <sub>data</sub>	data rate		-	20	-	24	-	24	Mbps
<b>V<sub>CC(A)</sub> = 2.5 V ± 0.2 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	0.9	ns
t <sub>en</sub>	enable time	OE to A, B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A, B; no external load [1] [2]	-	45	-	45	-	45	ns
		OE to A	-	220	-	220	-	220	ns
		OE to B	-	220	-	220	-	220	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns
t <sub>sk(o)</sub>	output skew time	between channels [3]	-	0.8	-	0.8	-	0.8	ns
t <sub>W</sub>	pulse width	data inputs	50	-	41	-	41	-	ns
f <sub>data</sub>	data rate		-	20	-	24	-	24	Mbps

Dual supply translating transceiver; open drain; auto direction sensing

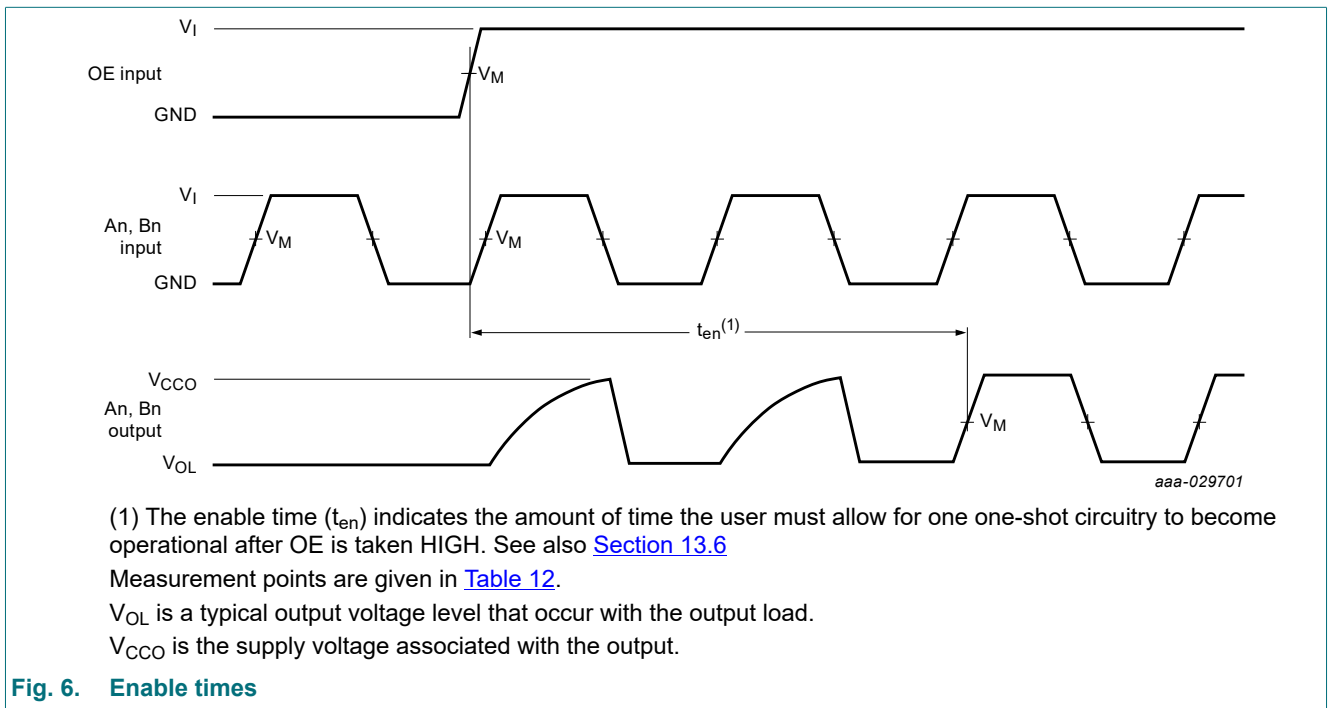
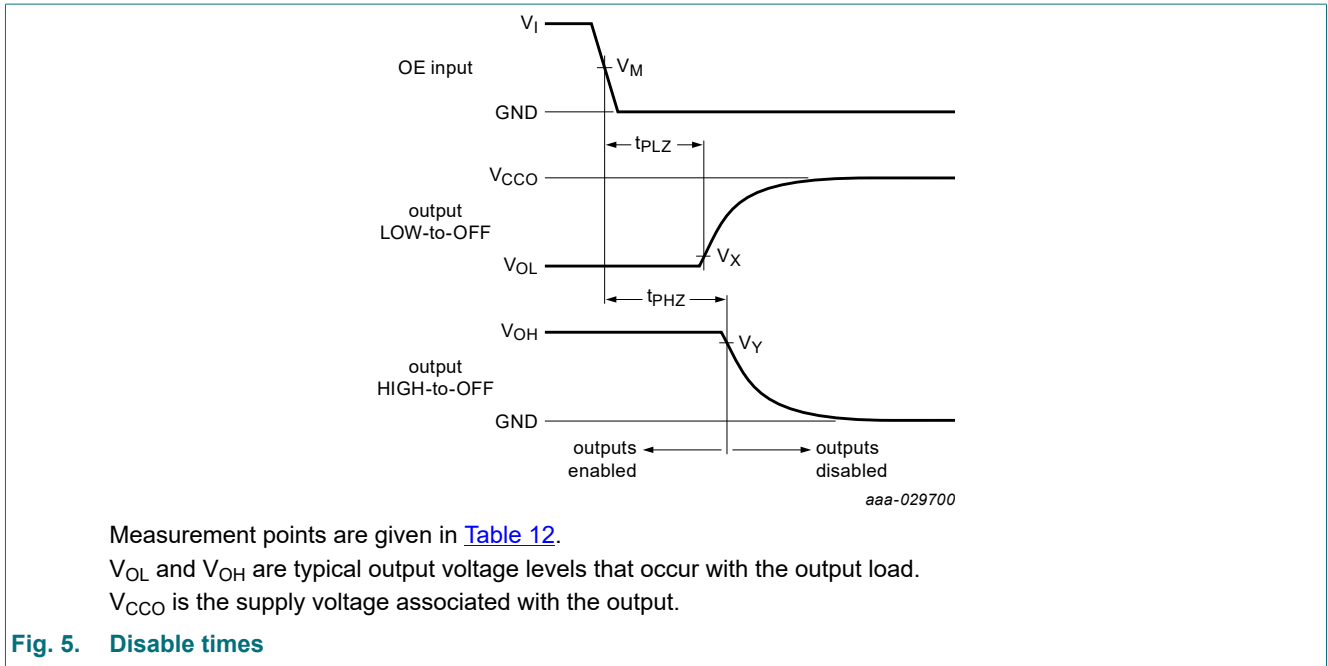
Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}$									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns
$t_{en}$	enable time	OE to A, B	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	-	-	45	-	45	ns
		OE to A	-	-	-	280	-	280	ns
		OE to B	-	-	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	2.3	7.0	1.9	7.4	ns
		B port	-	-	2.5	8.0	2.1	9.3	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	2.0	6.8	1.9	6.3	ns
		B port	-	-	2.3	9.3	2.4	9.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.8	-	0.8	ns
$t_W$	pulse width	data inputs	-	-	41	-	41	-	ns
$f_{data}$	data rate		-	-	-	24	-	24	Mbps

- [1]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [2] The disable time with no external load indicates the delay between when OE goes LOW and when outputs actually become disabled.
- [3] Skew between any two outputs of the same package switching in the same direction.

12.1. Waveforms and test circuit



Dual supply translating transceiver; open drain; auto direction sensing



**Table 12. Measurement points**

Supply voltage	Input	Output		
$V_{CCO}$	$V_M$ [1]	$V_M$ [2]	$V_X$	$V_Y$
1.8 V ± 0.15 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.5 V ± 0.2 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.3 V ± 0.3 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
5.0 V ± 0.5 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

[1]  $V_{CCI}$  is the supply voltage associated with the input.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output.

Dual supply translating transceiver; open drain; auto direction sensing

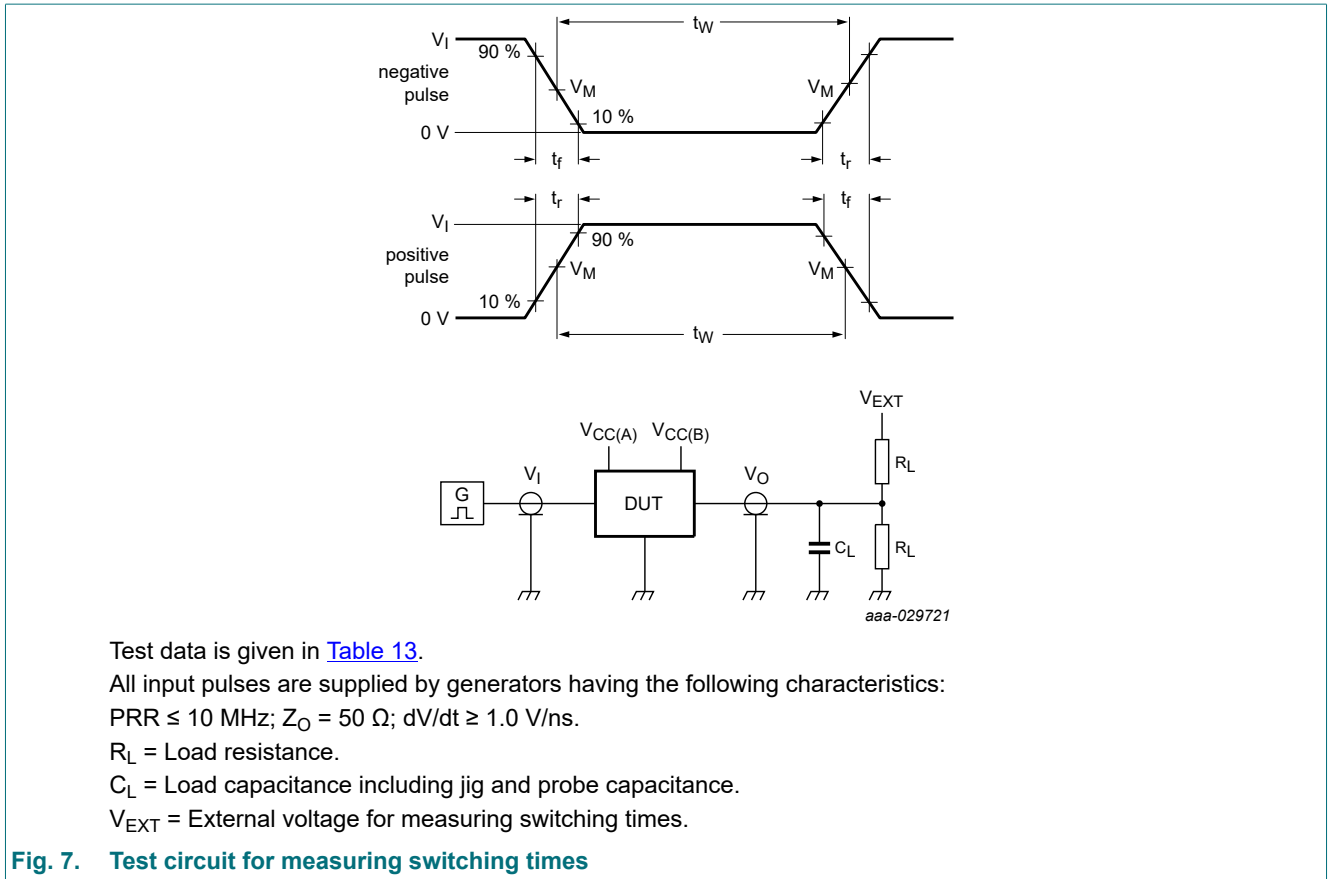


Table 13. Test data

Supply voltage		Input		Load		$V_{EXT}$		
$V_{CC(A)}$	$V_{CC(B)}$	$V_I$ [1]	$\Delta t/\Delta V$	$C_L$	$R_L$ [2]	$t_{PLH}$ , $t_{PHL}$	$t_{PZH}$ , $t_{PHZ}$	$t_{PZL}$ , $t_{PLZ}$ [3]
1.65 V to 3.6 V	2.3 V to 5.5 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	50 k $\Omega$ , 1 M $\Omega$	open	open	$2V_{CCO}$

- [1]  $V_{CCI}$  is the supply voltage associated with the input.
- [2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements,  $R_L = 1 \text{ M}\Omega$ ;  
 for measuring enable and disable times,  $R_L = 50 \text{ k}\Omega$ .
- [3]  $V_{CCO}$  is the supply voltage associated with the output.

## 13. Application information

### 13.1. Applications

Voltage level-translation applications. The NXS0102 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I<sup>2</sup>C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports, however the NXB0102 may be more suitable.

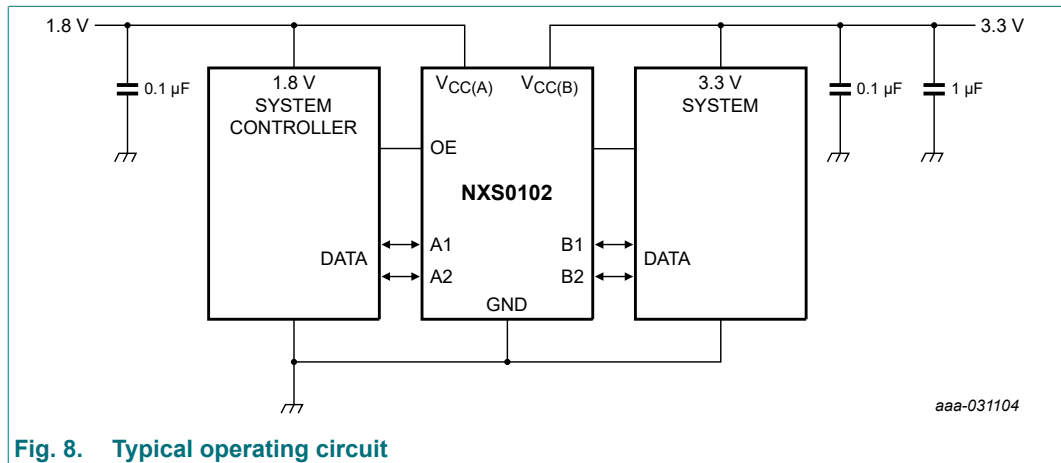


Fig. 8. Typical operating circuit

### 13.2. Architecture

The architecture of the NXS0102 is shown in Fig. 9. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

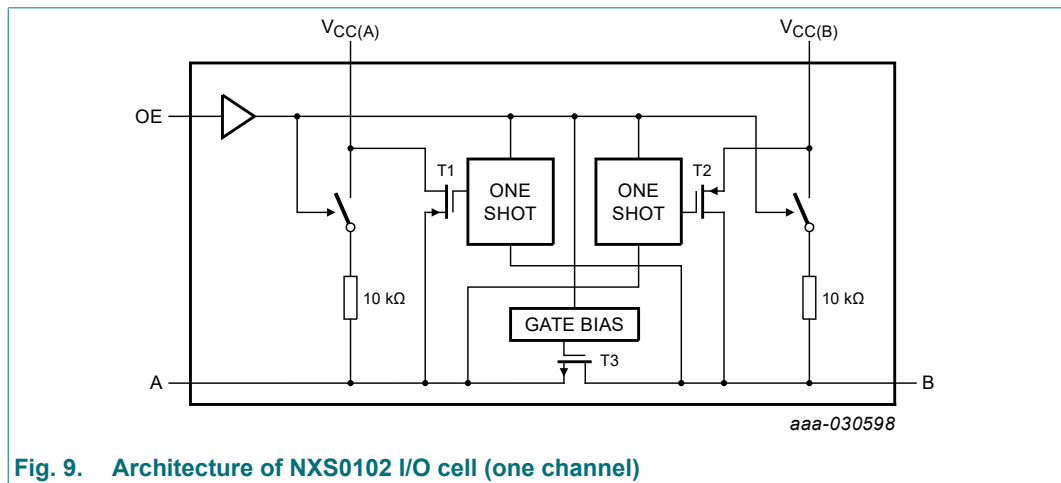


Fig. 9. Architecture of NXS0102 I/O cell (one channel)

The NXS0102 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the  $V_{CC(A)}$  level of the low-voltage side. During a rising edge, the one shots turn on the PMOS transistors (T1, T2) for a short duration, accelerating the low-to-high transition. The one-shot is activated once the input transition reaches approximately  $0.5V_{CC1}$ . During the acceleration time the driver output resistance is between approximately  $50\ \Omega$  and  $70\ \Omega$ . To avoid signal contention and minimize dynamic  $I_{CC}$ , the user should wait for the one-shot circuit to turn-off before applying a

## Dual supply translating transceiver; open drain; auto direction sensing

signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

### 13.3. Input driver requirements

As the NXS0102 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time ( $t_{THL}$ ) and propagation delay ( $t_{PHL}$ ) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50  $\Omega$  is used.

### 13.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on NXS0102 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration.

### 13.5. Power up

During operation  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ , however during power-up  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The NXS0102 includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

### 13.6. Enable and disable

An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### 13.7. Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(A)}$ , and each B port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(B)}$ . If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 k $\Omega$ , this will effect the  $V_{OL}$  level. When OE goes LOW the internal pull-ups of the NXS0102 are disabled.

14. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

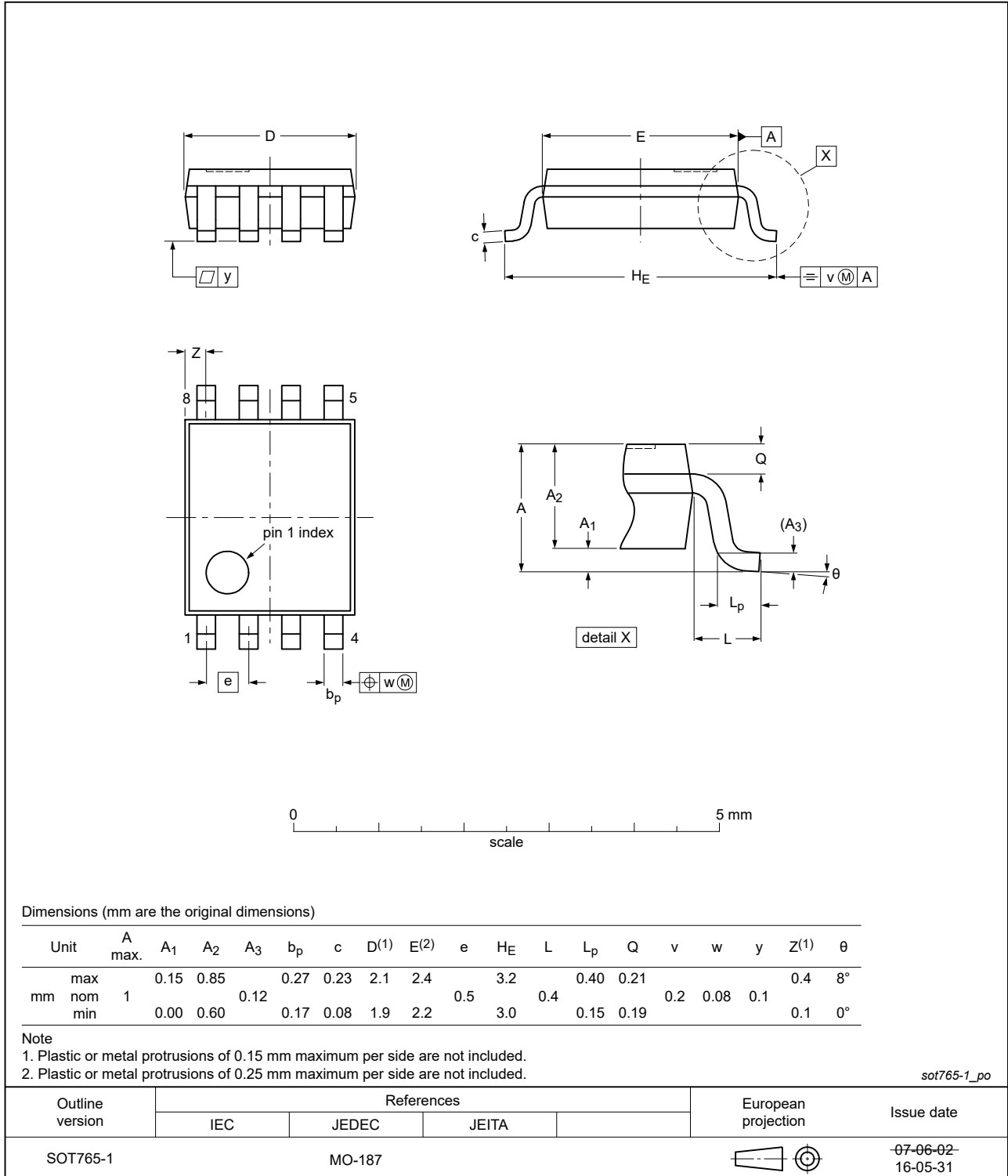
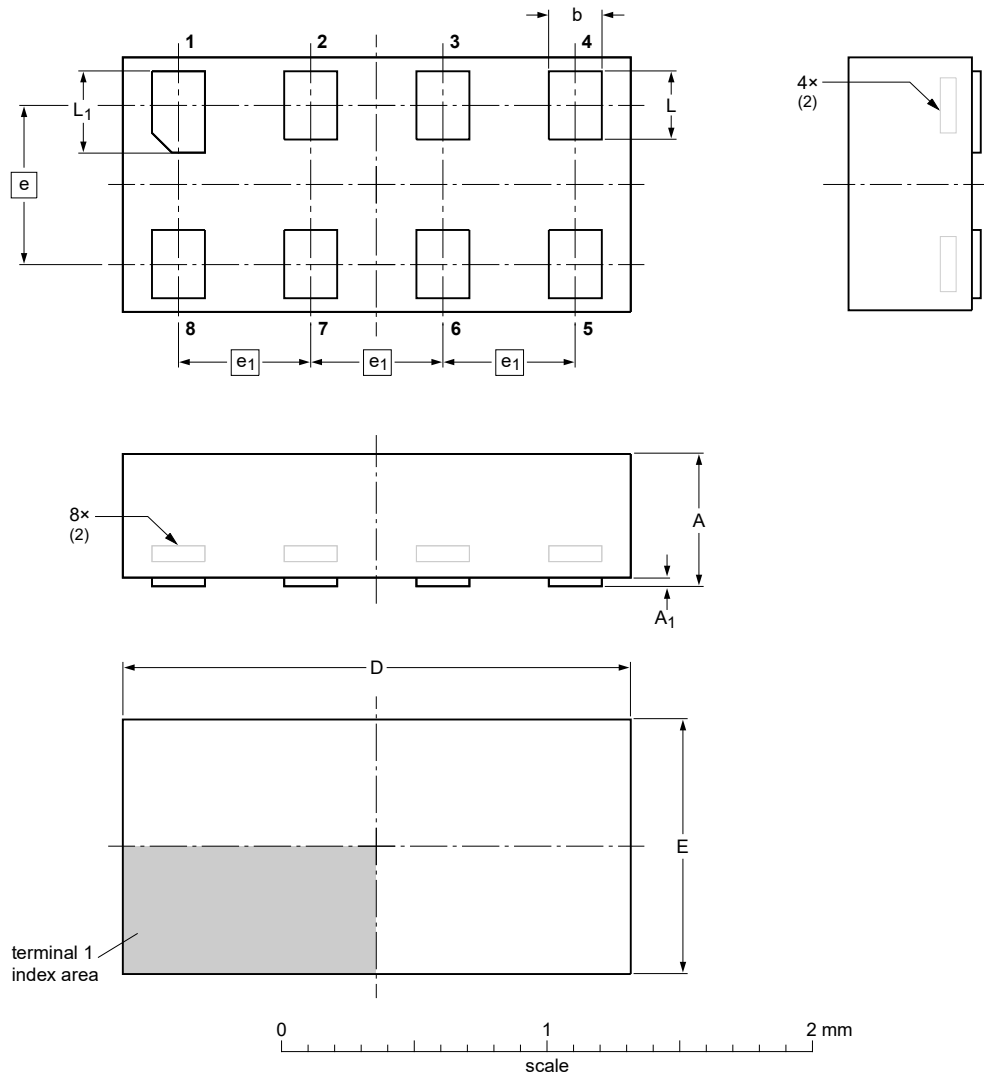


Fig. 10. Package outline SOT765-1 (VSSOP8)



XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max	A <sub>1</sub> max	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

**Notes**

- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		-07-11-14 07-12-07

**Fig. 11. Package outline SOT833-1 (XSON8)**

## 15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition

## 16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXS0102 v.2	20200923	Product data sheet	-	NXS0102 v.1
Modifications:	<ul style="list-style-type: none"> <li>Type number NXS0102GT (SOT833-1/XSON8) added.</li> </ul>			
NXS0102 v.1	20191217	Product data sheet	-	-

## 17. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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