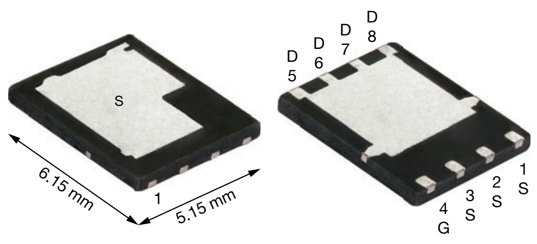
N-Channel 60 V (D-S) MOSFET

PowerPAK® SO-8DC



Top View　　Bottom View

PRODUCT SUMMARY

V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0015
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0021
Q_g typ. (nC)	41
I_D (A)	186
Configuration	Single

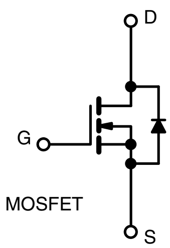
FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} - Q_g figure-of-merit (FOM)
- Tuned for the lowest R_{DS} - Q_{oss} FOM
- 100 % R_g and UIS tested
- Top side cooling feature provides additional venue for thermal transfer
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Solar micro inverter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR626LDP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	204	A
	T_C = 70 °C		163	
	T_A = 25 °C		45.6 [b, c]	
	T_A = 70 °C		36.5 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	300	
Continuous source-drain diode current	T_C = 25 °C	I_S	113	
	T_A = 25 °C		5.6 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	50	
Single pulse avalanche energy		E_{AS}	125	mJ
Maximum power dissipation	T_C = 25 °C	P_D	125	W
	T_C = 70 °C		80	
	T_A = 25 °C		6.25 [b, c]	
	T_A = 70 °C		4 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b]	t ≤ 10 s	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.8	1	
Maximum junction-to-case (source)	Steady state	R_{thJC}	1.1	1.4	

Notes

a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 54 °C/W
g. T_C = 25 °C

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 1 mA	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 1 mA	-	37	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 μA	-	-4.9	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1	-	2.5	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 70 °C	-	-	15	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \geq$ 10 V, V_{GS} = 10 V	40	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	-	0.0012	0.0015	Ω
		V_{GS} = 4.5 V, I_D = 20 A	-	0.0017	0.0021	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	-	140	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	-	5900	-	pF
Output capacitance	C_{oss}		-	1340	-	
Reverse transfer capacitance	C_{rss}		-	60	-	
Total gate charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 20 A	-	89	135	nC
		V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 20 A	-	41	62	
Gate-source charge	Q_{gs}		-	17.4	-	
Gate-drain charge	Q_{gd}		-	10.8	-	
Output charge	Q_{oss}	V_{DS} = 30 V, V_{GS} = 0 V	-	80	-	
Gate resistance	R_g	f = 1 MHz	0.3	0.88	1.5	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 3 Ω, $I_D \cong$ 20 A, V_{GEN} = 10 V, R_g = 1 Ω	-	17	34	ns
Rise time	t_r		-	64	128	
Turn-off delay time	$t_{d(off)}$		-	45	90	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1.5 Ω, $I_D \cong$ 20 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	40	80	
Rise time	t_r		-	235	470	
Turn-off delay time	$t_{d(off)}$		-	47	94	
Fall time	t_f		-	20	40	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	113	A
Pulse diode forward current	I_{SM}		-	-	400	
Body diode voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V	-	0.71	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 20 A, di/dt = 100 A/μs, T_J = 25 °C	-	54	108	ns
Body diode reverse recovery charge	Q_{rr}		-	70	140	nC
Reverse recovery fall time	t_a		-	27	-	ns
Reverse recovery rise time	t_b		-	27	-	

Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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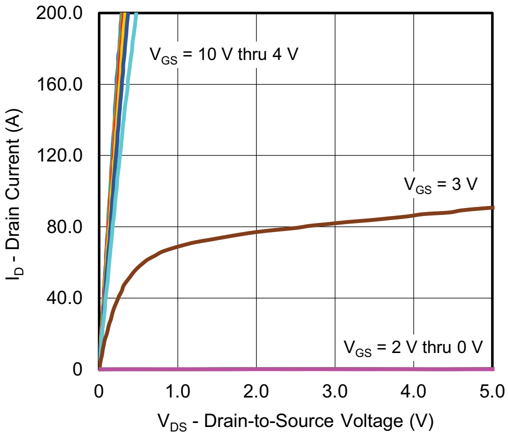
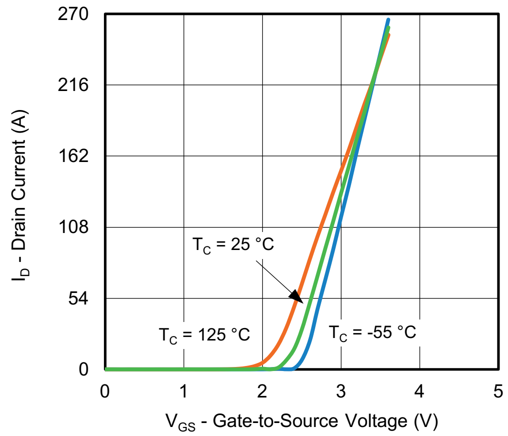
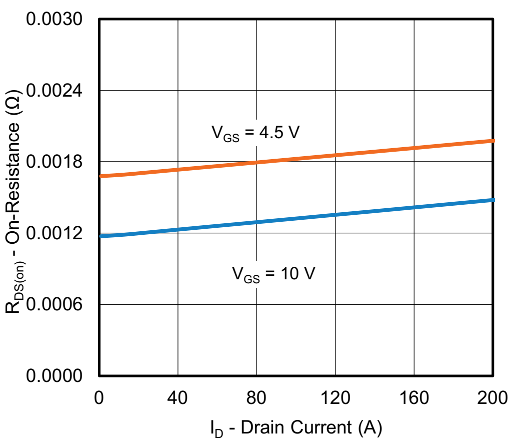
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



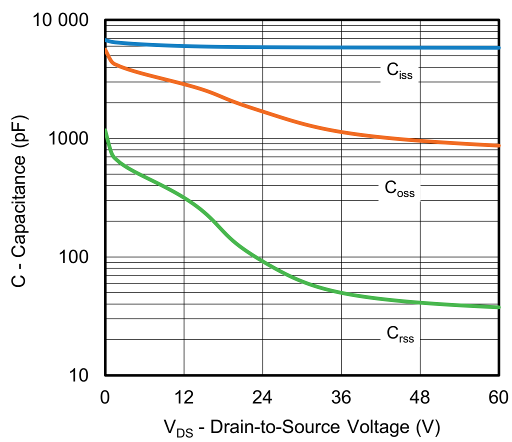
Output Characteristics



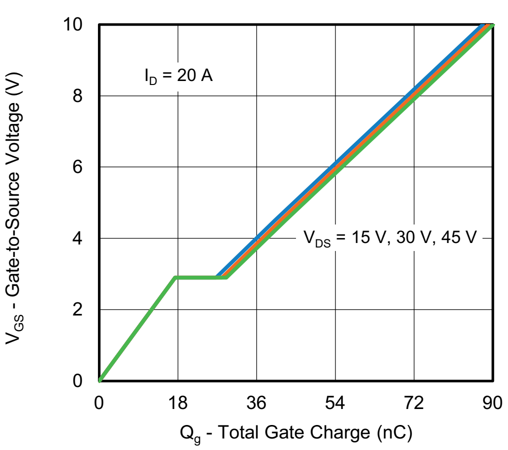
Transfer Characteristics



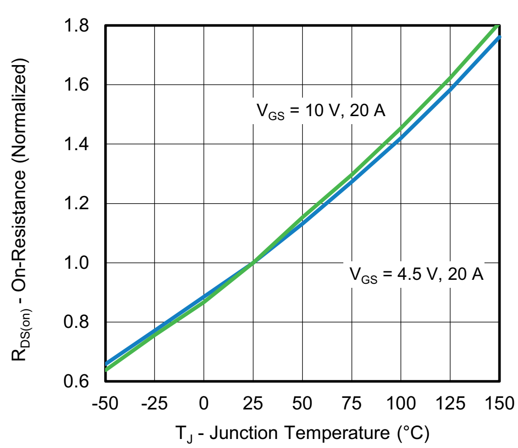
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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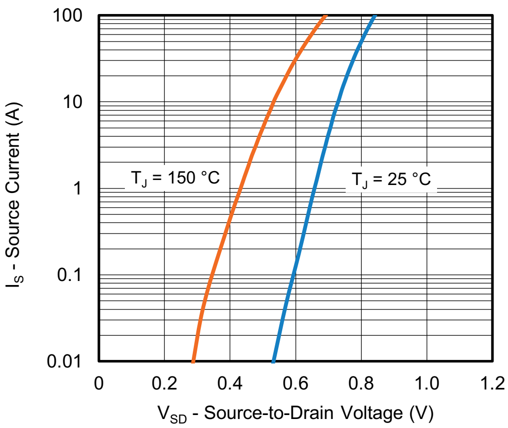
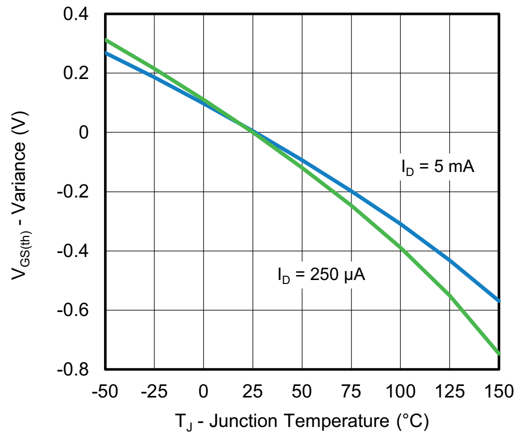
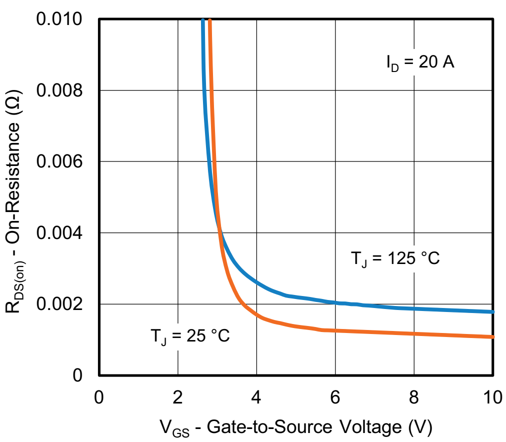


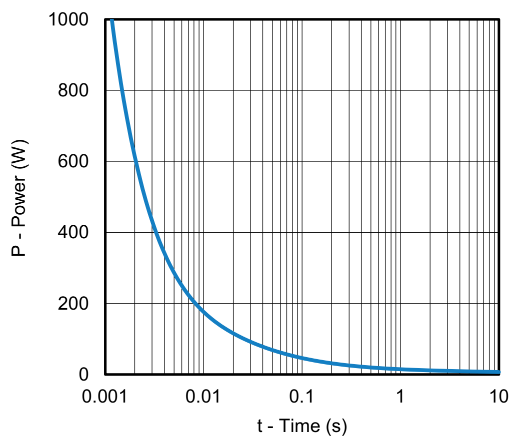
Source-Drain Diode Forward Voltage



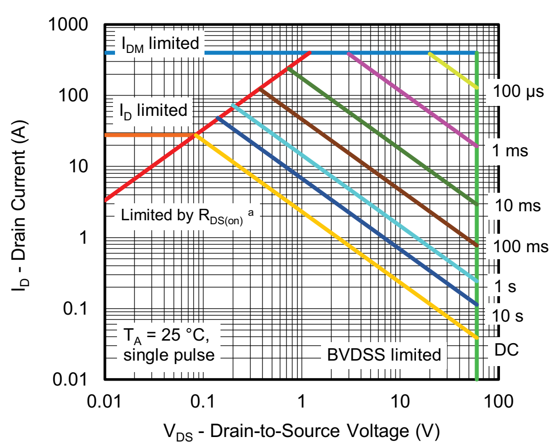
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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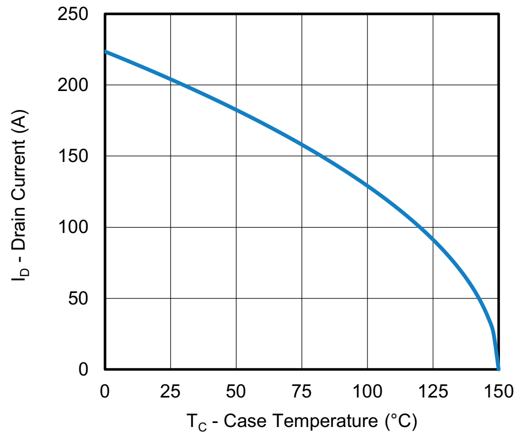
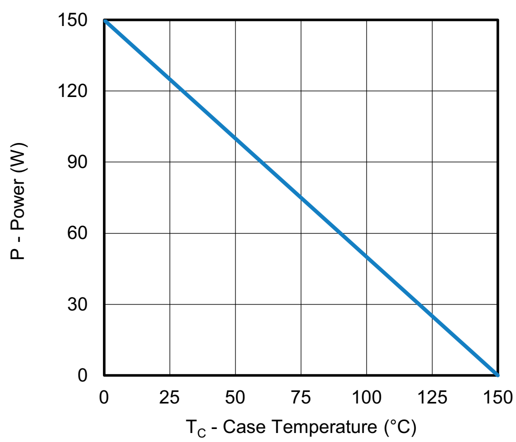
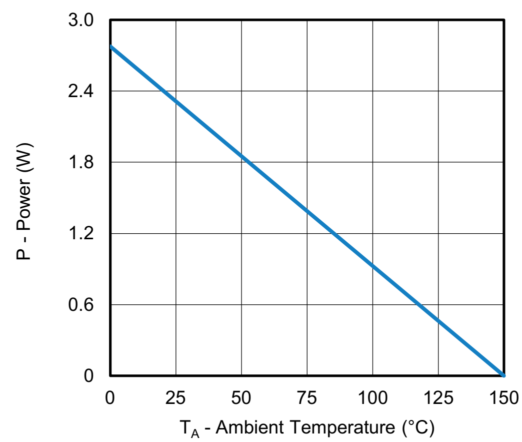


Current Derating [a]



Power, Junction-to-Case



Power, Junction-to-Ambient

Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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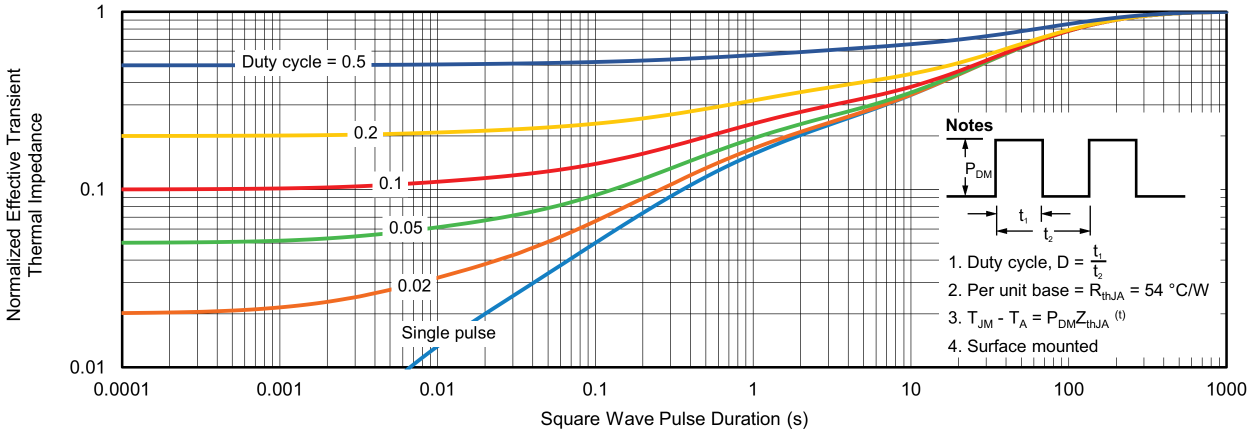
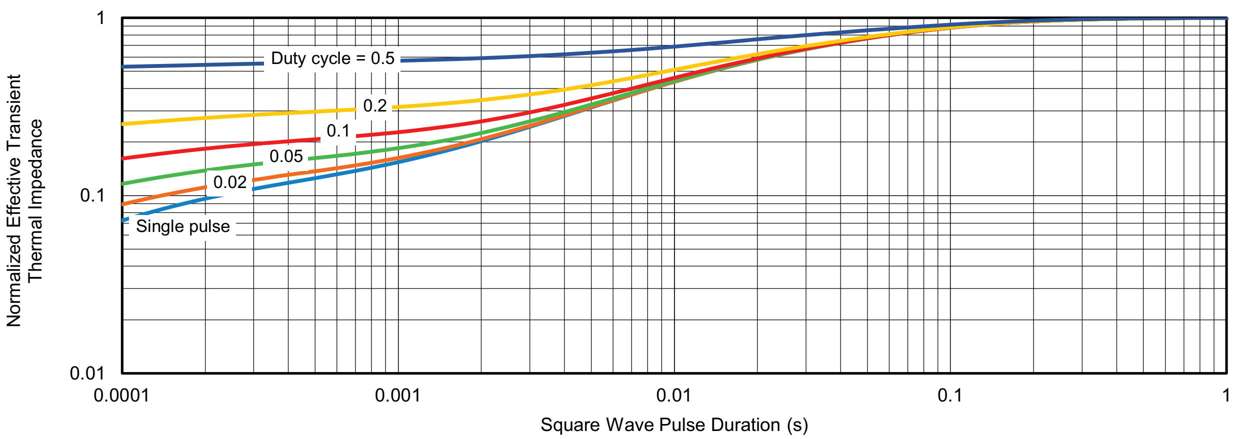


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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