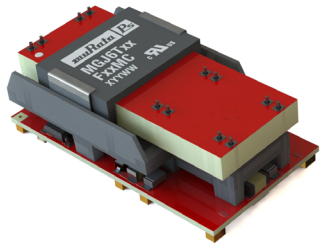
MGJ6 Full Bridge Series

5.7kVDC Isolated 6W Triple Output Gate Drive SM DC-DC Converters

Murata Power Solutions



FEATURES

- No opto feedback
- Patent protected
- Three isolated output voltages suitable for IGBT/SiC & Mosfet gate drives in a full bridge configuration
- Reinforced insulation to UL60950 with 8mm creepage & clearance recognised
- ANSI/AAMI ES60601-1, 2 MOPP recognised
- Characterised CMTI >100kV/µS
- Characterised partial discharge performance
- 5.7kVDC isolation test voltage 'Hi Pot Test'
- Ultra low isolation capacitance typically 15pF
- Continuous barrier withstand voltage 3kVDC
- 5V, 12V & 24V input voltages
- 105°C operating temperature

PRODUCT OVERVIEW

Offering Three isolated output voltages of 24V, the MGJ6-FB series of DC-DC converters is ideal for simultaneously powering 'high side' and 'low side' gate drive circuits for IGBTs, Silicon and Silicon Carbide Mosfets in full bridge circuits. The MGJ6-FB series is characterised for high isolation and dv/dt requirements commonly seen in bridge circuits used in motor drives and inverters.

SELECTION GUIDE

Order Code[1]	Input Voltage Range	Output 1 VHA / Output 2 VHB			Output 3 VL		
		Rated Output Voltage	Rated Output Current	Output Power	Rated Output Voltage	Rated Output Current	Output Power
	V	V	mA	W	V	mA	W
MGJ6T05F24MC	4.5 - 9	24	62.5	1.5	24	125	3
MGJ6T12F24MC	9 - 18	24	62.5	1.5	24	125	3
MGJ6T24F24MC	18 - 36	24	62.5	1.5	24	125	3

SELECTION GUIDE (Continued)

Order Code[1]	Input Voltage Range	Output 1 VHA / Output 2 VHB				Output 3 VL			
		Load Regulation (Typ)[4]	Load Regulation (Max)[4]	Ripple & Noise (Typ)[2]	Ripple & Noise (Max)[2]	Load Regulation (Typ)	Load Regulation (Max)	Ripple & Noise (Typ)[2]	Ripple & Noise (Max)[2]
	V	%		mVp-p		%		mVp-p	
MGJ6T05F24MC	4.5 - 9	2	3	100	150	2	3	100	150
MGJ6T12F24MC	9 - 18	2	3	150	200	2	3	150	200
MGJ6T24F24MC	18 - 36	2	3	150	200	2	3	150	200

SELECTION GUIDE (Continued)

Order Code[1]	Nominal Input Voltage	Input Current at Rated Load	Efficiency (Min)	Efficiency (Typ)	MTTF[3]	
					MIL 217	Telecordia
	V	mA	%		kHrs	
MGJ6T05F24MC	5	1500	76	80	686	2706
MGJ6T12F24MC	12	600	81	84	885	1971
MGJ6T24F24MC	24	300	82	85	885	1917

RoHS COMPLIANT

For full details go to www.murata-ps.com/rohs

1. Components are supplied in tape and reel packaging, please refer to tape and reel specification section. Orderable part numbers are MGJ6TXXF24MC-R7 (23 pieces per reel), or MGJ6TXXF24MC-R13 (92 pieces per reel).
2. See ripple & noise test method.
3. Calculated using MIL-HDBK-217 FN2 and Telecordia SR-332 calculation model at T_A=25°C with nominal input voltage at full load.
4. Between 50% and 100% rated output current.

All specifications typical at T_A=25°C, nominal input voltage and rated output current unless otherwise specified.

INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage range	5V input types	4.5	5	9	V
	12V input types	9	12	18	
	24V input types	18	24	36	
Under voltage lock out	Turn on threshold MGJ6T05		3.8		V
	Turn off threshold MGJ6T05		3.2		
	Turn on threshold MGJ6T12		8.1		
	Turn off threshold MGJ6T12		7.5		
	Turn on threshold MGJ6T24		16.7		
	Turn off threshold MGJ6T24		16.3		
Input ripple current	5V input types		30		mA p-p
	12V input types		45		
	24V input types		30		

OUTPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Minimum load	Below 10% load, output may rise to 30V maximum voltage	10			%
Voltage set point accuracy	All output types		+3 / -2		%
Total regulation				10	%
Line regulation	Low line to high line		0.5	1	%

GENERAL CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	Disable pin pulled low		45		mW
Switching frequency			100		kHz

ISOLATION CHARACTERISTICS

Parameter		Conditions	Min.	Typ.	Max.	Units
Isolation test voltage		Flash tested for 1 second (input to output)	4000			VAC
		Flash tested for 1 second (output to output)	2500			
		Qualification tested for 1 minute (input to output)	5700			VDC
		Qualification tested for 1 minute (output to output)	3000			
Resistance		Viso = 1kVDC	100			GΩ
Continuous barrier withstand voltage		Non-safety barrier application			3000	VDC
Safety standard	UL60950-1	Reinforced			250	Vrms
	ANSI/AAMI ES60601-1	2 MOPP			250	
Creepage & clearance		Input to output			8	mm
		Output to output			8	
Isolation capacitance		Primary to Output 1 VHA		15		pF
		Primary to Output 2 VHB		15		
		Primary to Output 3 VL		15		

TEMPERATURE CHARACTERISTICS

Parameter	Conditions		Min.	Typ.	Max.	Units
Operation	See derating graphs		-40		105	°C
Storage			-55		125	
Product temperature rise above ambient	100% Load, Nom V_{IN}, Still Air	5V input types		25		
		All other input types		19		

ABSOLUTE MAXIMUM RATINGS

Short-circuit protection	Continuous
Input voltage, MGJ6-FB 5V input types	12V
Input voltage, MGJ6-FB 12V input types	20V
Input voltage, MGJ6-FB 24V input types	40V

TECHNICAL NOTES

ISOLATION VOLTAGE

'Hi Pot Test', 'Flash Tested', 'Withstand Voltage', 'Proof Voltage', 'Dielectric Withstand Voltage' & 'Isolation Test Voltage' are all terms that relate to the same thing, a test voltage, applied for a specified time, across a component designed to provide electrical isolation, to verify the integrity of that isolation.

Murata Power Solutions MGJ6-FB series of DC-DC converters are all 100% production tested at 4kVACrms for 1 second from input to output and 2.5kVACrms for 1 second from output to output. Also they are all qualification tested at 5.7kVDC for 1 minute from input to output and 3kVDC for 1 minute from output to output.

The MGJ6-FB series is recognised by Underwriters Laboratory, please see safety approval section for more information. When the insulation in the MGJ6-FB series is not used as a safety barrier, i.e. provides functional isolation only, continuous or switched voltages across the barrier up to 3kV are sustainable. This is established by measuring the partial discharge Inception voltage in accordance with IEC 60270. Please contact Murata for further information.

REPEATED HIGH-VOLTAGE ISOLATION TESTING

It is well known that repeated high-voltage isolation testing of a barrier component can actually degrade isolation capability, to a lesser or greater degree depending on materials, construction and environment. We therefore strongly advise against repeated high voltage isolation testing, but if it is absolutely required, that the voltage be reduced by 20% from specified test voltage.

SAFETY APPROVAL

ANSI/AAMI ES60601-1

The MGJ6-FB series is recognised by Underwriters Laboratory (UL) to ANSI/AAMI ES60601-1 and provides 2 MOPP (Means Of Patient Protection) based on a working voltage of 250vrms.

UL60950

The MGJ6-FB series is recognised by Underwriters Laboratory (UL) to UL60950 for reinforced insulation to a working voltage of 250Vrms with a maximum measured product operating temperature of 130°C.

Creepage and clearance 8mm, input to output & across outputs.
Working altitude 5000m
Over voltage category (OVC) II

FUSING

The MGJ6-FB Series of converters are not internally fused so to meet the requirements of UL an anti-surge input line fuse should always be used with ratings as defined below.
Input Voltage, 5V 4A
Input Voltage, 12V 2A
Input Voltage, 24V 1A
All fuses should be UL recognised, 250Vac rated.

RoHS COMPLIANCE, MSL, PSL AND REFLOW SOLDERING INFORMATION

RoHS COMPLIANT

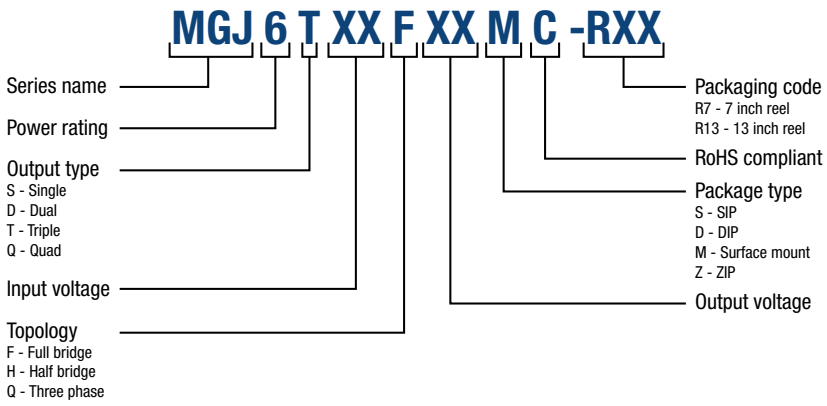
This series is compatible with Pb-Free soldering systems and is also backward compatible with Sn/Pb soldering systems. The MGJ6 full bridge series has a process, moisture, and reflow sensitivity classification of MSL2 PSL R7F as defined in J-STD-020 and J-STD-075. Please refer to application notes for further information. This translates to: MSL2 = 1 year floor life, PSL R7F = Peak reflow temperature 245°C with a limitation on the time above liquidus (217°C) which for this series is 90sec max. The pin termination finish on this product series is Gold with Nickel Pre-plate.

ENVIRONMENTAL VALIDATION TESTING

The following tests have been conducted on this product series, please contact Murata if further information about the tests is required.

Test	Standard	Condition
Temperature cycling	MIL-STD-883 Method 1010, Condition B	10 cycles between two chambers set to achieve -55°C and +125°C.The dwell time shall not be less than 10min and the load shall reach the specified temperature in 15min.
Humidity bias	JEDEC JESD22-A101	85±2°C, 85±5% R.H. for 1000 (+168/-24) hours.
High Temperature Storage life	JEDEC JESD22-A103, Condition A	125°C +10/-0°C for ≥1000 hours.
Vibration	BS EN 61373 with respect to BS EN 60068-2-64, Test Fh Category 1 Class B	5 – 150Hz. Level at each axis – Vertical, Traverse and Longitudinal: 5.72m/s^2 rms. 5 hours in each axis. Crest factor: 3 Sigma. Device is secured via surface mount pins.
Solderability	EIA/IPC/JEDEC J-STD-002, Test S and S1	The parts are conditioned in a steam ager for 8 hours ±15 min. at a temperature of 93±3°C. SnPb (Test S): The parts are placed onto a stencil with Sn60Pb40 solder paste on and then placed into the reflow oven at 215 ±5°C for 50–70 seconds. Pb-free (Test S1): The parts are placed onto a stencil with Sn96.5Ag3.0Cu0.5 solder paste on and then placed into the reflow oven at 245 ±5°C for 30–60 seconds.
Solvent cleaning	Resistance to cleaning agents.	Solvent – Novec 71IPA & Topklean EL-20A. Pulsed ultrasonic immersion 45°C - 65°C
Solvent Resistance	MIL-STD-883 Method 2015	The parts and the bristle portion of the brush are immersed in Isopropanol for a minimum of 1 minute. The parts are brushed 3 times, after the third time the parts are blown dry and inspected.
Moisture sensitivity level (MSL 2)	Based on IPC/JEDEC J-STD-020	Bake samples at 125 +5/-0°C for 24hours minimum before conditioning in the temperature/humidity chamber for 168 hours at 85°C/60%RH and Pb Free JEDEC Max profile conditioning with electrical testing, co-planarity inspection before and after.

PART NUMBER STRUCTURE



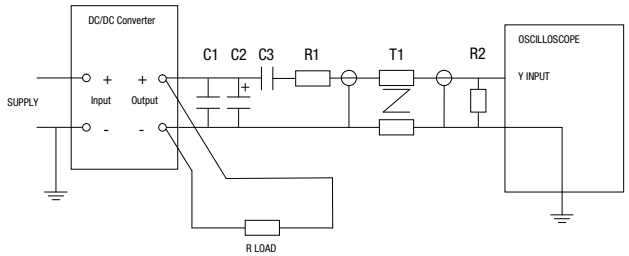
CHARACTERISATION TEST METHODS

Ripple & Noise Characterisation Method

Ripple and noise measurements are performed with the following test configuration.

C1	1µF X7R multilayer ceramic capacitor, voltage rating to be a minimum of 3 times the output voltage of the DC-DC converter
C2	10µF tantalum capacitor, voltage rating to be a minimum of 1.5 times the output voltage of the DC-DC converter with an ESR of less than 100mΩ at 100 kHz
C3	100nF multilayer ceramic capacitor, general purpose
R1	450Ω resistor, carbon film, ±1% tolerance
R2	50Ω BNC termination
T1	3T of the coax cable through a ferrite toroid
RLOAD	Resistive load to the maximum power rating of the DC-DC converter. Connections should be made via twisted wires
Measured values are multiplied by 10 to obtain the specified values.	

Differential Mode Noise Test Schematic



APPLICATION NOTES

Disable/Frequency synchronisation

Please refer to application notes for further information.

		Min	Typ	Max	Units
$\overline{\text{Disable}}$/Sync[1]	Pull Down Current		0.5		mA
	Input High	2		60	V
	Input Low	-0.6		0.8	V
Synchronisation	Frequency Range	90	100	110	kHz
	Duty Cycle	25		75	%

The $\overline{\text{Disable}}$/Synchronization pin has three modes:

1. When a DC logic low voltage is applied to this pin the MGJ6-FB is disabled and enters a low quiescent current sleep mode.
2. When this pin is left floating or a DC logic high (CMOS/TTL compatible) voltage is applied the MGJ6-FB is enabled and operates at the programmed frequency of 100kHz.
3. When a square wave of between 90kHz and 110kHz is applied to this pin, the switcher operates at the same frequency as the square wave. The falling edge of the square wave corresponds to the start of the switching cycle. If the signal is slower than 25Hz, it will be interpreted as enabling and disabling the part. If the MGJ6-FB is disabled, it must be disabled for 7 clock cycles before being re-enabled.

Note: The $\overline{\text{Dis}}$/Sync pin is a high impedance TTL input and can be triggered by noise from external circuits if not treated carefully.

Please refer to "LAYOUT CONSIDERATIONS" and "SYNCHRONISATION CIRCUIT" for further details.

Click here for general guidance for gate drive applications.

LAYOUT CONSIDERATIONS

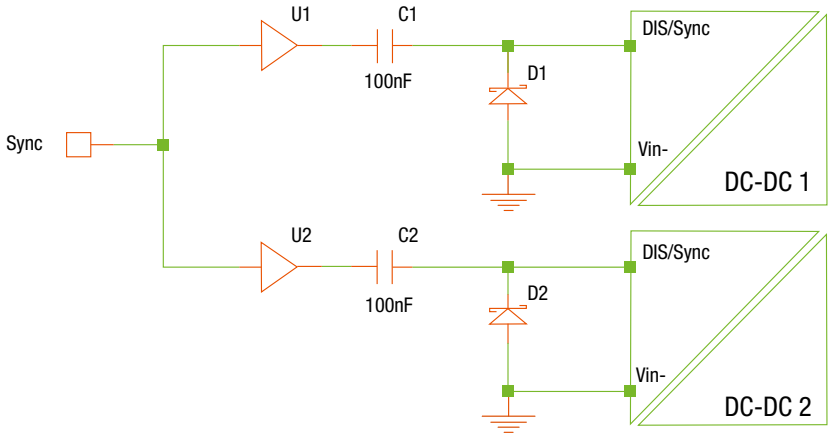
Unlike standard isolated DC-DC products the MGJ6-FB series has been designed specifically for high side gate drive applications where the outputs are being driven to a high voltage at a very high dV/dT. This is possible due to minimum transformer isolation capacitance and considered circuit design regarding common mode transient immunity. It is important that these few simple pcb layout guidelines are implemented so as not to compromise the performance of the DC-DC and that of the overall system.

1. The keep clear area shown must not have any copper traces even on internal layers. This is not only to avoid compromising the creepage and clearance distance but also to minimise capacitive isolation between the noisy output circuits and input control circuits. In general it is good practice to maintain the same band of clearance area running directly through both the DC-DC and the gate drive isolators as shown so that input and output are kept separate and do not overlap or mesh together at any point.

2. A top layer ground plane copper area connected to –Vin can be used to create an effective screen to the underside of the MGJ6-FB series and can also be used as a guard ring for the gate drive isolator inputs. If the $\overline{\text{Dis}}$/Synch pin is being used then it is imperative that it follows a route covered by this screen to avoid differential pick up. It should also be kept as short as possible.

Please refer to "PACKAGE SPECIFICATIONS" for recommended layout.

SYNCHRONISATION CIRCUIT



1. A suggested synchronisation circuit is shown. C1 and C2 are 100nF capacitors. D1 and D2 are schottky diodes. The capacitive isolation and close connected diode ensures that a transition from high to low is seen at the input pin even in a noisy environment or when there is a slight ground shift between devices.

2. If the $\overline{\text{Dis}}$/Sync pin is not used for synchronisation, then a 22nF capacitor can be added between the $\overline{\text{Dis}}$/Sync pin and –Vin pin to improve noise immunity. If the functionality of $\overline{\text{Dis}}$/Sync is not required, the $\overline{\text{Dis}}$/Sync pin can be connected directly to the +Vin pin to improve noise immunity.

3. One very effective method to reduce common mode transient interference is to add a common mode filter to the DC input. It may only be necessary to add one before splitting the supply to each DC-DC.

APPLICATION NOTES (Continued)

Start-up times

Typical start up times for this series, with recommended maximum additional output capacitance are:

Part No.	Start-up times
	ms
MGJ6T05F24MC	30
MGJ6T12F24MC	30
MGJ6T24F24MC	30

Output capacitance must not exceed:

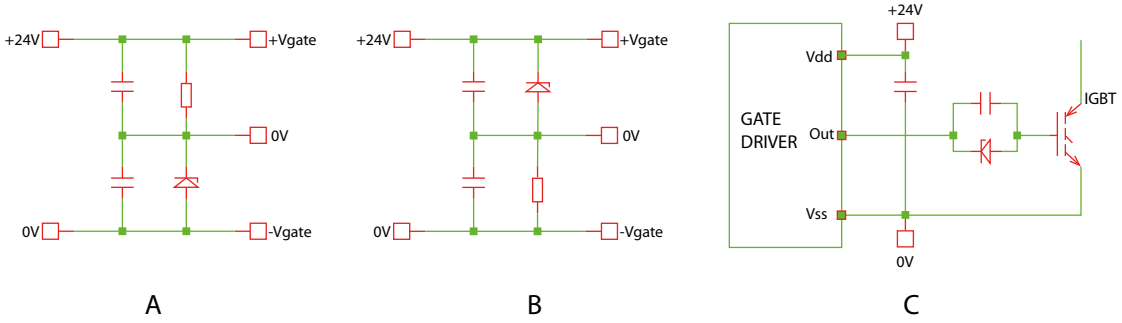
Output Voltage	Maximum output capacitance
V	µF
24 VHA	27
24 VHB	27
24 VL	56

Output configurations for power switches

There are several zener based divider circuits that can be used to configure a bipolar output for gate drives as shown below. The table below shows suggested component values for various power switches using circuit A.

Component	IGBT	SIC	MOSFET
Zener diode[1]	9V1	5V1	9V1
Resistor	15K	18K	15K

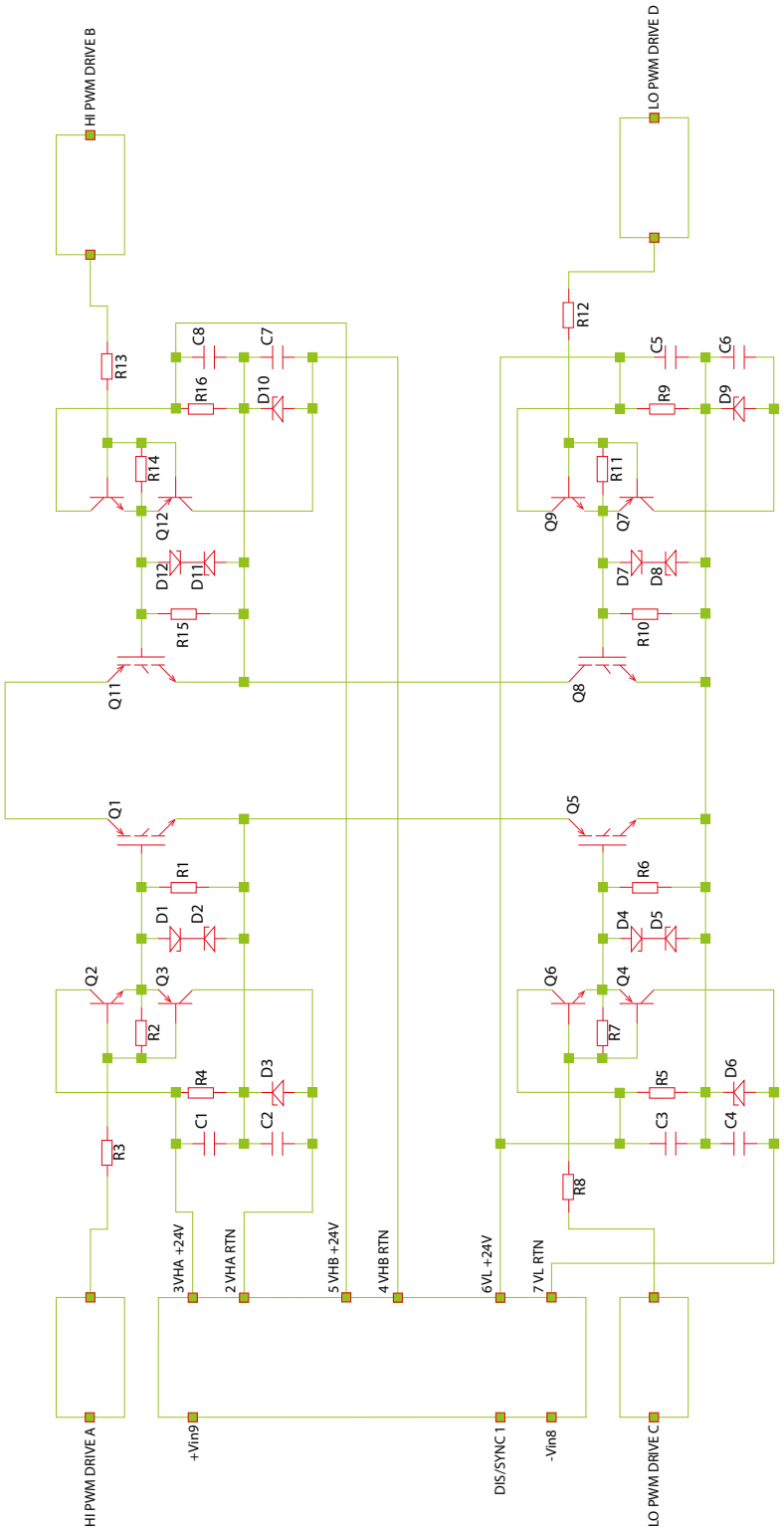
1. Suggested zener diode is BZX84C.



APPLICATION NOTES (Continued)

Schematic for driving IGBT

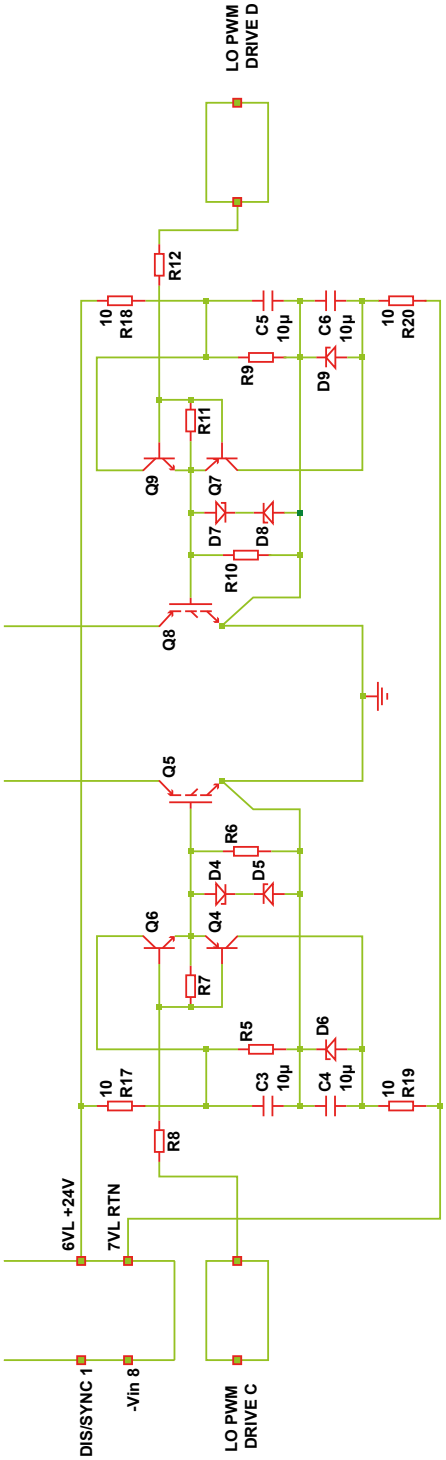
The following circuit shows an example of a complete full bridge and how the DC-DC would be connected using the zener divider in circuit A (page 5).



APPLICATION NOTES (Continued)

Schematic for driving IGBT

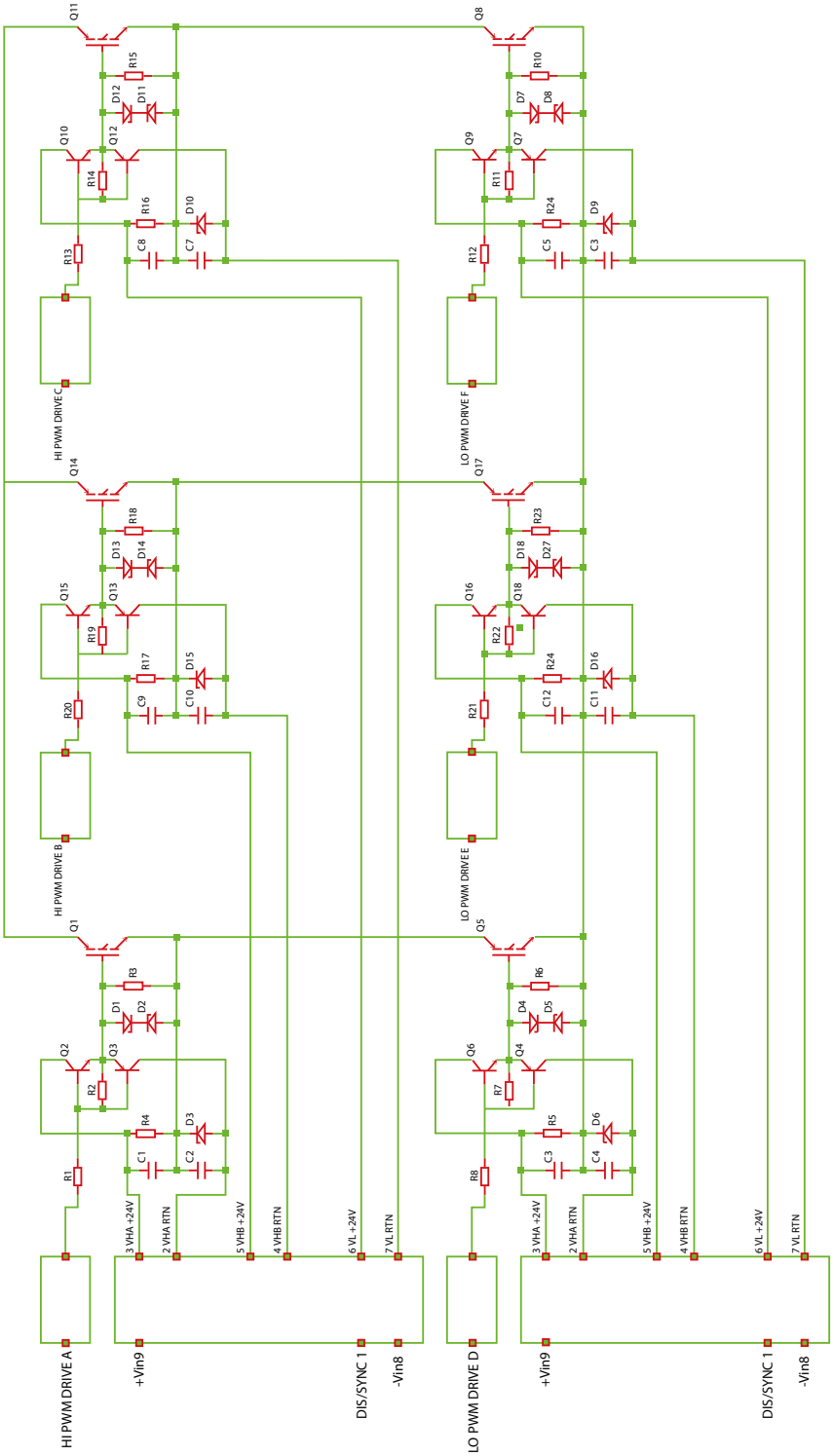
For some high frequency applications where each low side device has a kelvin sense terminal or it is necessary to connect the gate drive supply as close to the device terminal as possible the following circuit can be used. By adding 10 Ohm resistors in the positive and negative gate supply lines to each gate drive circuit it is possible to create a high frequency separation between the supplies. This means it is possible to significantly reduce the emitter inductance in the gate driving loop without the need for separate isolated supplies



APPLICATION NOTES (Continued)

Schematic for Powering Three Phase Drivers on Electrical Vehicle Systems

For three phase drives on an Electric Vehicle system it is sometimes necessary, for safety and diagnostic reasons to power the high side switches independently to the Low side switches. This means that if a fault occurs on a the high side switch it is possible to disable all of the high side switches without disabling the low side switches. The circuit below shows how two Full bridge MGJ6 units can be connected to achieve this.



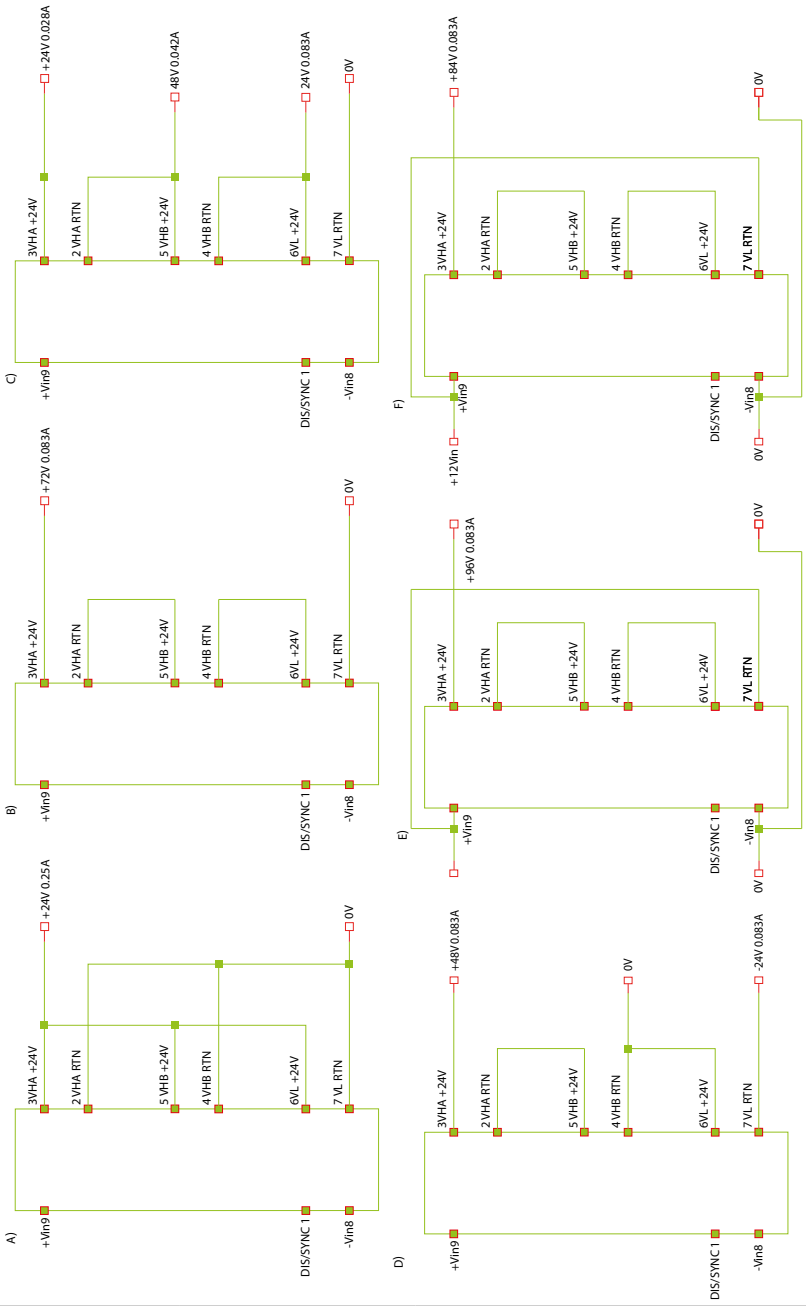
APPLICATION NOTES (Continued)

For convenience the three isolated 24V outputs have been labelled VHA (Voltage A for high side), VHB (Voltage B for high side), and VL (Voltage for low side) however they can be swapped if this helps to improve system layout. It is recommended however that if VHA or VHB are used in place of VL that an additional 4.7uF ceramic capacitor is added close to the output pins to reduce ripple voltage.

Any output can be connected in parallel with another and all three outputs can also be connected in series with one another. With the possibility of series and parallel output connections a number of output configurations are possible. Some are shown below:

A) 24V @ 0.25A
B) 72V @ 0.083A output
C) 72V @ 0.028A, 48V @0.042A and 24V @ 0.083A
D) +48V/-24V @ 0.083A
E) Non-isolated +24V to +96V boost converter @0.083A
F) Non-isolated +12V to +84V boost converter @0.083A

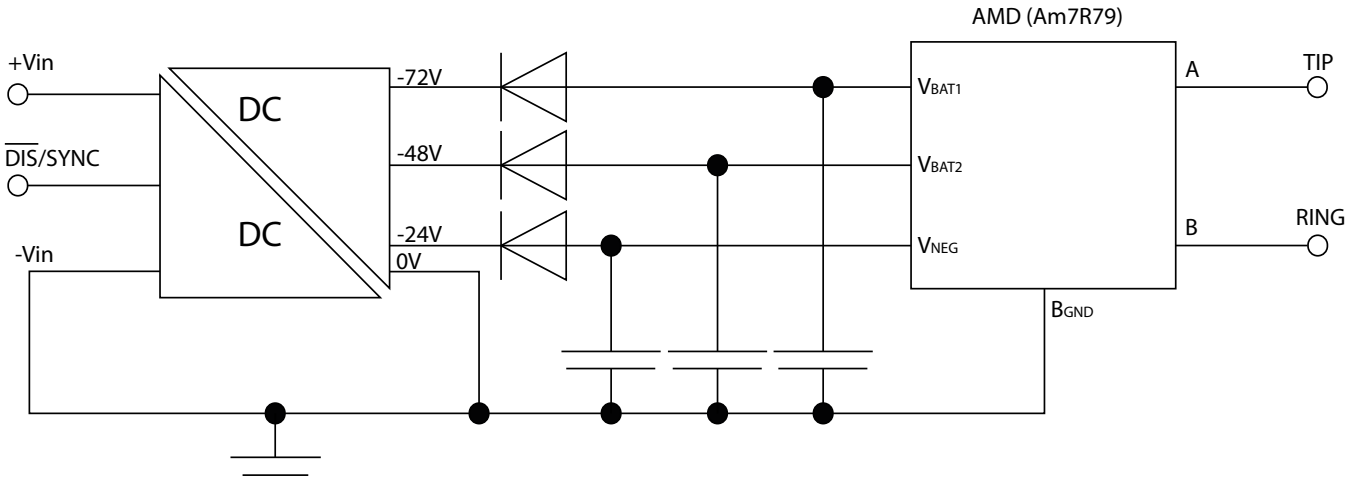
Note: Any single 24V output can deliver up to 3W however the output power from all outputs combined must not exceed 6W



APPLICATION NOTES (Continued)

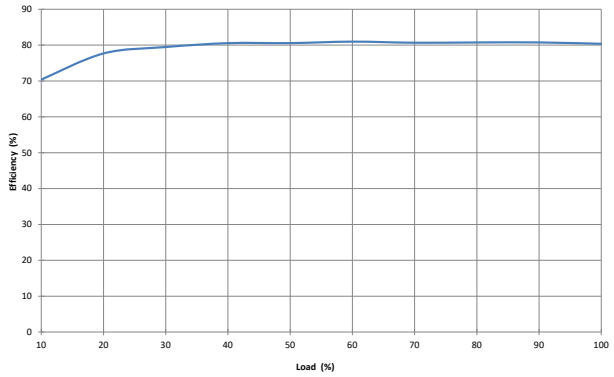
SLIC Circuits

The output configuration shown below could be used for subscriber line interface circuits (SLIC's), particularly for the Integrated Services Digital Network (ISDN) and also for standard telecommunications circuits where a local power source is preferred to the telephone system power due to either the power quality of the telecommunications system power supply or to avoid potential power line disturbances, such as lightning strikes and access switching, which will affect the target circuit function.
Another application area is in fibre-in-the-loop (FITL) or radio-in-the-loop (RITL) interfacing via a standard telecommunication SLIC, where the usual telecommunication battery voltage is not available due to the transmission media in use (fibre or radio). In particular, FITL/RITL interfaces directly on PC cards, in local monitor and boost circuits and at exchanges between the fibre/radio and wire media. The supply rails can be used for ringing generators as well as SLIC circuits or where both are combined, such as in the AMD AM79R79 Ringing SLIC device (see figure 2). The -72V rail is used primarily for the generation of the ringing signal (VBAT1), the -48V rail is used to supply in line access circuitry (VBAT2) and the -24V supply for the on-chip regulator for the logic interface (VNEG). Alternative devices from other manufacturers could use the -24V output for their internal circuit supply and -72V for ringing.

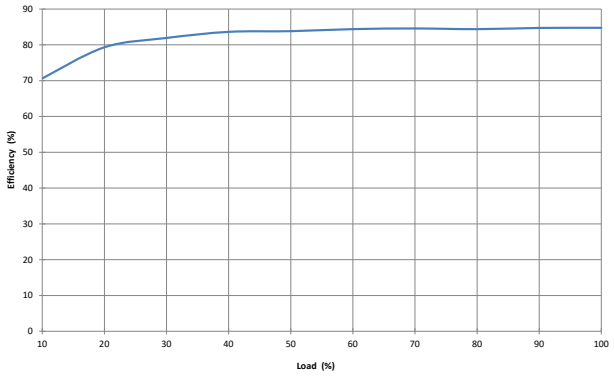


EFFICIENCY VS LOAD

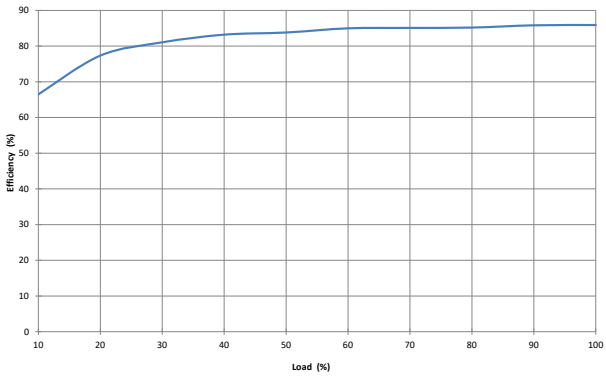
MGJ6T05F24MC



MGJ6T12F24MC



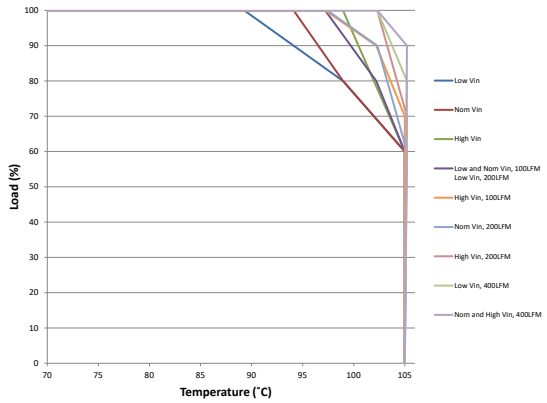
MGJ6T24F24MC



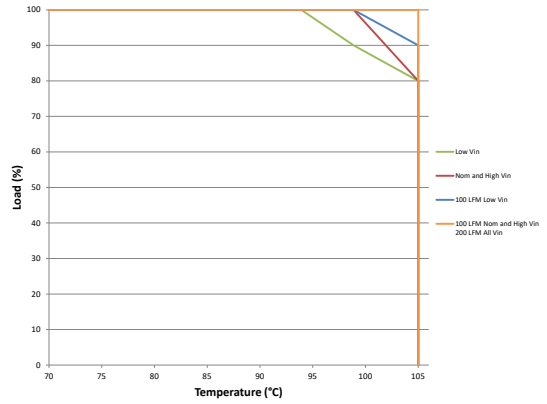
TEMPERATURE DERATING

Derating curves are based on IPC-9592. With no derating some components may be operating at the manufacturers maximum temperature ratings.

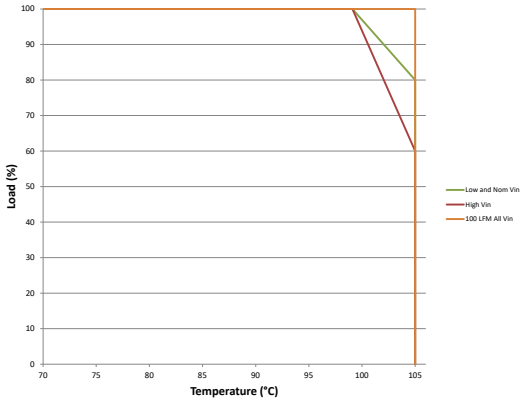
MGJ6T05F24MC



MGJ6T12F24MC



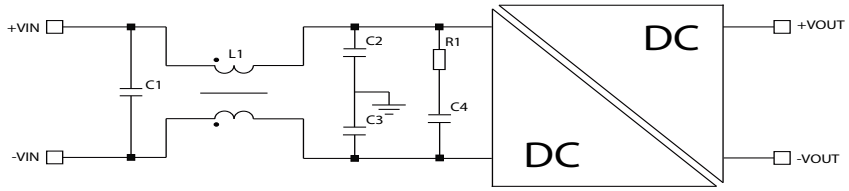
MGJ6T24F24MC



EMC FILTERING AND SPECTRA

FILTERING

The following filter circuit and filter table shows the input filters typically required to meet conducted emissions limits for EN 55022 curve B using Quasi-Peak (pink line) and average (green line) detectors according to CISPR22. The following plots show measurements of the positive (L1) and negative (L2) inputs for both Quasi-peak limit B adherence and Average limit B adherence. If a high dv/dt above 80kV/us is expected from output to input it is advised that a common mode filter is used on each output as this will reduce the common mode current circulating between outputs and input and causing interference.

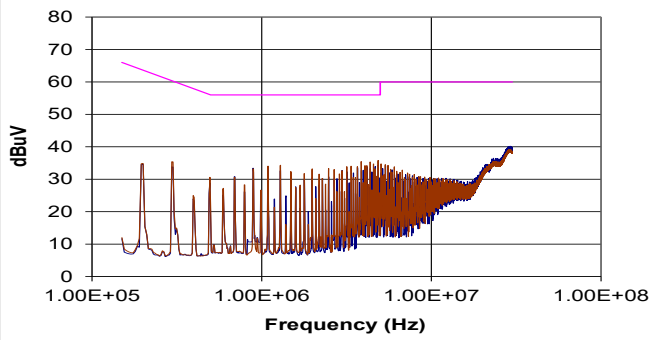


C1, C2 & C3 Polyester or ceramic capacitor

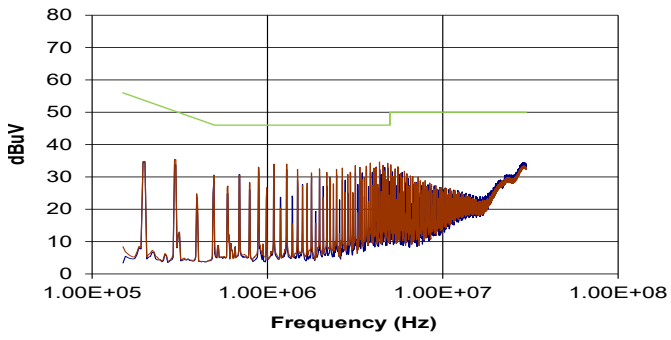
C4 Electrolytic capacitor (note R1 could be omitted if C4 has ESR >= R1)

TO MEET CURVE B							
Part Number	C1	L1	Part Number	C2	C3	R1	C4
MGJ6T05F24MC	10µF	1mH	51105C	1nF	1nF	1Ω	470µF
MGJ6T12F24MC	10µF	1mH	51105C	1nF	1nF	1Ω	470µF
MGJ6T24F24MC	10µF	1mH	51105C	1nF	1nF	1Ω	470µF

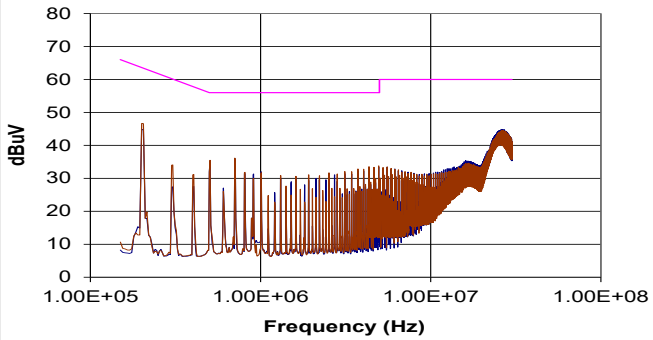
MGJ6T05F24MC (Quasi Peak)



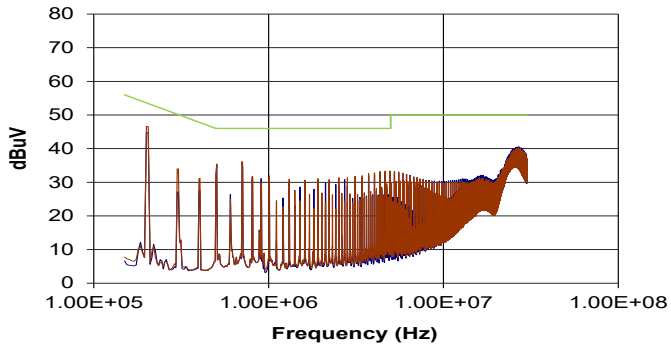
MGJ6T05F24MC (Average)



MGJ6T12F24MC (Quasi Peak)

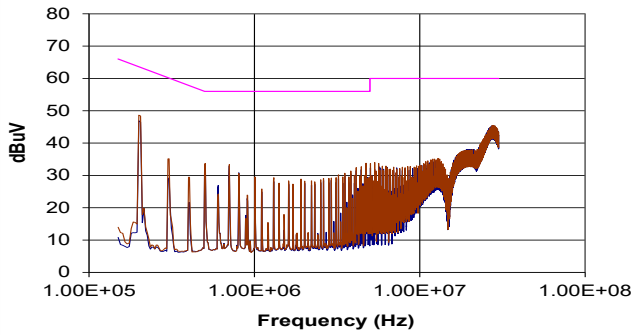


MGJ6T12F24MC (Average)

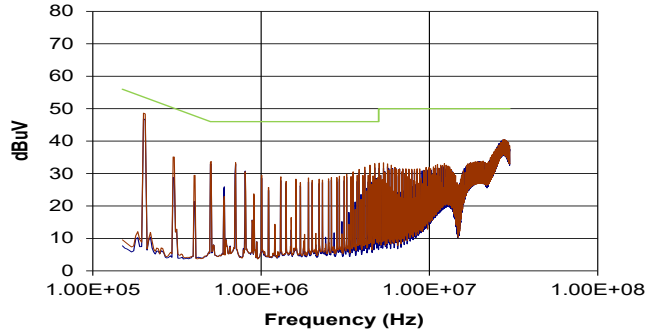


EMC FILTERING AND SPECTRA

MGJ6T24F24MC (Quasi Peak)

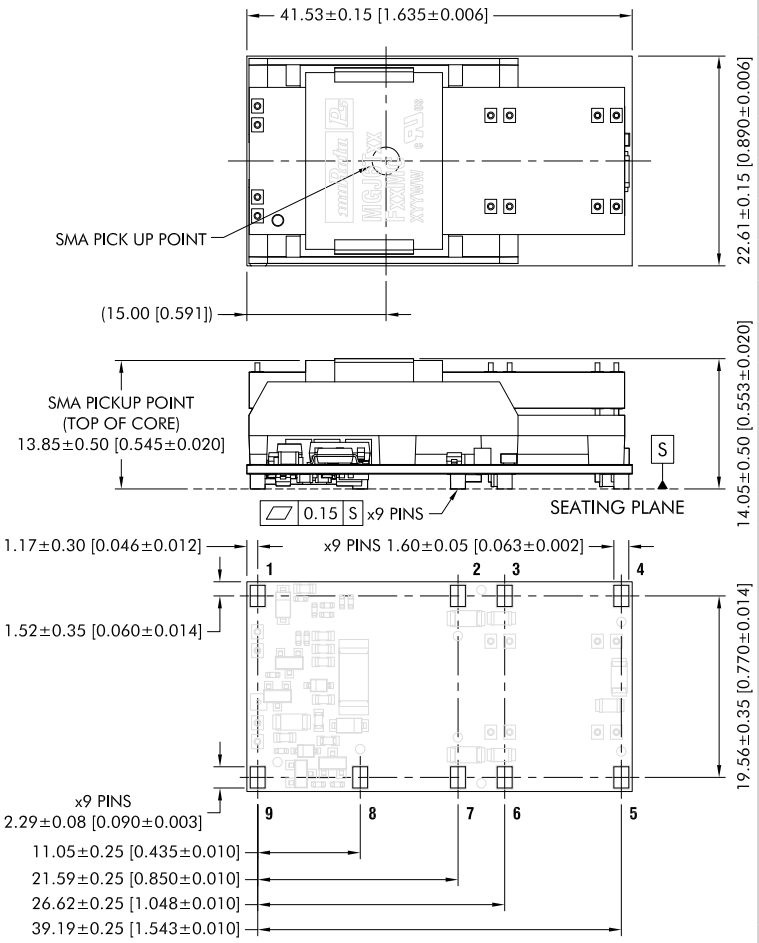


MGJ6T24F24MC (Average)



PACKAGE SPECIFICATIONS

MECHANICAL DIMENSIONS



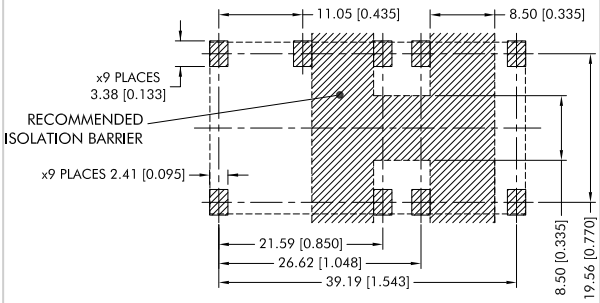
All dimensions in mm (inches), Controlling dimensions is mm.
Component shown for reference only.

Weight: 17.3g

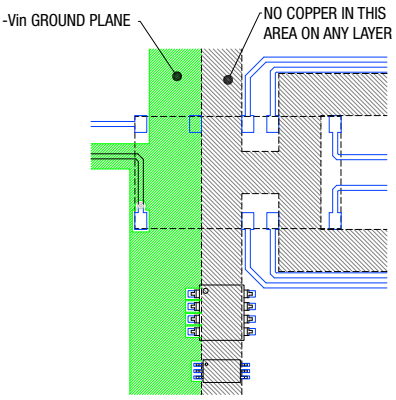
PIN CONNECTIONS

Pin	Function
1	$\overline{\text{Dis/Sync}}$
2	VHA RTN
3	VHA +24V
4	VHB RTN
5	VHB +24V
6	VL +24V
7	VL RTN
8	-Vin
9	+Vin

RECOMMENDED FOOTPRINT DETAILS



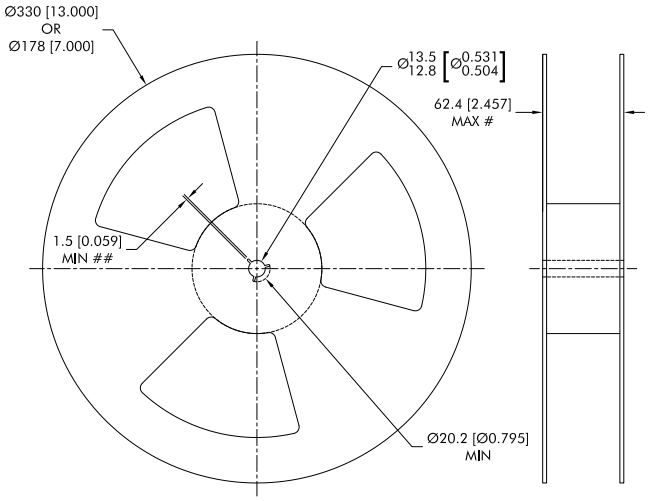
RECOMMENDED LAYOUT



Please refer to "LAYOUT CONSIDERATIONS" for further details.

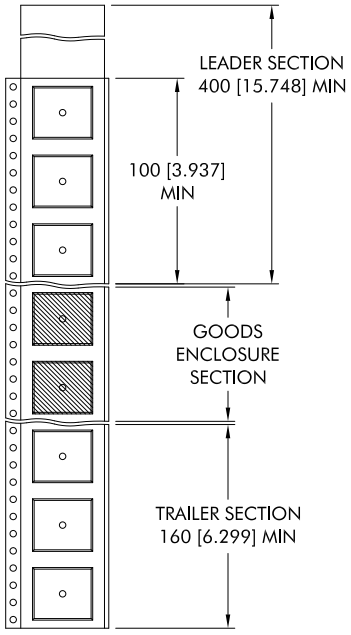
TAPE & REEL SPECIFICATIONS

REEL OUTLINE DIMENSIONS



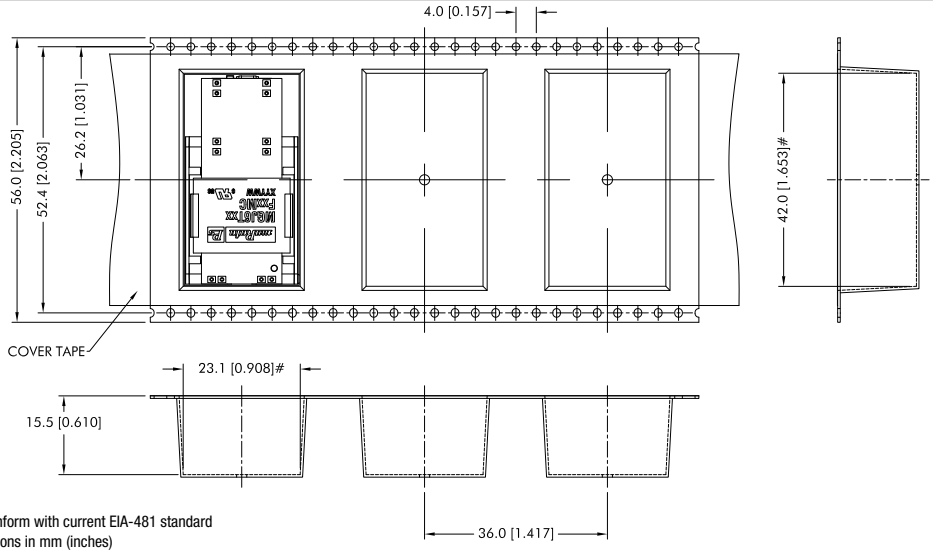
Tape & Reel specifications shall conform with current EIA-481 standard
Unless otherwise stated all dimensions in mm (inches)
Controlling dimension is mm
Measured at hub
Six equi-spaced slots on 180mm/7" reel

REEL PACKAGING DETAILS



Reel Quantity: 7" - 23 or 13" - 92
Carrier tape pockets shown are illustrative only - refer to carrier tape diagram for actual pocket details

TAPE OUTLINE DIMENSIONS



Tape & Reel specifications shall conform with current EIA-481 standard
Unless otherwise stated all dimensions in mm (inches)
Controlling dimension is mm
Components shall be orientated within the carrier tape as indicated
Measured on a plane 0.3mm above the bottom pocket