60V N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX T_C = +25°C
60V	1.6mΩ @ V_{GS} = 10V	205A

Features

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description and Applications

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize $R_{DS(ON)}$ yet maintain superior switching performance. This device is ideal for use in power management and load switch.

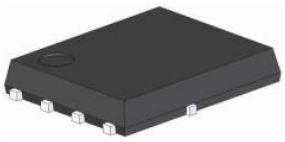
- Engine Management Systems
- Body Control Electronics
- DC-DC Converters

Mechanical Data

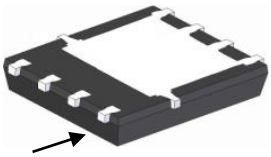
- Case: PowerDI®5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

Site1:

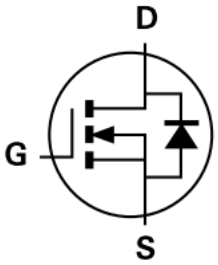
PowerDI5060-8 (Type K)



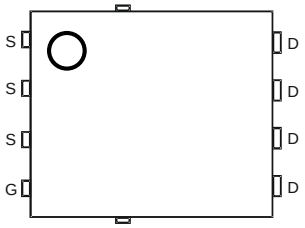
Top View



Bottom View



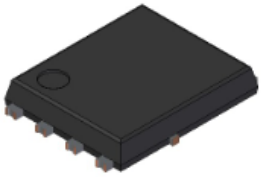
Internal Schematic



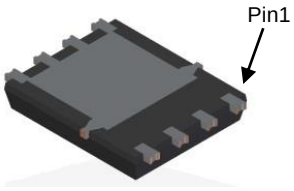
Top View
Pin Configuration

Site2:

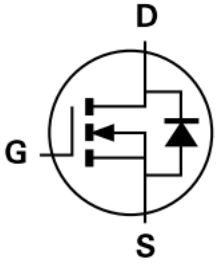
PowerDI5060-8 (SWP) (Type UX)



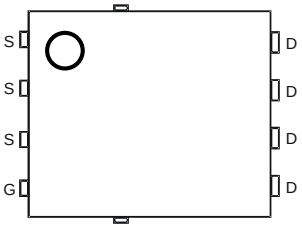
Top View



Bottom View



Internal Schematic



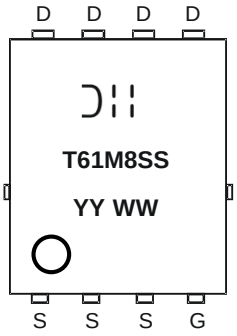
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT61M8SPS-13	PowerDI5060-8 (Type K)	2,500 / Tape & Reel
DMT61M8SPS-13	PowerDI5060-8 (SWP) (Type UX)	2,500 / Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
T61M8SS = Product Type Marking Code
YYWW or YYWW = Date Code Marking
YY or YY = Year (ex: 20 = 2020)
WW = Week (01 to 53)

Maximum Ratings (@T_C = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 6)	T_C = +25°C	I_D	205	A
	T_C = +70°C		160	
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	205	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	820	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	820	A
Avalanche Current, L = 1mH		I_{AS}	35.8	A
Avalanche Energy, L = 1mH		E_{AS}	640.8	mJ

Thermal Characteristics (@T_C = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	2.7	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	47	°C/W
Total Power Dissipation (Note 6)	T_C = +25°C	P_D	139	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	0.9	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
6. Thermal resistance from junction to soldering point (on the exposed drain pad).

Electrical Characteristics (@T_C = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 48V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	1.1	1.6	mΩ	V_{GS} = 10V, I_D = 30A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 20A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	8306	—	pF	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	2735	—		
Reverse Transfer Capacitance	C_{rss}	—	184	—		
Gate Resistance	R_g	—	3.0	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	130.6	—	nC	V_{DS} = 30V, I_D = 30A, V_{GS} = 10V
Gate-Source Charge	Q_{gs}	—	30.4	—		
Gate-Drain Charge	Q_{gd}	—	28.1	—		
Turn-On Delay Time	$t_{D(ON)}$	—	11.3	—	ns	V_{DD} = 30V, V_{GS} = 10V, I_D = 30A, R_g = 3Ω
Turn-On Rise Time	t_R	—	28.5	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	86.2	—		
Turn-Off Fall Time	t_F	—	47.6	—		
Body Diode Reverse Recovery Time	t_{RR}	—	70.4	—	ns	I_F = 30A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q_{RR}	—	127	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

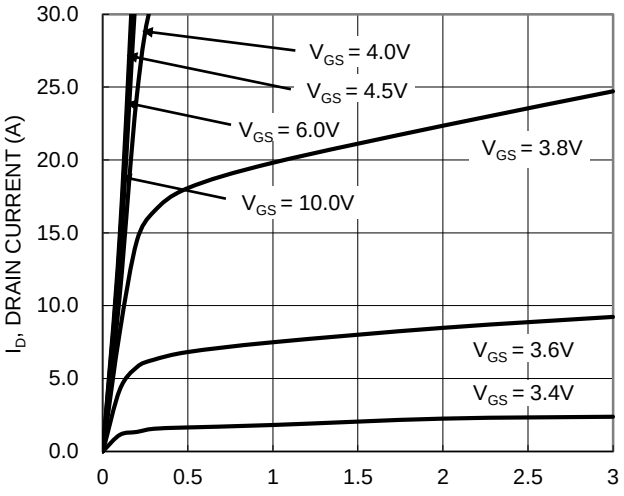


Figure 1. Typical Output Characteristic

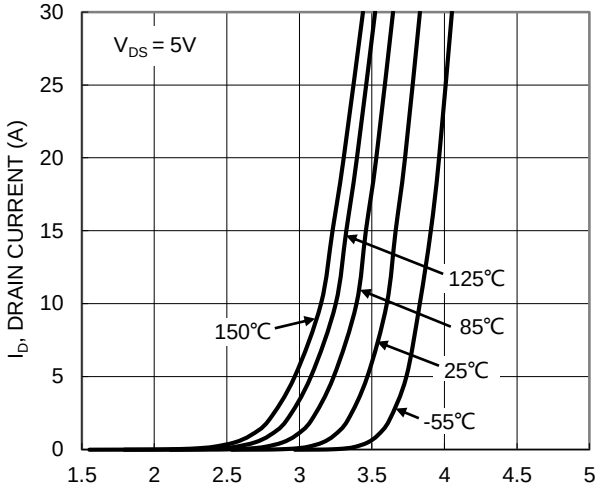


Figure 2. Typical Transfer Characteristic

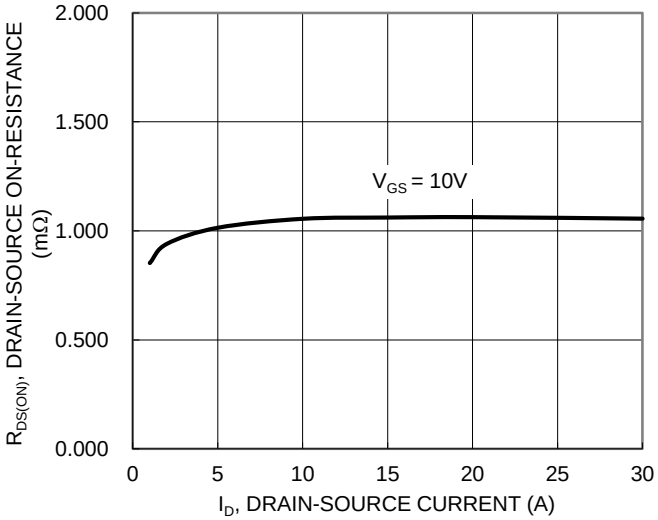


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

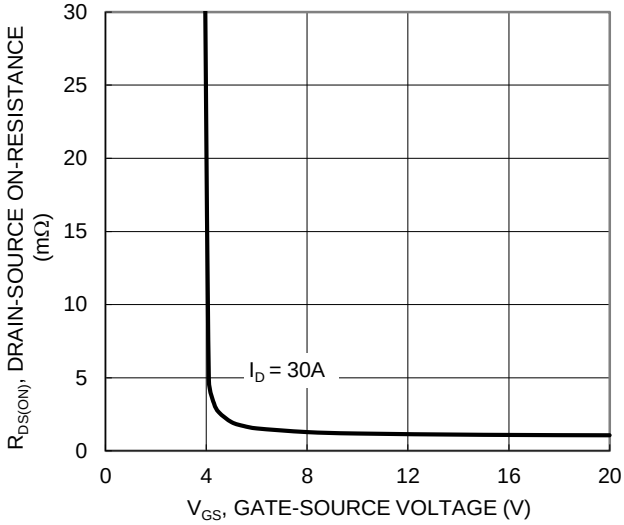


Figure 4. Typical Transfer Characteristic

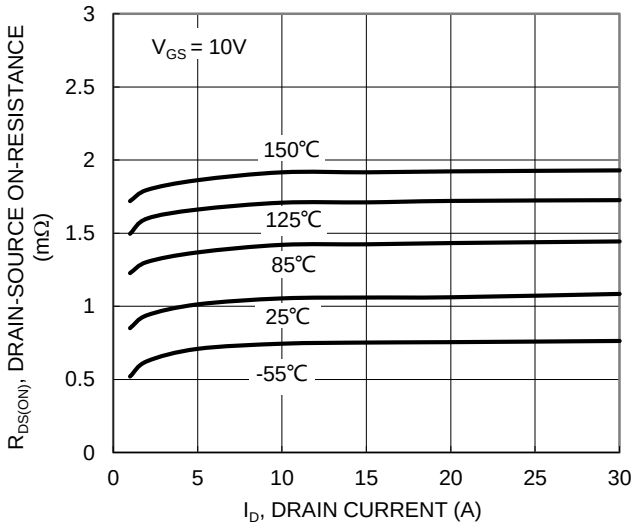


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

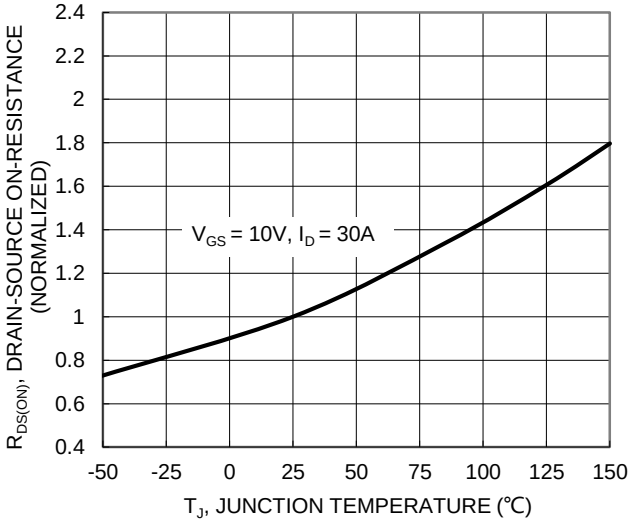


Figure 6. On-Resistance Variation with Temperature

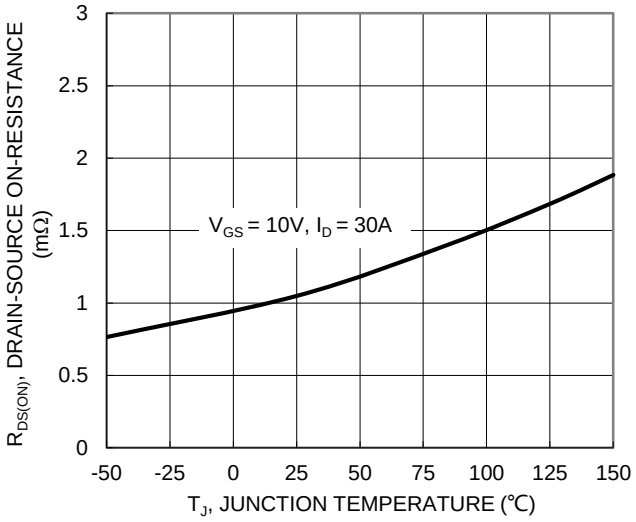


Figure 7. On-Resistance Variation with Temperature

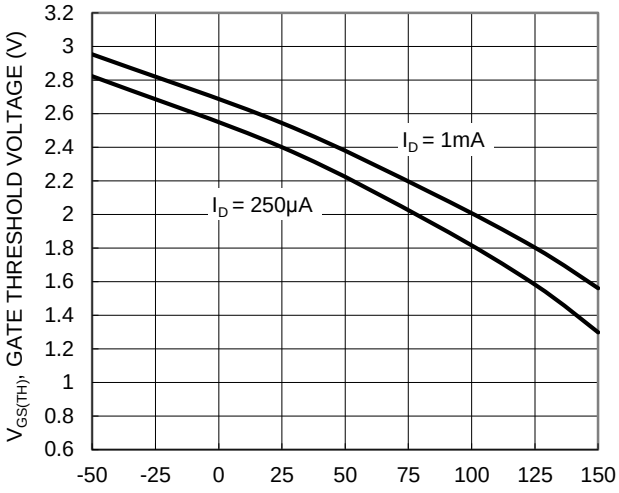


Figure 8. Gate Threshold Variation vs. Junction Temperature

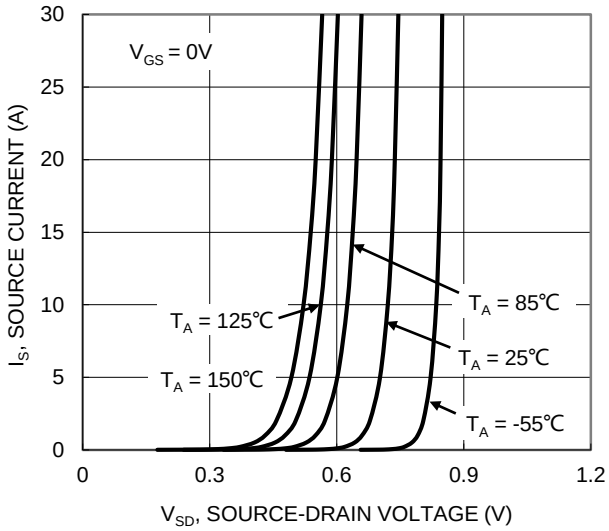


Figure 9. Diode Forward Voltage vs. Current

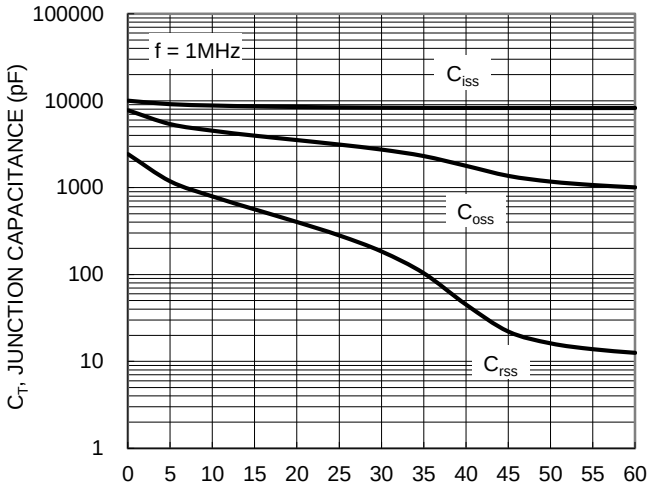


Figure 10. Typical Junction Capacitance

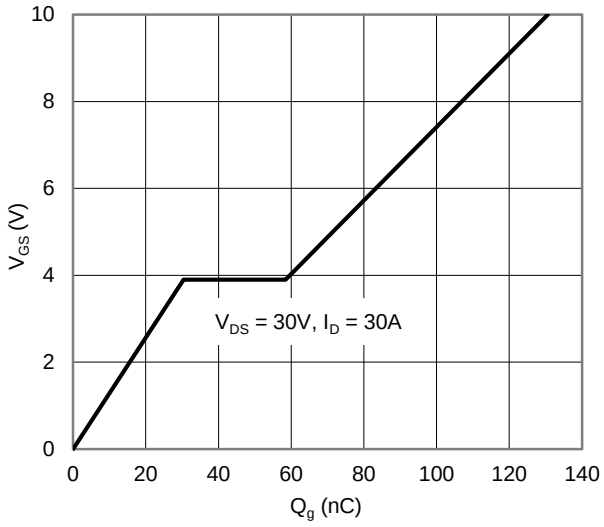


Figure 11. Gate Charge

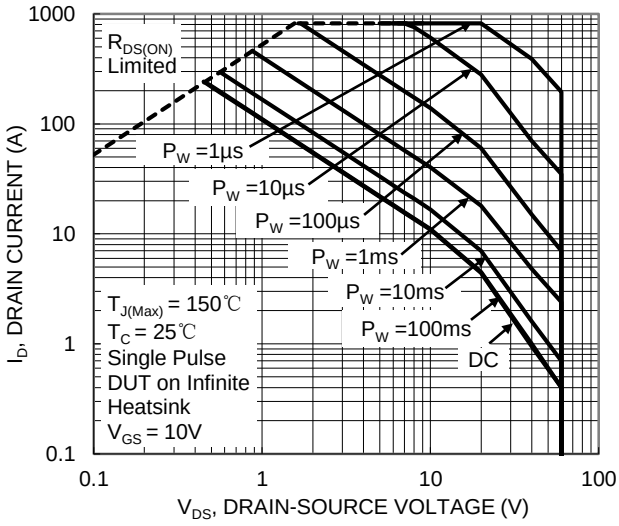


Figure 12. SOA, Safe Operation Area

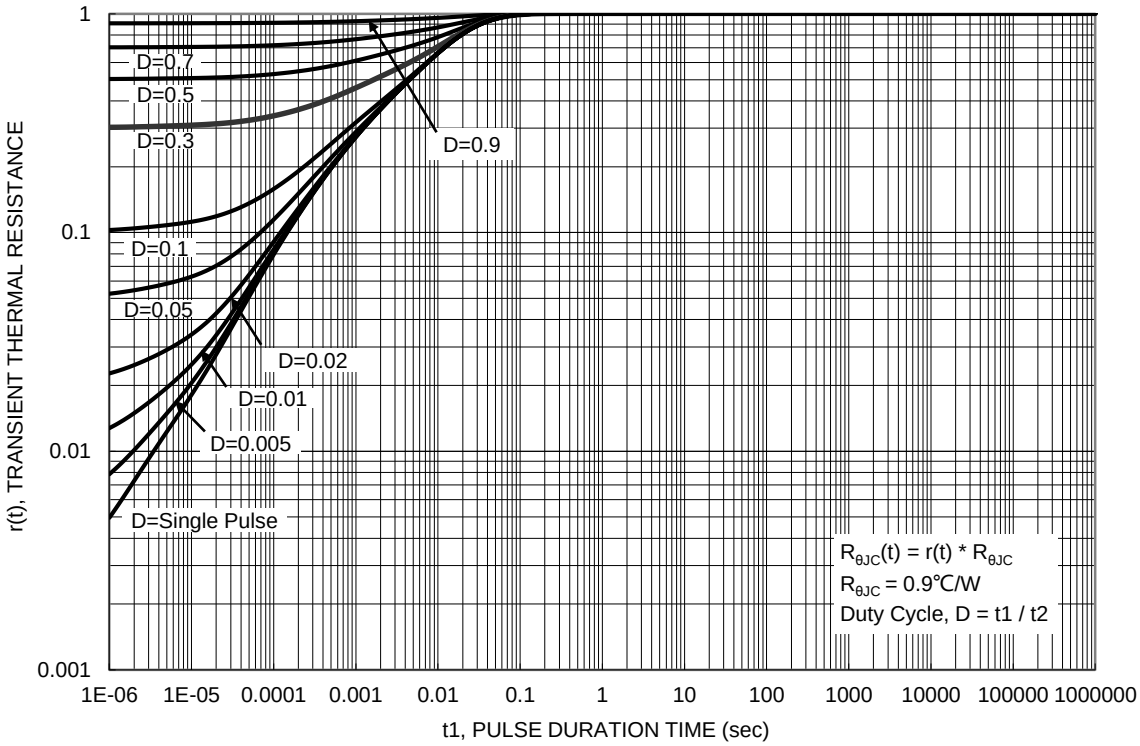


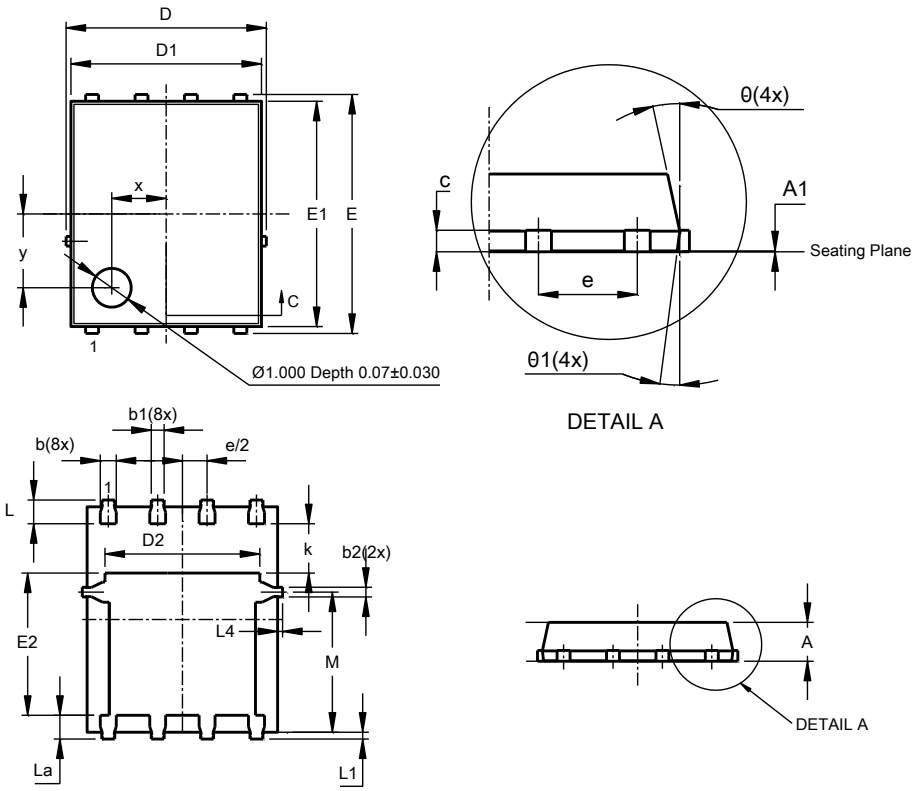
Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

Site1:

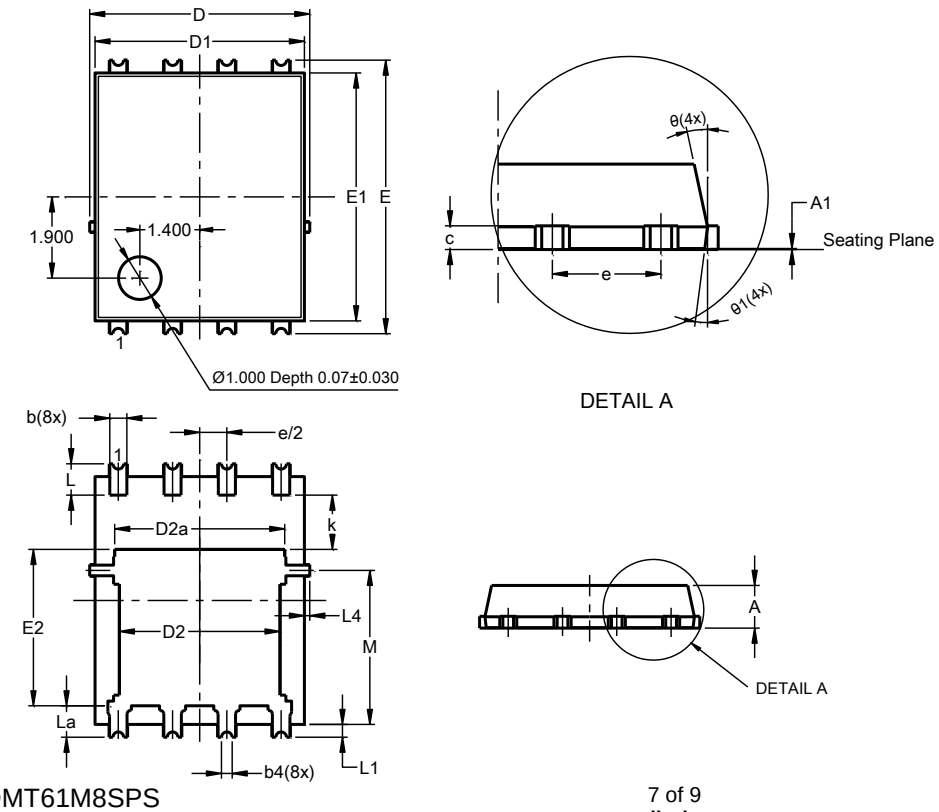
PowerDI5060-8 (Type K)



PowerDI5060-8 (Type K)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	0.02
b	0.33	0.51	0.41
b1	0.300	0.366	0.333
b2	0.20	0.35	0.25
c	0.23	0.33	0.277
D	5.15 BSC		
D1	4.85	4.95	4.90
D2	-	-	3.98
E	6.15 BSC		
E1	5.75	5.85	5.80
E2	3.56	3.725	3.66
e	1.27BSC		
k	-	-	1.27
L	0.51	0.71	0.61
La	0.51	0.675	0.61
L1	0.05	0.20	0.175
L4	-	-	0.125
M	3.50	3.71	3.605
x	-	-	1.400
y	-	-	1.900
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Site2:

PowerDI5060-8 (SWP) (Type UX)



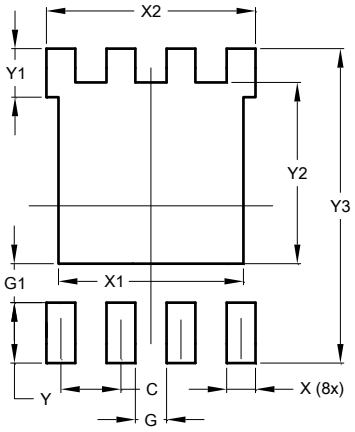
PowerDI5060-8 (SWP) (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

Site1:

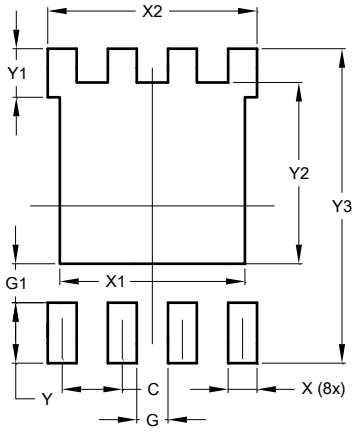
PowerDI5060-8 (Type K)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

Site2:

PowerDI5060-8 (SWP) (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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