N-channel 100 V, 10 mOhm, standard level MOSFET in D2PAK
28 October 2020 Product data sheet

1. General description

SuperSOA N-channel enhancement mode MOSFET in a D2PAK package qualified to 175 $^{\circ}$ C. PSMN8R9-100BSE delivers low R_{DSon} and very strong linear-mode (SOA) performance, and complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, low R_{DSon} to minimize I²R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- · Avalanche rated, 100% tested
- Low R_{DSon} for low I²R conduction losses
- D2PAK package

3. Applications

- Hot swap
- · Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	75	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$; Fig. 3		-	-	419	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	296	W
Static chara	cteristics						
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	8	10	mΩ
Dynamic cha	aracteristics						
Q_{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V;		-	32	45	nC
Q _{G(tot)}	total gate charge	Fig. 14; Fig. 15		-	114	160	nC
Avalanche re	uggedness		'				1
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 75 A; $V_{sup} \le 100$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4		-	-	422	mJ



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain[1]		
3	S	source		G—(FA)
mb	D	mounting base; connected to drain	1 3 D2PAK (SOT404)	mbb076 S

^[1] It is not possible to make connection to pin 2.

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN8R9-100BSE		plastic, single-ended surface-mounted package (D2PAK); 3 terminals (one lead cropped); 2.54 mm pitch; 11 mm x 10 mm x 4.3 mm body	SOT404		

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R9-100BSE	PSMN8R9 100BSE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit		
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	100	V		
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V		
V_{GS}	gate-source voltage			-20	20	V		
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	296	W		
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	75	А		
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>		-	74	А		
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$; Fig. 3		-	419	А		
T _{stg}	storage temperature			-55	175	°C		
Tj	junction temperature			-55	175	°C		
$T_{sld(M)}$	peak soldering temperature			-	260	°C		
Source-drain di	Source-drain diode							
Is	source current	T _{mb} = 25 °C		-	75	А		

Symbol	Parameter	Conditions		Min	Max	Unit		
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	419	А		
Avalanche rugge	Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 75 A; $V_{sup} \le 100$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4		-	422	mJ		

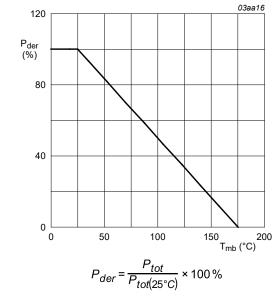
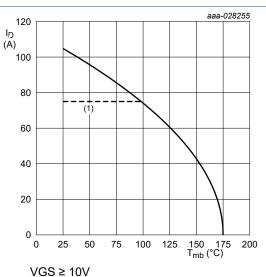
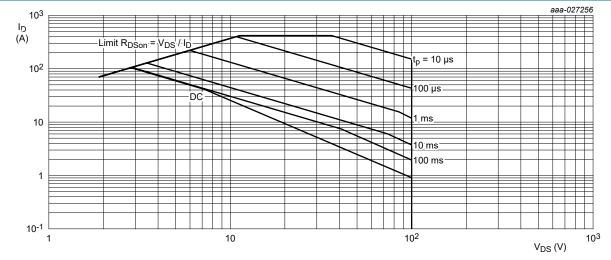


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



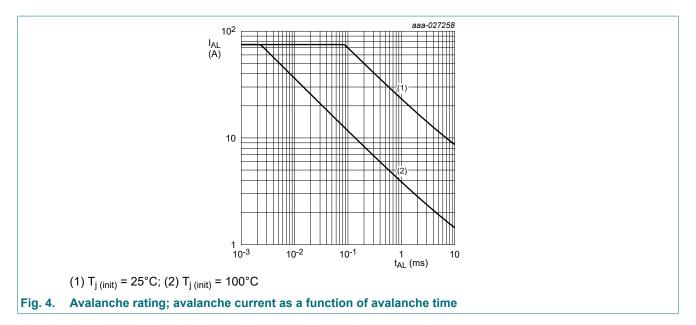
1) Capped at 75A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

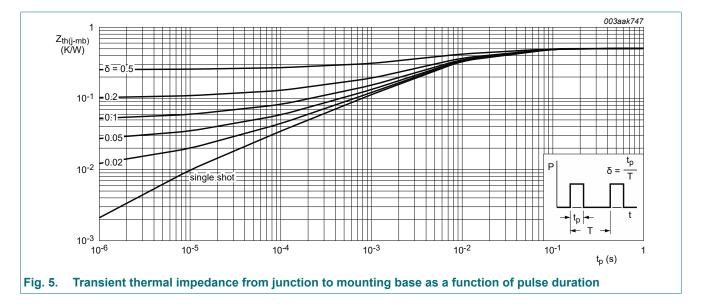
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	0.42	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	50	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
	breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; <u>Fig. 10</u> ; <u>Fig. 11</u>	1.8	2.7	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ °C};$ Fig. 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 11$	-	-	4.6	V
I _{DSS} dra	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.1	2	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	8	10	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 13	-	-	18.5	mΩ
		V_{GS} = 10 V; I_{D} = 25 A; T_{j} = 175 °C; Fig. 13	-	-	27	mΩ
R _G	gate resistance	f = 1 MHz	0.4	0.8	1.6	mΩ
Dynamic ch	aracteristics			'		
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14; Fig. 15	-	114	160	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	45	63	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V;	-	33	46	nC
Q _{GS(th)}	pre-threshold gate- source charge	Fig. 14; Fig. 15	-	18	-	nC
Q _{GS(th-pl)}	post-threshold gate- source charge		-	15	-	nC
Q_{GD}	gate-drain charge		-	32	45	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; <u>Fig. 14</u> ; <u>Fig. 15</u>	-	5.3	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz;	-	7028	9488	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 16</u>	-	447	603	pF
C _{rss}	reverse transfer capacitance		-	237	332	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \Omega; V_{GS} = 10 \text{ V};$	-	28	42	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	52	78	ns
$t_{d(off)}$	turn-off delay time	1	-	60	90	ns
t _f	fall time	1	-	44	66	ns
Source-drai	n diode					
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _i = 25 °C; <u>Fig. 17</u>	-	0.83	1.2	V

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	77	100	ns
Q _r	recovered charge	$V_{DS} = 50 \text{ V}$	[1]	-	248	322	nC

[1] includes capacitive recovery

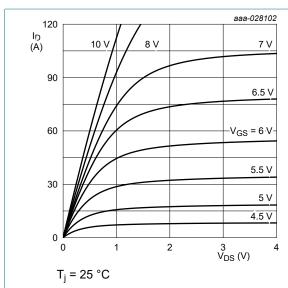


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

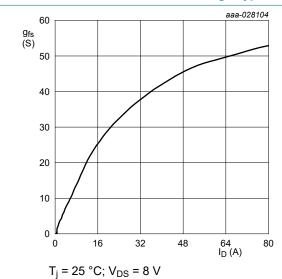


Fig. 8. Forward transconductance as a function of drain current; typical values

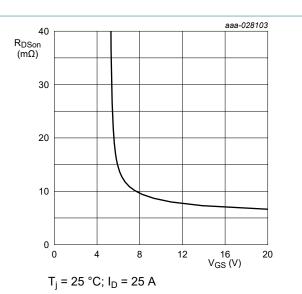


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

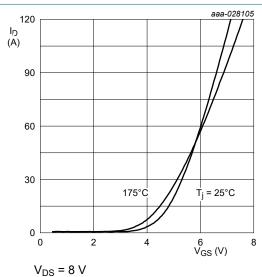


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

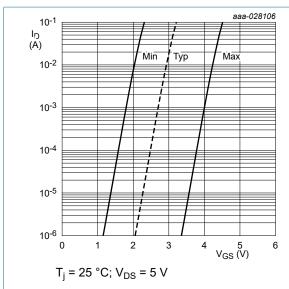


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

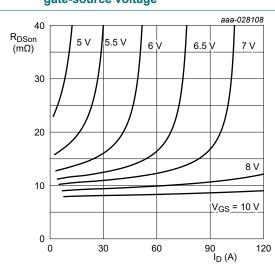


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

 $T_i = 25 °C$

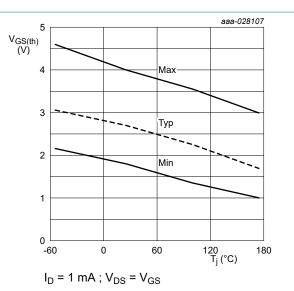


Fig. 11. Gate-source threshold voltage as a function of junction temperature

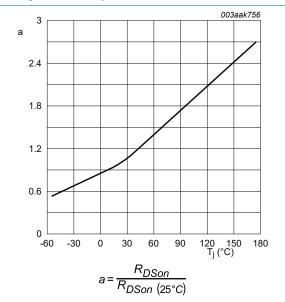


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

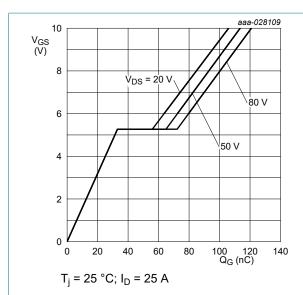


Fig. 14. Gate-source voltage as a function of gate charge; typical values

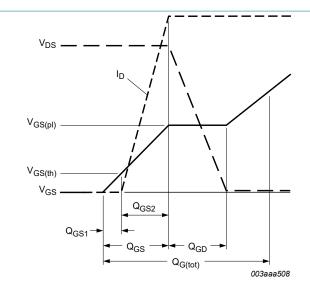


Fig. 15. Gate charge waveform definitions

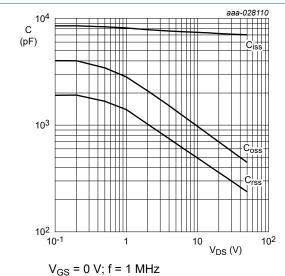
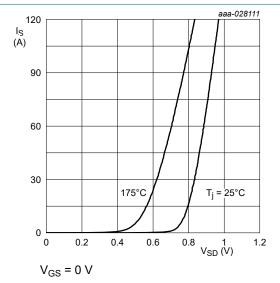
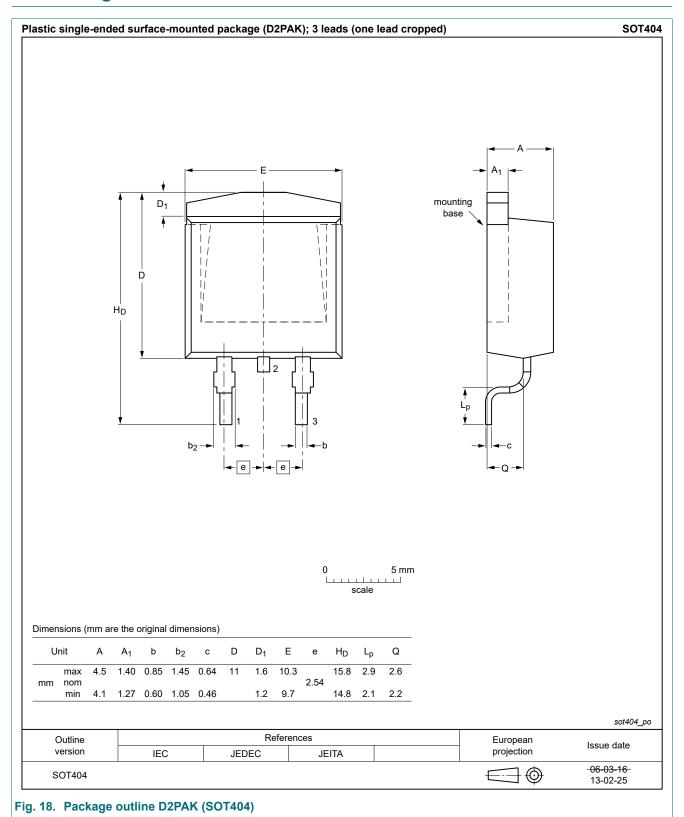


Fig. 16. Input, output and reverse transfer capacitances | Fig. 17. Source-drain (diode forward) current as a as a function of drain-source voltage; typical values

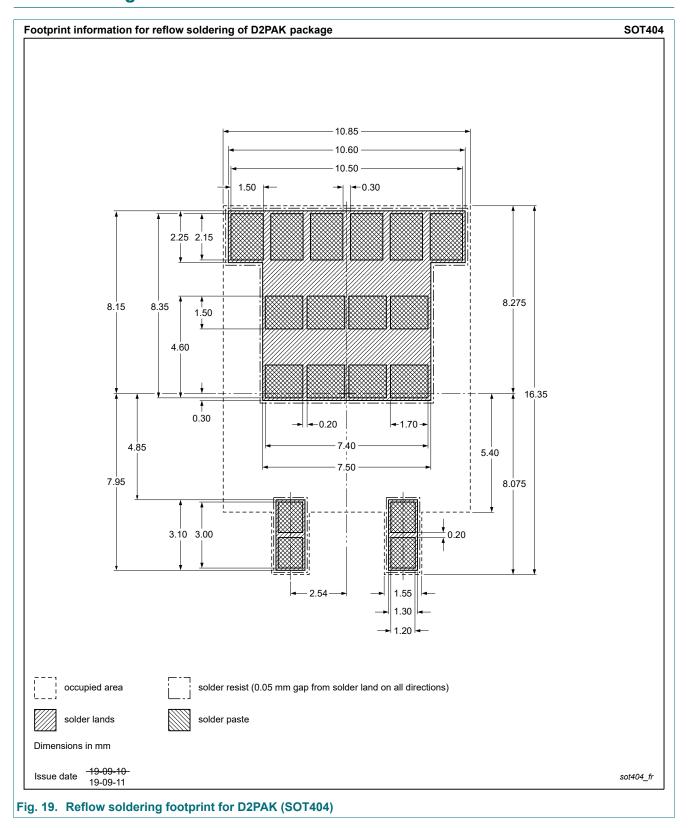


function of source-drain (diode forward) voltage; typical values

11. Package outline



12. Soldering



13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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