

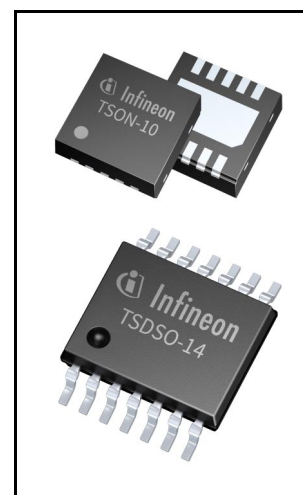
# TLF11251

## 2.5 A Half-Bridge with integrated driver and level shifter



### Features

- Integrated PMOS and NMOS complementary output bridge with 2.5 A current capability
- Integrated gate drivers
- Single control input with an integrated dead-time logic allows for optimized control and high efficiency
- Output current sensing and limitation
- Overtemperature protection
- Low quiescent current
- No external dead-time adjustment required
- Green product (RoHS compliant)
- AEC Qualified
  - Grade 1 PG-TSON-10
  - Grade 0 PG-TSDSO-14



### Potential applications

Core voltage regulation for AURIX™ TC3xx microcontroller with the power management IC TLF3558x.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The TLF11251 is an integrated gate driver and half-bridge with a high-side P-channel MOSFET and a low-side N-channel MOSFET in a single package. The integrated level shifting stage allows for conversion of the input logic signals to the supply voltage level of the gate drivers. The input signal levels are CMOS compatible. The level shifter and the gate driver provide a dead-time generation to simplify the interface with the embedded core voltage regulator of the AURIX™ TC3xx microcontroller. The low propagation delay allows for use in closed loop control applications with limited requirements for timing. The output stage allows for a high switching frequency. The TLF11251 integrates protection features against overcurrent at high-side MOSFETs and low-side MOSFETs and against overtemperature events. Internal power-on reset releases the digital logic and ensures its operation for supply voltage within the specified range.

Type	Package	Marking
TLF11251LD	PG-TSON-10	11251
TLF11251EP	PG-TSDSO-14	TLF11251

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## Block diagram

### 1 Block diagram

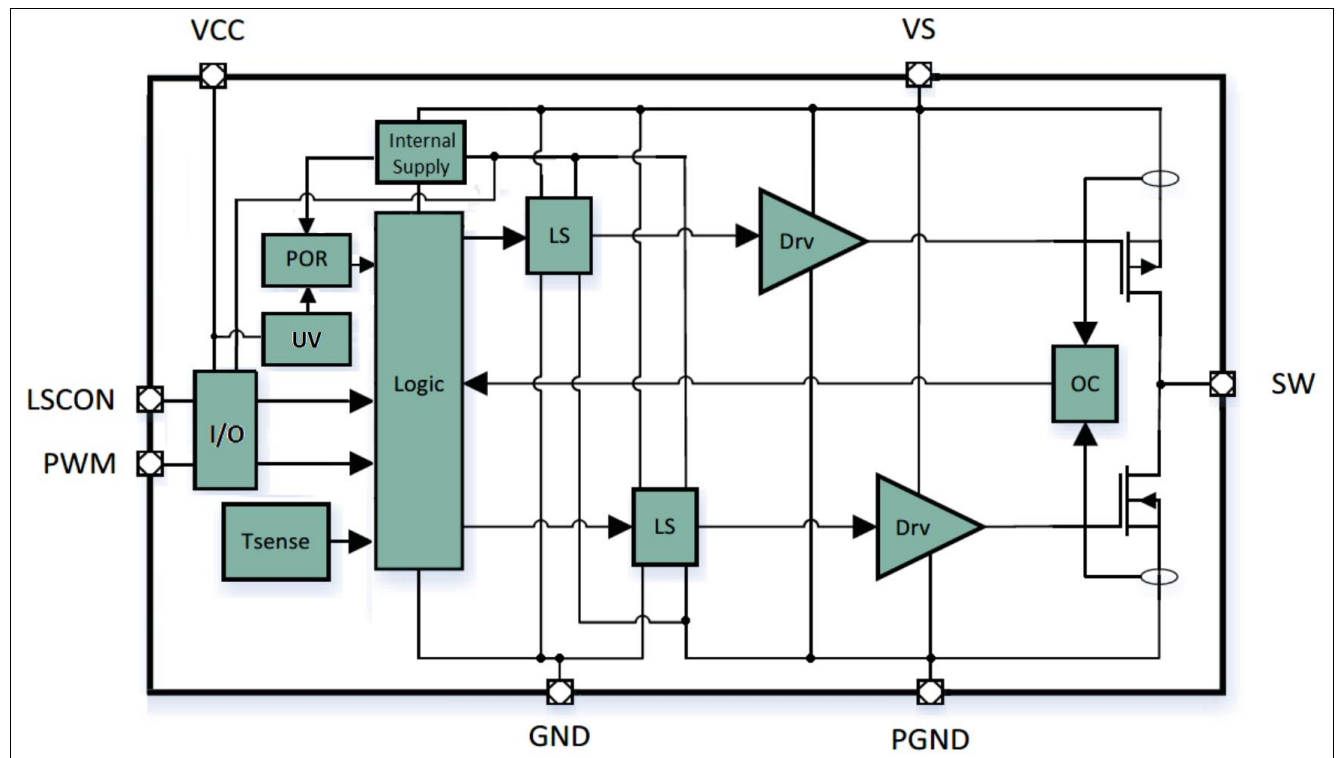


Figure 1 Block diagram

## Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment PG-TSON-10

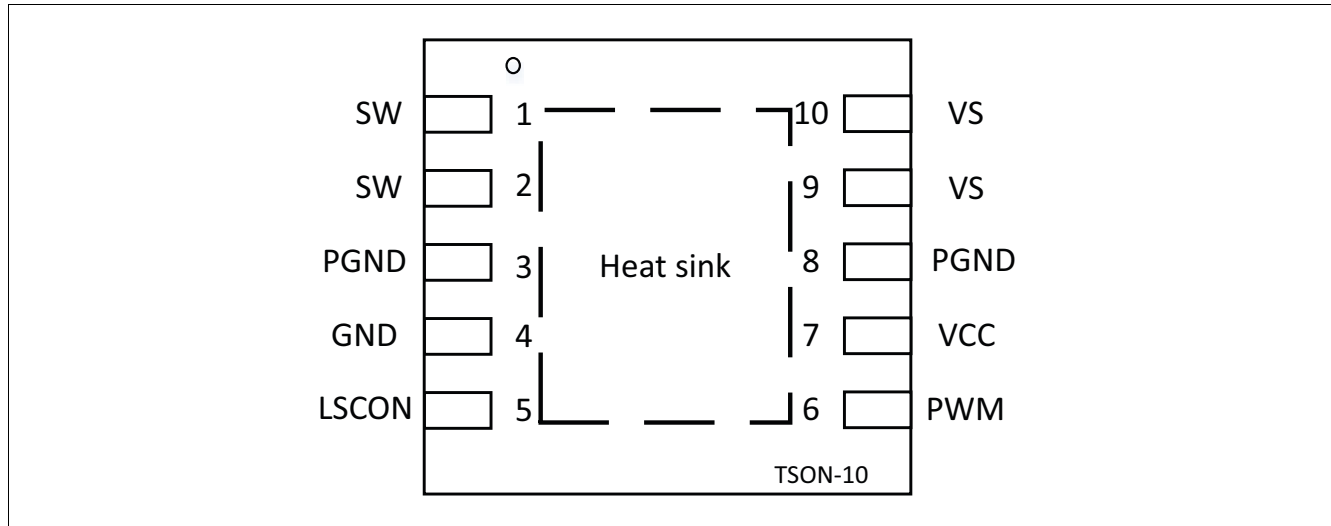


Figure 2 Pin configuration (TLF11251LD)

### 2.2 Pin definitions and functions PG-TSON-10

Pin	Symbol	Function
1, 2	SW	<b>Switch node;</b> half-bridge drains, typically connected to the input of LC filter in buck circuits
3, 8	PGND	<b>Power ground;</b> half-bridge low-side source
4	GND	<b>Ground;</b> Logical ground
5	LSCON	<b>Bridge control scheme;</b> Defines low-side state during PWM input "high". Switch to "high": enable synchronous control of high-side and low-side low-side, based on PWM input state Switch to "low": disable low-side control
6	PWM	<b>Control input;</b> Input for the logical signal that controls the state of the half-bridge transistors. Switch to "high": open high-side switch and close the low-side switch Switch to "low": close high-side switch and open low-side switch
7	VCC	<b>Supply voltage input;</b> Supply voltage for the PWM and LSCON inputs; typically the same as the supply of microcontroller output pins
9, 10	VS	<b>Supply voltage input;</b> Provides supply to gate drivers, connected to half-bridge high-side source
–	Heat Sink	Connect to heat sink area and to GND and PGND

## Pin configuration

## 2.3 Pin assignment PG-TSDSO-14

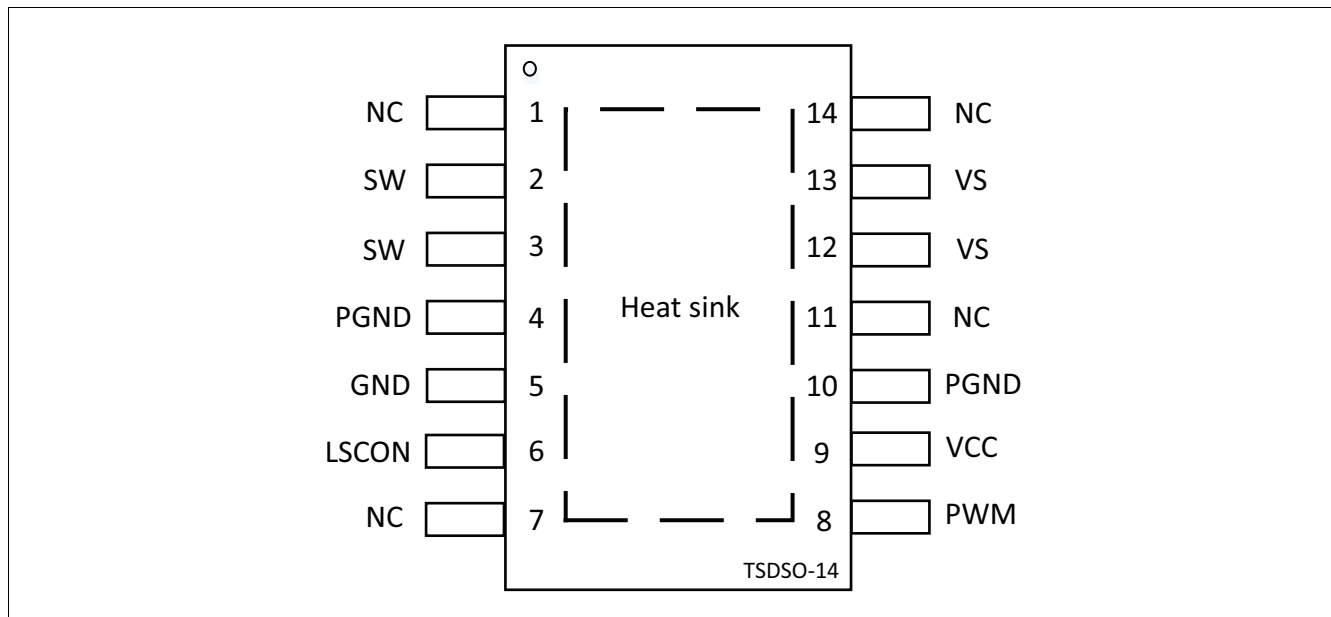


Figure 3 Pin configuration (TLF11251EP)

## 2.4 Pin definitions and functions PG-TSDSO-14

Pin	Symbol	Function
1	NC	<b>Not connected;</b> This pin is not connected internally. Leave open
2, 3	SW	<b>Switch node;</b> half-bridge drains, typically connected to the input of LC filter in buck circuits
4, 10	PGND	<b>Power ground;</b> half-bridge low-side source
5	GND	<b>Ground;</b> Logical ground
6	LSCON	<b>Bridge control scheme;</b> Defines low-side state during PWM input "high". Switch to "high": enable synchronous control of high-side and low-side, based on PWM input state Switch to "low": disable low-side control
7	NC	<b>Not connected;</b> This pin is not connected internally. Leave open
8	PWM	<b>Control input;</b> Input for the logical signal that controls the state of the half-bridge transistors. Switch to "high": open high-side switch and close the low-side switch Switch to "low": close high-side switch and open low-side switch
9	VCC	<b>Supply voltage input;</b> Supply voltage for the PWM and LSCON inputs; typically the same as the supply of microcontroller output pins

## Pin configuration

Pin	Symbol	Function
11	NC	<b>Not connected;</b> This pin is not connected internally. Leave open
12, 13	VS	<b>Supply voltage input;</b> Provides supply to gate drivers, connected to half-bridge high-side source
14	NC	<b>Not connected;</b> This pin is not connected internally. Leave open
–	Heat Sink	Connect to heat sink area and to GND and PGND

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 1** Absolute maximum ratings<sup>1)</sup>

$T_j$  = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS	VS	-0.3	–	7.0	V	–	P_3.1.1
Supply voltage VCC	VCC	-0.3	–	7.0	V	–	P_3.1.2
Switch node SW	VSW	-0.3	–	7.0	V	–	P_3.1.3
Input PWM	VPWM	-0.3	–	7.0	V	–	P_3.1.4
Input LSCON	VLSCON	-0.3	–	7.0	V	–	P_3.1.5
Currents							
Continuous drain current high-side	IDHS	–2.5	–	–	A	PWM = off	P_3.1.6
Continuous drain current low-side	IDLS	–	–	2.5	A	PWM = on	P_3.1.7
Pulsed drain current high-side	IDHS	–4.4	–	–	A	Valid during active overcurrent protection	P_3.1.8
Pulsed drain current low-side	IDLS	–	–	4.4	A	Valid during active overcurrent protection	P_3.1.9
Temperatures							
Junction temperature	Tj	-40	–	150	°C	–	P_3.1.10
Storage temperature	Tstg	-55	–	150	°C	–	P_3.1.11
ESD susceptibility							
ESD susceptibility all pins	VESD	-2	–	2	kV	HBM <sup>2)</sup>	P_3.1.12
ESD susceptibility all pins	VESD	-500	–	500	V	CDM <sup>3)</sup>	P_3.1.13
ESD susceptibility (corner pins)	VESD	-750	–	750	V	CDM <sup>3)</sup>	P_3.1.14

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF.).

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101.

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## General product characteristics

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.

### 3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range VS	$V_{S,nom}$	3.5	–	7.0	V	–	P_3.2.1
Supply voltage range VCC	$V_{CC,nom}$	2.35	–	7.0	V	–	P_3.2.2
Supply voltage VS transient slew rate	$dV_S/dt$	-120	–	120	V/ms	<sup>1)</sup>	P_3.2.3
Supply voltage VCC transient slew rate	$dV_{CC}/dt$	-120	–	120	V/ms	<sup>1)</sup>	P_3.2.4
Junction temperature	$T_j$	-40	–	150	°C	AEC-Q100 Grade 1	P_3.2.5
	$T_j$	-40	–	175	°C	AEC-Q100 Grade 0 PG-TSDSO14 only	P_3.2.6
Supply current total, normal operation	$I_{C,norm}$	–	–	35	mA	PWM input @1.8MHz	P_3.2.9
Supply current total, no switching	$I_{C,ns}$	–	200	–	μA	$V_S < 5.8\text{ V}$ , $V_{CC} < 5.1\text{ V}$ , $T_j < 85^\circ\text{C}$	P_3.2.10

1) Not subject to production test, specified by design.

**Note:** Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

## General product characteristics

## 3.3 Thermal resistance

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

Table 3 Thermal resistance <sup>1)</sup>

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PG-TSON-10							
Junction to case top - high-side	$R_{thJCT(HS)}$	51.6	–	57.0	K/W	–	P_3.3.1
Junction to case top - low-side	$R_{thJCT(LS)}$	64.5	–	71.2	K/W	–	P_3.3.2
Junction to case bottom - high-side	$R_{thJCB(HS)}$	6.3	–	6.9	K/W	–	P_3.3.3
Junction to case bottom - low-side	$R_{thJCB(LS)}$	9.4	–	10.4	K/W	–	P_3.3.4
Junction to ambient	$R_{thJA}$	–	54.5	–	K/W	2)	P_3.3.5
PG-TSDSO-14							
Junction to case top - high-side	$R_{thJCT(HS)}$	30.9	–	34.1	K/W	–	P_3.3.6
Junction to case top - low-side	$R_{thJCT(LS)}$	39.5	–	43.7	K/W	–	P_3.3.7
Junction to case bottom - high-side	$R_{thJCB(HS)}$	9.6	–	10.6	K/W	–	P_3.3.8
Junction to case bottom - low-side	$R_{thJCB(LS)}$	13.4	–	14.8	K/W	–	P_3.3.9
Junction to ambient	$R_{thJA}$	–	43.3	–	K/W	2)	P_3.3.10

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a  $76.2 \times 114.3 \times 1.5 \text{ mm}^3$  board with 2 inner copper layers ( $2 \times 70 \mu\text{m Cu}$ ,  $2 \times 35 \mu\text{m Cu}$ ). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

## Functional description

## 4 Functional description

The TLF11251 integrated driver and lever shifter simplifies the interface of microcontroller control outputs to the MOSFET half-bridge.

### 4.1 Behavior of logical inputs

A single PWM input controls the state of the half-bridge MOSFETs. The inverted logical scheme translates the PWM input state to the gate signal shifted to the output supply level, thus the high-side MOSFET is turned off during PWM logical ON state, and turned on during PWM logical OFF state. The built-in dead-time control circuitry prevents a shoot-through condition over the MOSFET bridge and improves system efficiency while used in buck power conversion circuits. No external dead-time adjustment is required.

In addition to the PWM input, the LSCON input determines the low-side MOSFET control scheme and allows for both synchronous as well as asynchronous operation in buck converter applications. Logical OFF state at the LSCON input turns off the low-side MOSFET independently of the PWM input signal, so that only the high-side MOSFET is controlled.

A permanent logical ON state at LSCON input allows both high-side and low-side operation according to PWM input state with the internal dead-time generation. The LSCON input can be pulled-up or connected directly to the VCC supply rail if such operation is required.

A toggling input signal at LSCON is recognized as a control request for synchronous low-side and high-side MOSFET switching. In this case the TLF11251 generates dead-time internally in accordance with the PWM input timing. Frequency detection at LSCON inputs detect toggling input signals within the acceptable range referred to as  $t_{det}$ .

**Table 4 Switching states**

LSCON	PWM	high-side MOSFET	low-side MOSFET
ON	ON <sup>1)</sup>	Turned off	Turned on
ON	OFF <sup>2)</sup>	Turned on	Turned off
OFF	ON	Turned off	Turned off
OFF	OFF	Turned on	Turned off
Toggling ON/OFF <sup>3)</sup>	ON	Turned off	Turned on
	OFF	Turned on	Turned off
Toggling ON/OFF stop <sup>4)</sup> ( $< t_{fil}$ )	ON	Turned off	Turned on
	OFF	Turned on	Turned off
Toggling ON/OFF stop ( $> t_{fil}$ ); LSCON=ON	ON	Turned off	Turned on
Toggling ON/OFF stop ( $> t_{fil}$ ); LSCON=ON	OFF	Turned on	Turned off
Toggling ON/OFF stop ( $> t_{fil}$ ); LSCON=OFF	ON	Turned off	Turned off
Toggling ON/OFF stop ( $> t_{fil}$ ); LSCON=OFF	OFF	Turned on	Turned off

1) ON: "high"

2) OFF: "low"

3) Toggling ON/OFF - detected ON/OFF switching with the frequency within the detection range  $t_{det}$  at LSCON input signal.

## Functional description

- 4) Toggling ON/OFF stop - detected permanent ON or OFF state after the Toggling ON/OFF operation

The states described in [Table 4](#) are only valid for device input supplies within the operational range and when no protection features are active.

If the PWM pin is not connected, then the integrated weak pull-up ensures a defined level.

An additional pull-down resistor should be placed at LSCON input to keep the low-side MOSFET turned off during power-down in the case where the TLF11251 is controlled by an AURIX™ TC3xx microcontroller. Please refer to [Chapter 5](#) for more details.

## 4.2 Control parameters

The TLF11251 provides a high frequency switching capability with a low propagation delay. The input stage and the drivers can react to fast changing PWM signals and provide a  $t_{res}$  resolution to the duty time of the input signal with a pulse duration longer than  $t_{pulse}$ . The low state pulse duration is limited to  $t_{pulse, min}$ .

The total propagation time  $t_{prop}$  is the time from the "low"-to-"high" or "high"-to-"low" edge transition at the PWM input to the SW output level transitions to 10% or 90% of  $V_S$  supply level accordingly. The internal dead-time generation provides optimal efficiency during switching phases and provides the state change of the switching node SW within the specified propagation delay.

The device is optimized for a switching frequency in a typical buck converter application in the range of 0.3 MHz to 2 MHz.

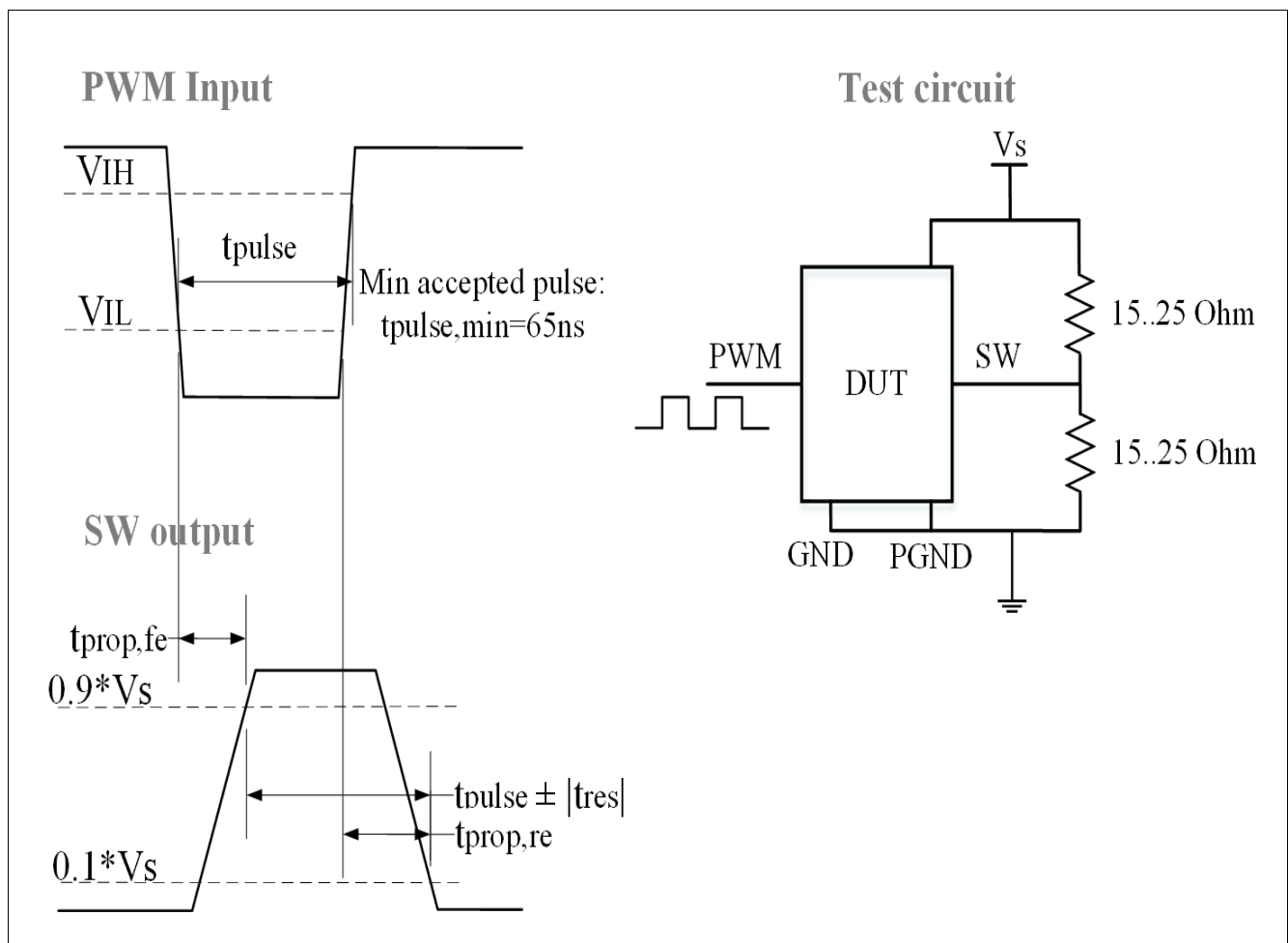


Figure 4 Control timing diagram

## Functional description

**Table 5** Electrical characteristics: control parameters

$V_S = 3.5 \text{ V to } 7 \text{ V}$ ,  $V_{CC} = 2.35 \text{ V to } 7 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation time, PWM falling edge	$t_{\text{prop,fe}}$	–	–	60	ns	HS drain connected to resistive load. $V_{CC} > 3.0 \text{ V}$ , $V_S > 4.5 \text{ V}$	P_4.2.1
Propagation time, PWM rising edge	$t_{\text{prop,re}}$	–	–	60	ns	LS drain connected to resistive load. $V_{CC} > 3.0 \text{ V}$ , $V_S > 4.5 \text{ V}$	P_4.2.2
Minimum pulse width input	$t_{\text{pulse,min}}$	65	–	–	ns	1)	P_4.2.3
Pulse resolution time	$t_{\text{res}}$	–	–	3	ns	1)	P_4.2.4
Dead-time "high"-to-"low"	$t_{\text{dead,hl}}$	–	15	–	ns	1)	P_4.2.5
Dead-time "low"-to-"high"	$t_{\text{dead,lh}}$	–	18	–	ns	1)	P_4.2.6
LSCON frequency detector, frequency range	$f_{\text{det,lscn}}$	0.72	–	–	MHz	–	P_4.2.7
LSCON frequency detector, filter time	$t_{\text{fil,lscn}}$	3	–	–	us	1)	P_4.2.8

**Logic inputs**

Input voltage "high"	$V_{IH}$	$0.67 \times V_{CC}$	–	–	V	CMOS function	P_4.2.9
Input voltage "low"	$V_{IL}$	–	–	$0.33 \times V_{CC}$	V	CMOS function	P_4.2.10
Input voltage hysteresis	$V_{IHYS}$	0.05	–	–	V	–	P_4.2.11
Input capacitance	$C_{IN}$	–	10	–	pF	1)	P_4.2.12

1) Not subject to production test, specified by design.

## Functional description

## 4.3 Output stage

The P-N-channel output half-bridge of the TLF11251 can operate at high switching frequency up to 2 MHz nominal range, providing very low power dissipation while used in synchronous buck converter topology. The P-channel MOSFET is used as a high-side switch, which eliminates the need to use a charge pump circuitry and also improves the EMI performance. The output stage delivers a minimum output current of at least 2.5 A within the specified voltage and temperature range.

**Table 6 Electrical characteristics: output stage**

$V_S = 3.5\text{ V to }7\text{ V}$ ,  $V_{CC} = 2.35\text{ V to }7\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

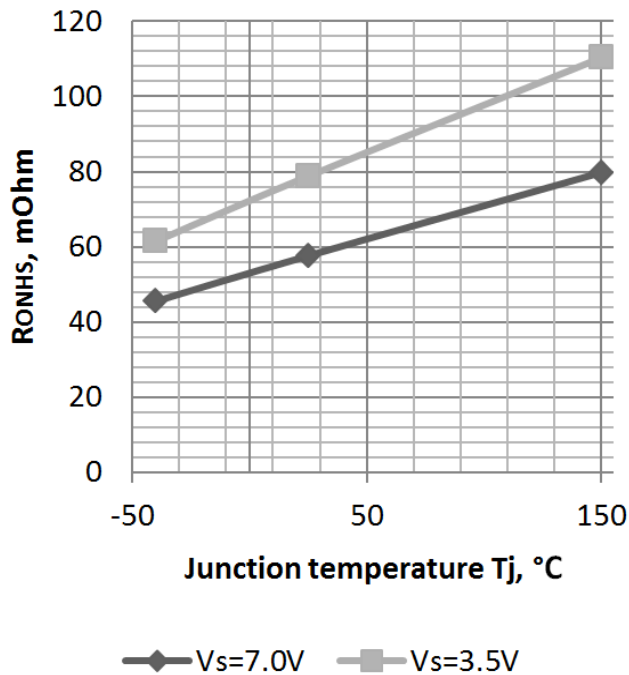
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON state resistance high-side	$R_{ONHS}$	–	–	100	mΩ	$T_j \leq 150^\circ\text{C}$ , $I_d = -2\text{ A}$ , $V_S = 5.8\text{ V}$	P_4.3.1
		–	–	70	mΩ	<sup>1)</sup> $T_j \leq 85^\circ\text{C}$ , $I_d = -2\text{ A}$ , $V_S = 5.8\text{ V}$	P_4.3.2
ON state resistance low-side	$R_{ONLS}$	–	–	105	mΩ	$T_j \leq 150^\circ\text{C}$ , $I_d = 2\text{ A}$ , $V_S = 5.8\text{ V}$	P_4.3.3
		–	–	75	mΩ	<sup>1)</sup> $T_j \leq 85^\circ\text{C}$ , $I_d = 2\text{ A}$ , $V_S = 5.8\text{ V}$	P_4.3.4
Body diode forward voltage high-side	$V_{DFHS}$	–	0.67	0.95	V	$I_{fw} = 2\text{ A}$	P_4.3.5
Body diode forward voltage low-side	$V_{DFLS}$	–	0.72	0.91	V	$I_{fw} = 2\text{ A}$	P_4.3.6

1) Not subject to production test, specified by design.

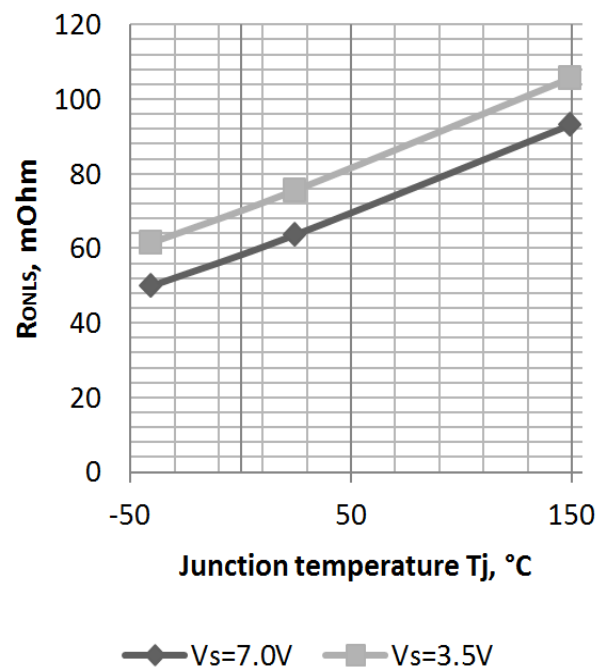
## Functional description

## Maximum ON state resistance

ON state resistance high-side  $R_{ONHS}$   
(PWM = "low"), versus  $T_j = -40, 25, 150^\circ\text{C}$



ON state resistance low-side  $R_{ONLS}$   
(PWM = "high"), versus  $T_j = -40, 25, 150^\circ\text{C}$



#### 4.4 Protection functions

Integrated protection functions prevent the TLF11251 and the output circuitry from destruction as well as from operation under unspecified conditions. The implemented features consist of:

- high-side and low-side overcurrent detection and limitation
- undervoltage shutdown
- overtemperature protection

The TLF11251 reacts within the time specified for each protection feature. In all cases this is related to the state change of the half-bridge MOSFETs independent from the PWM input signal. The input logic reset release is ensured at  $V_s$  voltage exceeding the minimum functional limit of 3.5 V, where protection functions are also operational. For the  $V_{CC}$  voltage below  $V_{CCUV}$ , the output half-bridge MOSFETs remain in the OFF state and the output switch node SW is floating.

##### 4.4.1 Undervoltage shutdown

The TLF11251 monitors the input supply  $V_{CC}$  for undervoltage conditions. If the output voltage drops below the  $V_{CCUV}$  limit, then the TLF11251 turns off the high-side and low-side MOSFETs, so that the device is only operational within the specified supply limits. The voltage hysteresis circuitry  $V_{CCUVh}$  protects from noise conditions.

## Functional description

**Table 7** Electrical characteristics: undervoltage shutdown

$V_S = 3.5\text{ V to }7\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

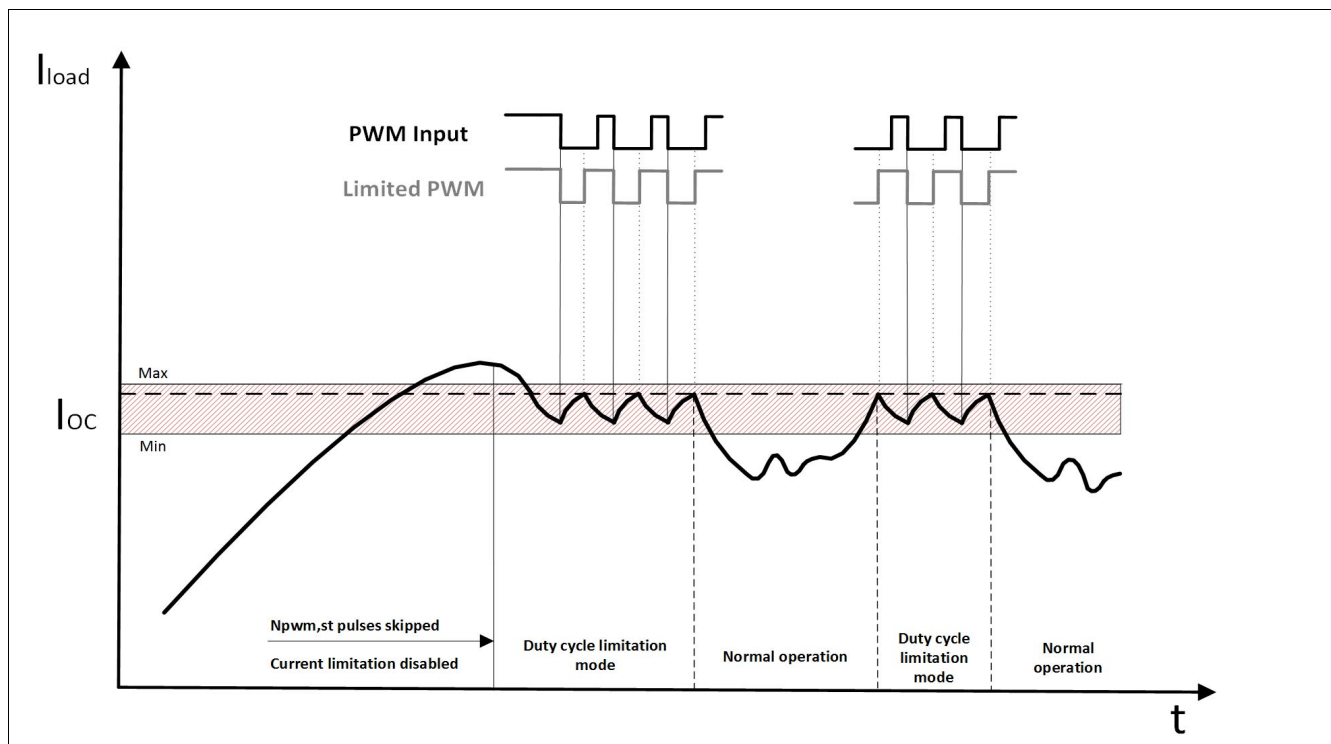
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Undervoltage limit at $V_{CC}$ supply	$V_{CCUV}$	1.95	–	2.28	V	$V_{CC}$ falling	P_4.4.2.1
Undervoltage detector hysteresis	$V_{CCUVH}$	0.05	–	0.1	V	–	P_4.4.2.2
Undervoltage detector reaction time	$V_{UVR}$	–	–	3	us	1)	P_4.4.2.3

1) Not subject to production test, specified by design.

**4.4.2 Overcurrent protection**

The overcurrent protection works in a cycle-by-cycle limitation mode. If the sensed input drain current exceeds the peak current limit  $I_{OC, \text{lim}}$  during a switching cycle, then the TLF11251 turns off the high-side MOSFET and the switch node SW current starts to decay. If the overcurrent protection circuitry is active, then the TLF11251 limits the PWM input duty cycle for each cycle.

During startup or with  $V_{CC}$  supply power cycle after the logic reset is released, the overcurrent protection remains inactive for the number of PWM pulses  $n_{\text{pwm,st}}$  to avoid accidental activation due to start-up current overshoot.

**Figure 5** Overcurrent protection function



## Functional description

**Table 8 Electrical characteristics: overcurrent protection**

$V_S = 3.5 \text{ V to } 7 \text{ V}$ ,  $V_{CC} = 2.35 \text{ V to } 7 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overcurrent sensing limit	$I_{oc,lim}$	-4.4	–	-2.6	A	–	P_4.4.3.1
Start-up protection inactive, number of PWM pulses	$n_{pwm,st}$	–	–	5500	–	$V_{CC}$ raising above $V_{CC,min}$	P_4.4.3.2

**4.4.3 Overtemperature protection**

If an overtemperature condition  $T_{jOT}$  occurs the integrated temperature sensor disables the device by switching off the high-side and low-side MOSFETs. Only if both the temperature decreases by the hysteresis temperature  $dT_j$  and the temperature falls below  $T_{jSO}$ , then the MOSFETs resume operation.

**Table 9 Electrical characteristics: overtemperature protection**

$V_S = 3.5 \text{ V to } 7 \text{ V}$ ,  $V_{CC} = 2.35 \text{ V to } 7 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overtemperature shut-down	$T_{jOT}$	175	–	200	$^\circ\text{C}$	1)	P_4.4.4.1
Switch on temperature	$T_{jSO}$	–	–	165	$^\circ\text{C}$	1)	P_4.4.4.2
Overtemperature switch-on hysteresis	$dT_j$	–	15	–	$^\circ\text{C}$	1)	P_4.4.4.3

1) Not subject to production test, specified by design.

## Application information

## 5 Application information

**Note:** The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

### 5.1 Typical application scenario

In the target application scenario the TLF11251 is the counterpart for an AURIX™ TC3xx microcontroller for core voltage generation with the system power supply TLF35584. The device configuration allows connectivity with the half-bridge control output of the microcontroller's Embedded Voltage Regulator Core (EVRC) converter, which generates the core voltage  $V_{dd}$ . The TLF11251 only supports power supply topologies that use different sources for the microcontroller pad supply domain  $V_{ext}$  and the EVRC input  $V_s$ , expecting different voltage levels. The system integrator must ensure that the  $V_s$  voltage exceeds the  $V_{CC}$  voltage during start-up, normal operation and power-down.

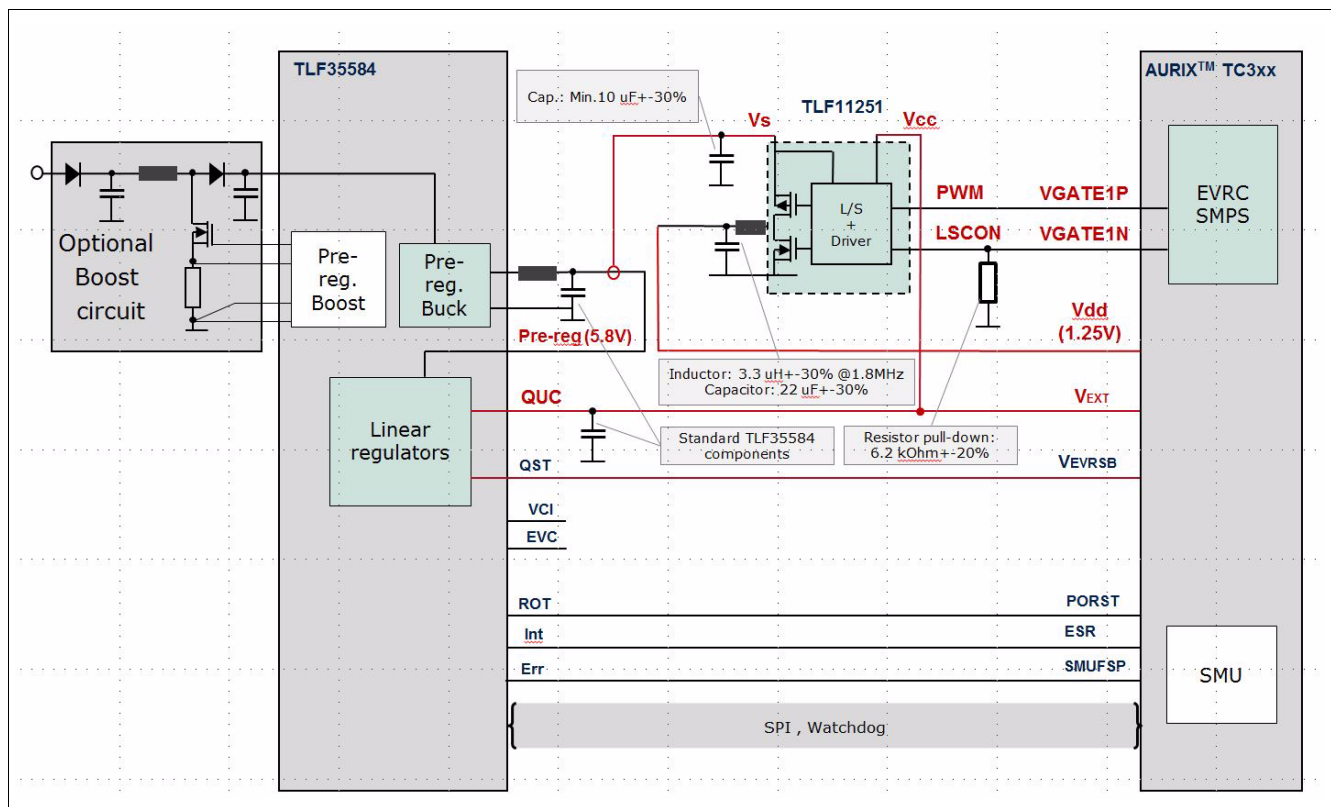


Figure 6 Application block diagram

As soon as the  $V_s$  supply voltage reaches 3.5 V during power-up, the internal logic reset will be released. During this phase the central function logic is operational. Only if the  $V_{CC}$  supply voltage is within the specified range, then the TLF11251 reacts to input signals LSCON and PWM as specified. However, the operational  $V_{CC}$  voltage minimum is specified at 2.35 V, which allows for early device readiness, even if the microcontroller is not yet operational.

The VGATEP output of the microcontroller controls the PWM signal, while the VGATEN output is connected to LSCON. The microcontroller typically starts in an open-loop mode, controlling only VGATEP and allowing for fast  $V_{dd}$  voltage ramp-up and start-up. After ramp-up time, the EVRC starts to control the high-side and low-side MOSFETs of the half-bridge. The LSCON input detects this phase with the frequency detector. If the microcontroller is switched into power-down mode and if the high-side and low-side control signals are off, then the frequency detector recognizes it as a request to set the SW output floating. Hence it is highly

## Application information

recommended to add a pull-down resistor for the LSCON signal in order to limit its possible variation during the power-down phase after the moment when the supply voltage reaches the hard reset limits of the microcontroller.

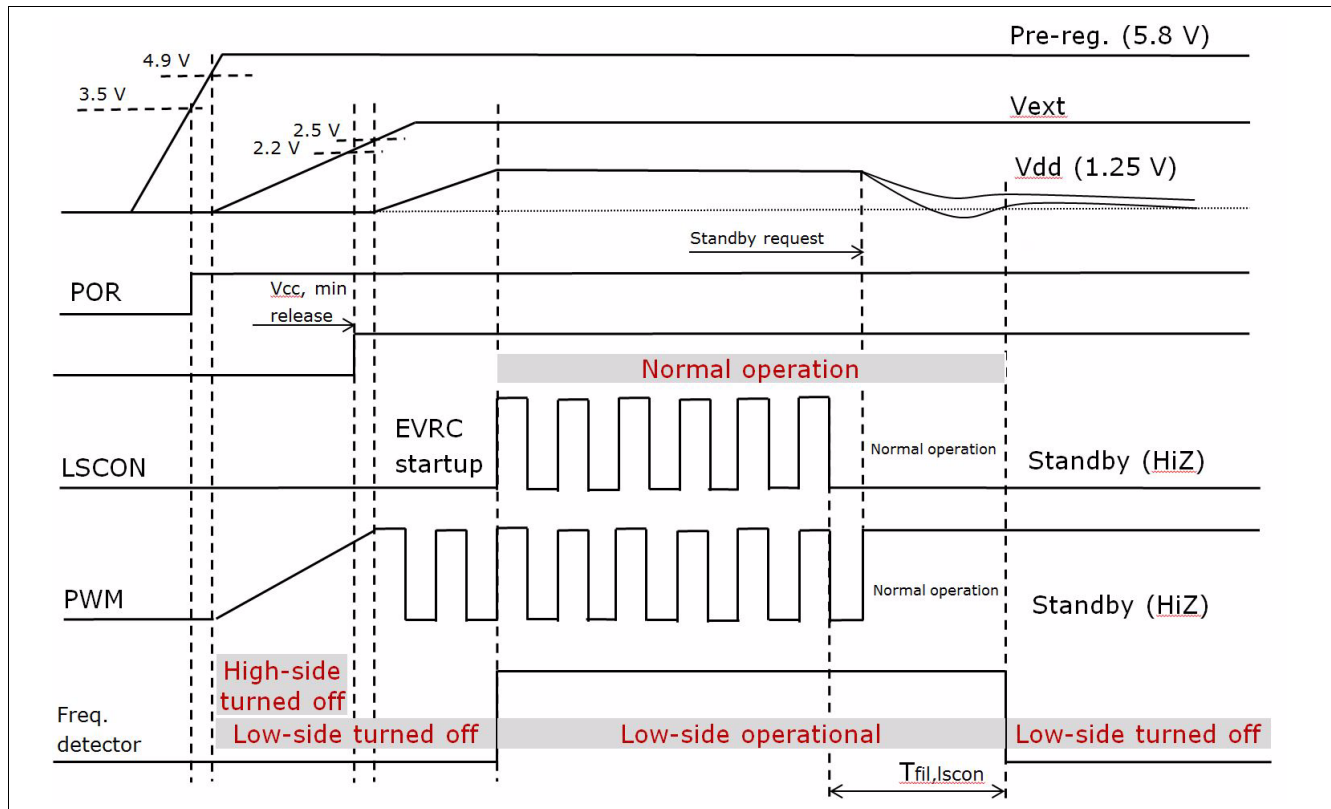


Figure 7 Start-up and ramp-down example flow<sub>B</sub>

Table 10 specify the required nominal values of the discrete components for proper operation.

Table 10 Nominal values of discrete components

Component name	Nominal value	Acceptable variation	Note
$C_{VS}$	10 $\mu$ F	+/-30%	Input capacitor
$C_{VDD}$	22 $\mu$ F	+/-30%	Output capacitor
$L_{VDD}$	3.3 $\mu$ H	+/-30% (@1.8 MHz)	Output inductor
$R_{LSCON}$	6.2 kOhm	+/-20%	LSCON input pull-down

## 5.2 Further application information

- Please contact us for information regarding the Pin Behavior Assessment
- For further information you may contact <http://www.infineon.com/>



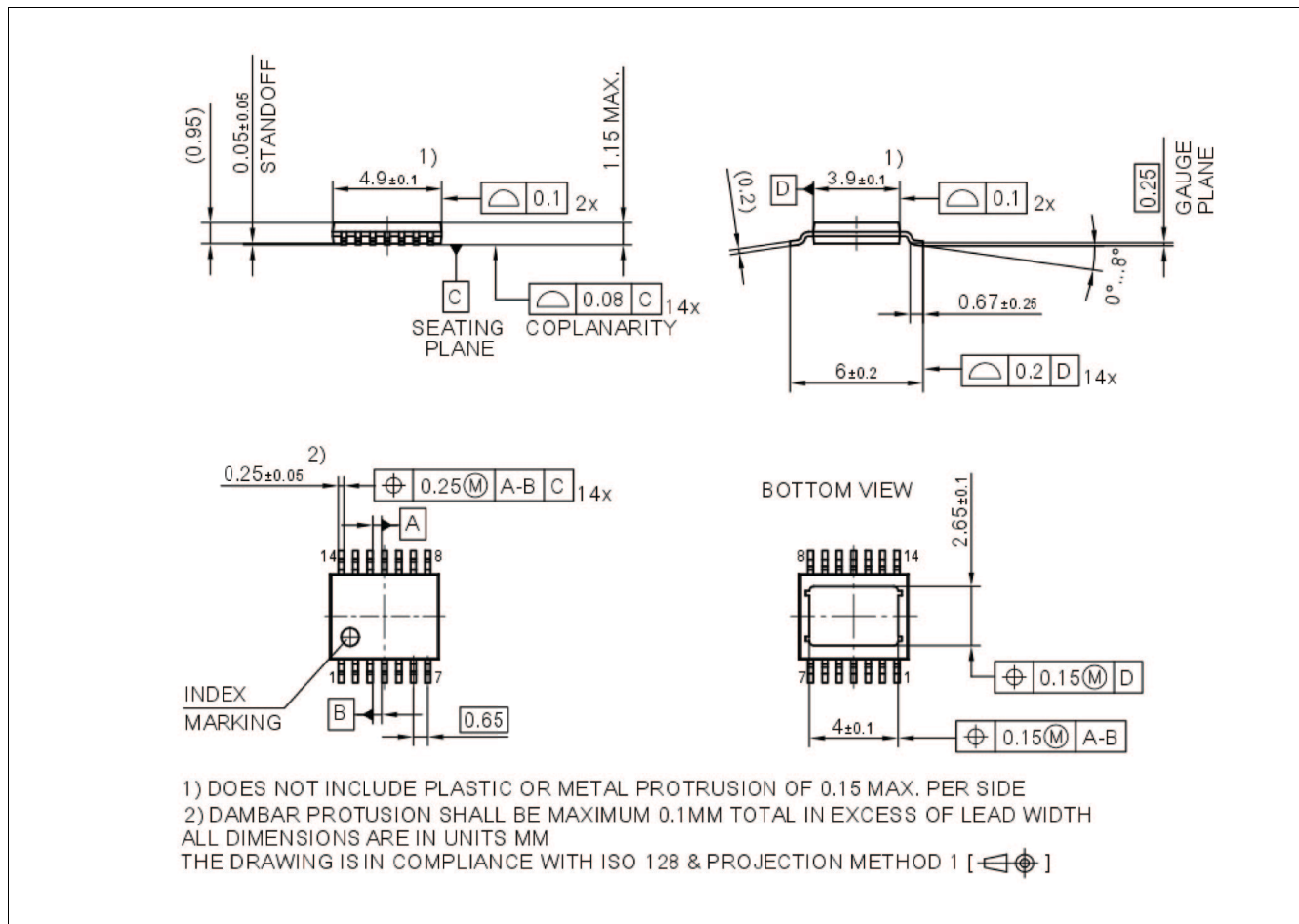


Figure 9 Package outline TLF11251EP - PG-TSDSO-14

### Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision history

## 7 Revision history

Table 11 Revision history

Revision	Date	Changes
1.0	2020-01-23	Initial datasheet

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