Product Change Notification / SYST-18CWHD261

Date:

24-Nov-2020

Product Category:

8-bit Microcontrollers

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - AVR64DA28/32/48/64 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-18CWHD261_Affected_CPN_11242020.pdf
SYST-18CWHD261_Affected_CPN_11242020.csv

Notification Text:

SYST-18CWHD261

Microchip has released a new Product Documents for the AVR64DA28/32/48/64 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at AVR64DA28/32/48/64 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
This revision includes the following updates to Data Sheet Clarifications:
1) Add new device revision (A4)
2) Added errata:
– Device: Some Reserved Fuse Bits Are '1'
– Device: CRC Check During Reset Initialization Is not Functional
– RSTCTRL: BOD Registers not Reset When UPDI Is Enabled
– TCA: Restart Will Reset Counter Direction in NORMAL and FRQ Mode
– TCB: CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode
– TCD: Asynchronous Input Events not Working When TCD Counter Prescaler Is Used
– USART: Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Nov 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

AVR64DA28/ 32/ 48/ 64 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

AVR64DA28-E/SO
AVR64DA28-E/SP
AVR64DA28-E/SS
AVR64DA28-I/SO
AVR64DA28-I/SP
AVR64DA28-I/SS
AVR64DA28T-E/SO
AVR64DA28T-E/SS
AVR64DA28T-I/SO
AVR64DA28T-I/SS
AVR64DA32-E/PT
AVR64DA32-E/RXB
AVR64DA32-I/PT
AVR64DA32-I/RXB
AVR64DA32T-E/PT
AVR64DA32T-E/RXB
AVR64DA32T-I/PT
AVR64DA32T-I/RXB
AVR64DA48-E/6LX
AVR64DA48-E/PT
AVR64DA48-I/6LX
AVR64DA48-I/PT
AVR64DA48T-E/6LX
AVR64DA48T-E/PT
AVR64DA48T-I/6LX
AVR64DA48T-I/PT
AVR64DA64-E/MR
AVR64DA64-E/PT
AVR64DA64-I/MR
AVR64DA64-I/PT
AVR64DA64T-E/MR
AVR64DA64T-E/PT
AVR64DA64T-I/MR
AVR64DA64T-I/PT

AVR64DA28/32/48/64

Silicon Errata and Data Sheet Clarification

The AVR64DA28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002233), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR64DA28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002233) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A3(1)	Rev. A4
Device	2.2.1 Some Reserved Fuse Bits Are '1'	X	-
Device	2.2.2 CRC Check During Reset Initialization Is not Functional	X	-
CCL	2.3.1 The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices	X	X
PORT	2.4.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input	X	X
RSTCTRL	2.5.1 BOD Registers not Reset When UPDI Is Enabled	X	X
TCA	2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.7.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X	X
TCD	2.8.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	X
TWI	2.9.1 The Output Pin Override Does not Function as Expected	X	X
USART	2.10.1 Open-Drain Mode Does not Work When TXD Is Configured as Output	X	X
USART	2.10.2 Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'	X	X
ZCD	2.11.1 All ZCD Output Selection Bits Are Tied to the ZCD0 Bit	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits Are '1'

The default fuse values may be not compliant with the data sheet. The fuse values will read out as listed below:

- OSCCFG = 0x78 (The device will use the OSCHF clock source)
- SYSCFG0 = 0xF2
- SYSCFG1 = 0xF8

Work Around

None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	-

2.2.2 CRC Check During Reset Initialization Is not Functional

The CRCSRC bit field in the SYSCFG0 fuse is ignored during Reset initialization. A CRC check will not be performed during Reset initialization. CRCSCAN is only available from the software.

Work Around

None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	-

2.3 CCL - Configurable Custom Logic

2.3.1 The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices

The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '0x2') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around

Connect LUT0 output to LUT3 input using the Event System.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.4 PORT - I/O Configuration

2.4.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input

If an input pin is selected to be analog input, the digital input function for those pins is automatically disabled.

Work Around
None

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.5 RSTCTRL - Reset Controller

2.5.1 BOD Registers not Reset When UPDI Is Enabled

If the UPDI is enabled, the VLMCTRL, INTCTRL, and INTFLAGS registers in BOD will not be reset by other reset sources than POR.

Work Around
None

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.6 TCA - 16-Bit Timer/Counter Type A

2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.7 TCB - 16-Bit Timer/Counter Type B

2.7.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.8 TCD - 12-Bit Timer/Counter Type D

2.8.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When the TCD is configured to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.9 TWI - Two-Wire Interface

2.9.1 The Output Pin Override Does not Function as Expected

When TWI is enabled, it overrides the output pin driver, but not the output value. The output on the line will always be high when the value in the PORTx.OUT register is '1' for the pins corresponding to the SDA or SCL.

Work Around

Ensure that the values in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.10 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.10.1 Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.10.2 Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'

The Start-of-Frame Detector can unintentionally be enabled when the device is in Active mode and when the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is '0'. If the Receive Data (RXDATA) registers are read while receiving new data, RXCIF is cleared, and the Start-of-Frame Detector will be enabled and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around
Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

2.11 ZCD - Zero-Cross Detector

2.11.1 All ZCD Output Selection Bits Are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around
Use the Event System or CCL to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A3	Rev. A4
X	X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002233).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Data Sheet Clarifications

None.

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Comments
B	11/2020	• Add new device revision (A4) • Added errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is not Functional* – RSTCTRL: *BOD Registers not Reset When UPDI Is Enabled* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events not Working When TCD Counter Prescaler Is Used* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'*
A	07/2020	Initial document release

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