MPQ4469

36V, 5A, Low Quiescent Current, Asynchronous, Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4469 is a step-down switching regulator with an integrated internal high-side power MOSFET and a configurable frequency from 350kHz to 2.5MHz. It provides up to 5A of highly efficient output current with current mode control for fast loop response.

The wide 3.3V to 36V input range accommodates a variety of step-down applications in automotive input environments. The device is ideal for battery-powered applications due to its extremely low quiescent current.

The MPQ4469 employs AAM (advanced asynchronous modulation) mode, which achieves high efficiency in light-load conditions by scaling down the switching frequency to reduce switching and gate-driving losses.

Standard features include soft start (SS), external clock sync, enable (EN) control, and a power good (PG) indicator. High duty cycle and low-dropout mode are provided for automotive cold crank conditions.

Over-current protection (OCP) is employed to prevent the inductor current from running away. Hiccup mode greatly reduces the average current in short circuit conditions. Thermal shutdown provides reliable, fault-tolerant operation.

The MPQ4469 is available in a QFN-20 (4mmx5mm) package.

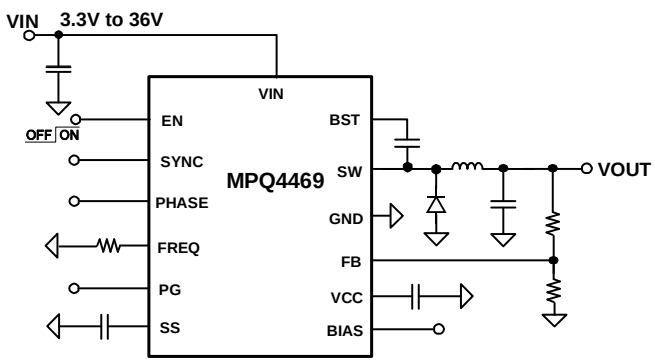
FEATURES

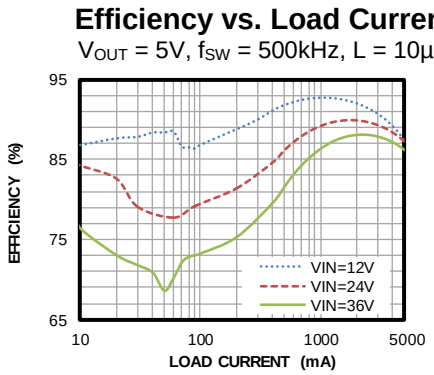
- Wide 3.3V to 36V Operating Input Range
- 5A Continuous Output Current
- 1μA Low Shutdown Mode Current
- 10μA Sleep Mode Quiescent Current
- Internal 110mΩ High-Side MOSFET
- 350kHz to 2.5MHz Configurable Switching Frequency
- Synchronize to External Clock
- Selectable In-Phase or 180° Out-of-Phase
- Power Good Indicator
- Configurable Soft-Start Time
- 100ns Minimum On Time
- Low Dropout Mode
- Over-Current Protection and Hiccup Mode
- AAM at Light Load
- Available in a QFN-20 (4mmx5mm) Package
- AEC-Q100 Grade-1

APPLICATIONS

- Automotive Systems
- Industrial Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4469GV-AEC1	QFN-20 (4mmx5mm)	*See Below*	2

* For Tape & Reel, add suffix –Z (e.g. MPQ4469GV–AEC1–Z).

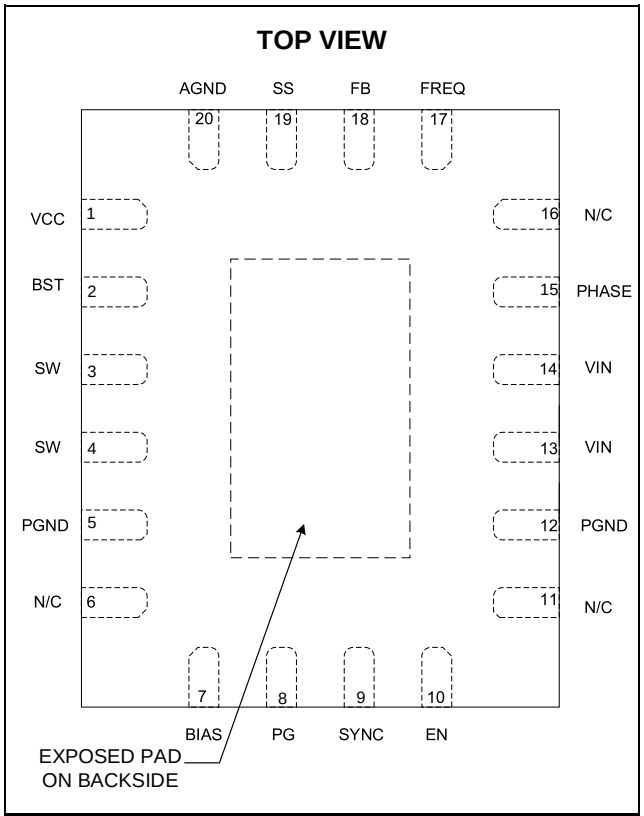
** Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
MP4469
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP4469: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-20 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Internal bias supply.** This pin supplies power to the internal control circuit and gate drivers. Place a decoupling capacitor greater than 1µF to ground and close to VCC.
2	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
3, 4	SW	**Switch node.** SW is the output of the internal power switch.
5, 12	PGND	**Power ground.** PGND is the reference ground of the power device and requires careful consideration during PCB layout. For the best results, connect PGND with copper pours and vias.
6, 11, 16	NC	**No connection.**
7	BIAS	**External power supply for the internal regulator.** Connect BIAS to an external power supply between 5V and 18V to reduce power dissipation and increase efficiency. When this pin is not being used, float it or connect it to ground.
8	PG	**Power good Indicator.** The output of this pin is an open drain and goes high if the output voltage is within ±10% of the nominal voltage.
9	SYNC	**Synchronize.** Apply a 350kHz to 2.5MHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz greater than R_{FREQ}'s set frequency. Connect to GND if not used.
10	EN	**Enable.** Pull this pin below the specified threshold to shut down the chip. Pull EN above the specified threshold to enable the chip.
13, 14	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. A decoupling capacitor connected to ground must be placed close to VIN to minimize switching spikes.
15	PHASE	**Selectable in-phase or 180° out-of-phase with SYNC input.** Drive PHASE high to be in phase; drive it low to be 180° out of phase. If SYNC is not being used, do not float the pin to avoid any uncertain status. It is recommended to connect PHASE to GND.
17	FREQ	**Switching frequency programming pin.** To set the switching frequency, connect a resistor from FREQ to ground.
18	FB	**Feedback input.** Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. The feedback voltage threshold is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
19	SS	**Soft-start input.** Place an external capacitor from SS to AGND to set the soft-start time. The MPQ4469 sources 10µA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	AGND	**Analog ground.** Reference ground of the logic circuit.
		Exposed pad. Connect to GND plane for improved thermal performance.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +40V
Switch voltage (V_{SW}) .....-0.3V to V_{IN} + 0.3V
BST voltage (V_{BST}) .....V_{SW} + 6.5V
EN voltage (V_{EN}) ..... -0.3V to +40V
BIAS voltage (V_{BIAS}) ..... -0.3V to +20V
All other pins..... -0.3V to +6V
Continuous power dissipation……(T_A = 25°C) (2)
QFN-20 (4mmx5mm).....3.12W
Operating junction temperature.....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

Electrostatic Discharge (ESD) Level

HBM (human body model).....±2000V
CDM (charged device model) .....±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 3.3V to 36V
Operating junction temp (T_J) .....
..... -40°C to +125°C (3)

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-20 (4mmx5mm)			
JESD51-7 (4)	40	9	°C/W
EVQ4469-V-00A (5)	35	3.4	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operation devices at junction temperature greater than 125°C is possible; contact MPS for details.
4) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
5) Measured on EVQ4469-V-00A, 4-layer PCB, 6.35cmx6.35cm.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, no switching, T_J = 25°C		10	18	µA
		V_{FB} = 0.85V, no load, no switching		10	25	
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		1	5	µA
VIN under-voltage lockout rising threshold	$INUV_{RISING}$		2.3	2.8	3.2	V
VIN under-voltage lockout hysteresis threshold	$INUV_{HYS}$			150		mV
Feedback reference voltage	V_{REF}		784	800	816	mV
		T_J = 25°C	792	800	808	mV
Switching frequency	f_{SW}	R_{FREQ} = 180kΩ, or from sync clock	400	475	550	kHz
		R_{FREQ} = 82kΩ, or from sync clock	850	1000	1150	kHz
		R_{FREQ} = 27kΩ, or from sync clock	2250	2500	2750	kHz
Minimum on time (6)	t_{ON_MIN}			100		ns
Sync input low voltage	V_{SYNC_LOW}				0.4	V
Sync input high voltage	V_{SYNC_HIGH}		1.8			V
Current limit	I_{LIMIT_HS}	Duty cycle = 40%	6.2	7.7	9.2	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		110	175	mΩ
Soft-start current	I_{SS}	V_{SS} = 0.8V	5	10	15	µA
EN rising threshold	V_{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V_{EN_HYS}			160		mV
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	79	84	89	%
		V_{FB} rising	113.5	118.5	123.5	%
PG deglitch timer	$t_{PG\_DEGLITCH}$	PG from low to high		30		µs
		PG from high to low		50		µs
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3	%
Thermal shutdown (6)	T_{SD}			170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			20		°C

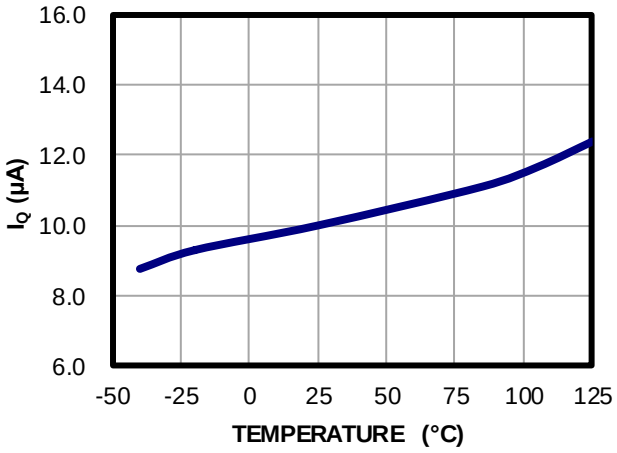
Note:

6) Not tested in production. Guaranteed by design and characterization.

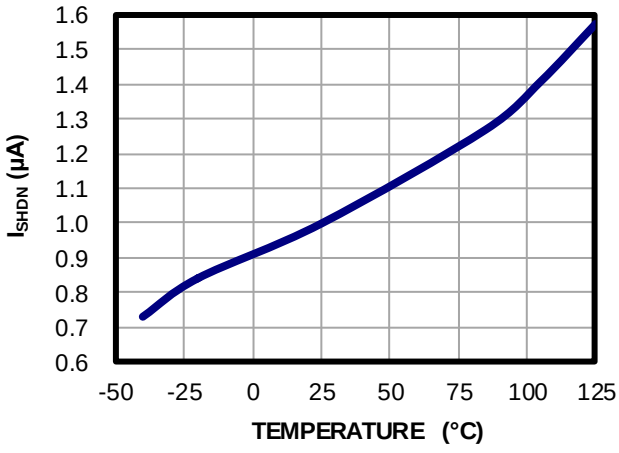
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

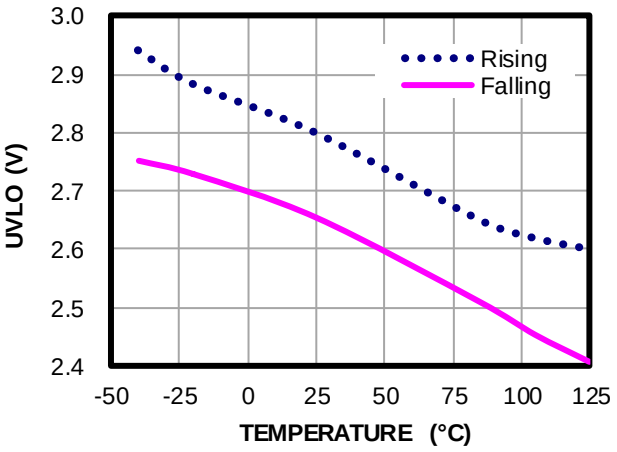
Quiescent Current vs. Temperature



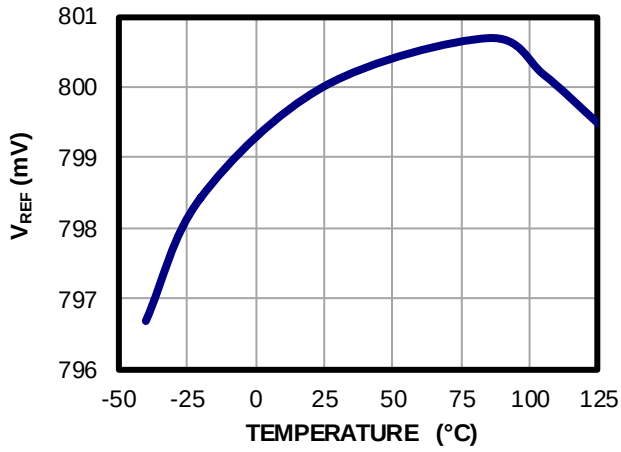
Shutdown Current vs. Temperature



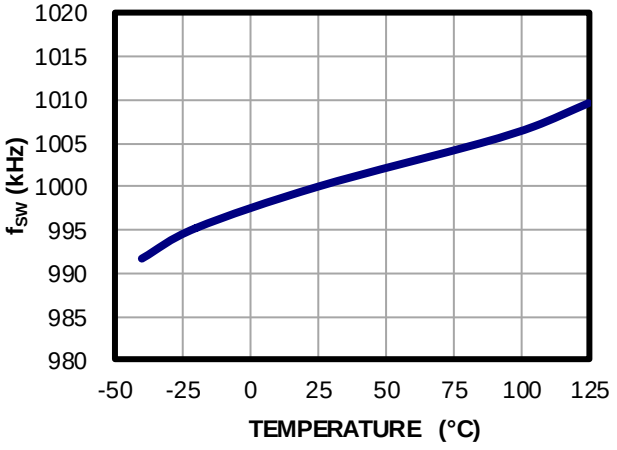
V_{IN} UVLO Threshold vs. Temperature



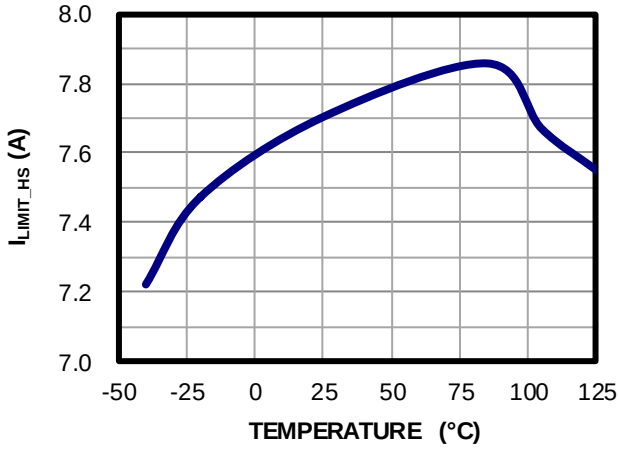
Feedback Reference vs. Temperature



Switching Frequency vs. Temperature



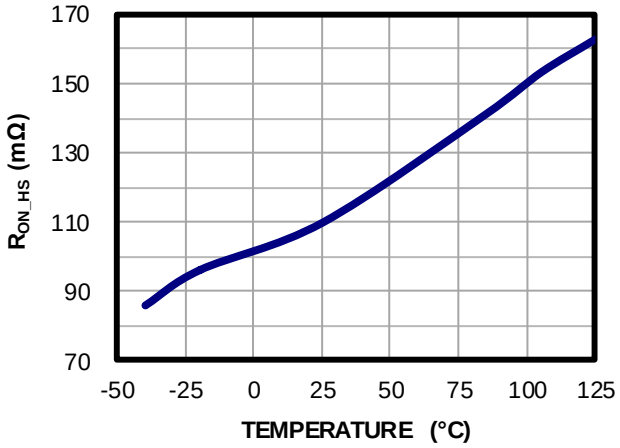
Current Limit vs. Temperature



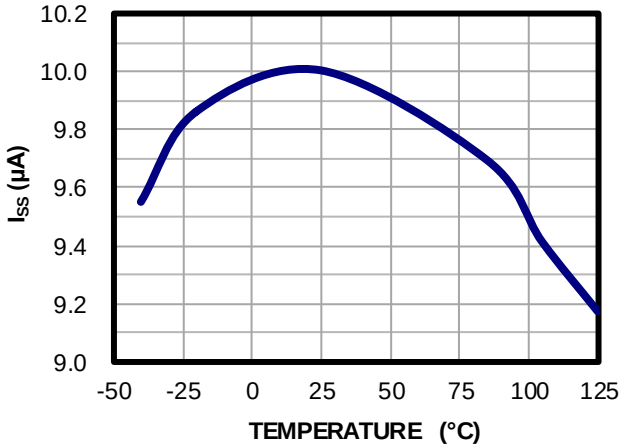
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

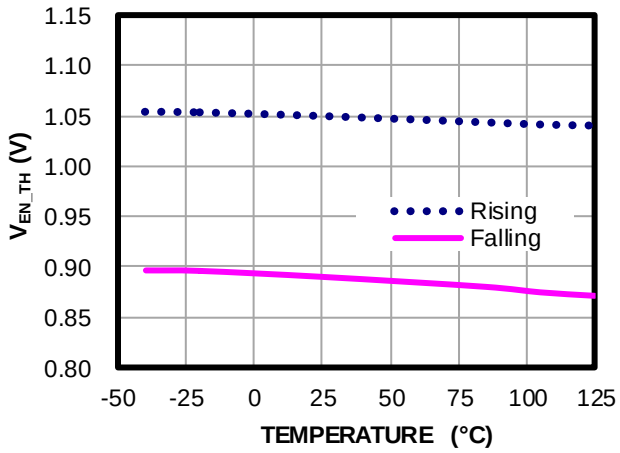
HS-FET On Resistance vs. Temperature



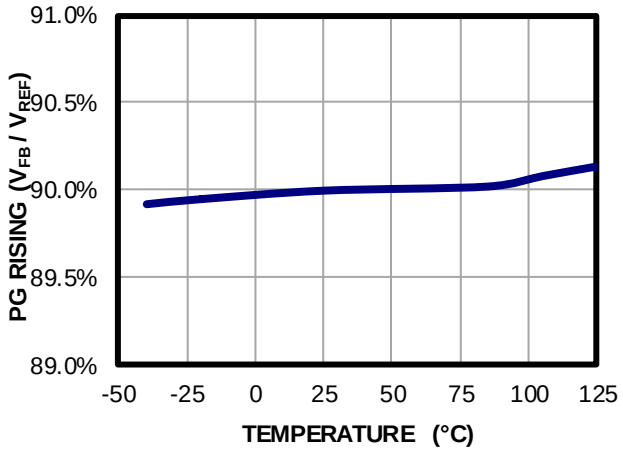
Soft-Start Current vs. Temperature



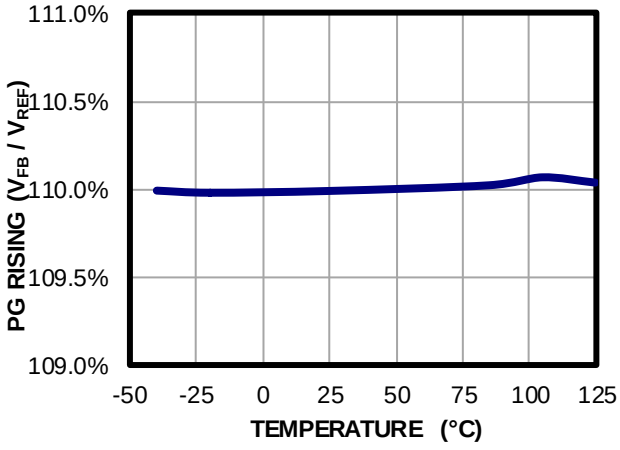
EN Threshold vs. Temperature



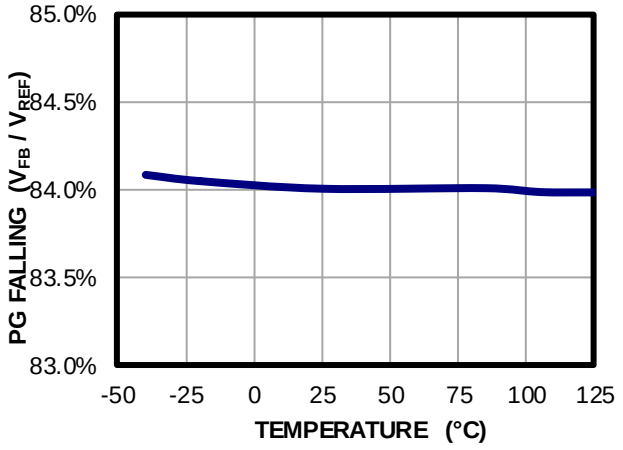
PG Rising Threshold (V_{FB} Rising) vs. Temperature



PG Rising Threshold (V_{FB} Falling) vs. Temperature



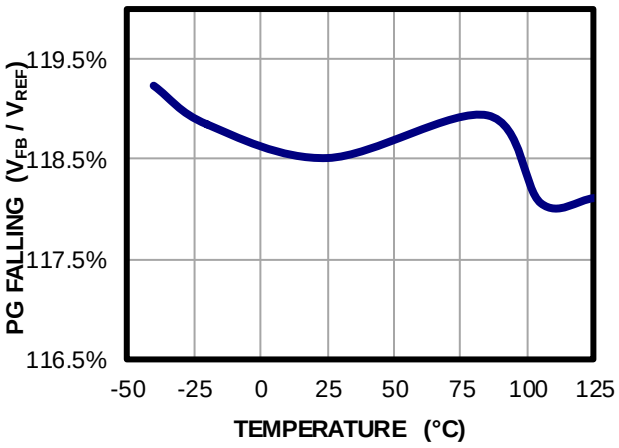
PG Falling Threshold (V_{FB} Falling) vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

PG Falling Threshold (V_{FB} Rising) vs. Temperature

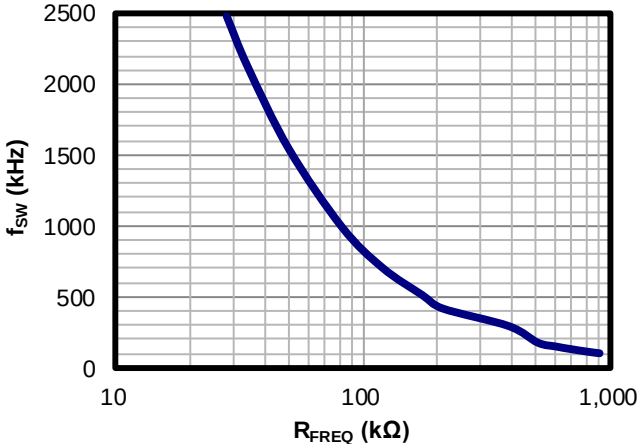


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

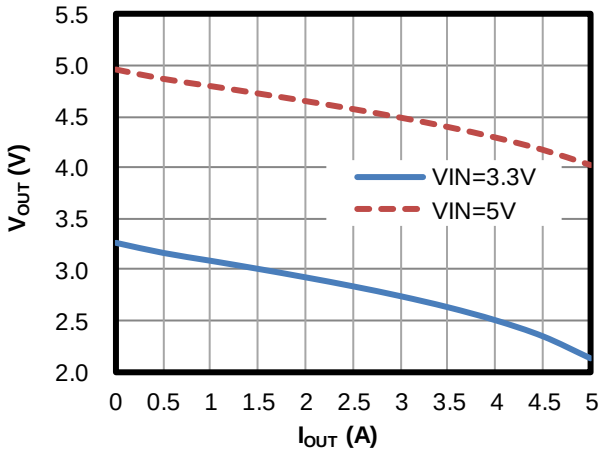
Current Limit vs. Duty Cycle

f_{SW} vs. R_{FREQ}

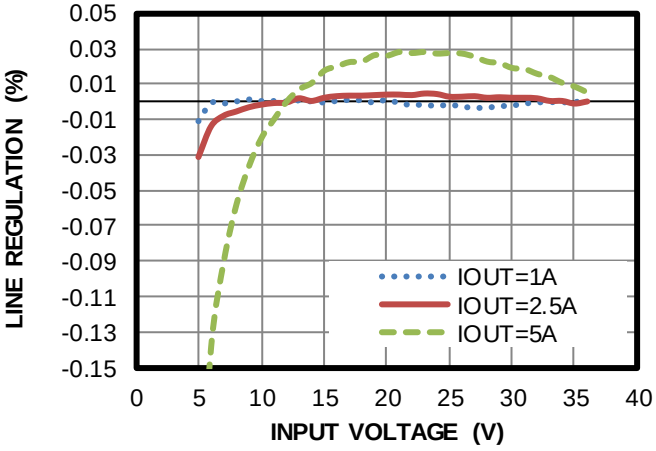


Output Voltage vs. Load Current Dropout Performance

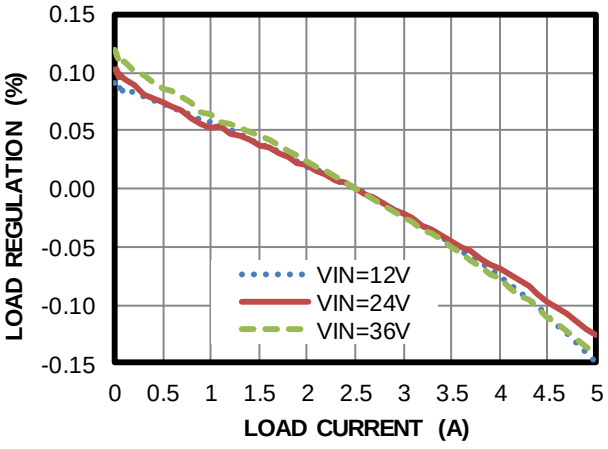
(Set nominal V_{OUT} > V_{IN})



Line Regulation



Load Regulation

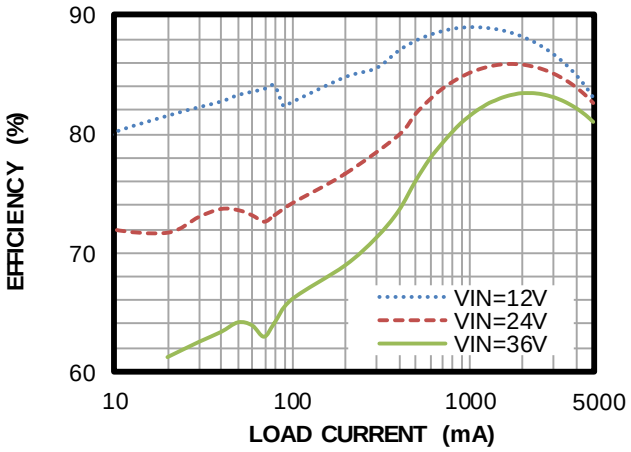


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

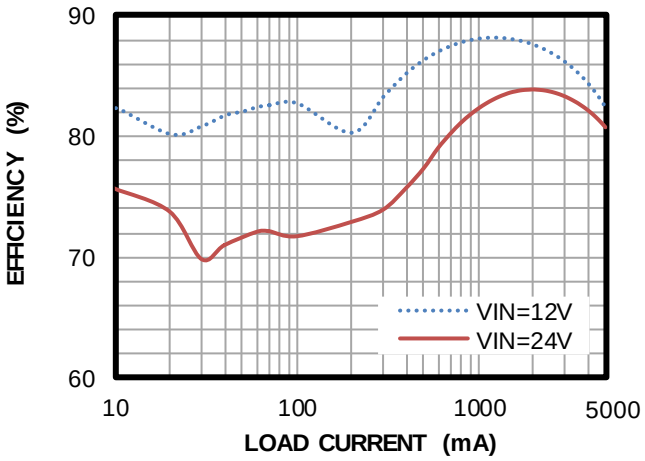
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 500kHz



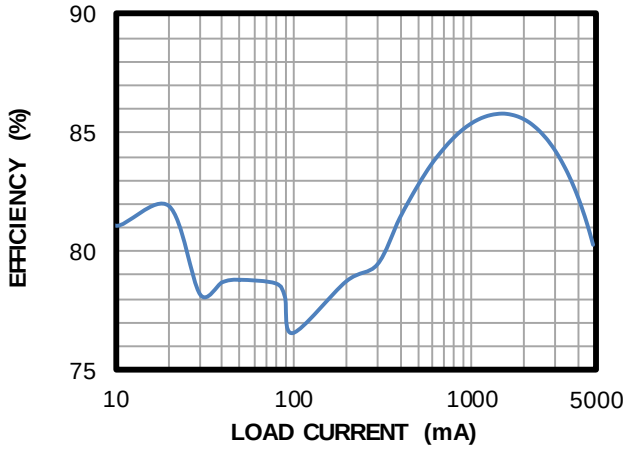
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 1MHz



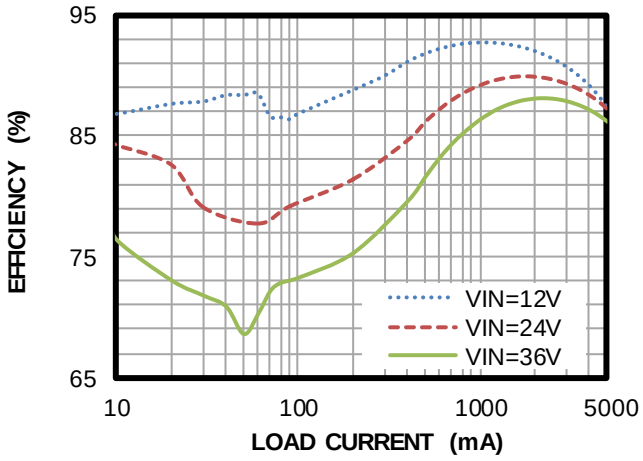
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 2.2MHz



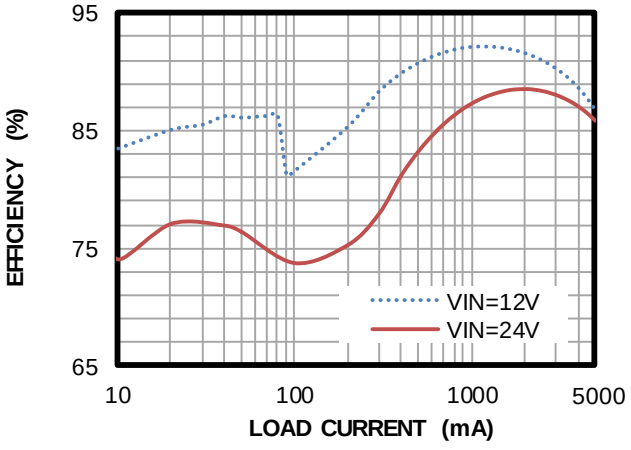
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 500kHz



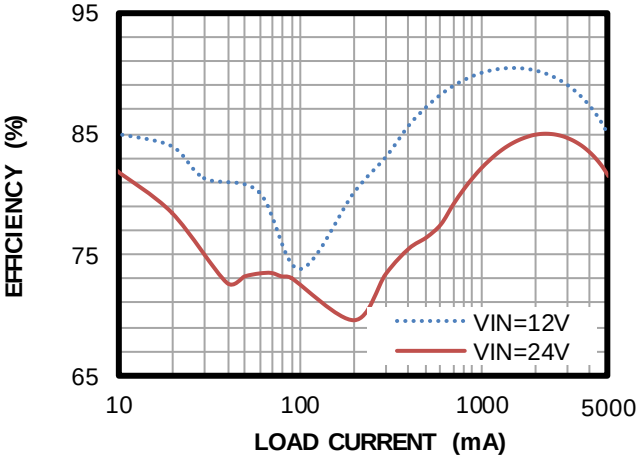
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 1MHz



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 2.2MHz

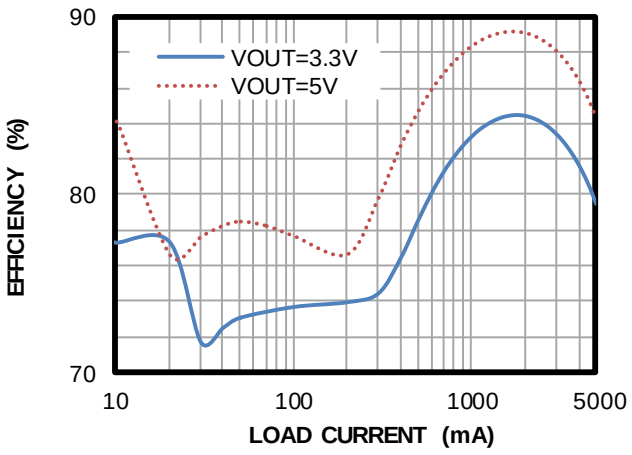


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

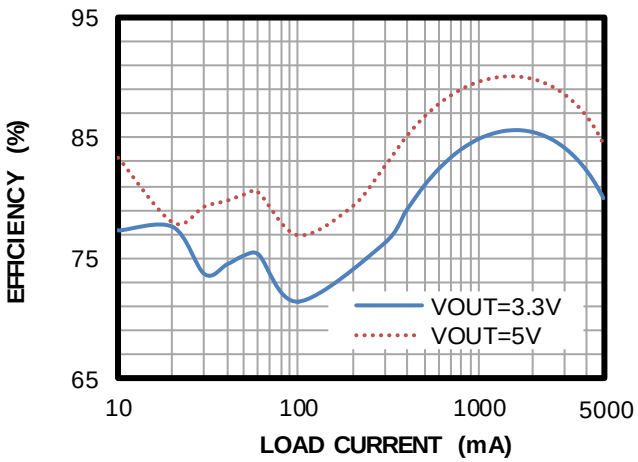
Efficiency vs. Load Current

V_{IN} = 14V, f_{SW} = 2.2MHz, L = 2.2µH



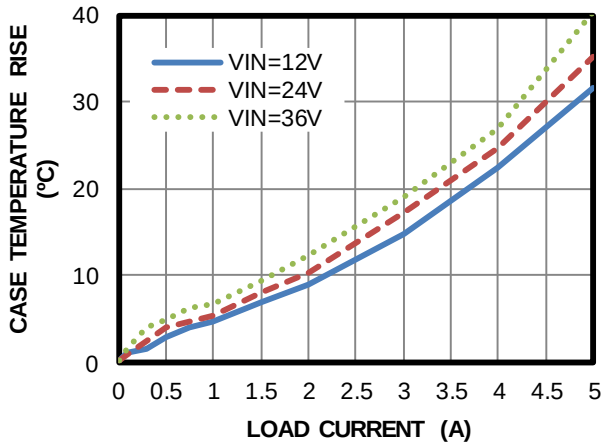
Efficiency vs. Load Current

V_{IN} = 12V, f_{SW} = 2.2MHz, L = 2.2µH



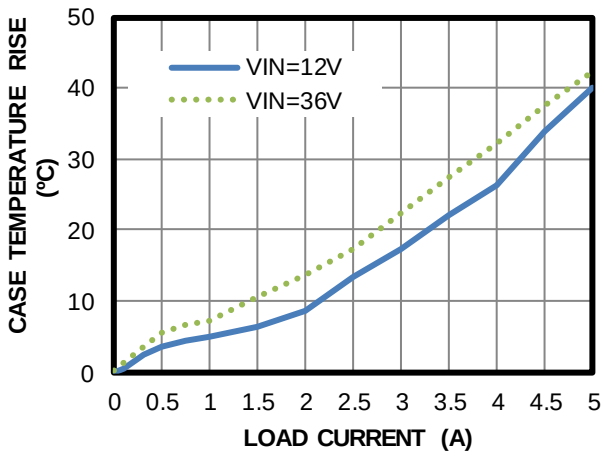
Case Temperature Rise vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 500kHz



Case Temperature Rise vs. Load Current

V_{OUT} = 5V, f_{SW} = 500kHz

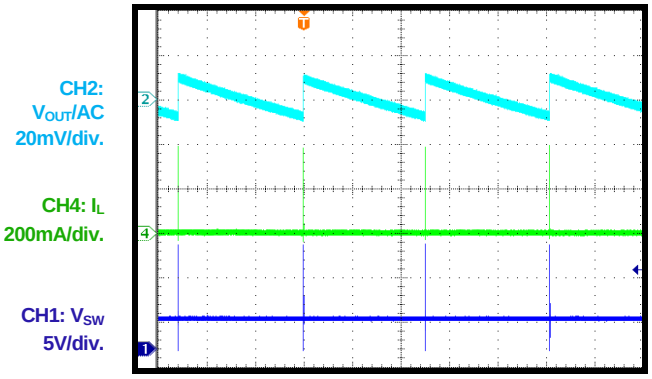


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

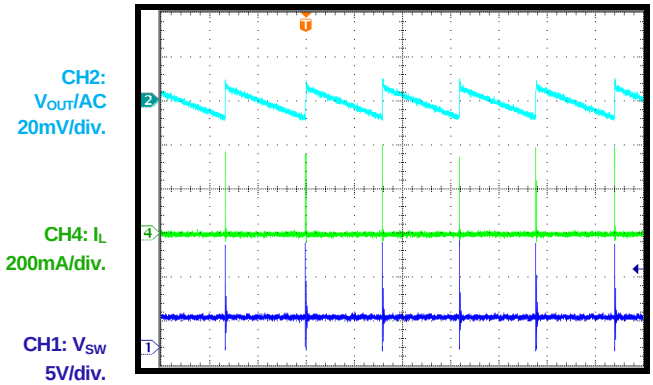
Steady State

I_{OUT} = 0A



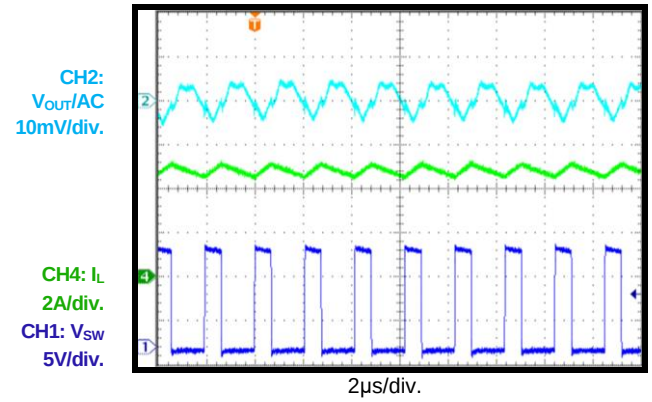
Steady State

I_{OUT} = 1mA



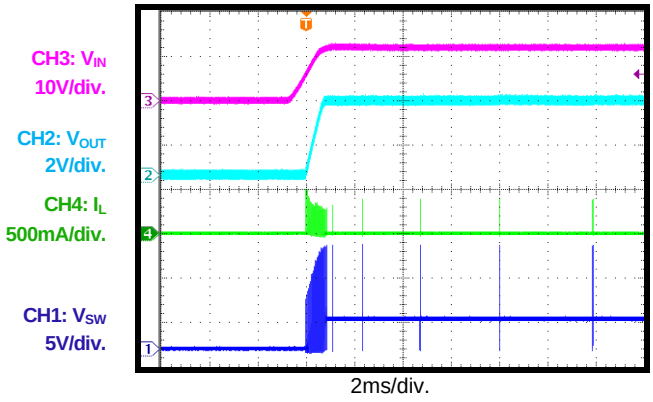
Steady State

I_{OUT} = 5A



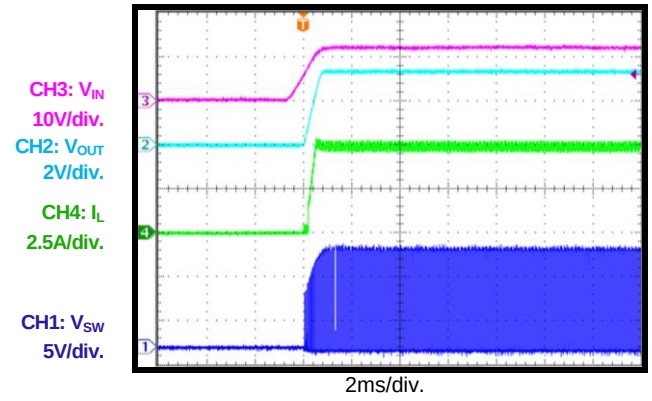
Start-Up through VIN

I_{OUT} = 0A



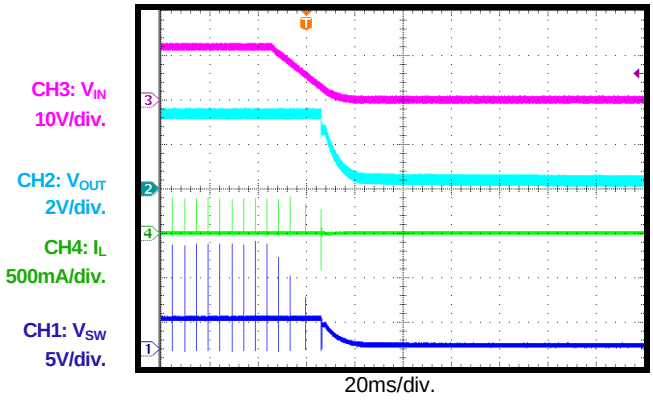
Start-Up through VIN

I_{OUT} = 5A



Shutdown through VIN

I_{OUT} = 0A

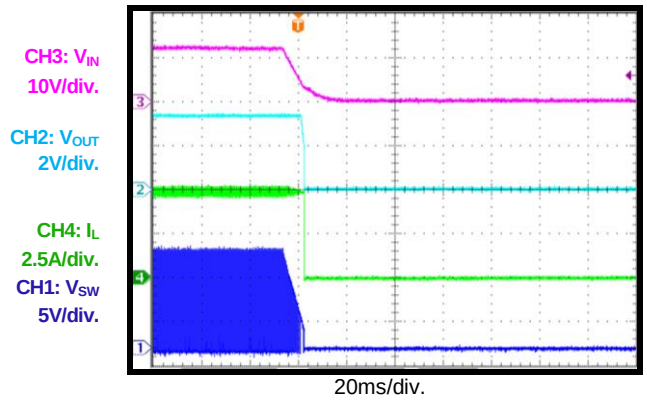


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

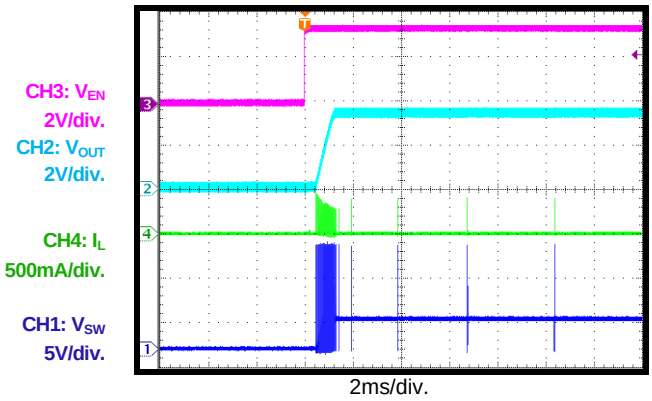
Shutdown through VIN

I_{OUT} = 5A



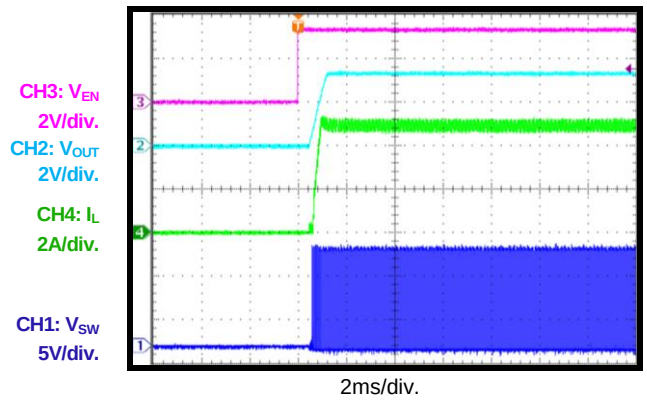
Start-Up through EN

I_{OUT} = 0A



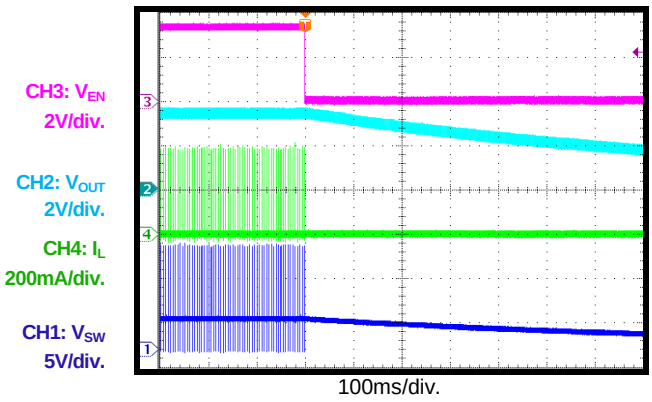
Start-Up through EN

I_{OUT} = 5A



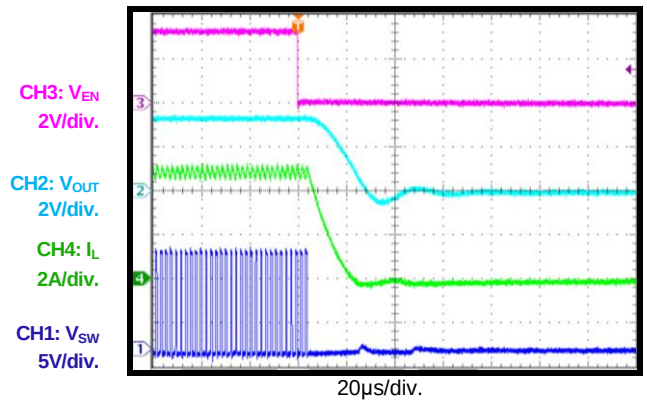
Shutdown through EN

I_{OUT} = 0A



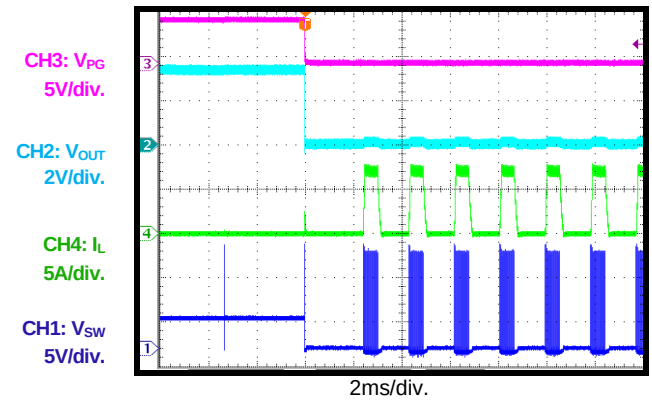
Shutdown through EN

I_{OUT} = 5A



SCP Entry

I_{OUT} = 0A to short circuit

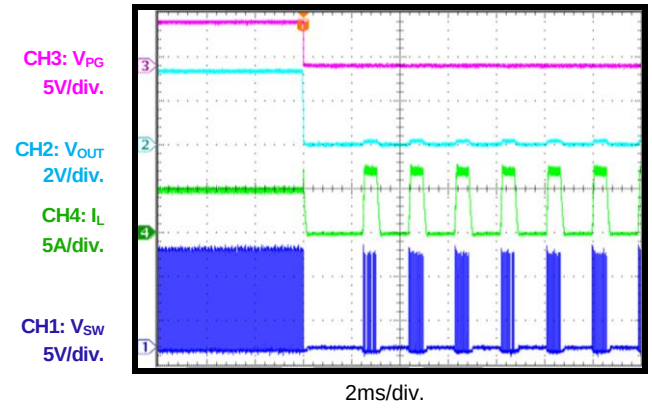


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

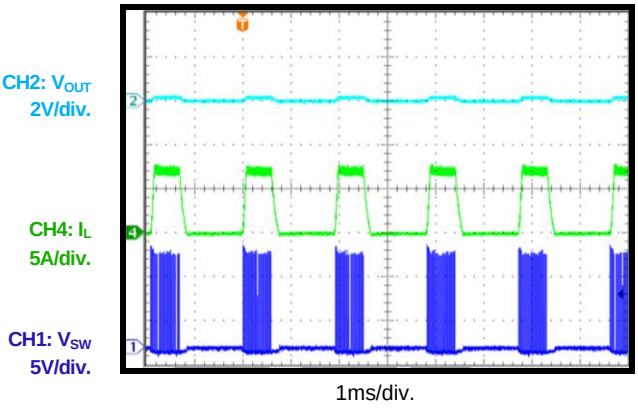
SCP Entry

I_{OUT} = 5A to short circuit



2ms/div.

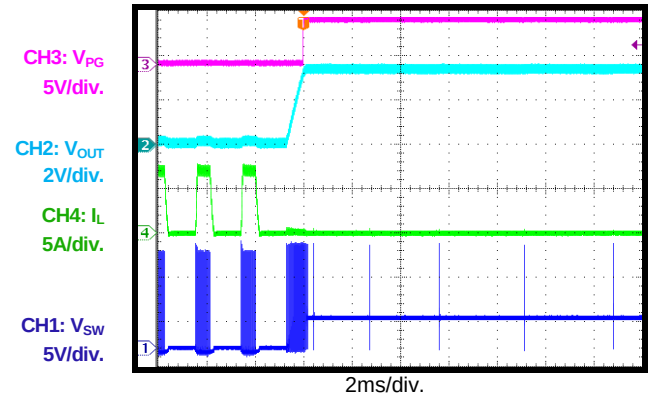
SCP Steady State



1ms/div.

SCP Recovery

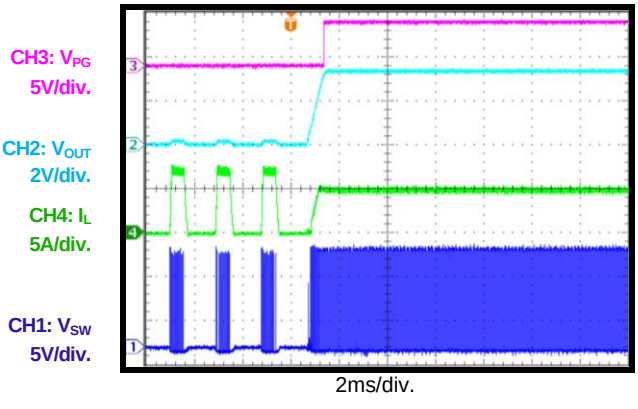
Short circuit to I_{OUT} = 0A



2ms/div.

SCP Recovery

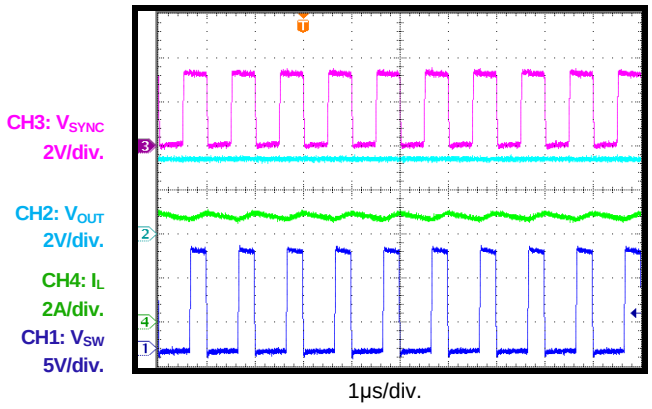
Short circuit to I_{OUT} = 5A



2ms/div.

SYNC Operation (In-Phase)

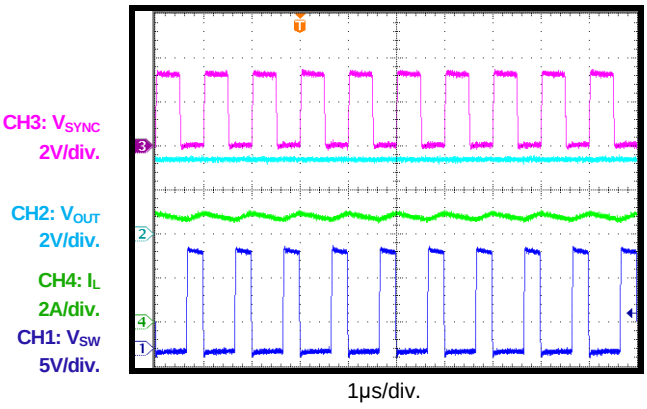
Drive PHASE high, I_{OUT} = 5A



1µs/div.

SYNC Operation (180° Out-Of-Phase)

Drive PHASE low, I_{OUT} = 5A



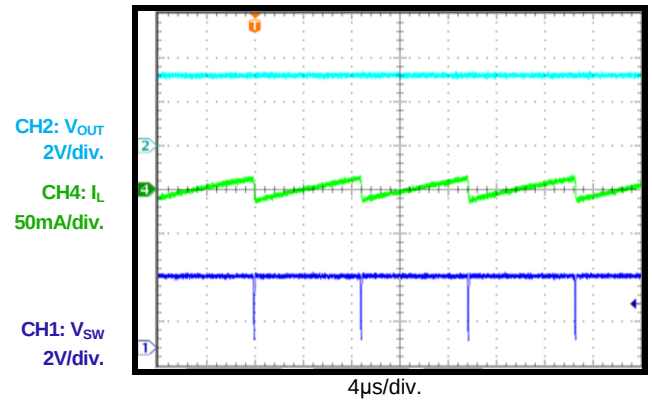
1µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

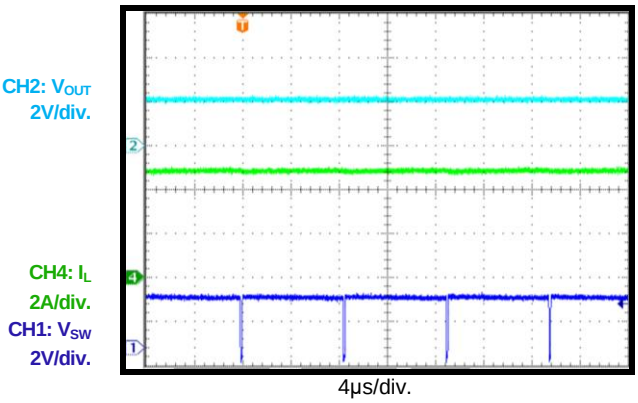
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



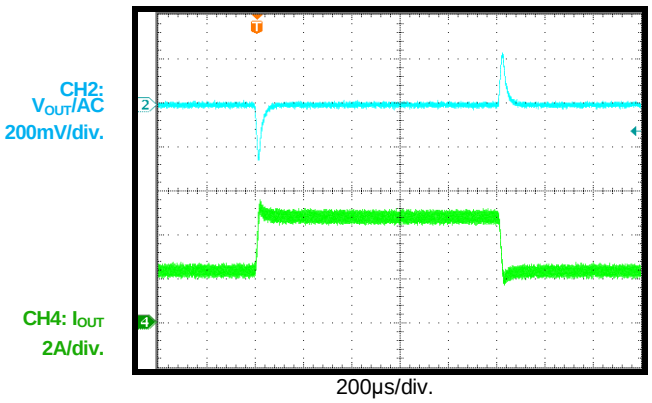
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 5A



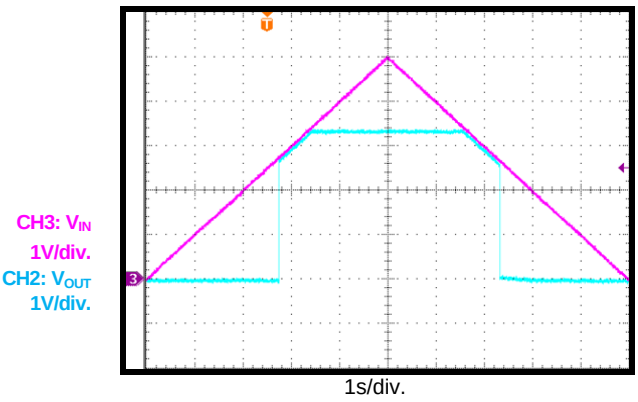
Load Transient

I_{OUT} = 2.5A to 5A, 1.6A/µs



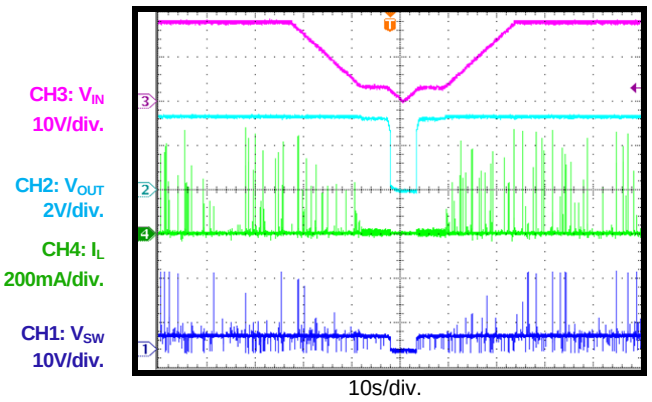
VIN Ramp Up and Down

I_{OUT} = 0.1A



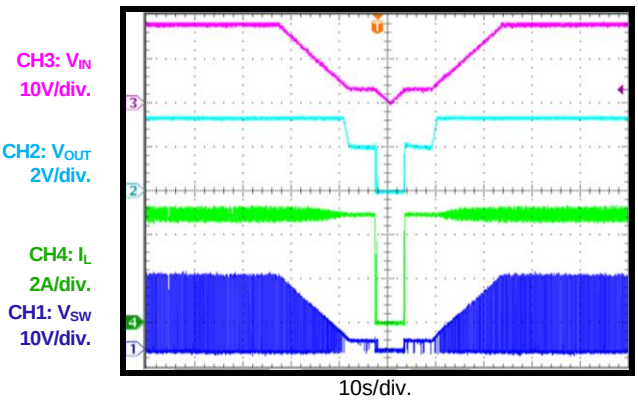
VIN Ramp Down and Up

I_{OUT} = 1mA



VIN Ramp Down and Up

I_{OUT} = 5A

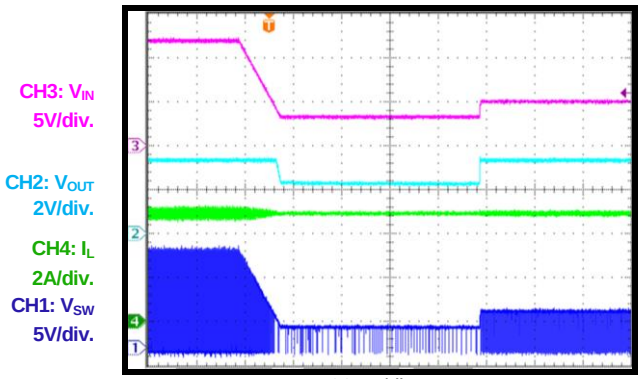


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

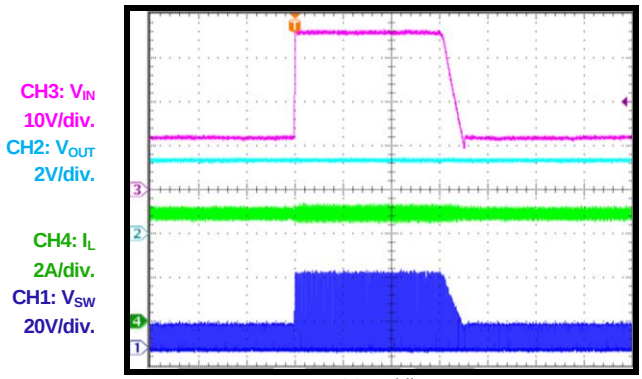
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 5A



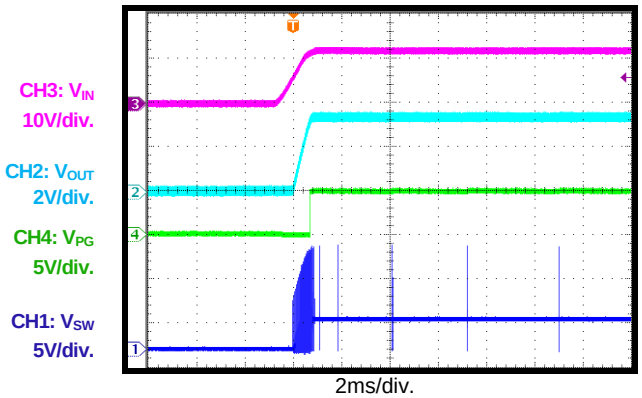
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 5A



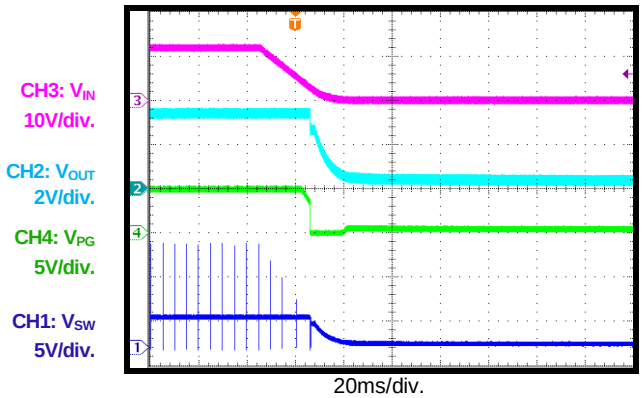
PG in Start-Up through VIN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor



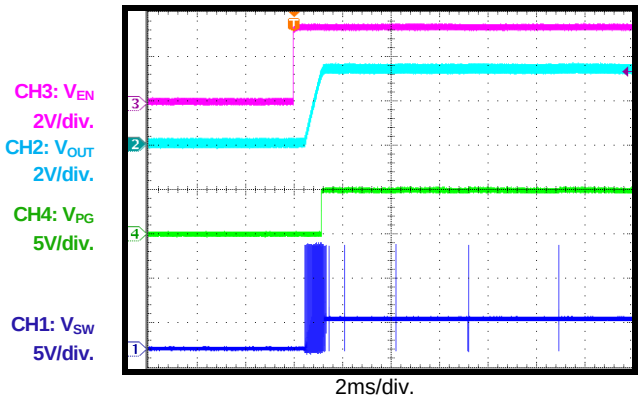
PG in Shutdown through VIN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor



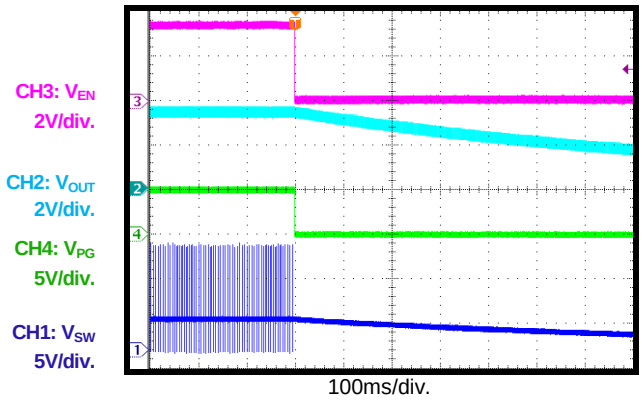
PG in Start-Up through EN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor



PG in Shutdown through EN

I_{OUT} = 0A, PG is pulled to 3.3V through a 100kΩ resistor

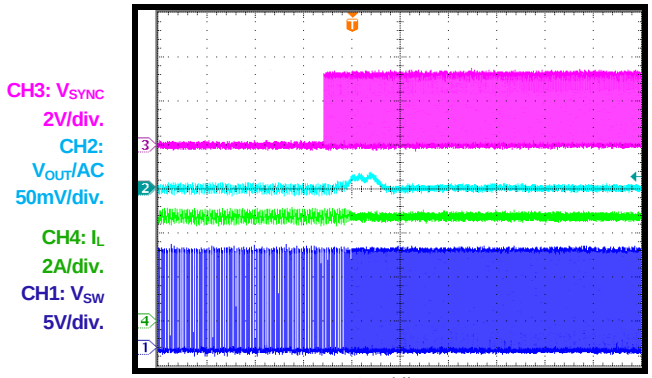


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

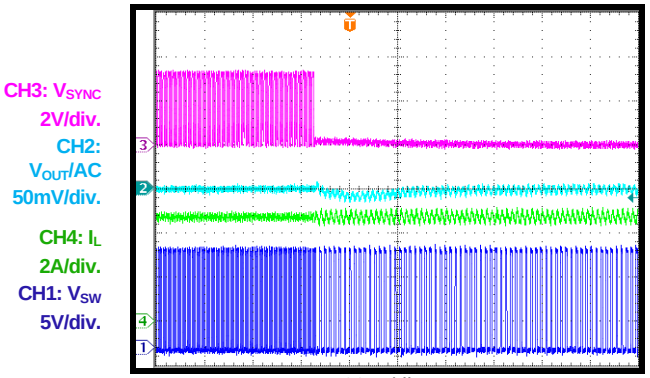
SYNC In Transient

I_{OUT} = 5A, SYNC = 1MHz



SYNC Out Transient

I_{OUT} = 5A, SYNC = 1MHz



FUNCTIONAL BLOCK DIAGRAM

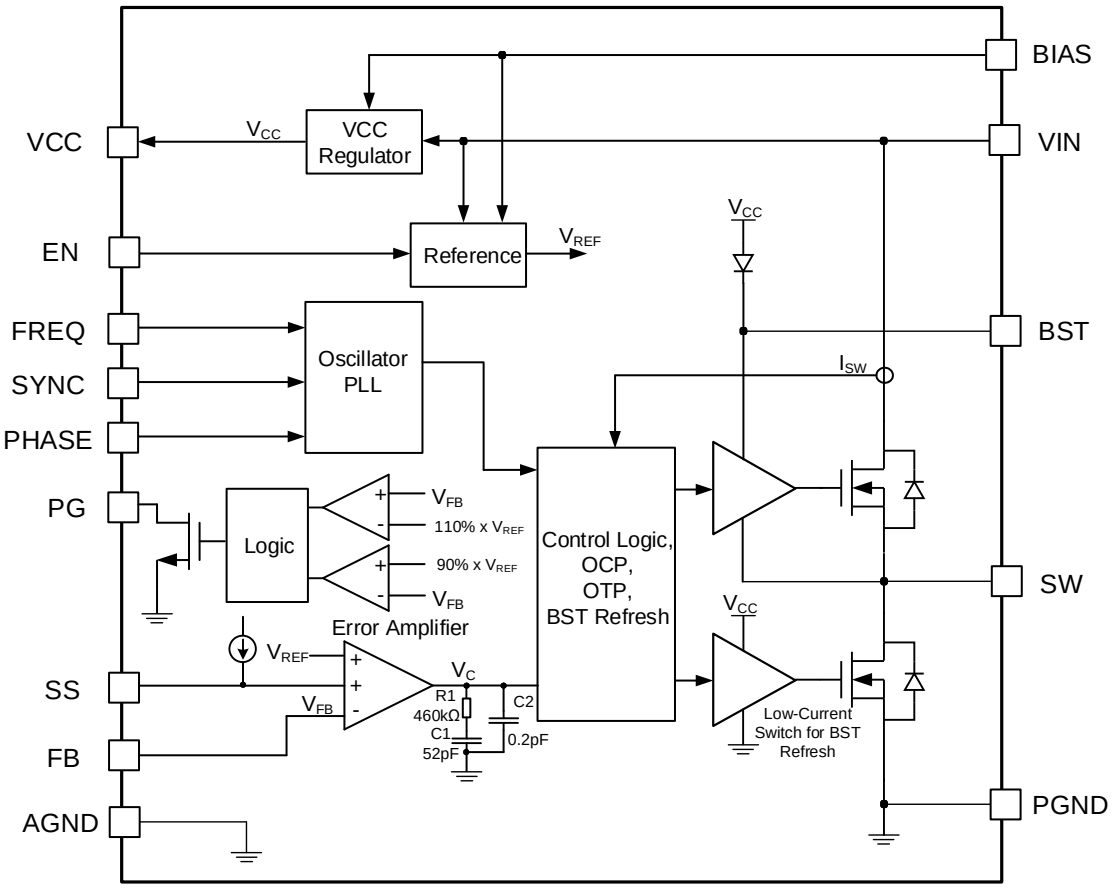


Figure 1: Functional Block Diagram

Timing Sequence

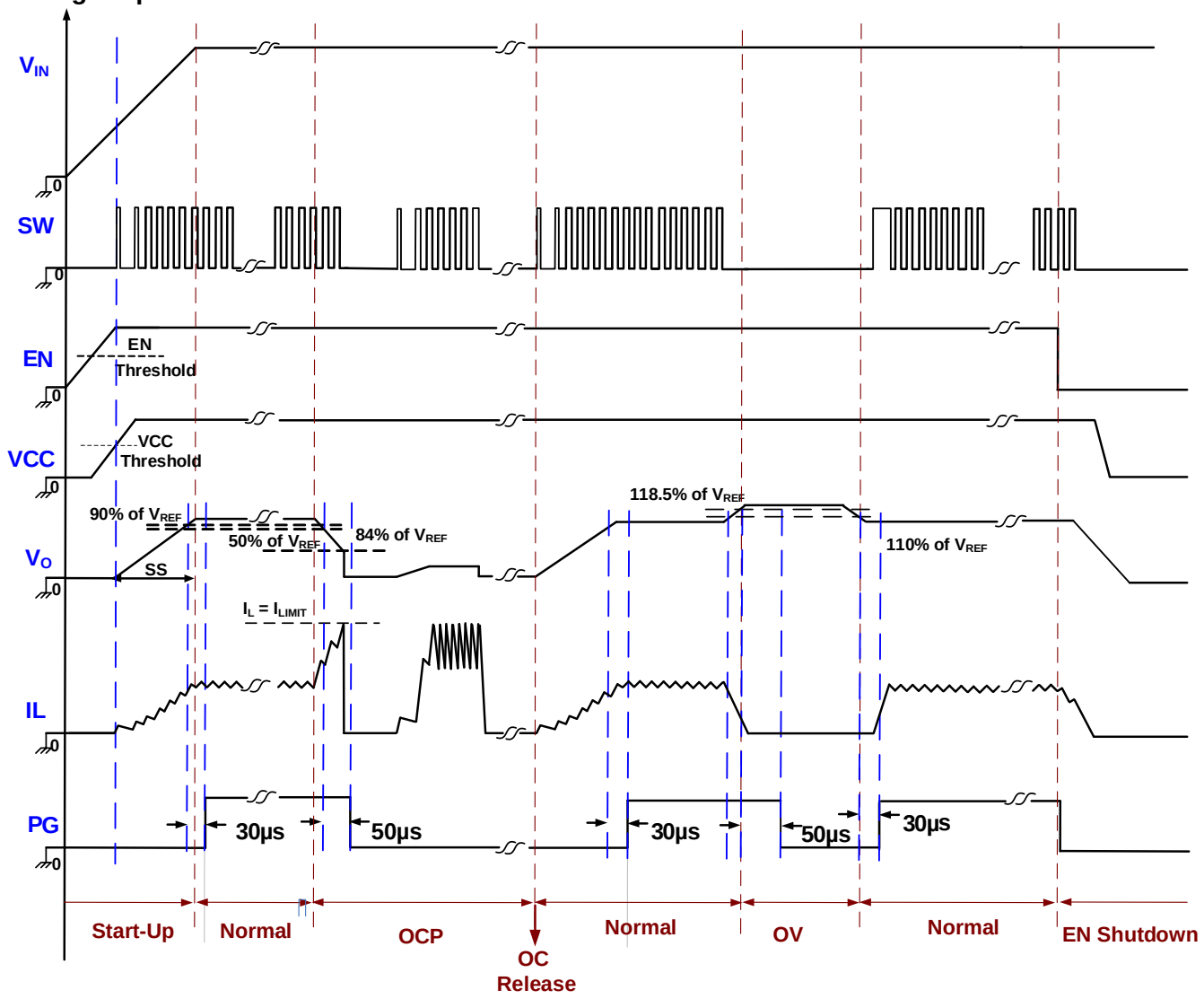


Figure 2: Timing Sequence

OPERATION

The MPQ4469 is a high frequency, asynchronous, rectified, step-down, switch-mode converter with an integrated, internal, high-side power MOSFET (see Figure 1). It offers a very compact solution that achieves 5A of continuous output current with excellent load and line regulation over a wide 3.3V to 36V input supply range.

The device features a configurable 350kHz to 2.5MHz switching frequency, external soft start, a power good indicator, and precision current limit. Its low operational quiescent current makes it ideal for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output current, the MPQ4469 operates in a fixed frequency, peak current control mode to regulate the output voltage. An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}), which is the output of the internal error amplifier. If the current in the HS-FET does not reach V_{COMP} within one PWM period, the HS-FET remains on, and saves a turn-off operation.

When the HS-FET is off, the inductor current flows through the freewheel diode, and the HS-FET remains off until the next clock cycle starts.

AAM Mode

The MPQ4469 enters discontinuous conduction mode (DCM) operation first, as long as the inductor current approaches zero at light-load. If the load further decreases, or there is no load to bring V_{COMP} below the internally set AAM value (V_{AAM}), the MPQ4469 enters sleep mode. In this mode, the device consumes a low quiescent current to further improve light-load efficiency.

In sleep mode, the internal clock is blocked first, and the MPQ4469 skips some pulses. As the feedback voltage (V_{FB}) drops below the internal 0.8V reference voltage (V_{REF}), V_{COMP} ramps up until it exceeds V_{AAM}. Then the internal clock is reset, and the crossover time is used as a benchmark for the next clock. This control scheme achieves high efficiency by scaling down the frequency to reduce the switching and gate-driver losses during light-load or no-load conditions (see Figure 3).

When the output current increases from a light-load condition, both V_{COMP} and the switching frequency increase. If the DC value of V_{COMP} exceeds V_{AAM}, the operation mode resumes DCM or CCM, which has a constant switching frequency.

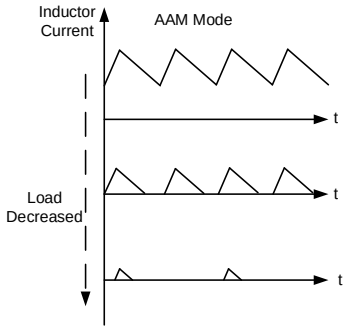


Figure 3: AAM Mode

Error Amplifier (EA)

The error amplifier compares V_{FB} with V_{REF} and outputs a current proportional to the difference between the two values. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal Regulator and BIAS

Most of the internal circuitry is powered by the 5V internal regulator. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 5V, the output of the regulator is in full regulation. When V_{IN} falls below 5V, the output decreases following V_{IN}. Place a decoupling ceramic capacitor as close as possible to the VCC pin.

For improved thermal performance, connect BIAS to an external power supply between 5V and 18V. The BIAS supply overrides V_{IN} to power the internal regulator. Using the BIAS supply allows VCC to be derived from a high-efficiency

external source, such as V_{OUT}. Float BIAS or connect it to ground if it is not being used.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 2.8V, with a 150mV hysteresis.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. When EN is pulled below its threshold voltage, the chip enters the lowest shutdown current mode. If EN is pulled above its threshold voltage, the part turns on. Do not float EN.

Power Good Indicator (PG)

The MPQ4469 has a power good (PG) indicator. The PG pin is the open drain of a MOSFET. To use PG indicator, It must be connected to VCC or another voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled low before SS is ready. When the regulator output is within ±10% of its nominal output, the PG output is pulled high after a delay of 30μs. When the output voltage moves outside this range with a hysteresis, the PG output is pulled to low with a 50μs delay to indicate a failure output status.

Programmable Frequency

The oscillating frequency of the MPQ4469 can be programmed either by an external frequency resistor (R_{FREQ}) or by a logic-level synchronous clock. The frequency resistor should be located between FREQ and ground, as close to the device as possible.

R_{FREQ} can be estimated with Equation (1):

$$R_{FREQ}(k\Omega) = \frac{170000}{f_{SW}^{1.11}(kHz)} \quad (1)$$

The calculated resistance may need fine-tuning by bench test.

FREQ must not be floated, even if an external SYNC clock is added.

SYNC and PHASE

The internal oscillator frequency can be synchronized to an external clock, ranging from 350kHz up to 2.5MHz, through the SYNC pin. The external clock should be at least 250kHz greater than the R_{FREQ} set frequency. Ensure the high amplitude of the SYNC clock is above 1.8V, and the low amplitude is below 0.4V. There is no pulse width requirement, but there is always parasitic capacitance of the pad. If the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

The PHASE pin is used when two or more MPQ4469s are in parallel with the same sync clock. Pulling PHASE high forces the device to operate in phase with the SYNC clock. Pulling it low forces the device to be 180° out of phase with the SYNC clock. By setting a different PHASE voltage, two devices can operate in 180° out-of-phase mode to reduce the total input current ripple, so a smaller input bypass capacitor can be used (see Figure 4). The PHASE rising threshold is about 2.5V, with a 400mV hysteresis.

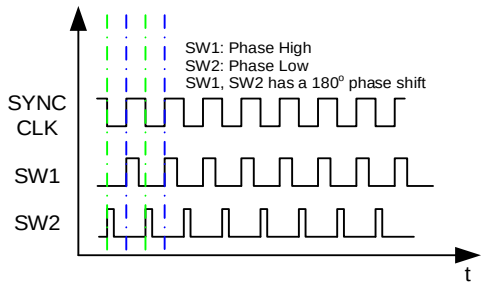


Figure 4: In-Phase and 180° Out-of-Phase

Soft Start (SS)

Soft start (SS) is implemented to prevent the device's output voltage from overshooting during start-up. When the chip starts up, an internal current source begins charging the external soft-start capacitor. The internal SS voltage (V_{SSI}) rises with the soft-start voltage (V_{SS}), but V_{SSI} is a different value from V_{SS} due to a 0.5V offset and some delay.

When V_{SS} is below 0.5V, V_{SSI} is 0V. V_{SSI} rises from 0V to 0.8V as V_{SS} rises from 0.5V to 1.6V. During this time, the error amplifier uses V_{SSI} as the reference, and the output voltage ramps up from 0V to the regulated value, following V_{SSI} rising. When V_{SS} reaches 1.6V, V_{SSI} is 0.8V and overrides the internal V_{REF}, so the error amplifier uses the internal V_{REF} as the reference.

To minimize the delay for SS to reach 0.5V, an internal pull-up circuit with an average 100μA current pulls SS up to 0.4V. Then a 10μA constant current charges SS up to about 4V.

The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 1.1V}{I_{SS}(\mu A)} \quad (2)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 10μA SS charge current.

The delay time for SS to reach 0.5V can be estimated with Equation (3):

$$t_{SS\_delay}(ms) = \frac{C_{SS}(nF) \times 0.4V}{100\,\mu A} + \frac{C_{SS}(nF) \times 0.1V}{10\,\mu A}$$

SS can be used for tracking and sequencing.

Pre-Bias Start-Up

At start-up, if V_{FB} exceeds V_{SSI} - 150mV, which means the output has a pre-bias voltage, the HS-FET does not turn on until V_{SSI} - 150mV exceeds V_{FB}.

Over-Current Protection (OCP) and Hiccup Mode

The MPQ4469 has cycle-by-cycle peak current limit protection and hiccup mode.

The power MOSFET current is accurately sensed via a current-sense MOSFET. It is then fed to the high-speed current comparator for current-mode control. If the HS-FET is on and the sensed current exceeds the peak-current limit value set by the COMP high clamp voltage, the HS-FET turns off immediately. Then the inductor current flows through the external freewheel diode and decreases. The HS-FET remains off until the next clock cycle starts. During OCP, the clock frequency is related to the FB voltage, and decreases as the FB voltage decreases. Both the peak current limit and frequency foldback prevent the inductor current from running away during an overload or short-circuit condition.

When the output is shorted to ground, and the output voltage drops below 55% of its nominal output, the peak current limit is kicked. The MPQ4469 considers this an output dead short, and triggers hiccup mode to periodically restart the part.

In hiccup mode, the MPQ4469 disables its output power stage and discharges the soft-start capacitor slowly. The device restarts with a full soft start when the soft-start capacitor is fully discharged. If the short-circuit condition still remains after soft start ends, the device repeats this operation until the fault is removed and the output returns to the regulation level. This protection mode greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator.

Floating Driver and Bootstrap Charging

A 0.1μF to 1μF external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection with a rising threshold of 2.5V and a hysteresis of 200mV.

VCC charges the bootstrap capacitor voltage to about 5V through a PMOS pass transistor when the SW node is low.

During high-duty cycle operation or sleep mode, the bootstrap charging time period is shorter, so the bootstrap capacitor may not charge sufficiently. If the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage is within its normal operation range.

BST Refresh

To improve dropout, the MPQ4469 is designed to operate at close to 100% of the duty cycle while the BST to SW voltage exceeds 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET turns off using a UVLO circuit, which forces an internal low-current switch to pull the SW node low and refresh the charge on the BST capacitor.

Since the supply current sourced from the BST capacitor is low, the HS-FET remains on for more switching cycles than are required to refresh the capacitor, making the effective duty cycle of the switching regulator high.

The effective duty cycle during the dropout of the regulator is mainly influenced by the voltage drops across the HS-FET, inductor resistance, and PCB resistance.

Thermal Shutdown (TSD)

Thermal shutdown is implemented to prevent thermal runaway. When the silicon die temperature exceeds its upper threshold, the power MOSFET shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first by generating a stable reference voltage and current. Then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

When the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank start-up glitches. When the soft-start block is enabled, it holds the SS output low to ensure the rest of the circuitries are ready, then slowly ramps up.

Three events can shut down the chip: V_{IN} low, EN low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set by connecting the external resistor divider to the FB pin (see Figure 5).

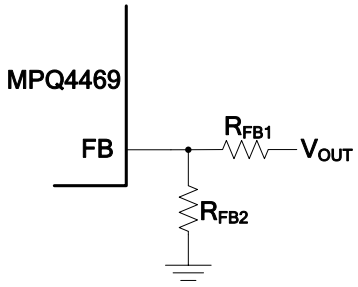


Figure 5: Feedback Network

Set R_{FB1} first. R_{FB2} can then be calculated with Equation (3):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	41.2 (1%)	13 (1%)
5	68.1 (1%)	13 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the small capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (5):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. Estimate the input voltage ripple caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4469 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% above the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with lower DC resistance. An inductor with a higher inductance results in a lower ripple current and a lower output ripple voltage. However, these inductors also have a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (10):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Set the inductor ripple current at approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (11):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Selecting the Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery times. Choose a diode with a maximum reverse voltage rating greater than the maximum input voltage, and a current rating greater than the maximum load current.

V_{IN} UVLO Setting

The MPQ4469 has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is 2.8V, and the falling threshold is about 2.65V. For applications that require a higher UVLO point, place an external resistor divider between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 6).

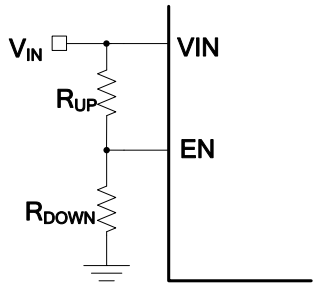


Figure 6: Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (12) and Equation (13), for UVLO rising and UVLO falling, respectively:

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (12)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (13)$$

Where V_{EN_RISING} = 1.05V, and $V_{EN\_FALLING}$ = 0.93V.

External BST Diode and Resistor

An external BST diode enhances the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can power the external bootstrap diode. VCC or V_{OUT} is recommended to be the power supply in this circuit (see Figure 7).

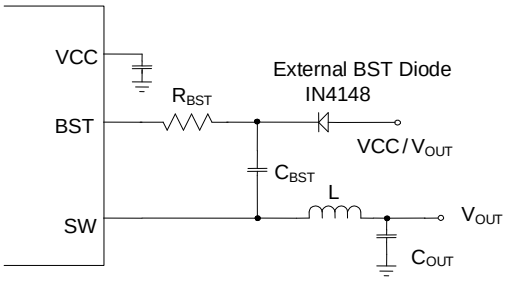


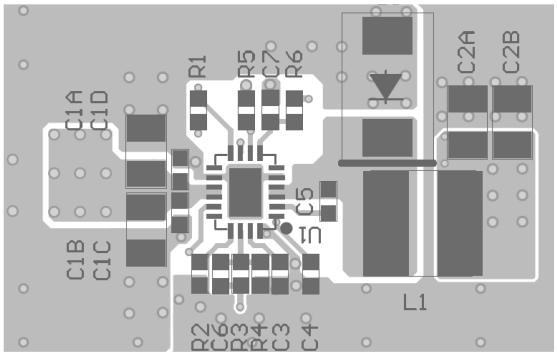
Figure 7: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value range is 0.1µF to 1µF. A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces the voltage stress at high VIN. A higher resistance benefits SW spike reduction but compromises efficiency. For an ideal trade off, it is recommended to make R_{BST} no greater than 20Ω.

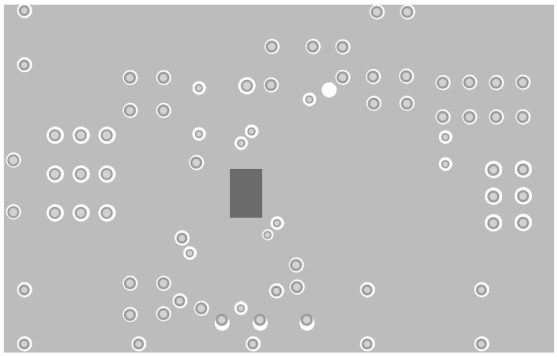
PCB Layout Guidelines (7)

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 8 and follow the guidelines below:

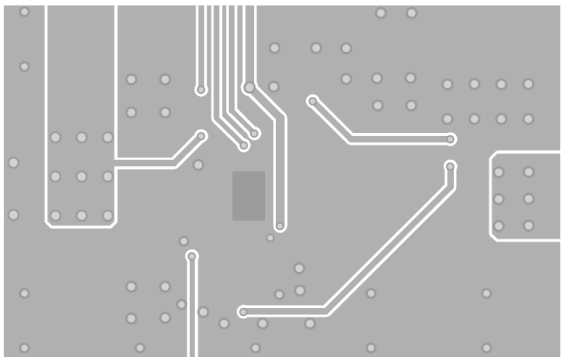
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
5. Keep the connection between the input capacitor and IN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and GND as possible.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Place the FB resistors as close to the chip as possible, and keep the trace connecting to FB as short as possible.
9. Use multiple vias to connect the power planes to internal layers.



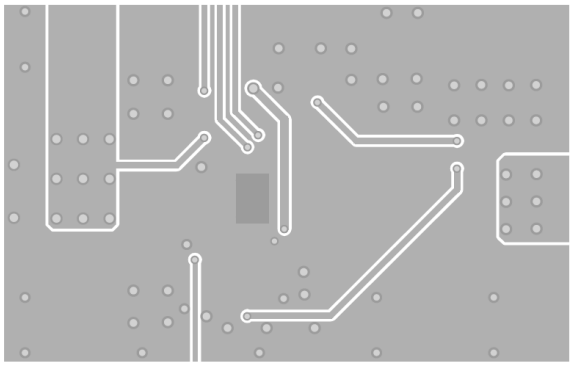
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 8: Recommended PCB Layout

Note:

7) The recommended PCB layout is based on Figure 9.

TYPICAL APPLICATION CIRCUITS

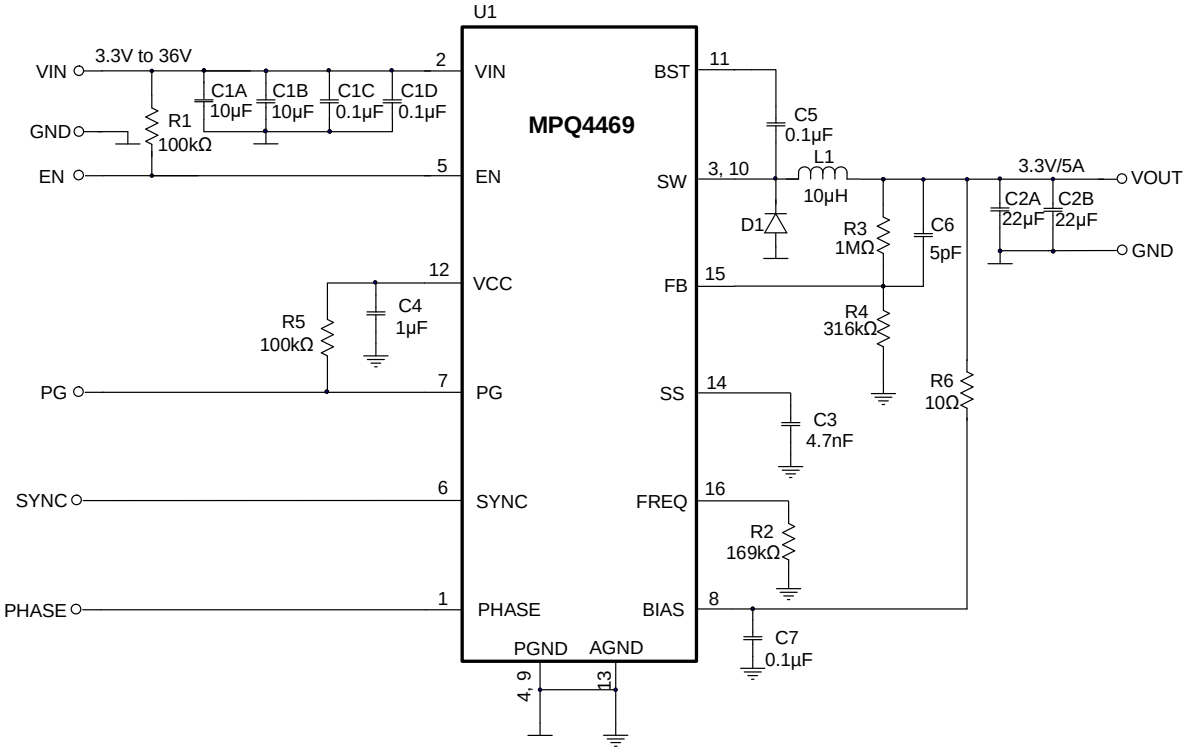


Figure 9: V_{OUT} = 3.3V, f_{SW} = 500kHz

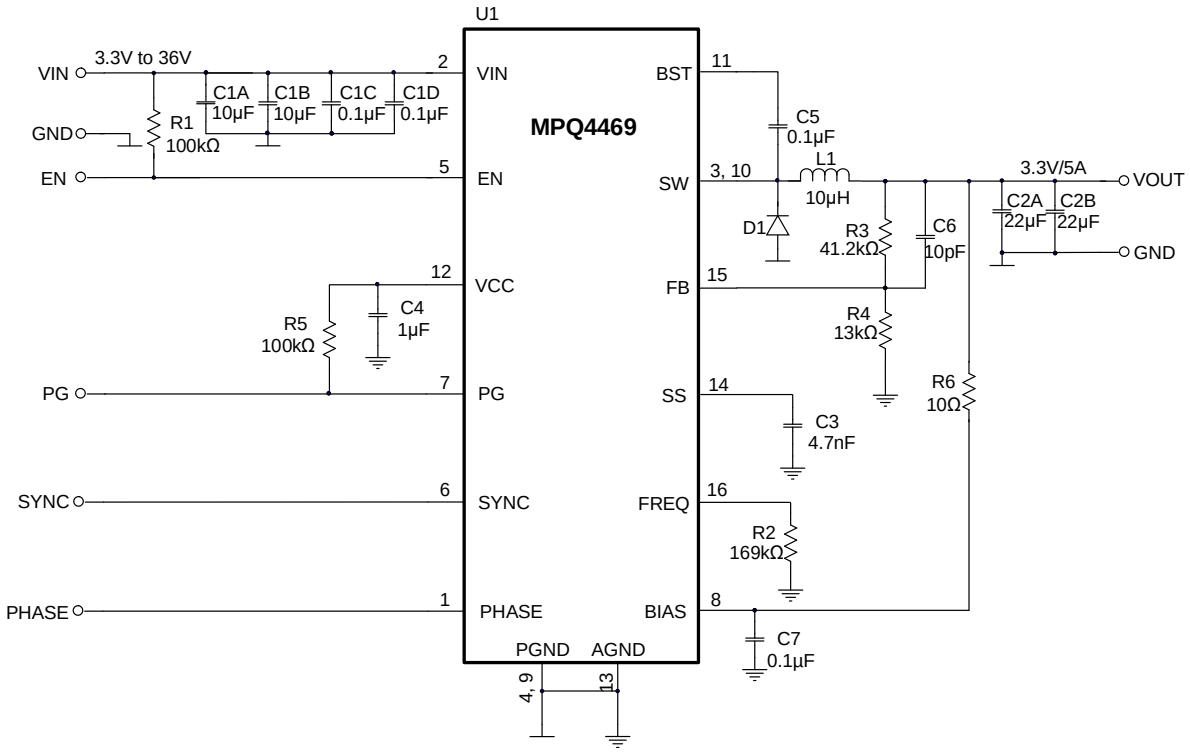


Figure 10: V_{OUT} = 3.3V, f_{SW} = 500kHz for < 100kΩ FB Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

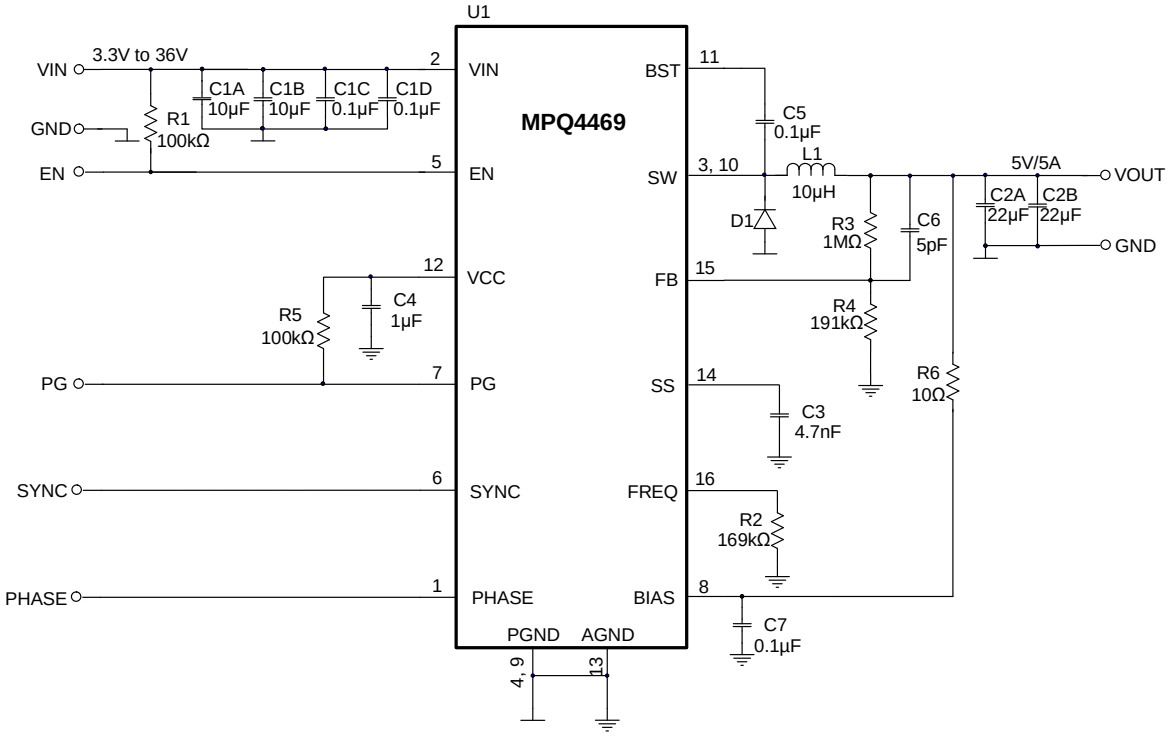


Figure 11: V_{OUT} = 5V, f_{SW} = 500kHz

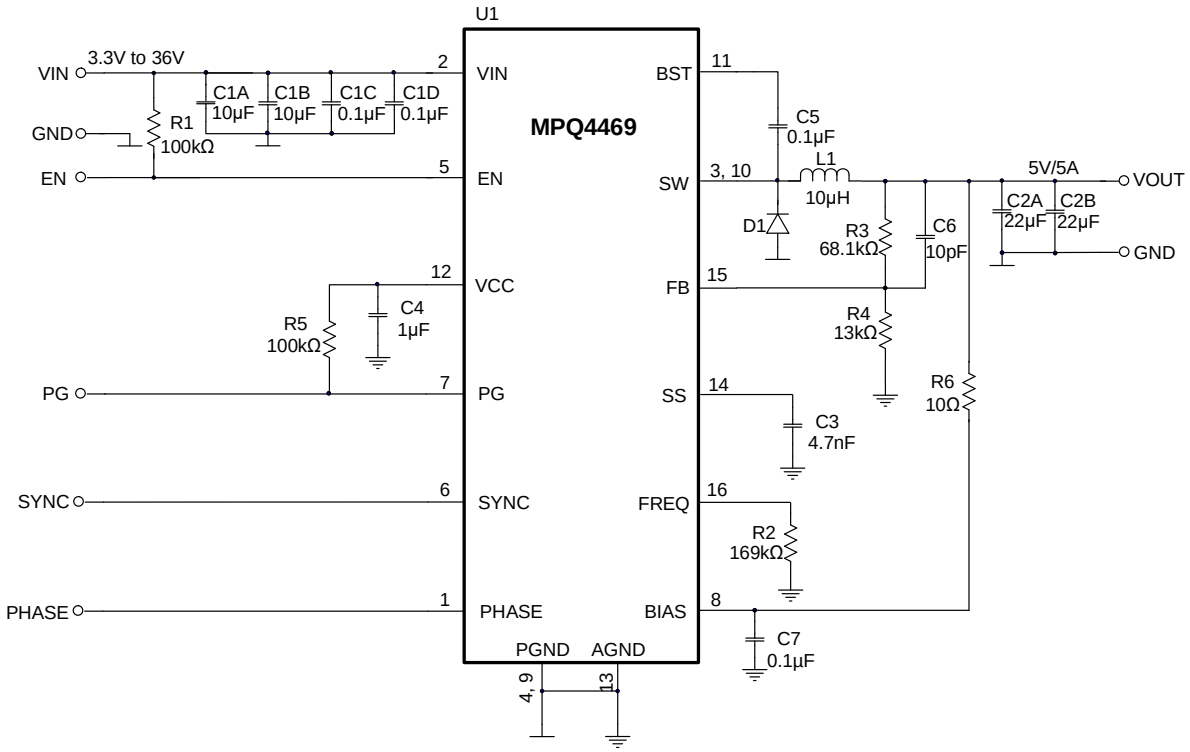


Figure 12: V_{OUT} = 5V, f_{SW} = 500kHz for < 100kΩ FB Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

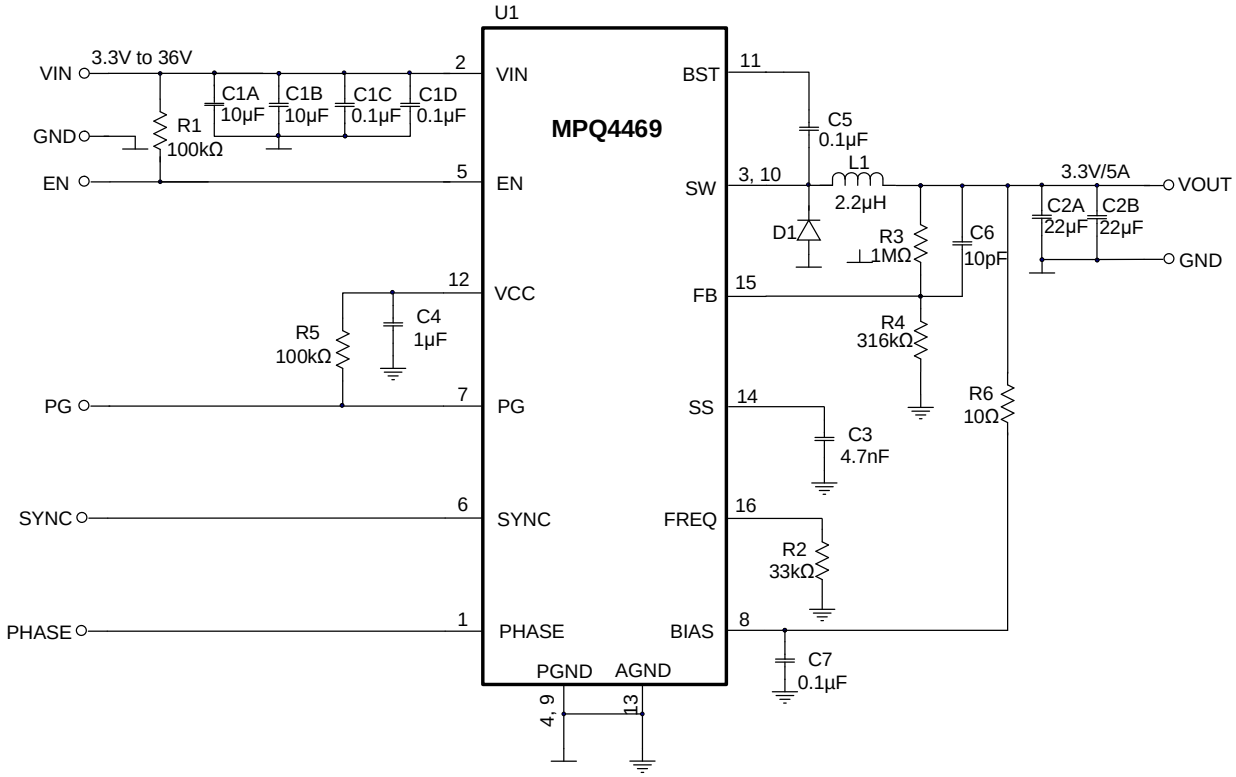


Figure 13: V_{OUT} = 3.3V, f_{SW} = 2.2MHz

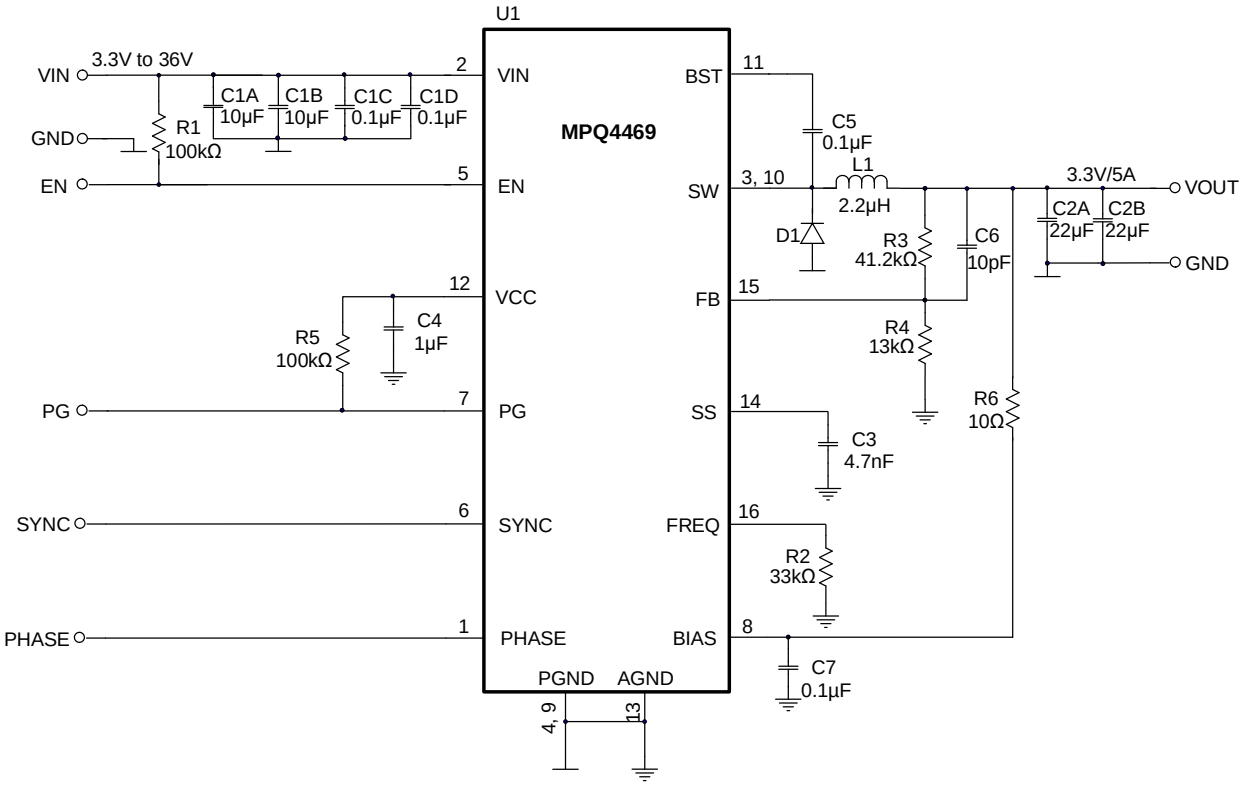


Figure 14: V_{OUT} = 3.3V, f_{SW} = 2.2MHz for < 100kΩ FB Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

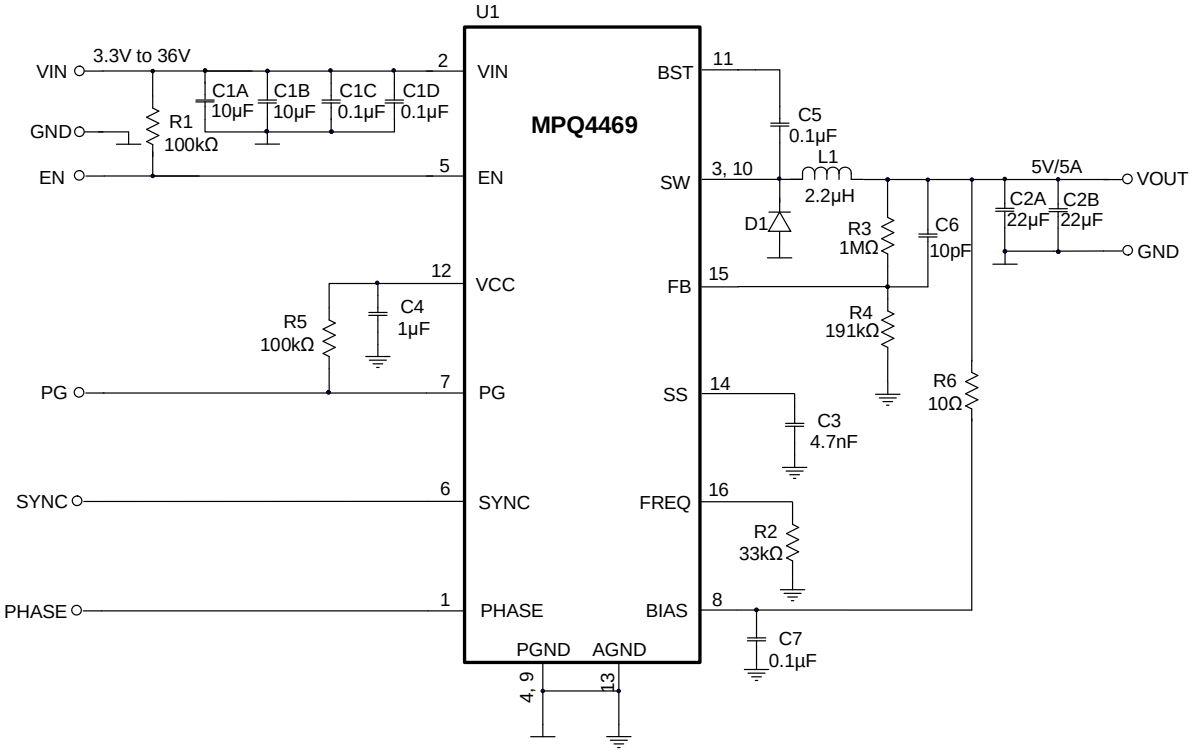


Figure 15: V_{OUT} = 5V, f_{SW} = 2.2MHz

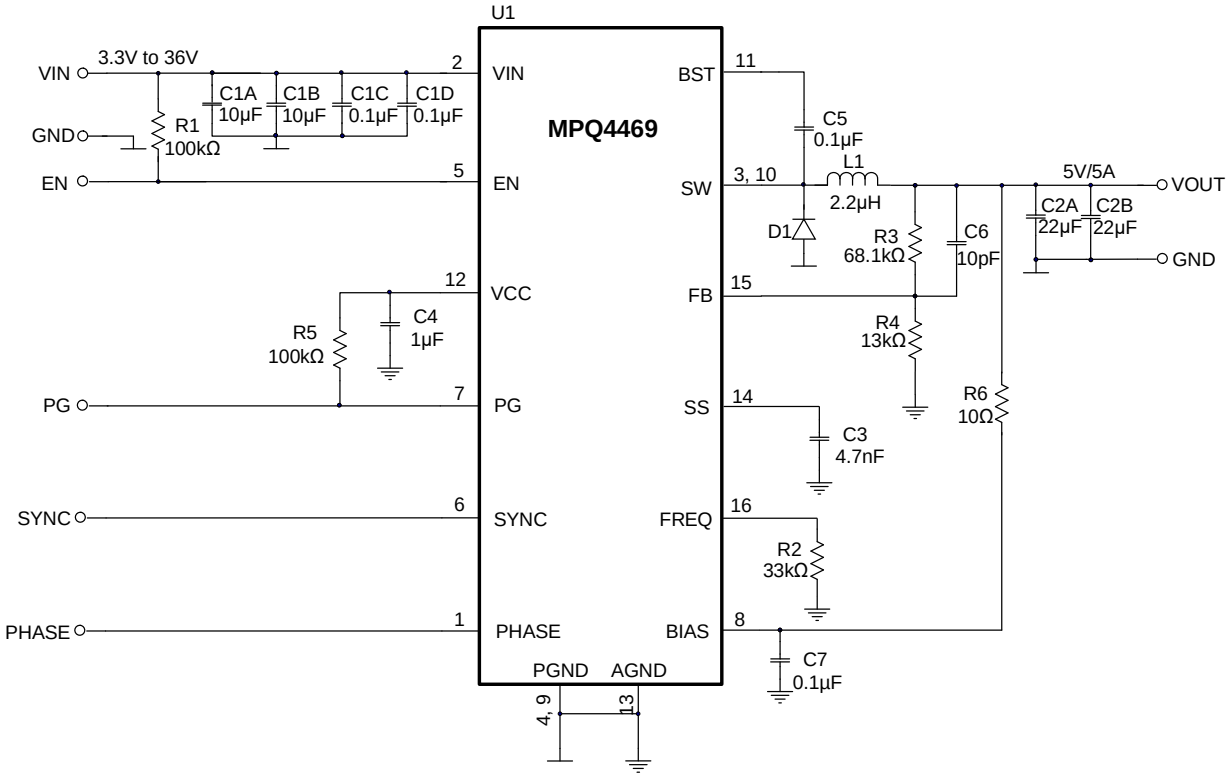
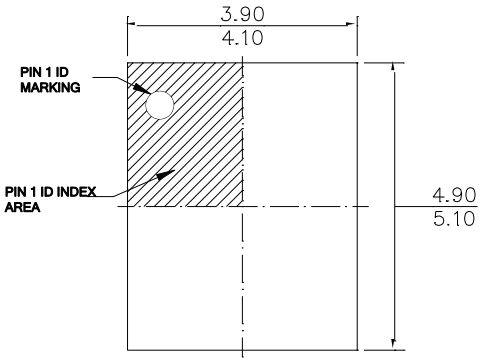


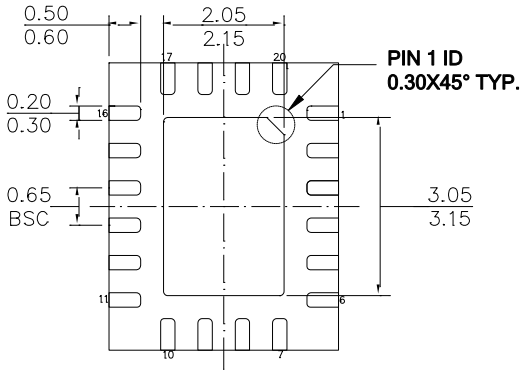
Figure 16: V_{OUT} = 5V, f_{SW} = 2.2MHz for < 100kΩ FB Divider Application

PACKAGE INFORMATION

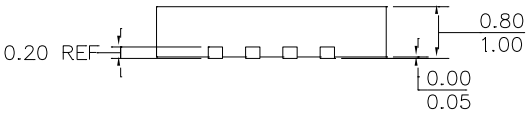
QFN-20 (4mmx5mm)



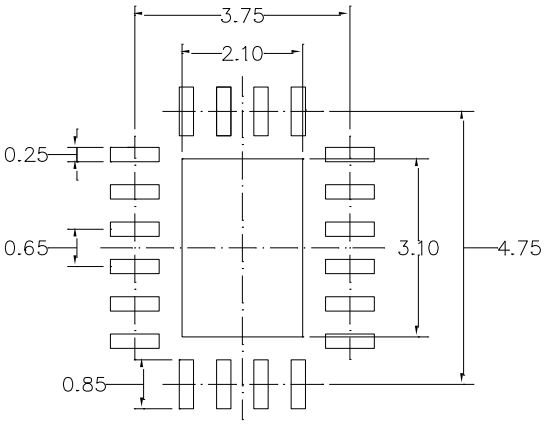
TOP VIEW



BOTTOM VIEW



SIDE VIEW

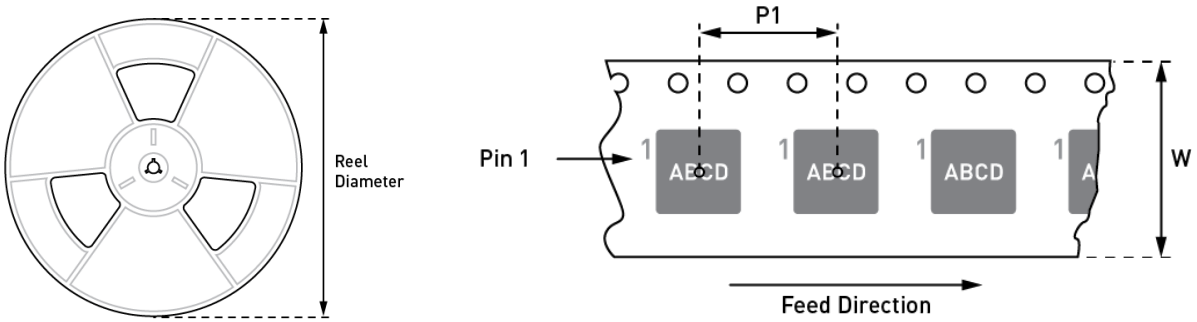


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4469GV-AEC1	QFN-20 (4mmx5mm)	5000	13in	12mm	8mm