Product Change Notification / SYST-10NIVQ377

Date:

17-Dec-2020

Product Category:

8-bit Microcontrollers

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - ATtiny202/402 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-10NIVQ377_Affected_CPN_12172020.pdf
SYST-10NIVQ377_Affected_CPN_12172020.csv

Notification Text:

SYST-10NIVQ377

Microchip has released a new Product Documents for the ATtiny202/402 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny202/402 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added silicon revision C 2) Added new errata: Device: Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values 3) ADC: Pending Event Stuck When Disabling the ADC 4) CCL: The CCL Must be Disabled to Change the Configuration of a Single LUT 5) TCA: Restart Will Reset Counter Direction in NORMAL and FRQ Mode 6) TCB: CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode 7) USART: Full Range Duty Cycle Not Supported When Validating LIN Sync Field , Open-Drain Mode Does Not Work When TXD is Configured as Output and Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0' 8) Added new data sheet clarifications: USART and Package Drawings

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 17 Dec 2020

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachments:

ATtiny202/ 402 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATTINY202-SSB-VAO
ATTINY202-SSBT-VAO
ATTINY202-SSF
ATTINY202-SSFR
ATTINY202-SSN
ATTINY202-SSNR
ATTINY202-SSZ-VAO
ATTINY202-SSZT-VAO
ATTINY402-SSB-VAO
ATTINY402-SSBT-VAO
ATTINY402-SSF
ATTINY402-SSFR
ATTINY402-SSN
ATTINY402-SSNR
ATTINY402-SSZ-VAO
ATTINY402-SSZT-VAO

ATtiny202/402

ATtiny202/402 Silicon Errata and Data Sheet Clarification

The ATtiny202/402 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40001969), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny202/402 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40001969) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. B(1)	Rev. C
Device	2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)	X	-
	2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X	X
ADC	2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X	X
	2.3.2 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X	X
	2.3.3 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X	X
	2.3.4 Pending Event Stuck When Disabling the ADC	X	X
CCL	2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X	X
	2.4.2 D-latch is Not Functional	X	X
	2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X
RTC	2.5.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X	X
	2.5.2 Disabling the RTC Stops the PIT	X	X
TCA	2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.7.1 Minimum Event Duration Must Exceed the Selected Clock Period	X	X
	2.7.2 The TCA Restart Command Does Not Force a Restart of TCB	X	X
	2.7.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X	X
USART	2.8.1 TXD Pin Override Not Released When Disabling the Transmitter	X	X
	2.8.2 Frame Error on a Previous Message May Cause False Start Bit Detection	X	X
	2.8.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X	X
	2.8.4 Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X
	2.8.5 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)

The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

Work Around
If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

Affected Silicon Revisions

Rev. B	Rev. C
X	-

2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around
Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCK in CLKCTRL.OSC20MCALIBB to '1'.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3 ADC - Analog-to-Digital Converter

2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around
Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.2 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work Around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.3 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and VDD < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for VDD < 2.7V.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.4 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around

Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around

Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around
None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around
None

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.5 RTC - Real-Time Counter

2.5.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler resulting in a longer period on the current count or period.

Work Around
None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.5.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around
Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.6 TCA - Timer/Counter A

2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.7 TCB - Timer/Counter B

2.7.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work Around

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.7.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.7.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.8.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work Around

Wait for the RXD pin to go high before reading RXDATA, for instance, by polling the bit in PORTn.IN where the RXD pin is located.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART is validating each bit to be within ±15% instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

Work Around
None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8.4 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8.5 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'

The Start-of-Frame Detector can unintentionally be enabled when the device is in Active mode and when the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is '0'. If the Receive Data (RXDATA) registers are read while receiving new data, RXCIF is cleared, and the Start-of-Frame Detector will be enabled and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode, so no interrupt will be triggered.

Work Around
Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

3. Data Sheet Clarifications

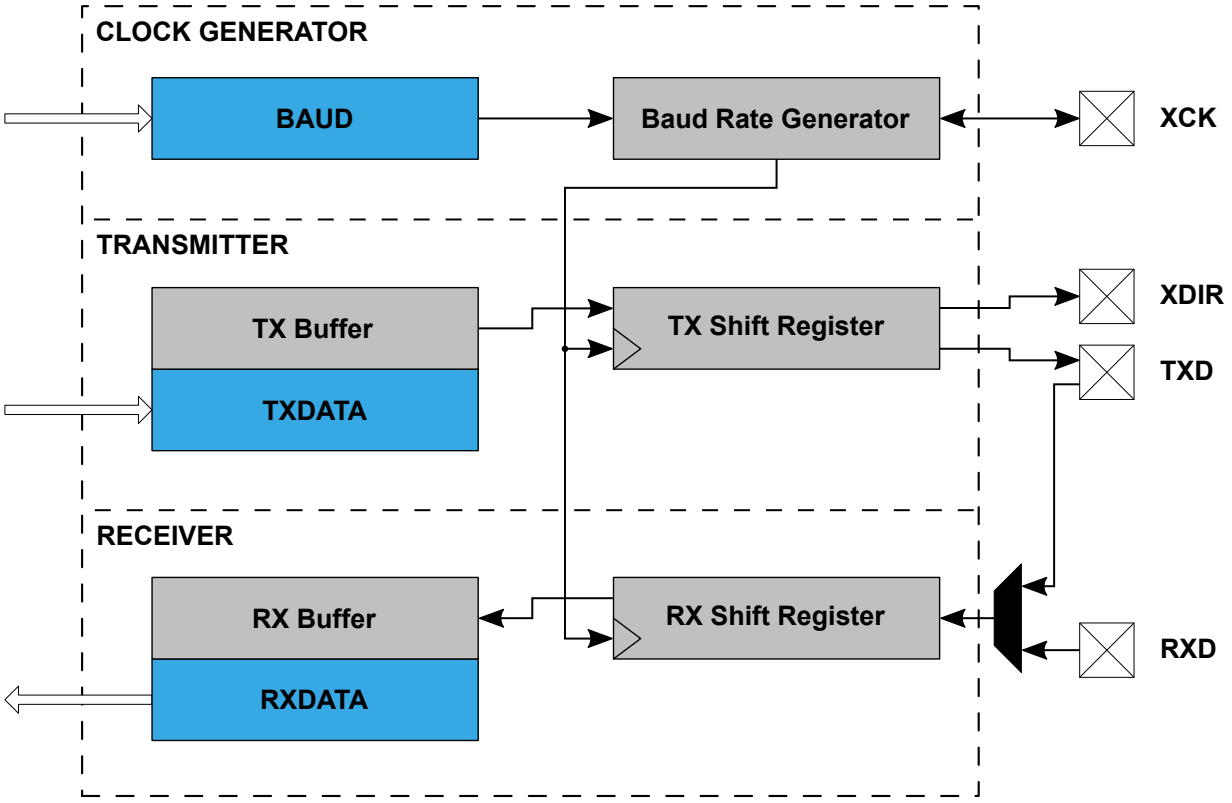
The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40001969).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

The block diagram is missing that USART TX is double-buffered from figure 25-1 in the data sheet. Added **TX Buffer** is shown below.

Figure 3-1. Block Diagram



The following text is changed in the *Overview* section:

The transmitter consists of a **two-level** write buffer.

The following text is changed in the *Data Transmission* section:

The data transmission is initiated by loading the **Transmit Data (USARTn.TXDATAL and USARTn.TXDATAH)** registers with the data to be sent. The data in the **Transmit Data registers are moved to the TX Buffer** once it is empty and onwards to the Shift register once it is empty and ready to send a new frame.

3.2 Electrical Characteristics

3.2.1 ADC

A clarification has been made to the electrical characteristics for the ADC peripheral:

- Added a note for 50% duty cycle

Table 3-1. Clock and Timing Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{ADC}	Sample rate	1.1V ≤ V_{REF}	15	-	115	ksps
		1.1V ≤ V_{REF} (8-bit resolution)	15	-	150	
		V_{REF} = 0.55V (10-bit)	7.5	-	20	
CLK_{ADC}	Clock frequency	V_{REF} = 0.55V (10-bit)	100	-	260	kHz
		1.1V ≤ V_{REF} (10-bit)	200	-	1500	
		1.1V ≤ V_{REF} (8-bit resolution)	200	-	2000(1)	
Ts	Sampling time		2	2	33	CLK_{ADC} cycles
T_{CONV}	Conversion time (latency)	Sampling time = 2 CLK_{ADC}	8.7	-	50	µs
T_{START}	Start-up time	Internal V_{REF}	-	22	-	µs

Note:

1. 50% duty cycle is required for clock frequencies above 1500 kHz.

3.3 Package Drawings

The information in the *Device and Package Maximum Weight* and *Package Reference* tables might be outdated. Refer to the RoHS information table on the device product page for up to date information.

The Moisture Sensitivity Level (MSL) information in the data sheet might be wrong, as this is dependent on the assembly site. To determine the MSL information for Microchip device shipments received from Microchip, review the label that is affixed to each bag, reel and inner box.

If neither the bag, reel or inner box is available, MSL information can be determined by reviewing Table 3.3 in the *Package Qualification Summary Report* posted at microchip.com/quality. The report is organized by package type and assembly site.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
C	12/2020	• Added silicon revision C • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – ADC: *Pending Event Stuck When Disabling the ADC* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'* • Added new data sheet clarifications: – *USART* – *Package Drawings*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics
A	06/2019	Initial document release

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