Product Change Notification / SYST-06IDRP388

Date:

08-Jan-2021

Product Category:

Power Management - PMIC

PCN Type:

Document Change

Notification Subject:

Data Sheet - MIC23450 - 3 MHz, PWM, 2A Triple Buck Regulator with HyperLight Load and Power Good

Affected CPNs:

SYST-06IDRP388_Affected_CPN_01082021.pdf
SYST-06IDRP388_Affected_CPN_01082021.csv

Notification Text:

SYST-06IDRP388

Microchip has released a new Product Documents for the MIC23450 - 3 MHz, PWM, 2A Triple Buck Regulator with HyperLight Load and Power Good of devices. If you are using one of these devices please read the document located at MIC23450 - 3 MHz, PWM, 2A Triple Buck Regulator with HyperLight Load and Power Good.

Notification Status: Final

Description of Change:
1) Converted Micrel document MIC23450 to Microchip data sheet DS20006479A.
2) Minor text changes throughout.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 08 Jan 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

MIC23450 - 3 MHz, PWM, 2A Triple Buck Regulator with HyperLight Load and Power Good

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

MIC23450-AAAYML-EV
MIC23450-AAAYML-T5
MIC23450-AAAYML-TR

MIC23450

3 MHz, PWM, 2A Triple Buck Regulator with HyperLight Load and Power Good

Features

- 2.7V to 5.5V Input Voltage
- Three Independent 2A Outputs
- Up to 93% Peak Efficiency
- 81% Typical Efficiency at 1 mA
- Three Independent Power Good Indicators
- 23 µA Typical Quiescent Current (Per Channel)
- 3 MHz PWM Operation in Continuous Mode
- Ultra-Fast Transient Response
- Low Voltage Output Ripple
    - 30 mV_{PP} Ripple in HyperLight Load® Mode
    - 5 mV Output Voltage Ripple in Full PWM Mode
- Fully Integrated MOSFET Switches
- 0.01 µA Shutdown Current (Per Channel)
- Thermal-Shutdown and Current-Limit Protection
- Output Voltage as Low as 1V
- 32-Pin 5 mm x 5 mm QFN Package
- –40°C to +125°C Junction Temperature Range

Applications

- Solid State Drives (SSD)
- µC/µP, FPGA, and DSP power
- Test and Measurement Systems
- Set-Top Boxes and DTV
- High-Performance Servers
- Security/Surveillance Cameras
- 5V POL Applications

General Description

The MIC23450 is a high-efficiency, 3 MHz, triple 2A, synchronous buck regulator with HyperLight Load® mode. HyperLight Load provides very high efficiency at light loads and ultra-fast transient response which is perfectly suited for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. The 5 mm x 5 mm QFN package saves board space and requires only five external components for each channel.

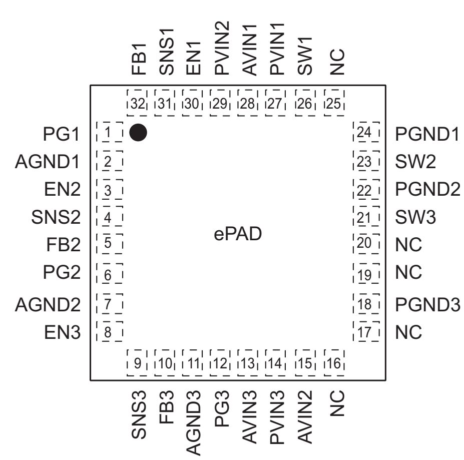
The MIC23450 is designed for use with a very small inductor, down to 0.47 µH, and an output capacitor as small as 2.2 µF that enables a total solution size, less than 1 mm height.

The MIC23450 has a very low quiescent current of 23 µA each channel and achieves as high as 81% efficiency at 1 mA. At higher loads, the MIC23450 provides a constant switching frequency around 3 MHz while achieving peak efficiencies up to 93%.

The MIC23450 is available in 32-pin 5 mm x 5 mm QFN package with an operating junction temperature range from –40°C to +125°C.

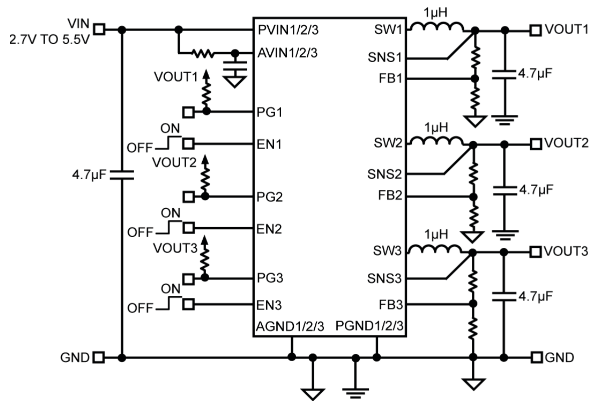
Package Type

MIC23450
32-Lead QFN (ML) - Adjustable
(Top View)



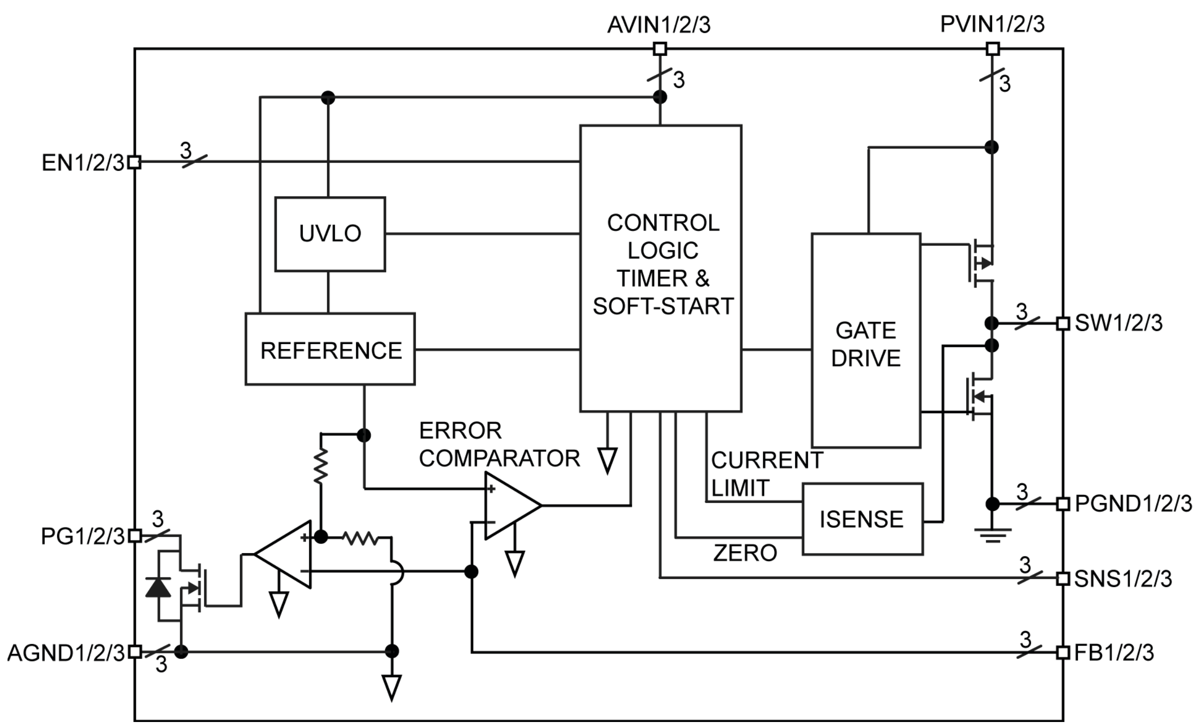
Typical Application Circuit

MIC23450



Functional Block Diagram

Simplified MIC23450 Functional Block Diagram - Adjustable Output Voltage



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (PV_{IN}, AV_{IN}) .... –0.3V to +6V
Sense (V_{SNS1}, V_{SNS2}, V_{SNS3}) .... –0.3V to +6V
Power Good (PG1, PG2, PG3) .... –0.3V to +6V
Output Switch Voltage (V_{SW1}, V_{SW2}, V_{SW3} .... –0.3V to +6V
Enable Input Voltage (V_{EN1}, V_{EN2}, V_{EN3}) .... –0.3V to V_{IN}
ESD Rating (Note 1) .... ESD Sensitive

Operating Ratings ‡

Supply Voltage (V_{IN}) .... +2.7V to +5.5V
Enable Input Voltage (V_{EN1}, V_{EN2}, V_{EN3}) .... 0V to V_{IN}
Output Voltage Range (V_{SNS1}, V_{SNS2}, V_{SNS3}) .... +1.0V to +3.3V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = +25°C; V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6V; L1 = L2 = L3 = 1 µH; C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7µF, unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	—	**2.7**	—	**5.5**	V	—
Undervoltage Lockout Threshold	UVLO	**2.45**	2.55	**2.65**	V	Turn-on
Undervoltage Lockout Hysteresis	UVLO_HYST	—	75	—	mV	—
Quiescent Current	—	—	69	**120**	µA	I_{OUT} = 0 mA, SNS > 1.2 * V_{OUTNOM}
Per Channel Shutdown Current	I_{SHDN}	—	0.01	**5**	µA	V_{EN1}, V_{EN2}, V_{EN3} = 0V; V_{IN} = 5.5V
Output Voltage Accuracy	V_{OUT}_ACC	**–2.5**	—	**+2.5**	%	V_{IN} = 3.6V if $_{VOUT(NOM)}$ < 2.5V, I_{LOAD} = 20 mA
	—					V_{IN} = 4.5V if $V_{OUT(NOM)}$ ≥ 2.5V, I_{LOAD} = 20 mA
Feedback Voltage (V_{FB1}, V_{FB2}, V_{FB3})	V_{FB}	**0.604**	0.62	**0.635**	V	—
Peak Current Limit	I_{PEAK}	**2**	4.5	—	A	I_{OUT1}, I_{OUT2}, I_{OUT3} SNS1, SNS2, SNS3 = 0.9 x V_{OUTNOM}
Foldback Current Limit	I_{FB}	—	1.8	—	A	—
Output Voltage Line Regulation (V_{OUT1}, V_{OUT2}, V_{OUT3})	—	—	0.3	—	%/V	V_{IN} = 3.6V to 5.5V if $V_{OUTNOM1,2,3}$ < 2.5V, I_{LOAD} = 20 mA
		—		—		V_{IN} = 4.5V to 5.5V if V_{OUTNOM} ≥ 2.5V, I_{LOAD} = 20 mA

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C; V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6V; L1 = L2 = L3 = 1 µH; C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7µF, unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Load Regulation (V_{OUT1}, V_{OUT2}, V_{OUT3})	—	—	0.2	—	%	DCM: 20 mA < I_{LOAD} < 130 mA, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V
		—	0.4	—		DCM: 20 mA < I_{LOAD} < 130 mA, V_{IN} = 5.0V if V_{OUTNOM} > 2.5V
		—	0.6	—		CCM: 200 mA < I_{LOAD} < 500 mA, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V
		—	0.3	—		CCM: 200 mA < I_{LOAD} < 1A, V_{IN} = 5.0V if V_{OUTNOM} > 2.5V
PWM Switch On Resistance (R_{SW1}, R_{SW2}, R_{SW3})	—	—	0.2	—	Ω	I_{SW1}, I_{SW2}, I_{SW3} = +100 mA (PMOS)
		—		—		I_{SW1}, I_{SW2}, I_{SW3} = –100 mA (NMOS)
Maximum Frequency	f_{SW}	—	3	—	MHz	I_{OUT1}, I_{OUT2}, I_{OUT3} = 120 mA
Soft-Start Time	t_{SS}	—	115	—	µs	V_{OUT1}, V_{OUT2}, V_{OUT3} = 90%
Power Good Threshold	PG_TH	83	90	96	%	% of V_{NOM}
Power Good Hysteresis	PG_{HYST}	—	10	—	%	—
Power Good Pull-Down Voltage	—	—	—	200	mV	V_{SNS} = 90% V_{NOM}, I_{PG} = 1 mA
Enable Threshold	EN_TH	**0.5**	0.8	**1.2**	V	Turn-on
Enable Input Current	—	—	0.1	**1**	µA	—
Overtemperature Shutdown	T_{SHDN}	—	160	—	°C	—
Overtemperature Shutdown Hysteresis	T_{SHDN_HYST}	—	20	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance 5 mm x 5 mm QFN-32	θ_{JA}	—	30	—	°C/W	—
Thermal Resistance 5 mm x 5 mm QFN-32	θ_{JC}	—	10	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

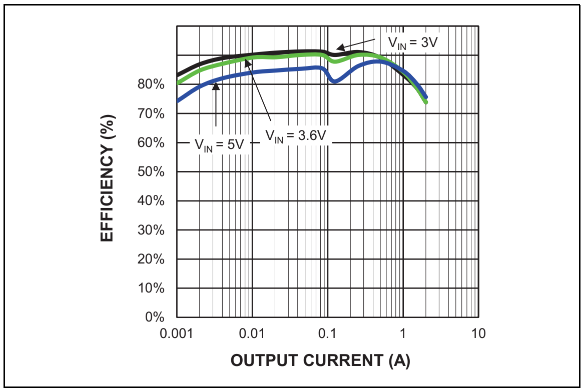


FIGURE 2-1: *Efficiency (V_{OUT} = 1.8V) vs. Output Current.*

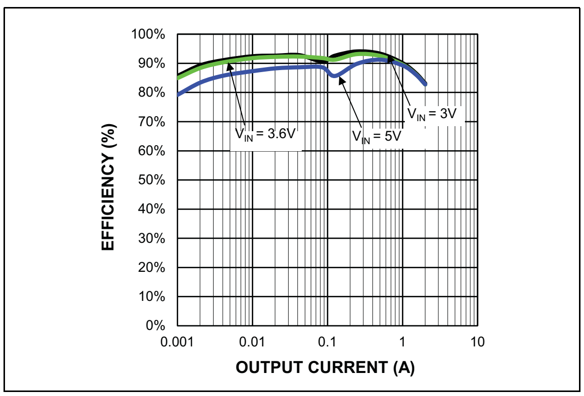


FIGURE 2-2: *Efficiency (V_{OUT} = 2.5V) vs. Output Current.*

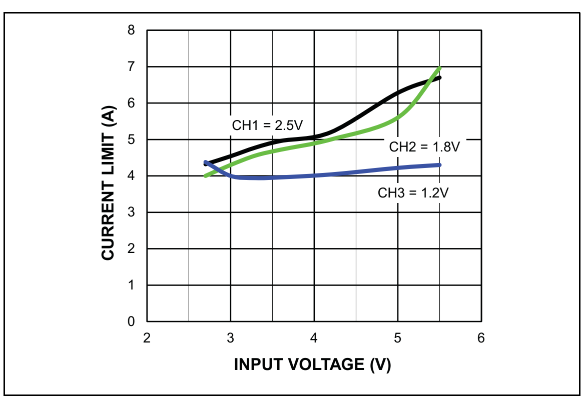


FIGURE 2-3: *Current Limit vs. Input Voltage.*

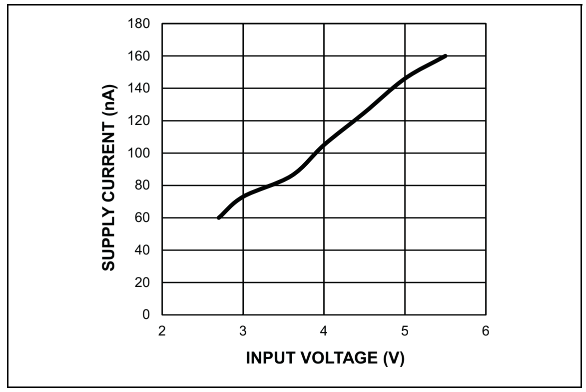


FIGURE 2-4: *Shutdown Current vs. Input Voltage.*

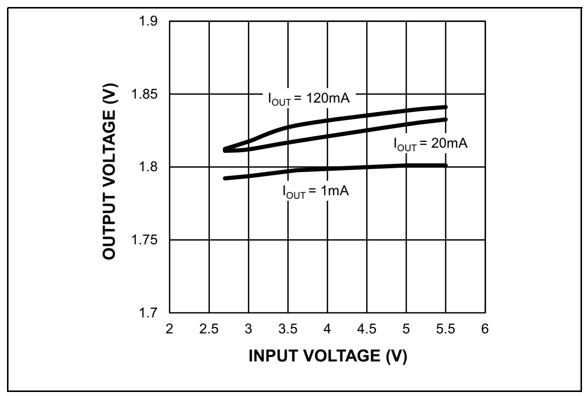


FIGURE 2-5: *Line Regulation (Low Loads).*

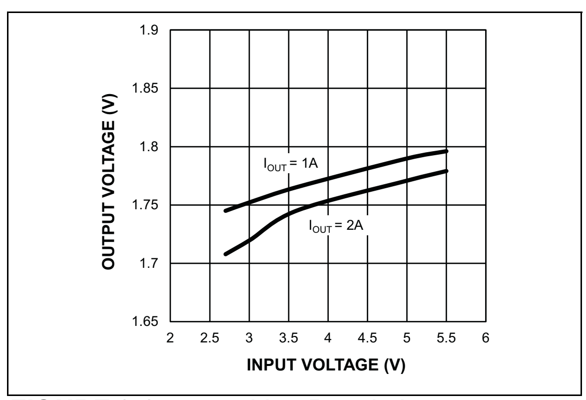


FIGURE 2-6: *Line Regulation (High Loads).*

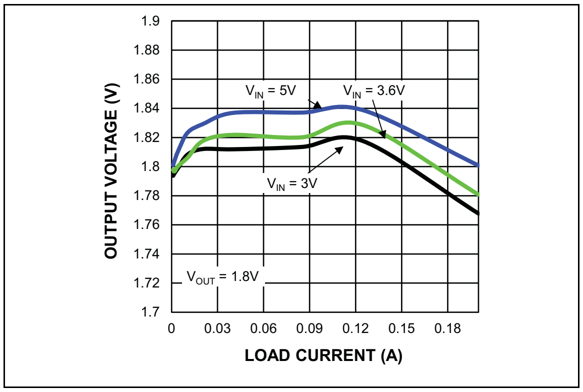


FIGURE 2-7: *Output Voltage vs. Output Current (HLL).*

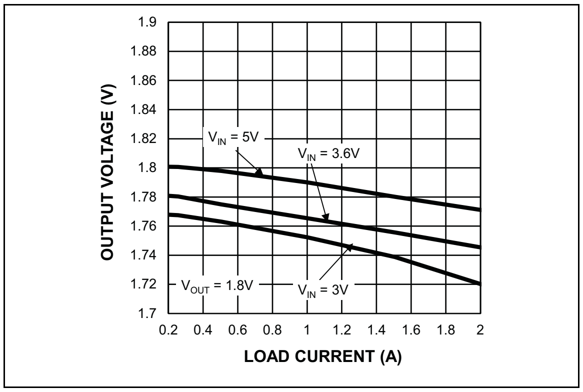


FIGURE 2-8: *Output Voltage vs. Output Current (CCM).*

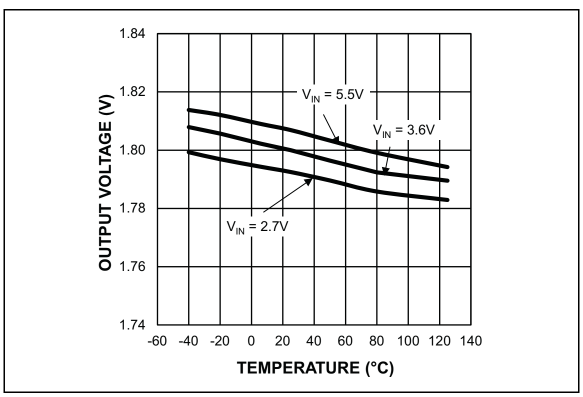


FIGURE 2-9: *Output Voltage vs. Temperature.*

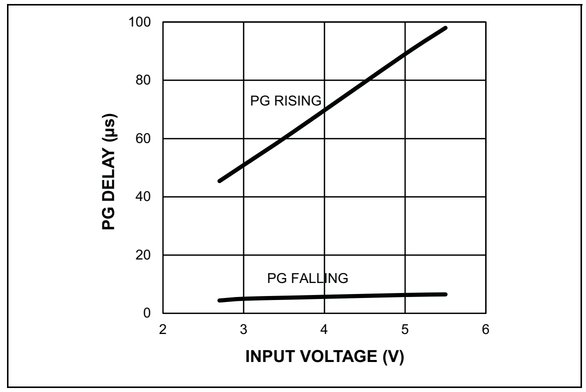


FIGURE 2-10: *PG Delay Time vs. Input Voltage.*

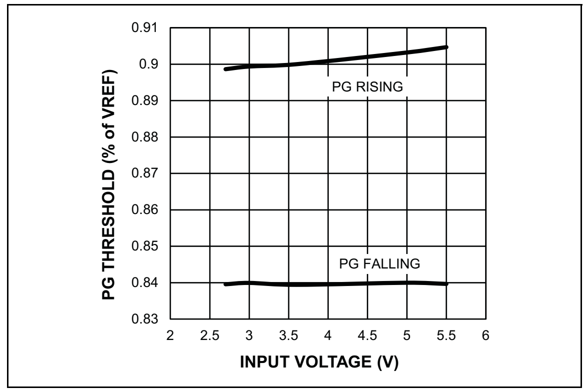


FIGURE 2-11: *PG Threshold vs. Input Voltage.*

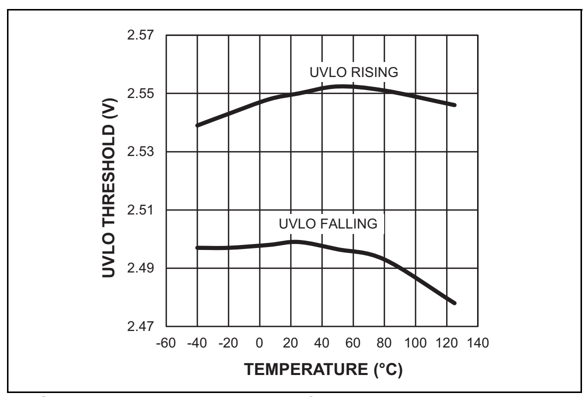


FIGURE 2-12: *UVLO Threshold vs. Temperature.*

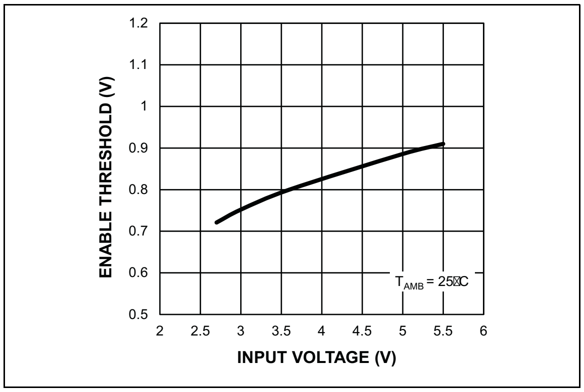


FIGURE 2-13: *Enable Threshold vs. Input Voltage.*

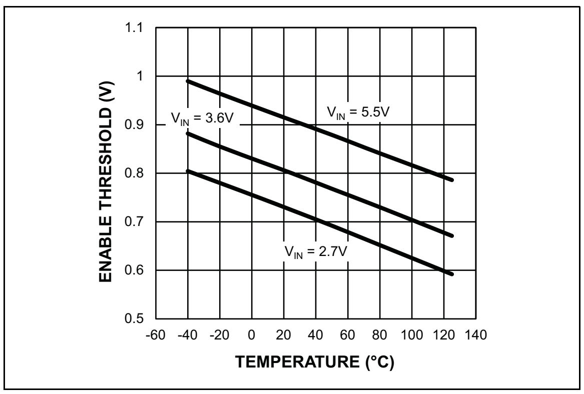


FIGURE 2-14: *Enable Threshold vs. Temperature.*

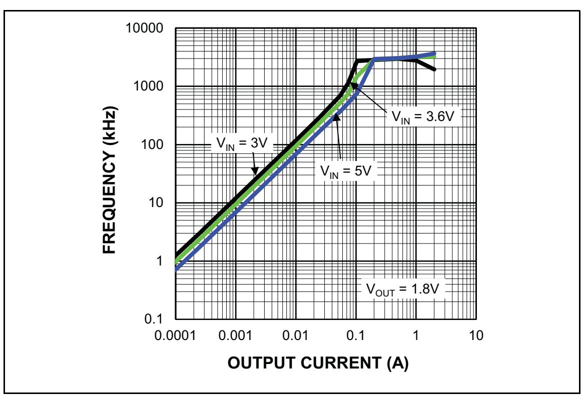


FIGURE 2-15: *Switching Frequency vs. Load Current.*

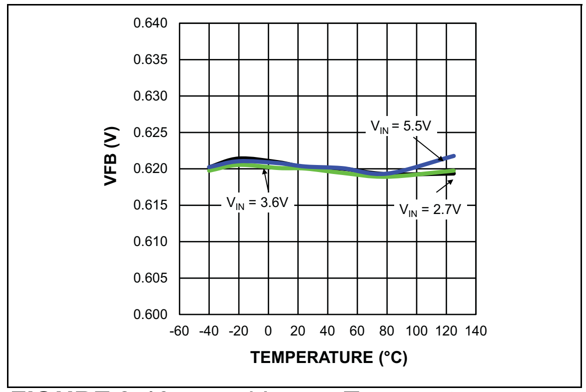


FIGURE 2-16: *V_{FB} vs. Temperature.*

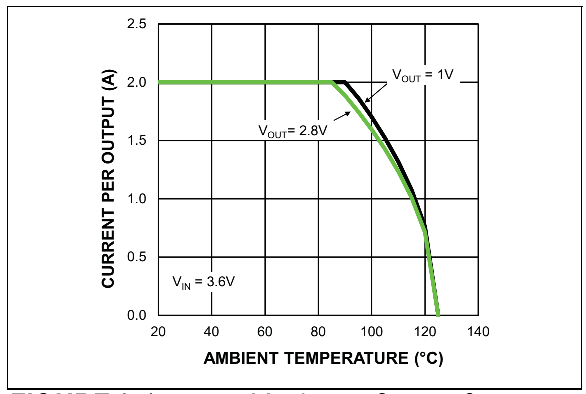


FIGURE 2-17: *Maximum Output Current per O/P vs. Temperature(1 O/P).*

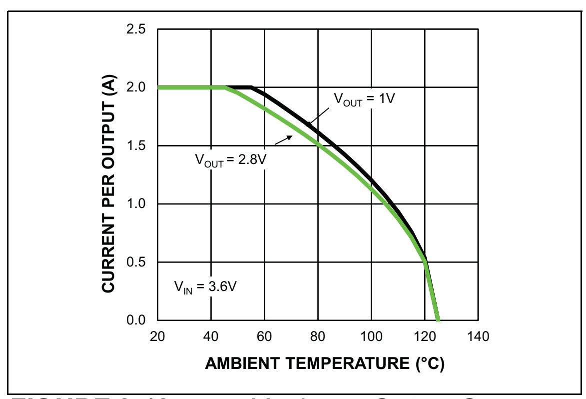


FIGURE 2-18: *Maximum Output Current per O/P vs. Temperature(2 O/P).*

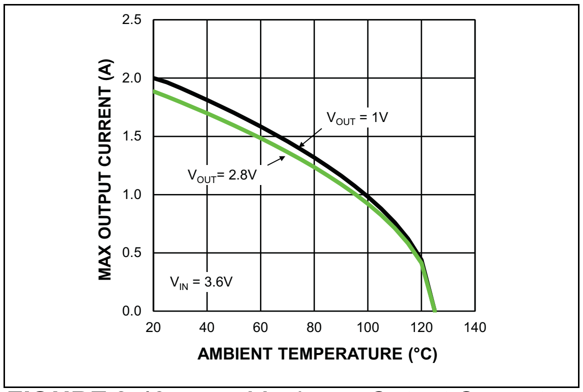


FIGURE 2-19: Maximum Output Current per O/P vs. Temperature(3 O/P).

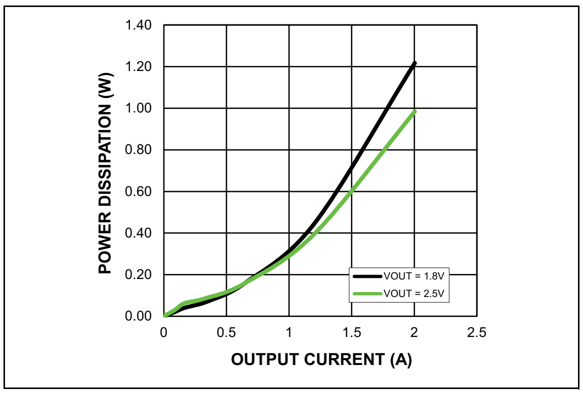


FIGURE 2-20: Power Dissipation vs. Load Current (Per Channel).

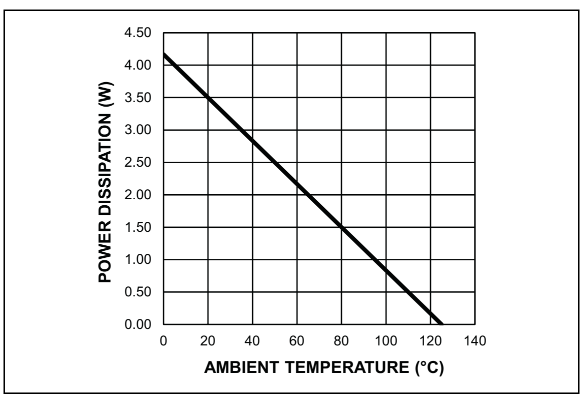


FIGURE 2-21: Maximum Package Dissipation vs. Ambient Temperature.

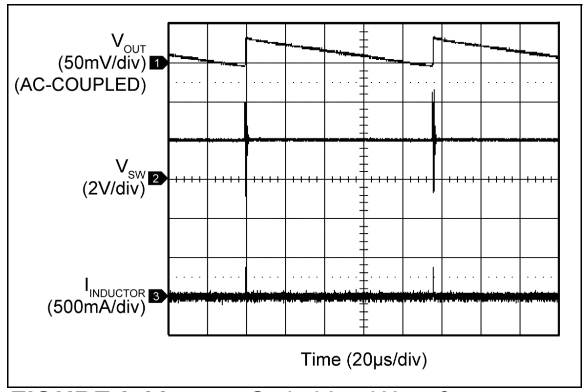


FIGURE 2-22: Switching Waveform Discontinuous Mode (1 mA).

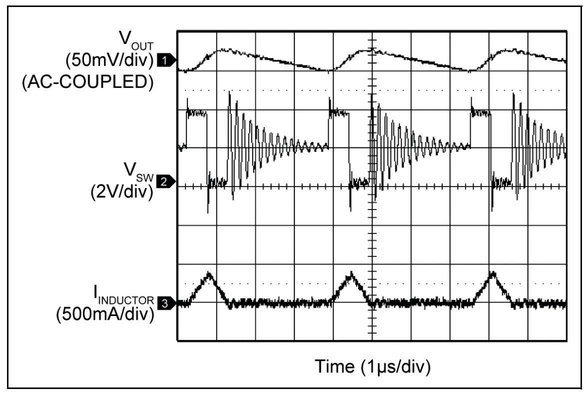


FIGURE 2-23: Switching Waveform Discontinuous Mode (50 mA).

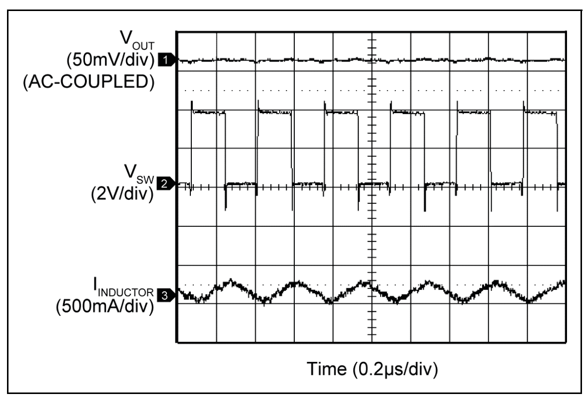


FIGURE 2-24: Switching Waveform Continuous Mode (150 mA).

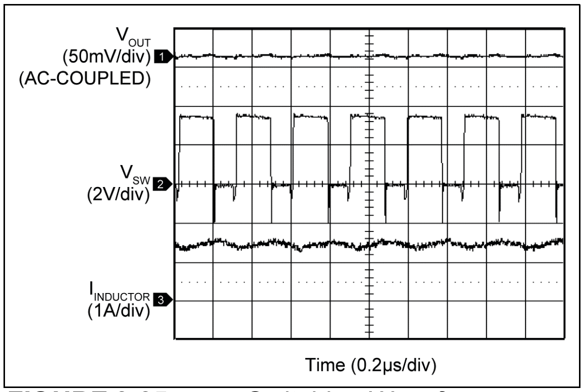


FIGURE 2-25: *Switching Waveform Continuous Mode (1.5A).*

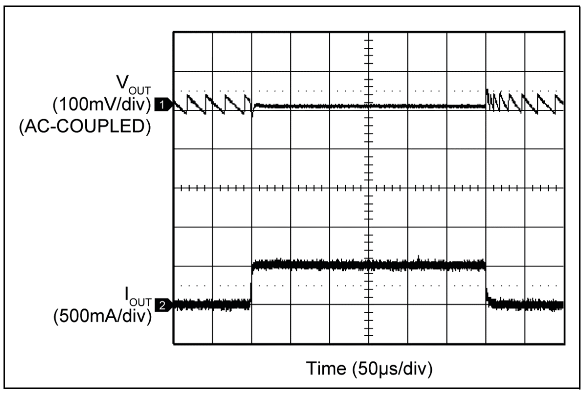


FIGURE 2-26: *Load Transient (10 mA to 500 mA).*

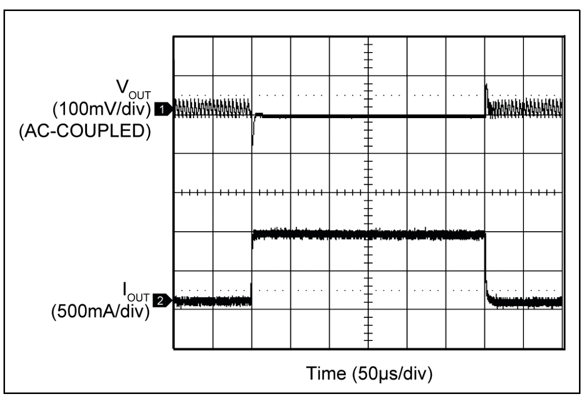


FIGURE 2-27: *Load Transient (50 mA to 1A).*

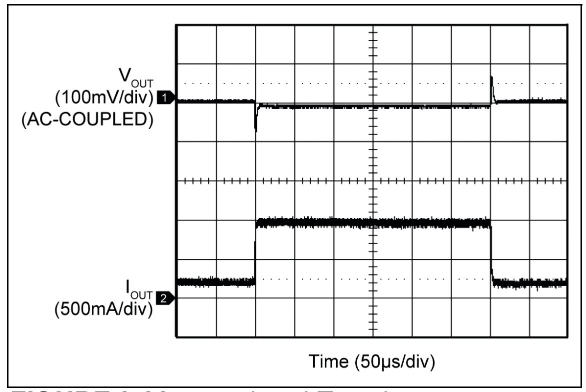


FIGURE 2-28: *Load Transient (200 mA to 1A).*

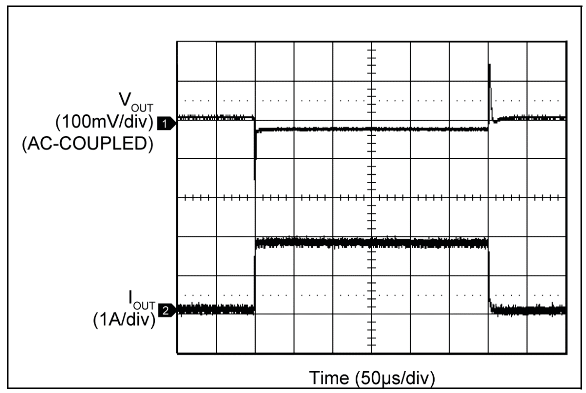


FIGURE 2-29: *Load Transient (200 mA to 2A).*

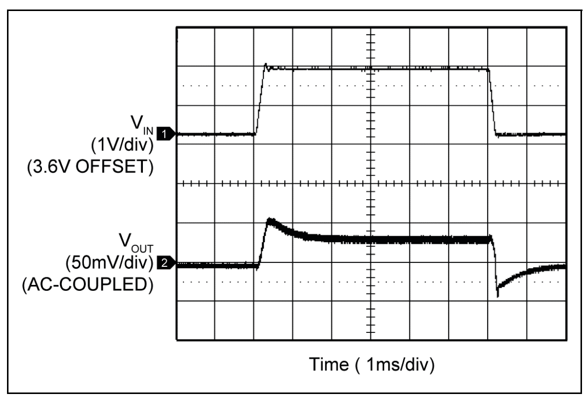


FIGURE 2-30: *Line Transient (3.6V to 5.5V @ 1.5A Load).*

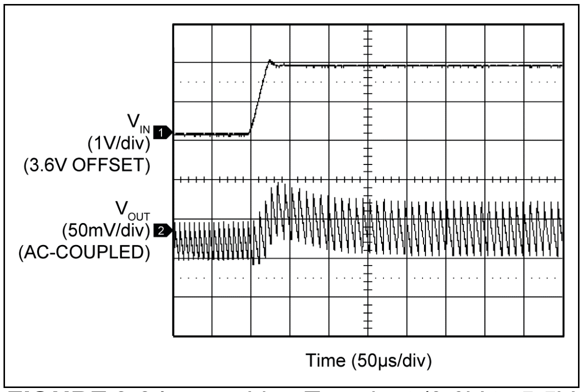


FIGURE 2-31: *Line Transient (3.6V to 5.5V @ 20 mA Load).*

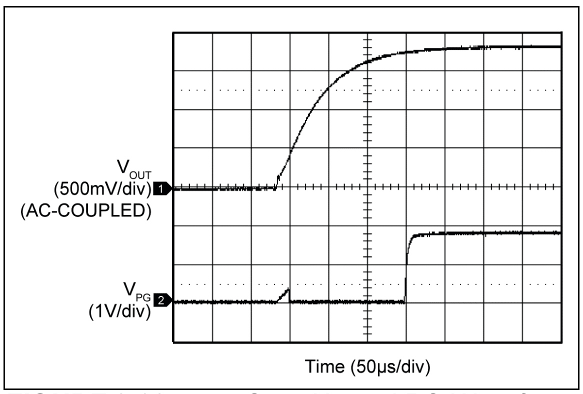


FIGURE 2-32: *Start-Up and PG Waveform.*

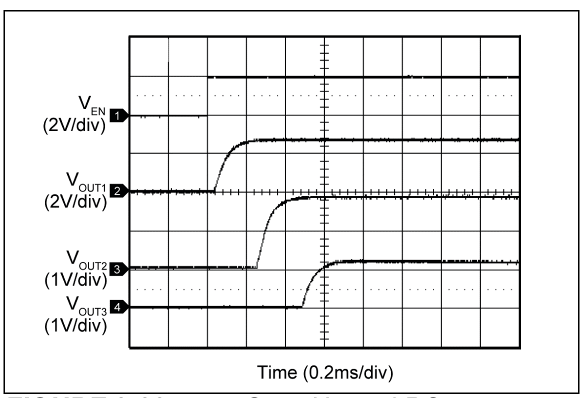


FIGURE 2-33: *Start-Up and PG Waveform - Sequenced (EN = EN1, PG1 = EN2, PG2 = EN3).*

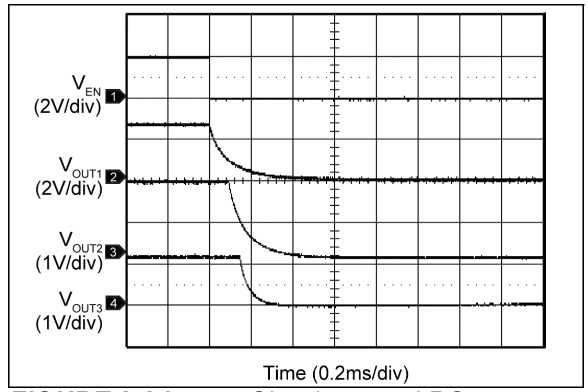


FIGURE 2-34: *Shutdown and PG Waveform - Sequenced (EN = EN1, PG1 = EN2, PG2 = EN3).*

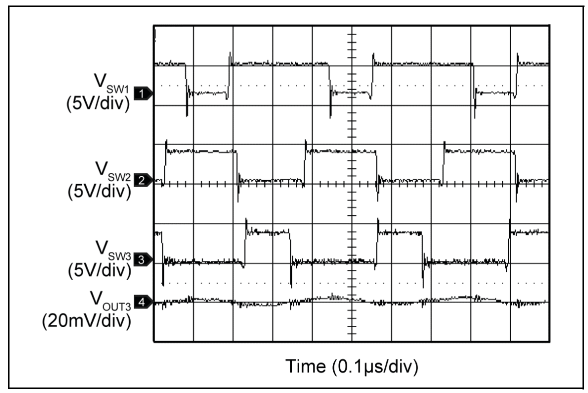


FIGURE 2-35: *Switching Waveform (All Channels in Continuous Mode).*

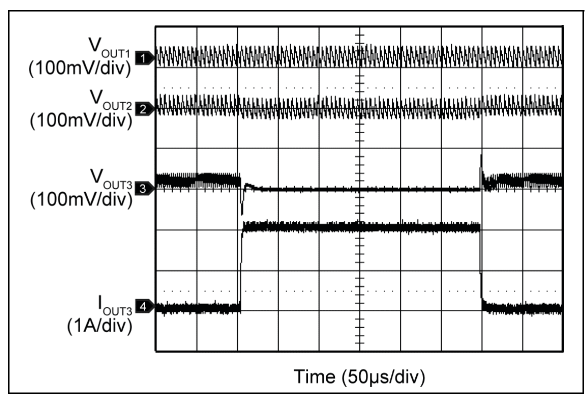


FIGURE 2-36: *Transient Cross Regulation (I_{OUT3} = 50 mA to 2A, I_{OUT1}, I_{OUT2} = 20 mA)*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
26, 23, 21	SW1, 2, 3	Switch (Output). Internal power MOSFET output switches for Output 1/2/3.
30, 3,8	EN1, 2, 3	Enable (Input). Logic high enables operation of regulator 1/2/3. Logic low will shut down the device. Do not leave floating.
31, 4, 9	SNS1, 2, 3	Sense. Connect to $V_{OUT1,2,3}$ as close to output capacitor as possible to sense output voltage.
32, 5, 10	FB1, 2, 3	Feedback. Connect a resistor Divider from output 1/2/3 to ground to set the output voltage.
1, 6, 12	PG1, 2, 3	Power Good. Open Drain output for the power good indicator for output 1/2/3. Place a resistor between this pin and a voltage source to detect a power good condition.
2, 7, 11	AGND1, 2, 3	Analog Ground. Connect to quiet ground point away from high current paths, e.g., C_{OUT} for best operation. Must be connected externally to PGND.
27, 29, 14	PVIN1, 2, 3	Power Input Voltage. Connect a capacitor to PGND to localize loop currents and decouple switching noise.
28, 15, 13	AVIN1, 2, 3	Analog Input Voltage. Connect a capacitor to AGND to decouple noise.
24, 22, 18	PGND1, 2, 3	Power ground.
16, 17, 19, 20, 25	NC	No connect.
EP	ePAD	Exposed Heat Sink Pad. Connect to PGND.

4.0 FUNCTIONAL DESCRIPTION

4.1 PVIN

The input supply (PVIN) provides power to the internal MOSFETs for the switch mode regulator. The VIN operating range is 2.7V to 5.5V so an input capacitor, with a minimum voltage rating of 6.3V, is recommended. Due to the high di/dt switching speeds, a minimum 2.2 µF or 4.7 µF recommended bypass capacitor placed close to PVIN and the power ground (PGND) pin is required.

4.2 AVIN

The input supply (AVIN) provides power to the internal control circuitry. As the high di/dt switching speeds on PVIN cause small voltage spikes, an RC filter comprising 50Ω and a minimum 100 nF decoupling capacitor placed close to the AVIN and signal ground (AGND) pin is required.

4.3 EN

A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.01 µA. MIC23450 features internal soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up. Do not leave the EN pin floating.

4.4 SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

4.5 SNS

The sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor.

4.6 AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop.

4.7 PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop as applicable.

4.8 PG

The power good (PG) pin is an open drain output which indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5 kΩ should be connected from PG to V_{OUT}.

4.9 FB

The feedback (FB) pin is the control input for programming the output voltage. A resistor divider network is connected to this pin from the output and is compared to the internal 0.62V reference within the regulation loop.

The output voltage can be programmed between 1V and 3.3V using Equation 4-1:

EQUATION 4-1:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right)$$

Where:

V_{REF} =	0.62V
R1 =	Top resistor
V_{OUT} =	Desired output voltage
R2 =	Bottom resistor

TABLE 4-1: FEEDBACK RESISTOR VALUES

V_{OUT}	R1	R2
1.2V	274 kΩ	294 kΩ
1.5V	316 kΩ	221 kΩ
1.8V	301 kΩ	158 kΩ
2.5V	324 kΩ	107 kΩ
3.3V	309 kΩ	71.5 kΩ

5.0 APPLICATION INFORMATION

The MIC23450 is a triple high performance DC-to-DC step down regulator offering a small solution size. Supporting 3 outputs with currents up to 2A inside a 5 mm x 5 mm QFN package, the IC requires only five external components per channel while meeting today's miniature portable electronic device needs. Using the HyperLight Load switching scheme, the MIC23450 is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. The following sections provide additional device application information.

5.1 Input Capacitor

A 2.2 µF ceramic capacitor or greater should be placed close to the PVIN pin for each channel and it's corresponding PGND pin for bypassing. For example, Murata GRM188R60J475ME84D, size 0603, 4.7 µF ceramic capacitor is ideal, based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

5.2 Output Capacitor

The MIC23450 is designed for use with a 2.2 µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the Murata GRM188R60J475ME84D, size 0603, 4.7 µF ceramic capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

5.3 Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23450 is designed for use with a 0.47 µH to 2.2 µH inductor. For faster transient response, a 0.47 µH inductor will yield the best result. On the other hand, a 2.2 µH inductor will yield lower output voltage ripple. For the best compromise of these, generally, a 1 µH is recommended.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as shown in Equation 5-1:

EQUATION 5-1:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT}\left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L}\right)\right]$$

Where:

I_{OUT} =	Output currrent
V_{OUT} =	Output voltage
V_{IN} =	Input voltage
f =	Switching frequency
L =	Inductor value

As shown in Equation 5-1, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations.

The transition between high loads (CCM) to HyperLight Load (HLL) mode is determined by the inductor ripple current and the load current as illustrated in Figure 5-1.

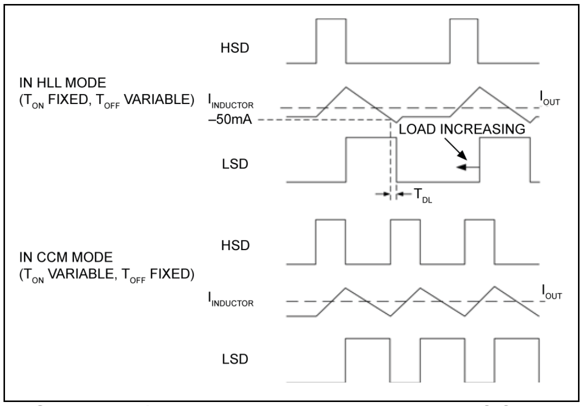


FIGURE 5-1: *Transition between CCM Mode and HLL Mode.*

Figure 5-1 shows the signals for high side switch drive (HSD) for T_{ON} control, the Inductor current and the low side switch drive (LSD) for T_{OFF} control.

In HLL mode, the inductor is charged with a fixed T_{ON} pulse on the high side switch (HSD). After this, the LSD is switched on and current falls at a rate V_{OUT}/L. The controller remains in HLL mode while the inductor falling current is detected to cross approximately –50 mA. When the LSD (or T_{OFF}) time reaches its minimum and the inductor falling current is no longer able to reach this –50mA threshold, the part is in CCM mode and switching at a virtually constant frequency.

Once in CCM mode, the T_{OFF} time will not vary. Therefore, it is important to note that if L is large enough, the HLL transition level will not be triggered.

That inductor is:

EQUATION 5-2:

$$L_{MAX} = \frac{V_{OUT} \times 135ns}{2 \times 50mA}$$

5.4 Compensation

The MIC23450 is designed to be stable with a 0.47 µH to 2.2 µH inductor with a 4.7 µF ceramic (X5R) output capacitor.

5.5 Duty Cycle

The typical maximum duty cycle of the MIC23450 is 80%.

5.6 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

EQUATION 5-3:

$$Efficiency = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET RDSON multiplied by the Switch Current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 3 MHz frequency and the switching transitions make up the switching losses.

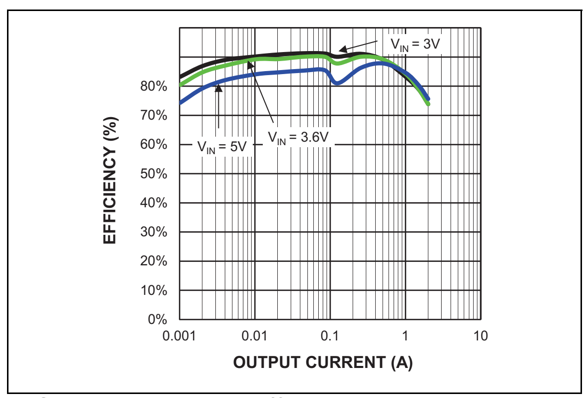


FIGURE 5-2: *Efficiency Under Load.*

The figure above shows an efficiency curve. From no load to 100 mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load mode, the MIC23450 is able to maintain high efficiency at low output currents.

Over 100 mA, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, thereby reducing the internal $R_{DS(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations.

As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

EQUATION 5-4:

$$P_{DCR} = I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

EQUATION 5-5:

$$Eff_{Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

5.7 Thermal Considerations

As most applications will not require 2A continuous current from all outputs at all times, it is useful to know what the thermal limits will be for various loading profiles.

The allowable overall package dissipation is limited by the intrinsic thermal resistance of the package ($R\theta_{(J\text{-}C)}$) and the area of copper used to spread heat from the package case to the ambient surrounding temperature ($R\theta_{(C\text{-}A)}$). The composite of these two thermal resistances is ($R\theta_{(J\text{-}A)}$), which represents the package thermal resistance with at least 1 square inch of copper ground plane. From this figure, which for the MIC23450 is 30°C/W, we can calculate maximum internal power dissipation as shown in Equation 5-6:

EQUATION 5-6:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMB}}{R\theta_{(J-A)}}$$

Where:

T_{JMAX} =	Maximum junction temp (125°C)
T_{AMB} =	Ambient temperature
$R\theta_{(J\text{-}A)}$ =	30°C/W

As can be expected, the allowable dissipation tends towards zero as the ambient temperature increases towards the maximum operating junction temperature.

The graph of PD_{MAX} vs. Ambient temperature could be drawn quite simply using this equation. However, a more useful measure is the maximum output current per regulator vs. ambient temperature. For this, we must first create an ‘exchange rate’ between power dissipation per regulator (P_{DISS}) and its output current (I_{OUT}).

An accurate measure of this function can utilize the efficiency curve, as illustrated in Equation 5-7 and Equation 5-8:

EQUATION 5-7:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

EQUATION 5-8:

$$P_{LOSS} = \frac{P_{OUT}(1 - \eta)}{\eta}$$

Where:

η =	Efficiency
P_{OUT} =	I_{OUT} x V_{OUT}

To arrive at the internal package dissipation P_{DISS}, one would need to remove the inductor loss P_{DCR} which is not dissipated within the package. This however, does not give a worst case figure, since efficiency is typically measured on a nominal part at nominal temperatures. The I_{OUT} to P_{DISS} function we use therefore is a synthesized P_{DISS} which accounts for worst case values at maximum operating temperature, as shown in Equation 5-9:

EQUATION 5-9:

$$P_{DISS} = I_{OUT}^{2}\left(R_{DSON\_P} \times \frac{V_{OUT}}{V_{IN}} + R_{DSON\_N}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right)$$

Where:

R_{DSON_P} =	Maximum $R_{DS(ON)}$ of the high side, P-Channel switch at T_{JMAX}
R_{DSON_N} =	Maximum $R_{DS(ON)}$ of the low side, N-Channel switch at T_{JMAX}
V_{OUT} =	Output voltage
V_{IN} =	Input voltage

Since ripple current and switching losses are small with respect to resistive losses at maximum output current, they can be considered negligible for the purpose of this method, but could be included if required.

Now we have a function describing P_{DISS} in terms of I_{OUT}, we can substitute P_{DISS} with Equation 5-6 to form the function of maximum output current $I_{OUT(MAX)}$ vs. ambient temperature T_{AMB} (Equation 5-10):

EQUATION 5-10:

$$I_{OUTMAX} = \sqrt{\frac{\frac{T_{JMAX} - T_{AMB}}{R\theta_{(J-A)}}}{R_{DSON\_P} \times \frac{V_{OUT}}{V_{IN}} + \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}}$$

The curves shown in the characteristic curves section are plots of this function adjusted to account for 1, 2 or 3 regulators running simultaneously.

5.8 HyperLight Load Mode

Each regulator in the MIC23450 uses a minimum on and off time proprietary control loop (patented by Microchip). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23450 works in pulse-frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus provides more energy to the output. This switching scheme improves the efficiency of MIC23450 during light load currents by only switching when it is needed. As the load current increases, the MIC23450 goes into continuous conduction mode (CCM) and switches at a frequency centered at 3MHz. The equation to calculate the load when the MIC23450 goes into continuous conduction mode may be approximated in Equation 5-11:

EQUATION 5-11:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f}\right)$$

Where:

V_{IN} =	Input voltage
V_{OUT} =	Output voltage
D =	Duty cycle
f =	Switching frequency
L =	Inductor value

As shown in Equation 5-11, the load at which the MIC23450 transitions from HyperLight Load mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). As shown in Figure 5-3, as the Output Current increases, the switching frequency also increases until the MIC23450 goes from HyperLight Load mode to PWM mode at approximately 120 mA. The MIC23450 will switch at a relatively constant frequency around 3 MHz once the output current is over 120 mA.

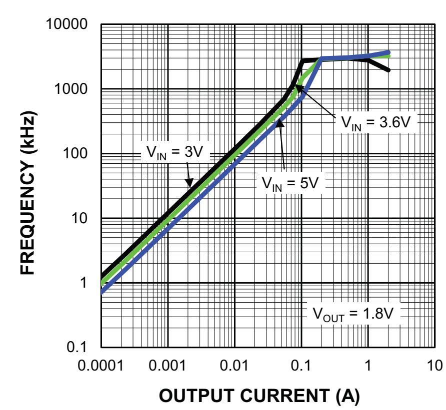


FIGURE 5-3: *Switching Frequency vs. Load Current.*

5.9 Multiple Sources

The MIC23450 provides all the pins necessary to operate the three regulators from independent sources. This can be useful in partitioning power within a multi rail system. For example, it is possible that within a system, two supplies are available; 3.3V and 5V. The MIC23450 can be connected to use the 3.3V supply to provide two, low voltage outputs (e.g. 1.2V and 1.8V) and use the 5V rail to provide a higher output (e.g. 2.5V), resulting in the power blocks shown in Figure 5-4.

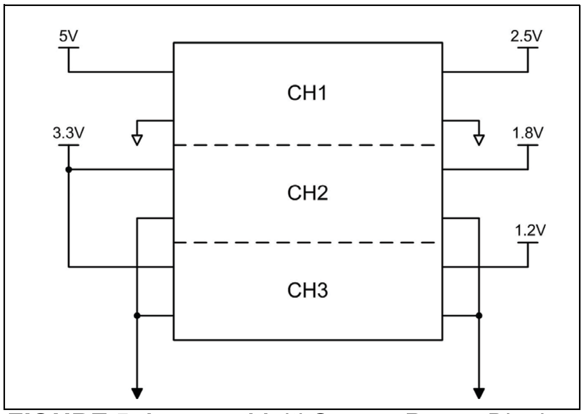
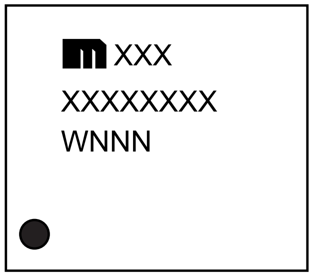


FIGURE 5-4: *Multi-Source Power Block Diagram.*

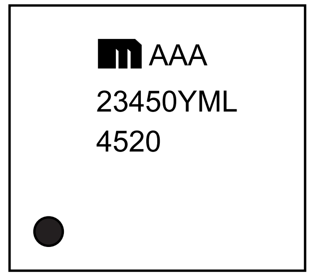
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

32-Lead QFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

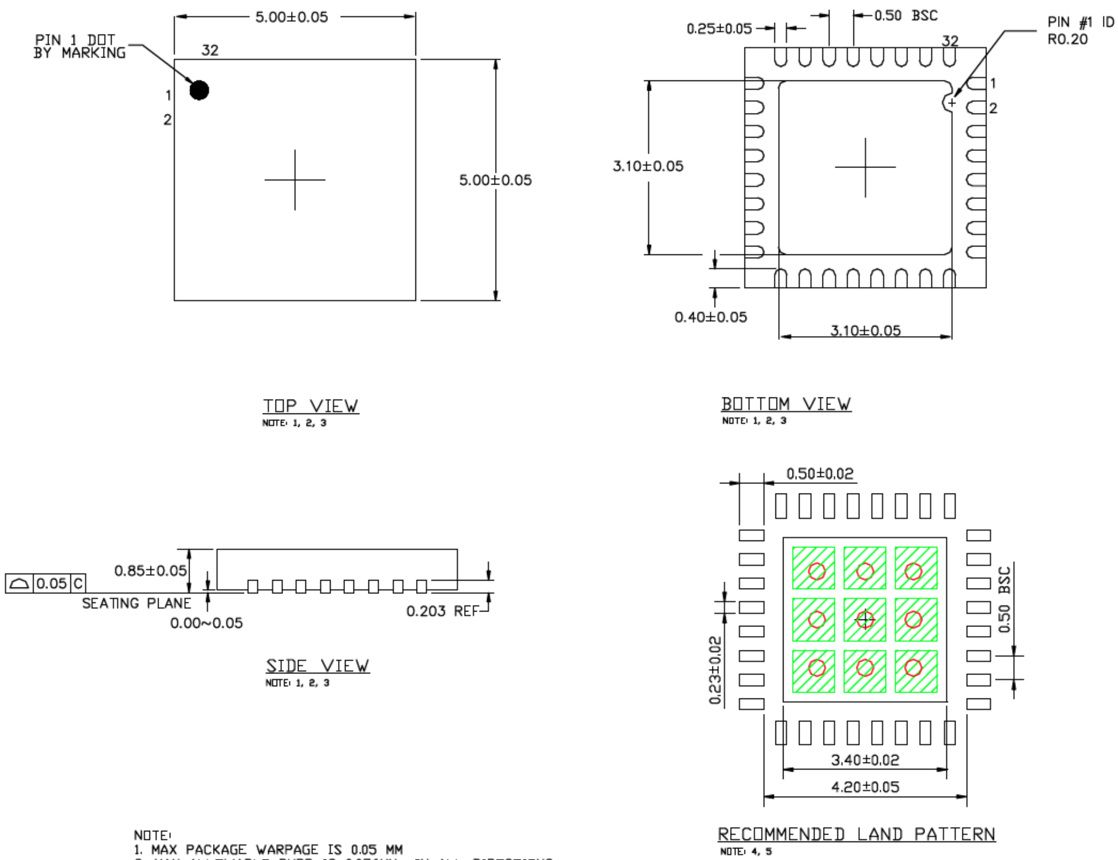
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

32-Lead QFN 5 mm x 5 mm Package Outline and Recommended Land Pattern

TITLE
32 LEAD QFN 5x5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN55-32LD-PL-1	**UNIT**	MM



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (January 2021)

- Converted Micrel document MIC23450 to Microchip data sheet DS20006479A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device: MIC23450: 3 MHz, PWM, 2A Triple Buck Regulator with HyperLight Load and Power Good

Junction Temperature Range: Y = –40°C to +125°C, RoHS-Compliant

Package: ML = 32-Lead 5 mm x 5 mm QFN

Media Type:
T5 = 500/Reel
TR = 1,000/Reel

Examples:

a) MIC23450AAAYML-T5: MIC23450, –40°C to +125°C Temperature Range, 32-Lead QFN, 500/Reel

b) MIC23450AAAYML-TR: MIC23450, –40°C to +125°C Temperature Range, 20-Lead QFN, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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02/28/20