G2R120MT33J
3300 V 120 mΩ SiC MOSFET

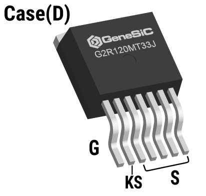
Silicon Carbide MOSFET
N-Channel Enhancement Mode

V_{DS} = 3300 V
$R_{DS(ON)(Typ.)}$ = 120 mΩ
$I_{D(T_C = 100°C)}$ = 24 A

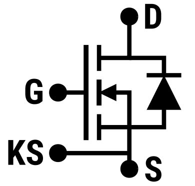
Features

- G2R™ Technology with +20 V Gate Drive
- Superior Q_G x $R_{DS(ON)}$ Figure of Merit
- Superior Cost-Performance Index
- Low Capacitances and Low Gate Charge
- Fast and Reliable Body Diode
- Low Losses at All Temperatures
- Optimized Package with Separate Driver Source Pin

Package



TO-263-7



D = Drain
G = Gate
S = Source
KS = Kelvin Source

Advantages

- Compatible with Commercial Gate Drivers
- Increased Power Density for Compact System
- High Frequency Switching
- Improved Thermal Capability
- Ease of Paralleing without Thermal Runaway

Applications

- Solar String Inverters
- EV- Fast Chargers
- Pulsed Power
- Switched Mode Power Supply
- Energy Storage
- Solid State Transformers
- Solid State Circuit Breakers

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	3300	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +25	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +20	V	
Continuous Forward Current	I_D	T_C = 25°C, V_{GS} = -5 / +20 V	34	A	Fig. 15
		T_C = 100°C, V_{GS} = -5 / +20 V	24		
		T_C = 135°C, V_{GS} = -5 / +20 V	17		
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \leq$ 3µs, D ≤ 1%, V_{GS} = 20 V, Note 1	100	A	Fig. 14
Power Dissipation	P_D	T_C = 25°C	366	W	Fig. 16
Non-Repetitive Avalanche Energy	E_{AS}	L = 34.0 mH, I_{AS} = 7.5 A	955	mJ	
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Case	R_{thJC}			0.34	0.41	°C/W	Fig. 13
Weight	W_T			1.45		g	

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

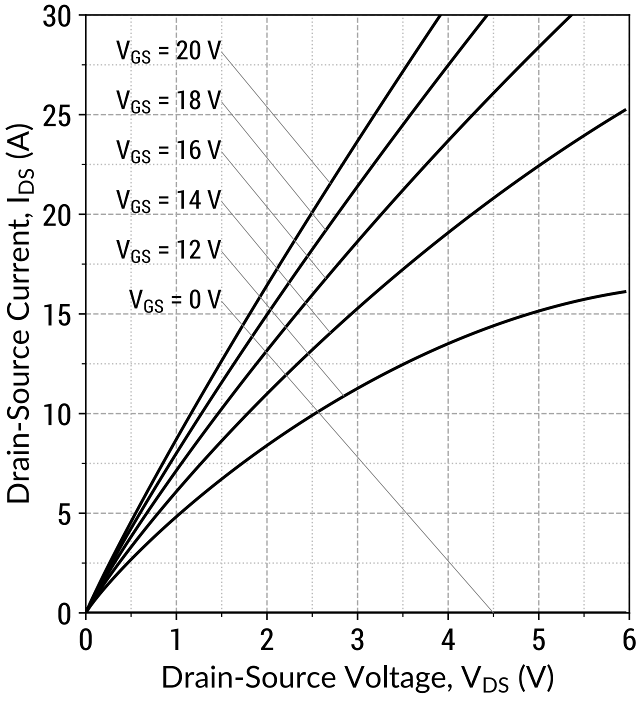
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	3300			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 3300 V, V_{GS} = 0 V		1		µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 25 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 4.0 mA V_{DS} = V_{GS}, I_D = 4.0 mA, T_j = 175°C	2.5	4.50 3.40		V	Fig. 9
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 15 A V_{DS} = 10 V, I_D = 15 A, T_j = 175°C		5.8 6.3		S	Fig. 4
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 20 V, I_D = 15 A V_{GS} = 20 V, I_D = 15 A, T_j = 175°C		120 246	156	mΩ	Fig. 5-8
Input Capacitance	C_{iss}	V_{DS} = 1000 V, V_{GS} = 0 V f = 1 MHz, V_{AC} = 25mV		3099		pF	Fig. 11
Output Capacitance	C_{oss}			55			
Reverse Transfer Capacitance	C_{rss}			5.2			
C_{oss} Stored Energy	E_{oss}			36		µJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}			108		nC	
Gate-Source Charge	Q_{gs}	V_{DS} = 1000 V, V_{GS} = -5 / +20 V I_D = 15 A Per IEC607478-4		41		nC	Fig. 10
Gate-Drain Charge	Q_{gd}			43			
Total Gate Charge	Q_g			130			
Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V_{AC} = 25 mV		1.3		Ω	
Turn-On Switching Energy (Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+20V, $R_{G(ext)}$ = 10 Ω, L = 220.0 µH, I_D = 15 A, V_{DD} = 1700 V		501		µJ	Fig. 22
Turn-Off Switching Energy (Body Diode)	E_{Off}			168			
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1700 V, V_{GS} = -5/+20V $R_{G(ext)}$ = 10 Ω, L = 220.0 µH, I_D = 15 A Timing relative to V_{DS}, Inductive load		96		ns	Fig. 24
Rise Time	t_r			26			
Turn-Off Delay Time	$t_{d(off)}$			35			
Fall Time	t_f			16			

Reverse Diode Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 7 A V_{GS} = -5 V, I_{SD} = 7 A, T_j = 175°C		4.0 3.4		V	Fig. 17-18
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 100°C	29			A	
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V, Note 1		116		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 15 A, V_R = 1700 V dif/dt = 500 A/µs, T_j = 25°C		72		ns	
Reverse Recovery Charge	Q_{rr}			340		nC	
Peak Reverse Recovery Current	I_{rrm}			8		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 15 A, V_R = 1700 V dif/dt = 500 A/µs, T_j = 175°C		95		ns	
Reverse Recovery Charge	Q_{rr}			1305		nC	
Peak Reverse Recovery Current	I_{rrm}			18		A	

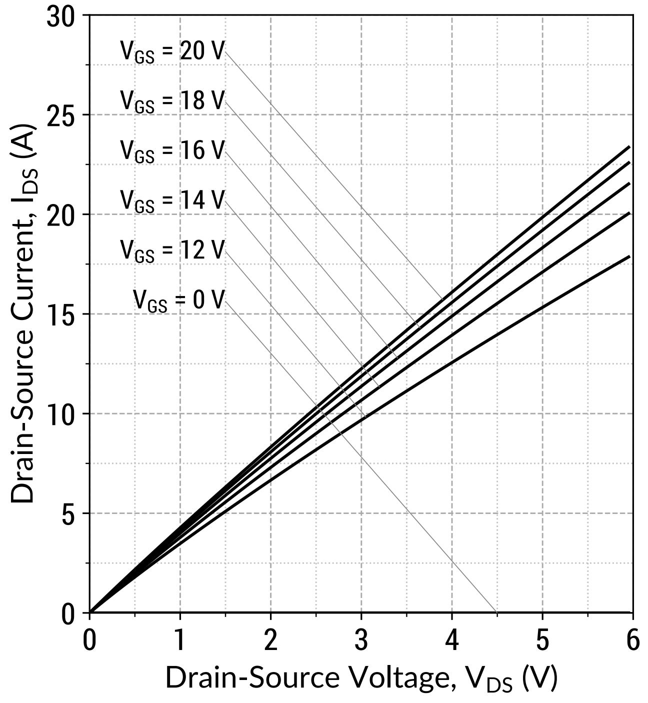
**The chip technology was characterized up to 200 V/ns. The measured dV/dt was limited by measurement test setup and package.*

Figure 1: Output Characteristics (T_j = 25°C)



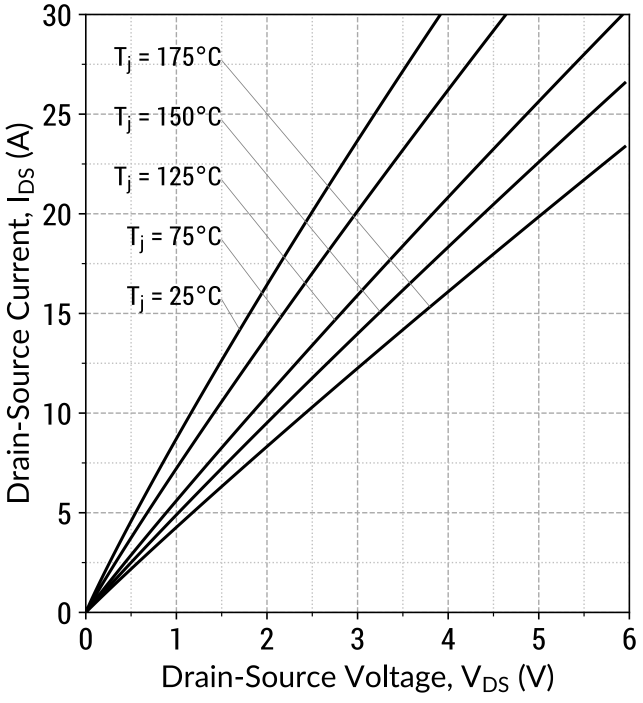
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 2: Output Characteristics (T_j = 175°C)



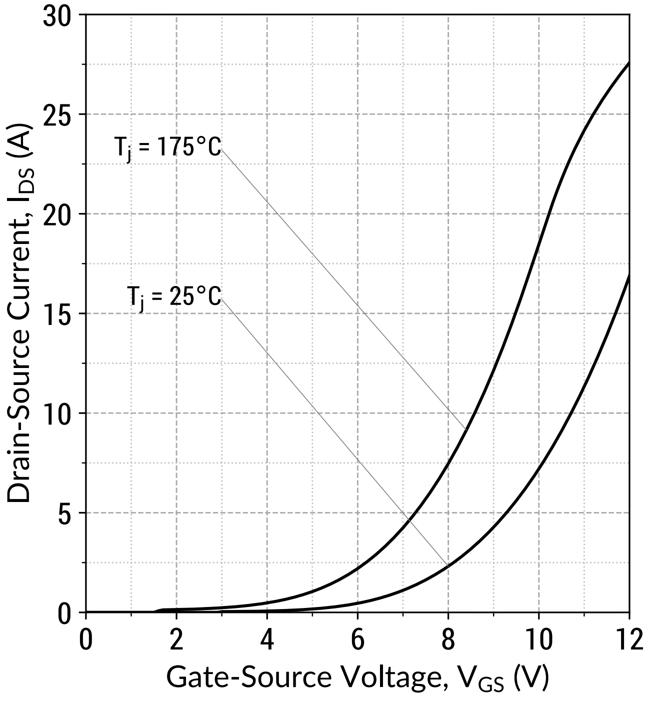
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 3: Output Characteristics (V_{GS} = 20 V)



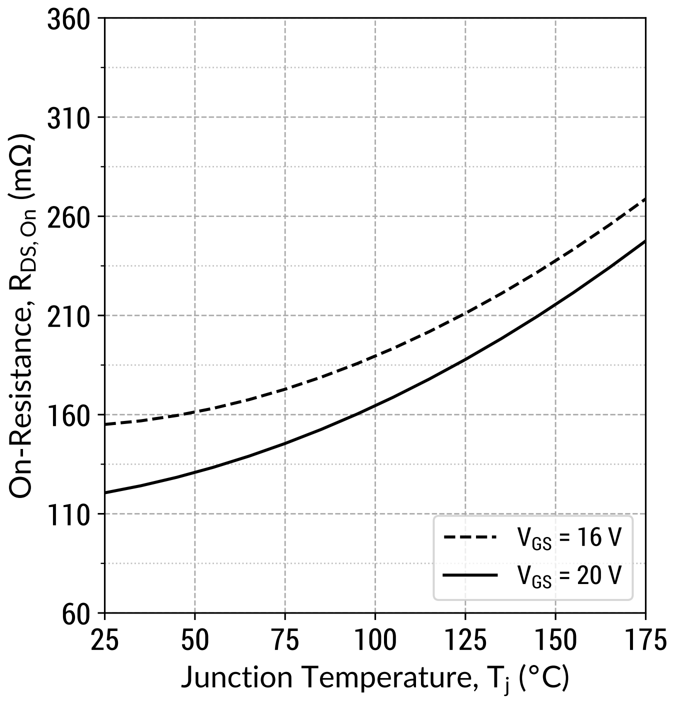
$I_D = f(V_{DS}, T_j)$; t_P = 250 µs

Figure 4: Transfer Characteristics (V_{DS} = 10 V)



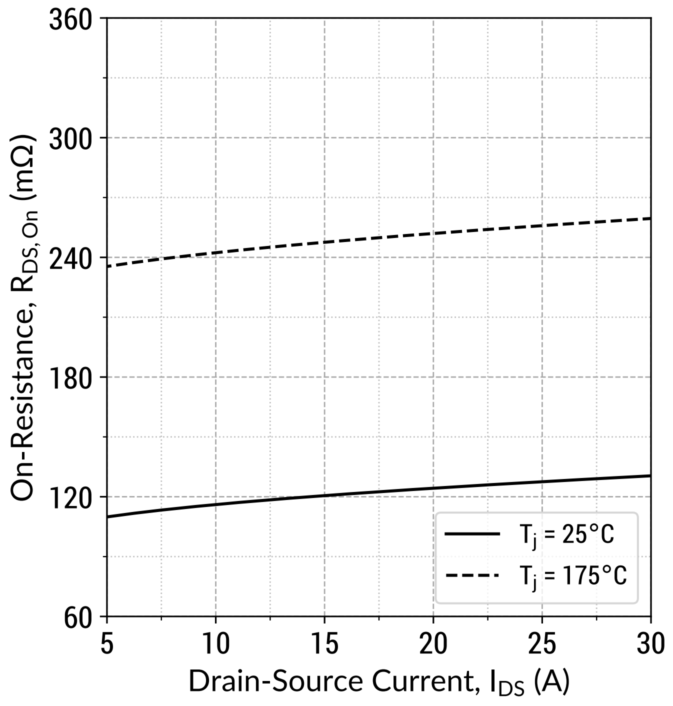
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Figure 5: On-State Resistance v/s Temperature



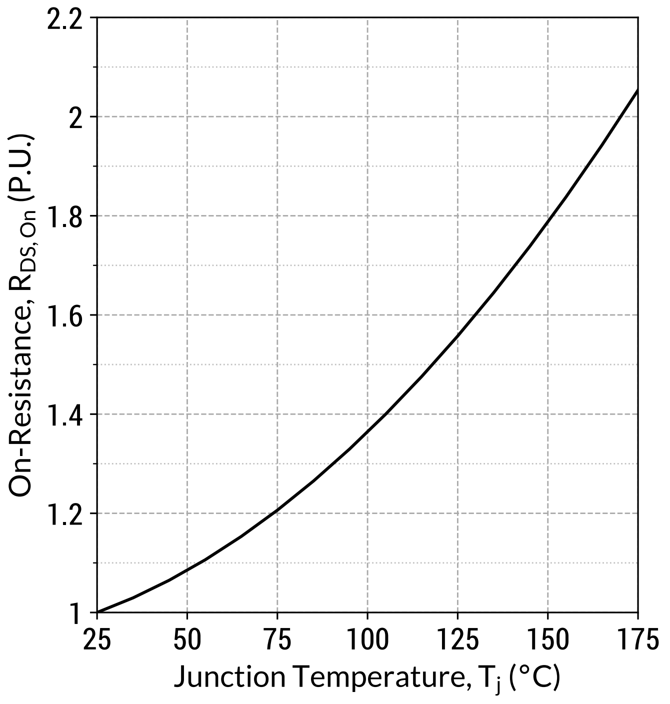
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 15 A

Figure 6: On-State Resistance v/s Drain Current



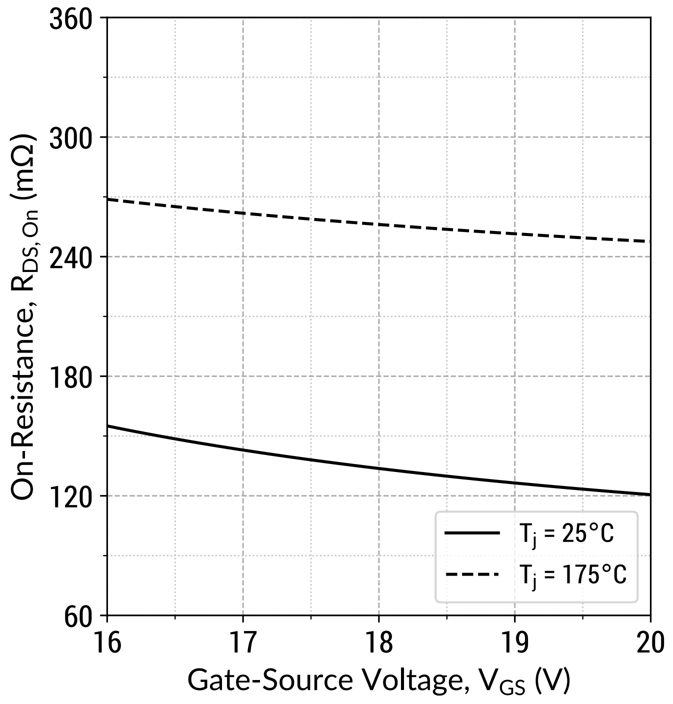
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 250 µs; V_{GS} = 20 V

Figure 7: Normalized On-State Resistance v/s Temperature



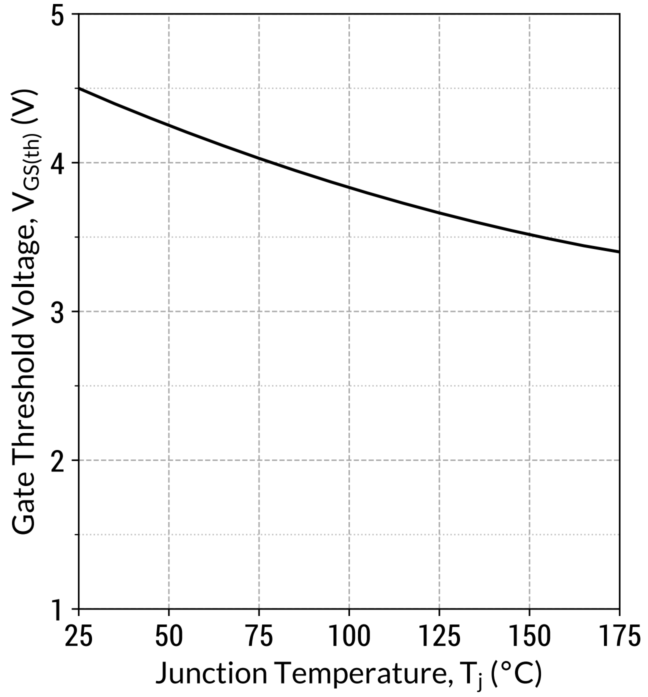
$R_{DS(ON)} = f(T_j)$; t_P = 250 µs; I_D = 15 A; V_{GS} = 20 V

Figure 8: On-State Resistance v/s Gate Voltage



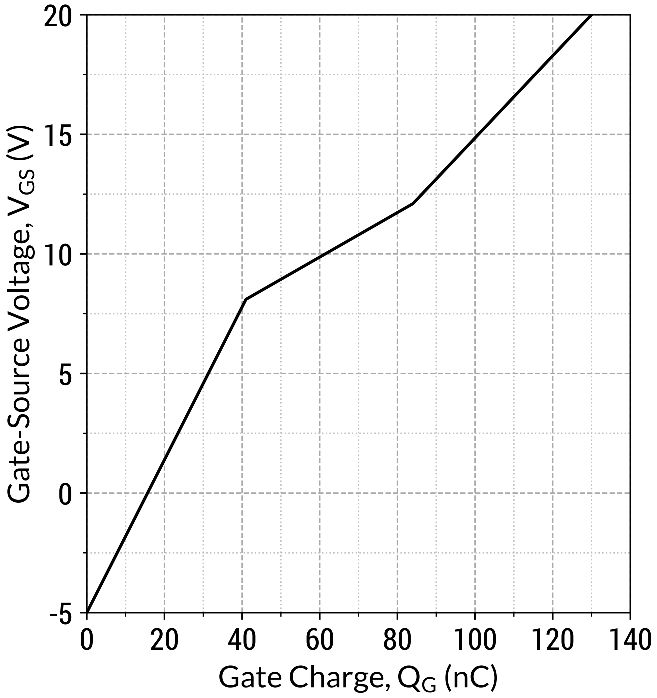
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 15 A

Figure 9: Threshold Voltage Characteristics



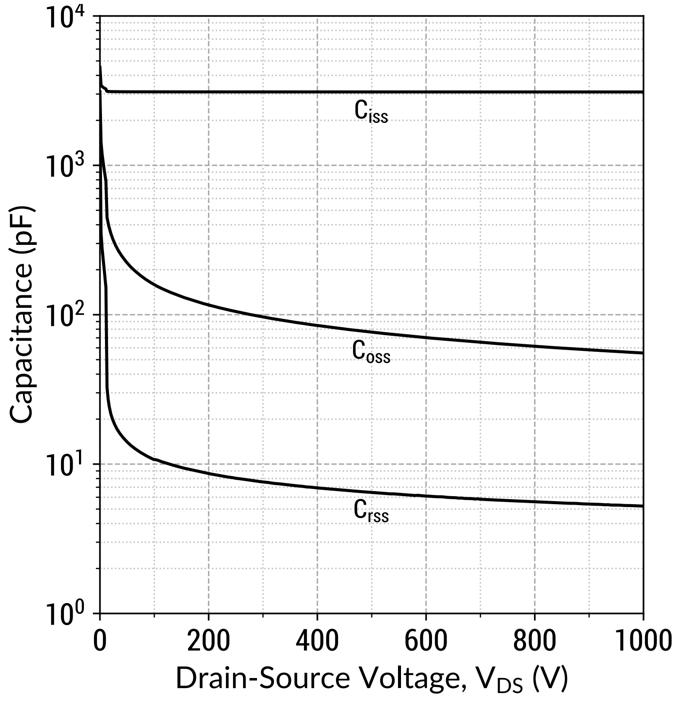
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; I_D = 4.0 mA

Figure 10: Gate Charge Characteristics



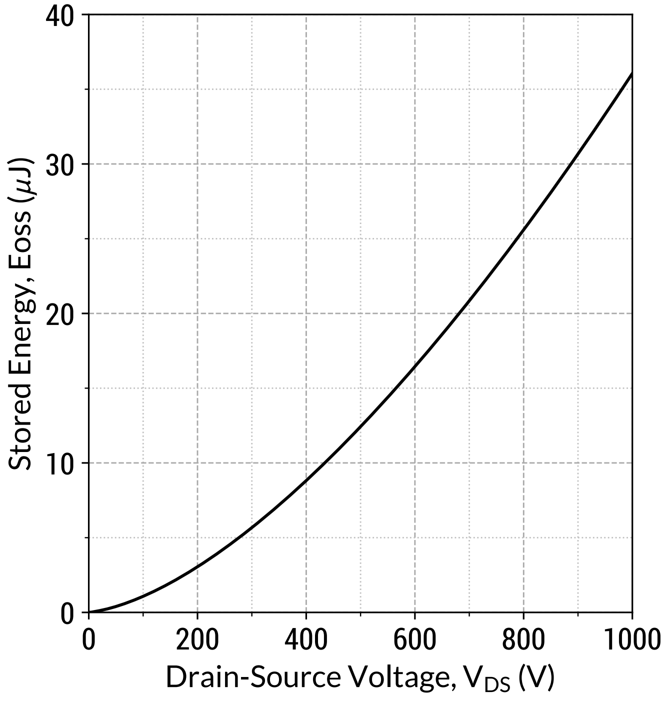
I_D = 15 A; V_{DS} = 1000 V; T_c = 25°C

Figure 11: Capacitance v/s Drain-Source Voltage



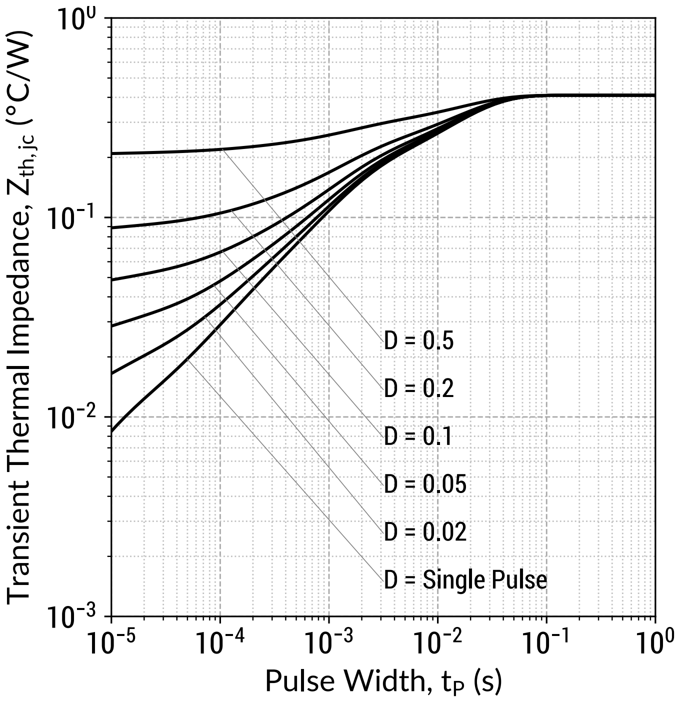
f = 1 MHz; V_{AC} = 25mV

Figure 12: Output Capacitor Stored Energy



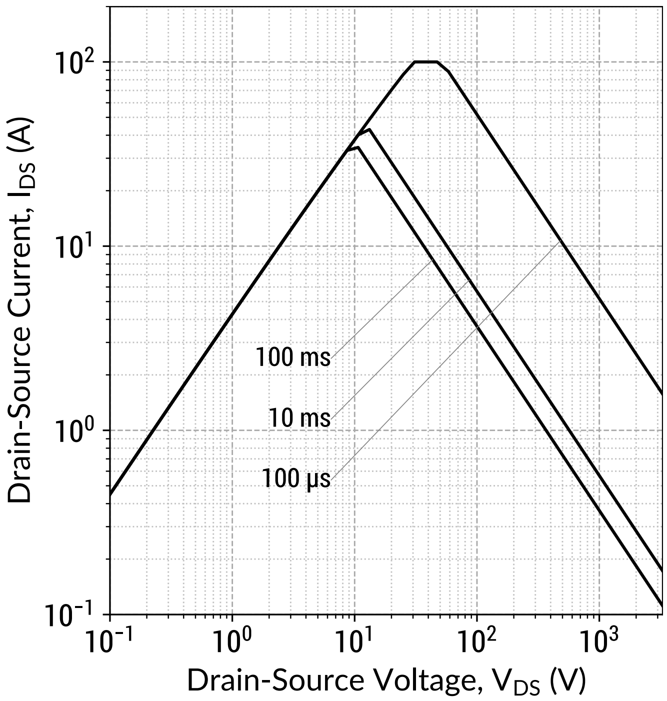
$E_{oss} = f(V_{DS})$

Figure 13: Transient Thermal Impedance



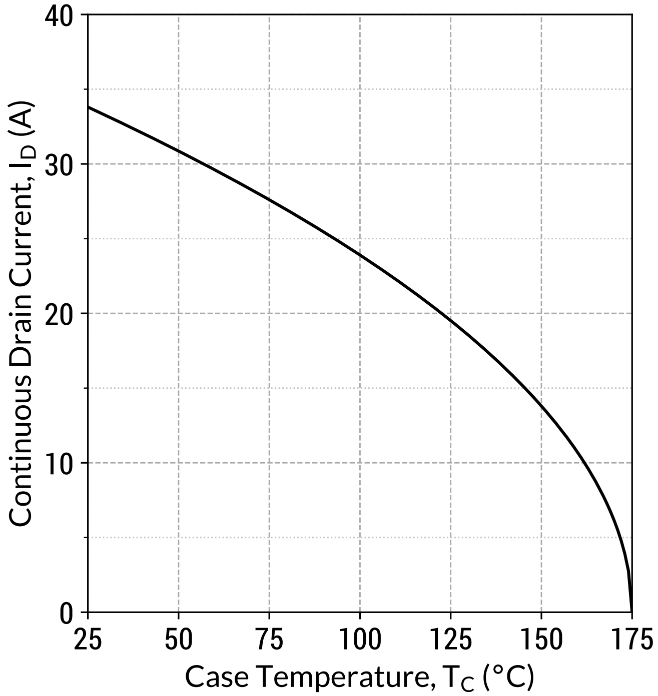
$Z_{th,jc} = f(t_P, D)$; $D = t_P/T$

Figure 14: Safe Operating Area (T_c = 25°C)



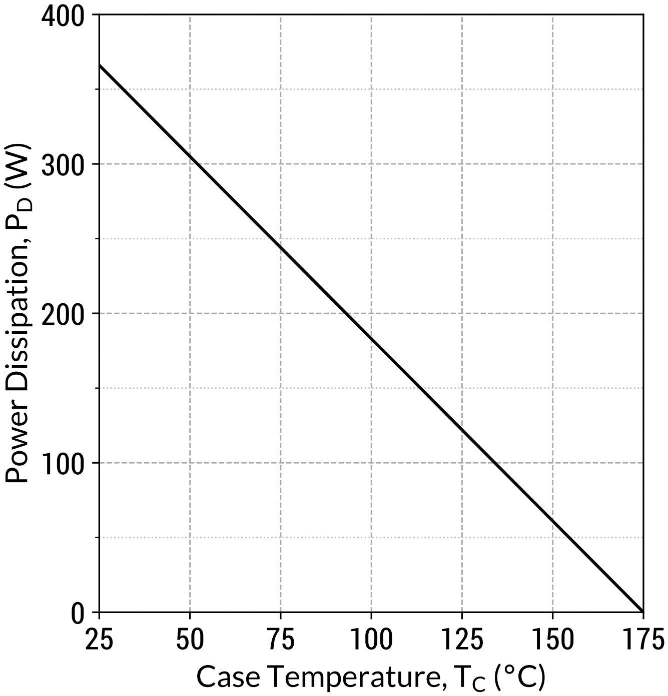
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175$°C; D = 0

Figure 15: Current De-rating Curve



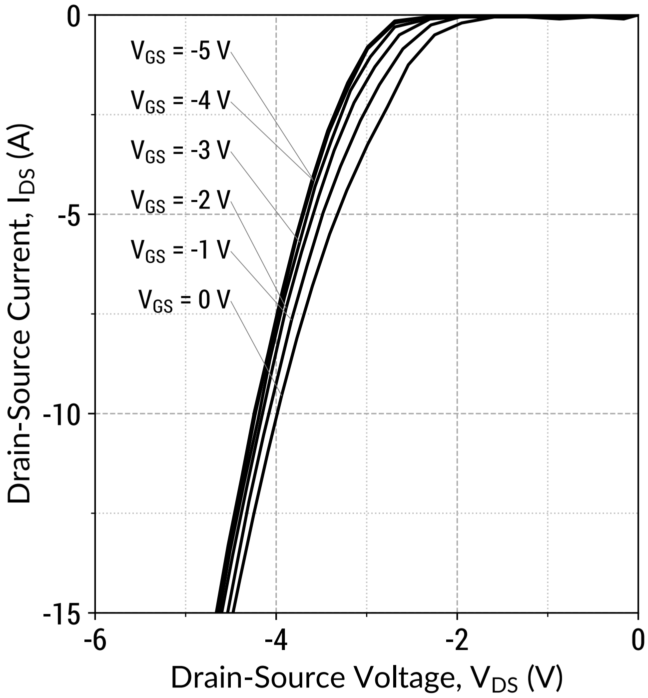
$I_D = f(T_C)$; $T_j \leq 175$°C

Figure 16: Power De-rating Curve



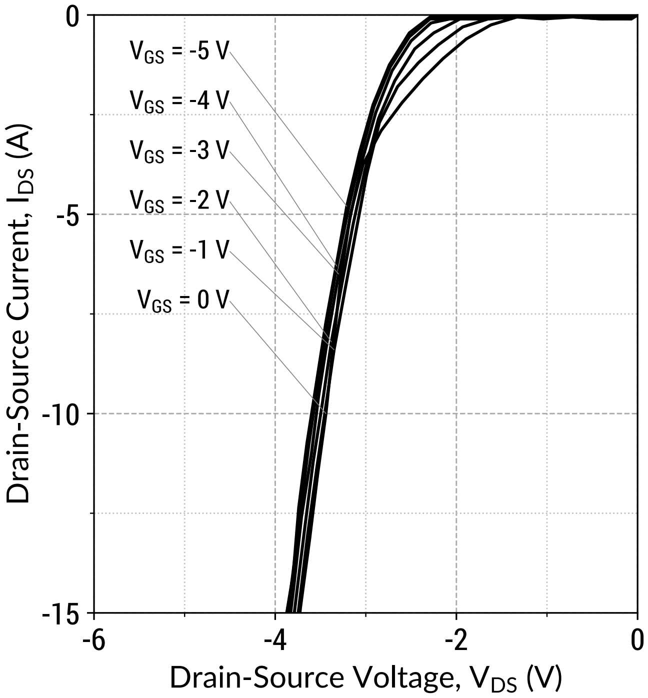
$P_D = f(T_C)$; $T_j \leq 175$°C

Figure 17: Body Diode Characteristics (T_j = 25°C)



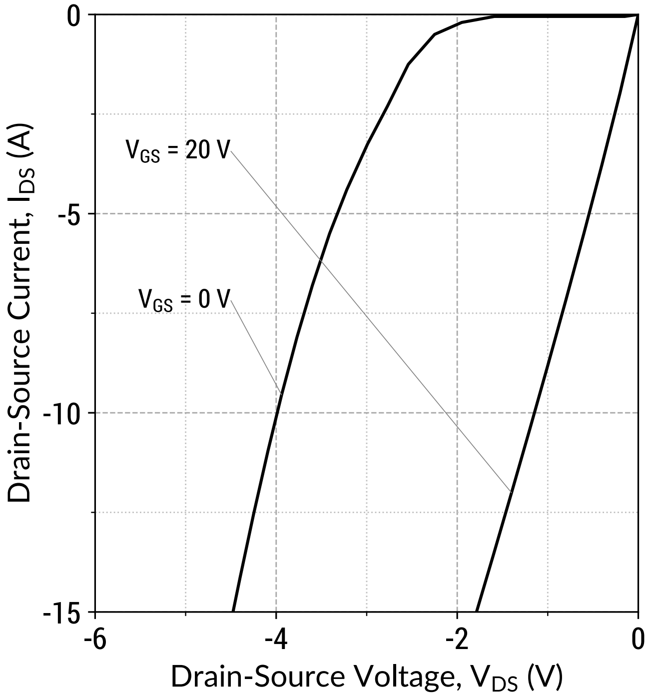
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 18: Body Diode Characteristics (T_j = 175°C)



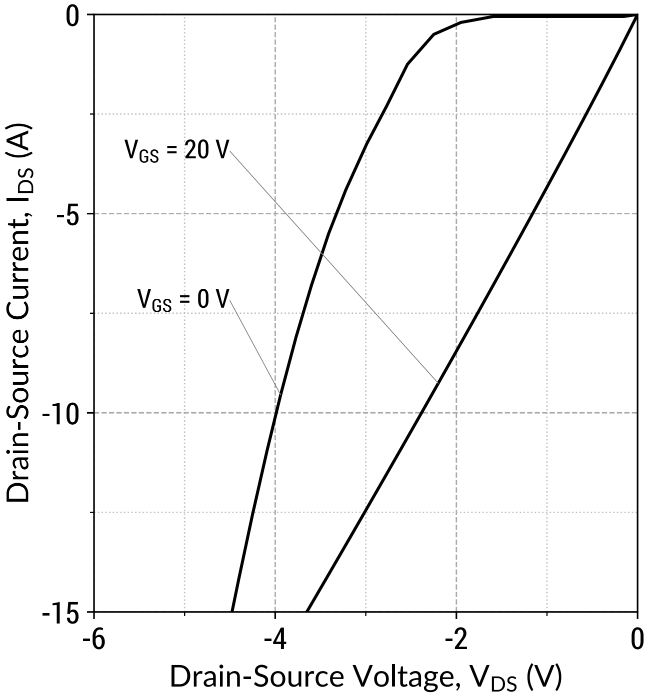
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 19: Third Quadrant Characteristics (T_j = 25°C)



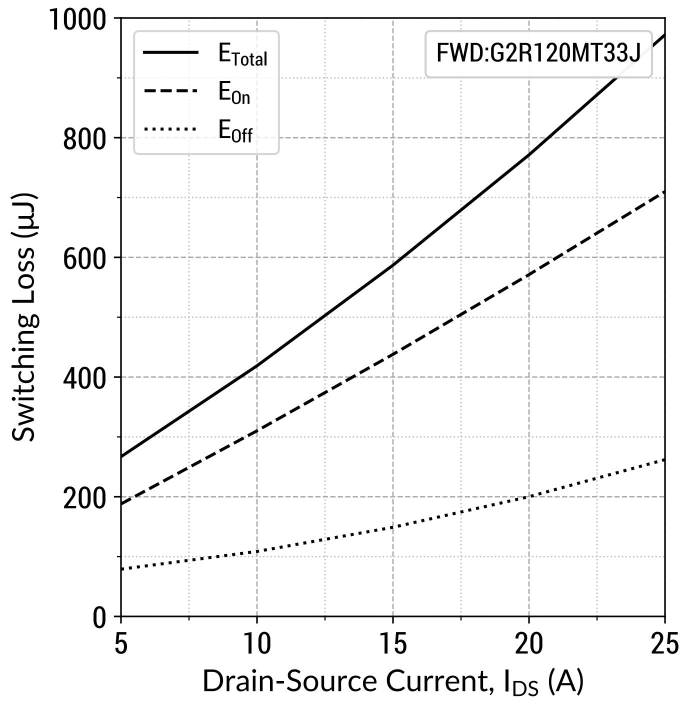
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 20: Third Quadrant Characteristics (T_j = 175°C)



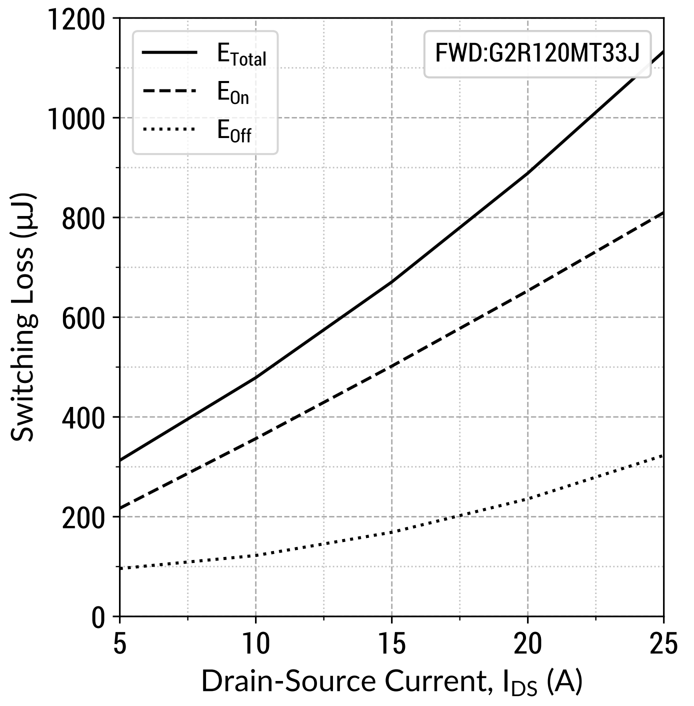
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 21: Inductive Switching Energy v/s Drain Current (V_{DD} = 1500V)



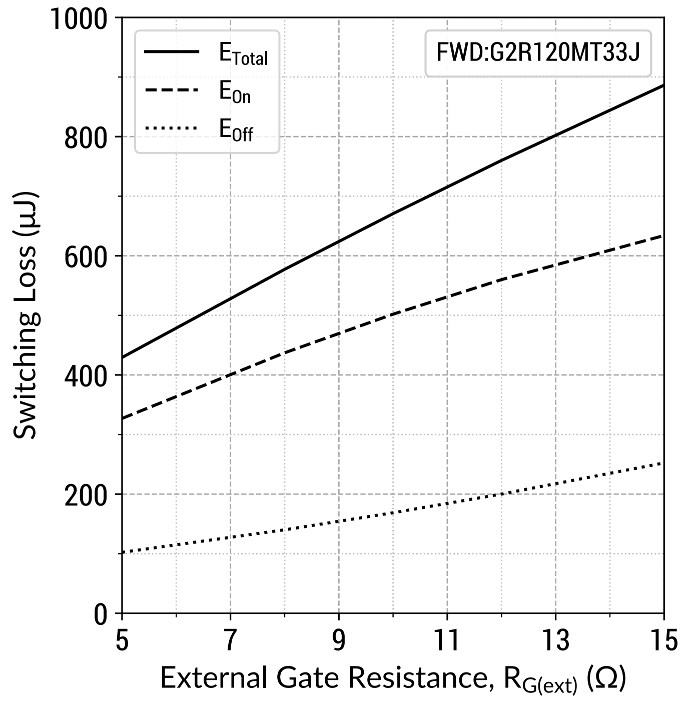
T_j = 25°C; V_{GS} = -5/+20V; $R_{G(ext)}$ = 10 Ω; L = 220.0μH

Figure 22: Inductive Switching Energy v/s Drain Current (V_{DD} = 1700V)



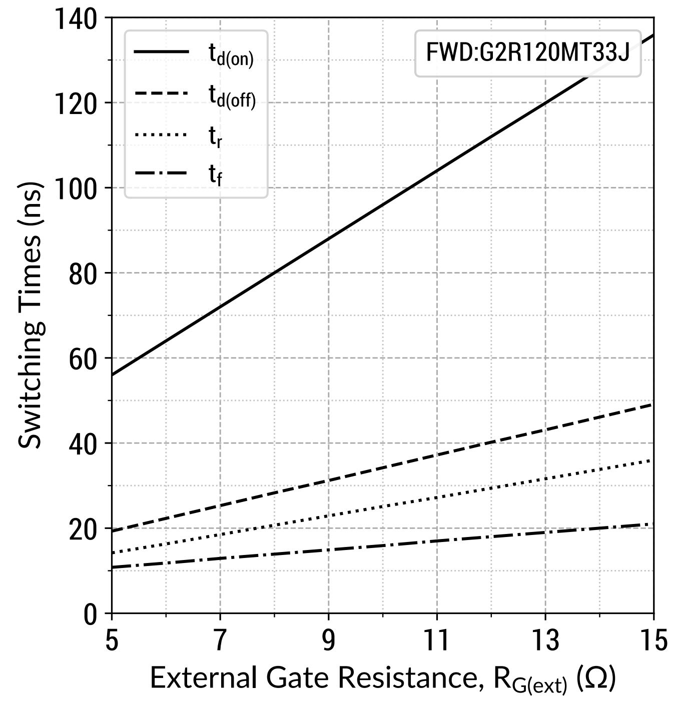
T_j = 25°C; V_{GS} = -5/+20V; $R_{G(ext)}$ = 10 Ω; L = 220.0μH

Figure 23: Inductive Switching Energy v/s $R_{G(ext)}$ (V_{DD} = 1700V)



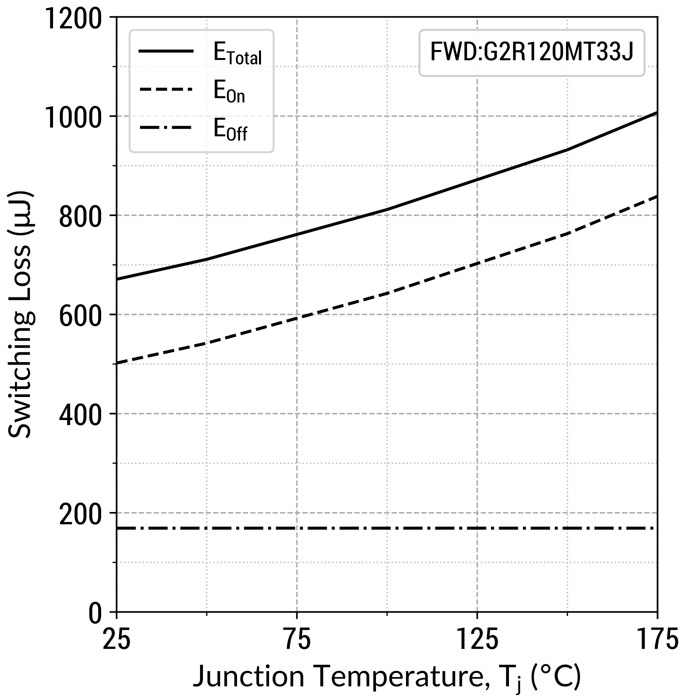
T_j = 25°C; V_{GS} = -5/+20V; I_{DS} = 15 A; L = 220.0μH

Figure 24: Switching Time v/s $R_{G(ext)}$ (V_{DD} = 1700V)



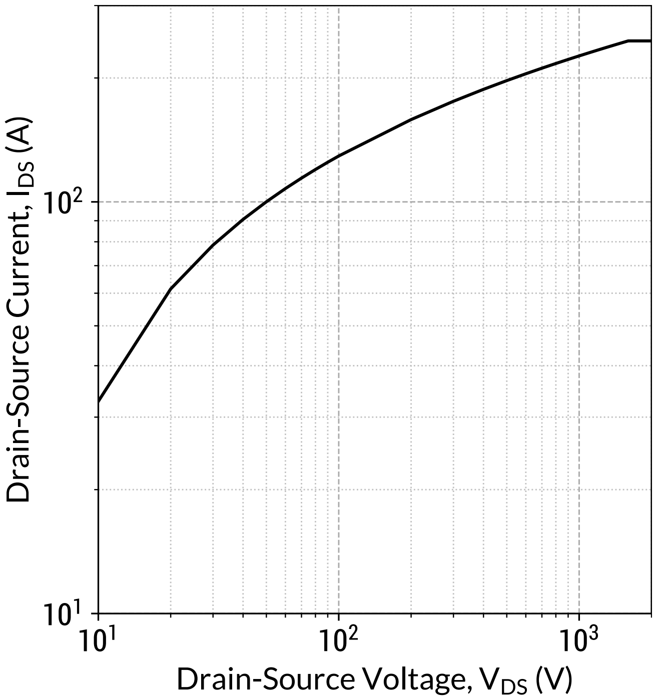
T_j = 25°C; V_{GS} = -5/+20V; I_{DS} = 15 A; L = 220.0μH

Figure 25: Inductive Switching Energy v/s Temperature (V_{DD} = 1700V)



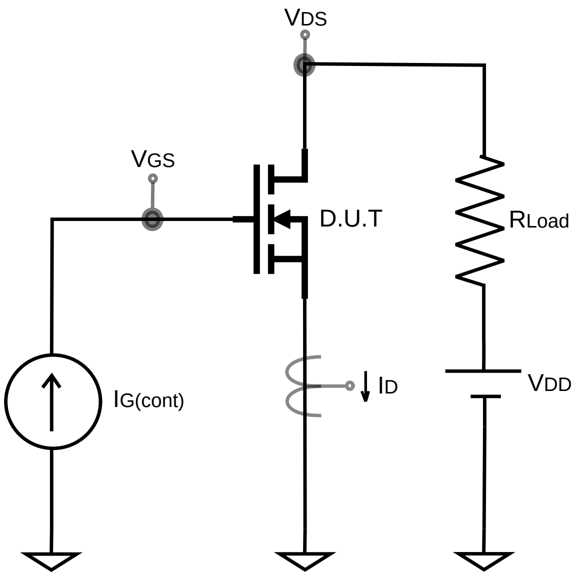
T_j = 25°C; V_{GS} = -5/+20V; $R_{G(ext)}$ = 10 Ω; I_{DS} = 15 A; L = 220.0μH

Figure 26: High Current IV

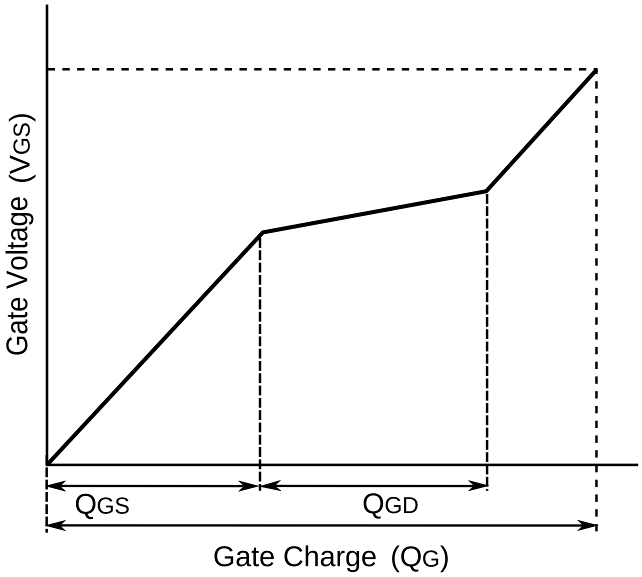


$I_D = f(V_{DS})$; $t_P \leq 3$ μs; V_{GS} = 20 V

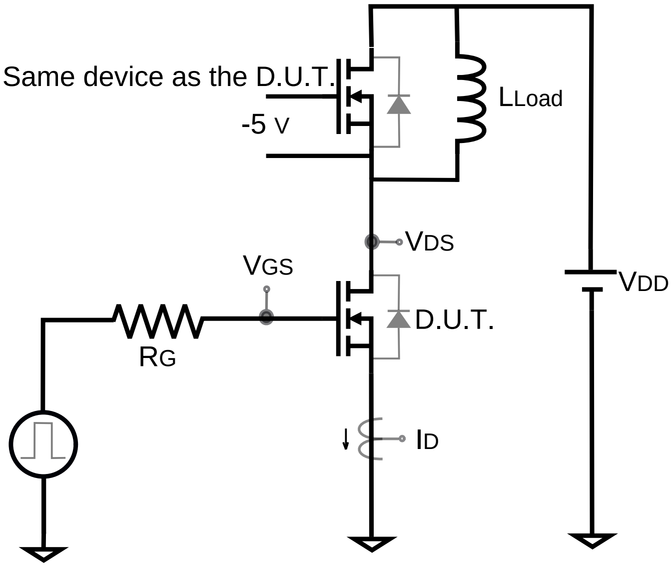
Gate Charge Circuit



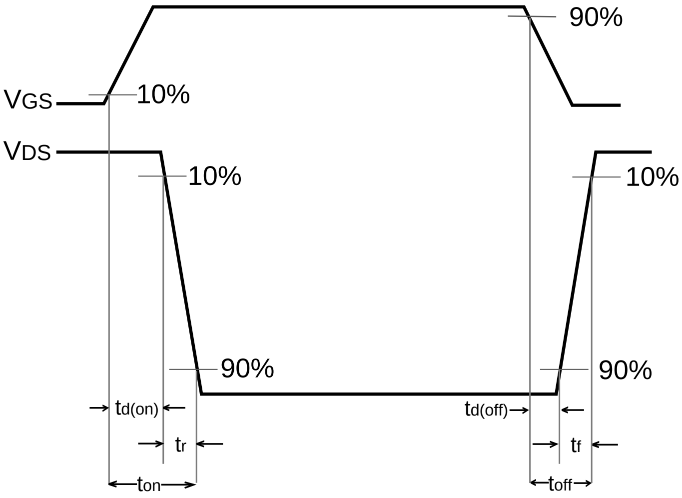
Gate Charge Waveform



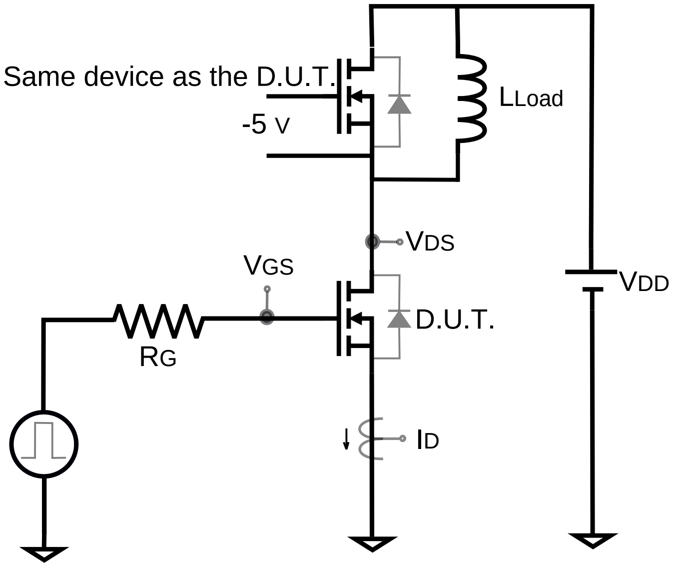
Switching Time Circuit



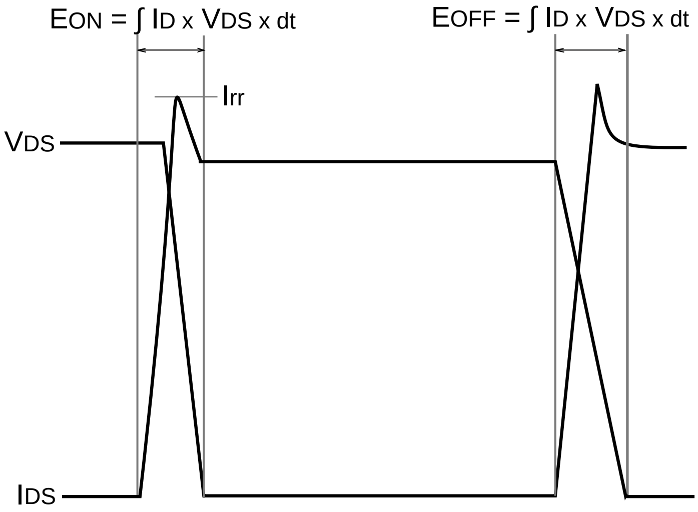
Switching Time Waveform



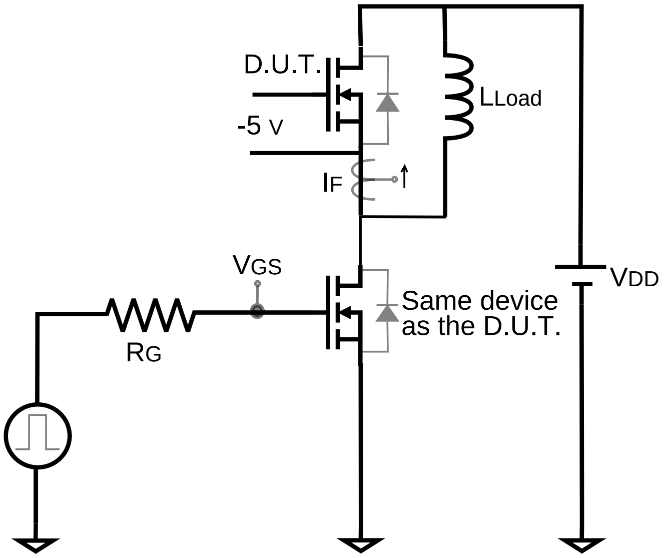
Switching Energy Circuit



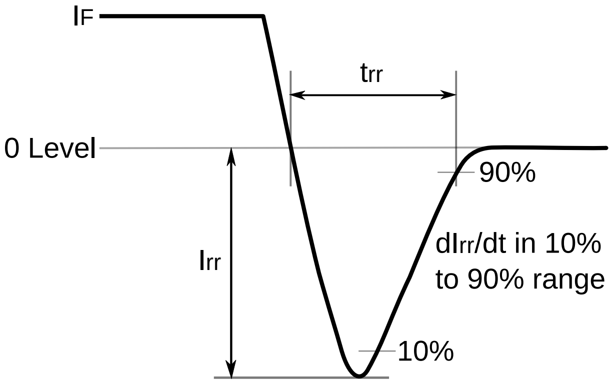
Switching Energy Waveform



Reverse Recovery Circuit

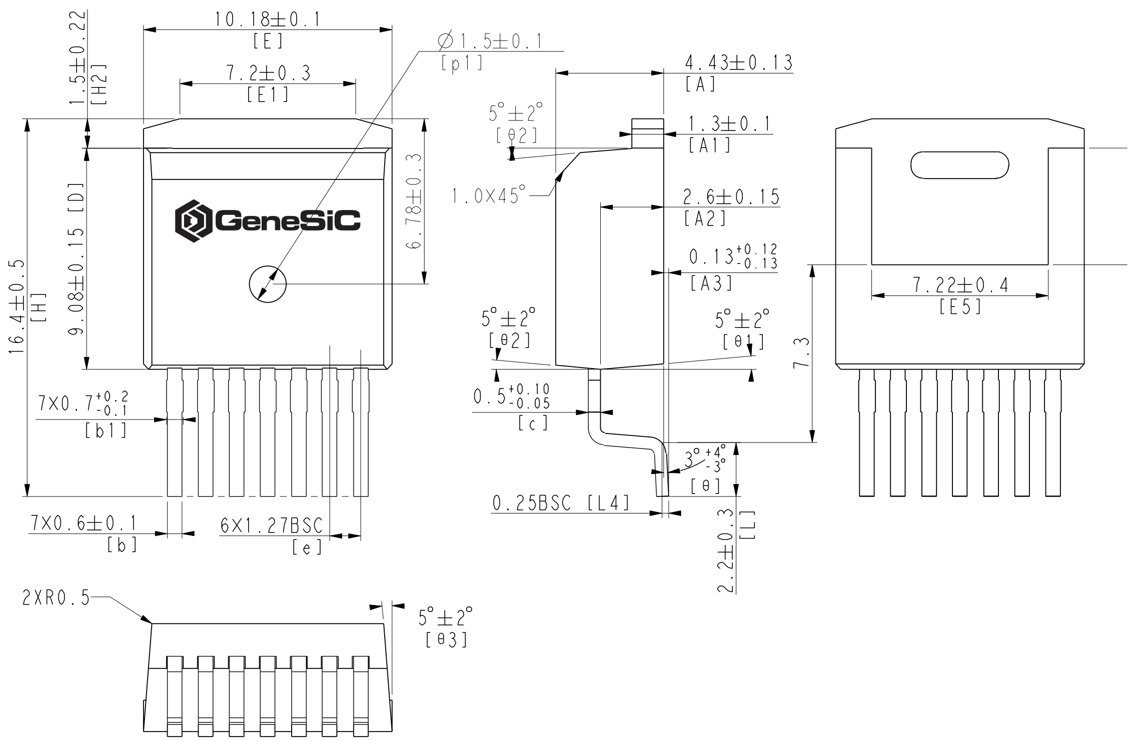


Reverse Recovery Waveform

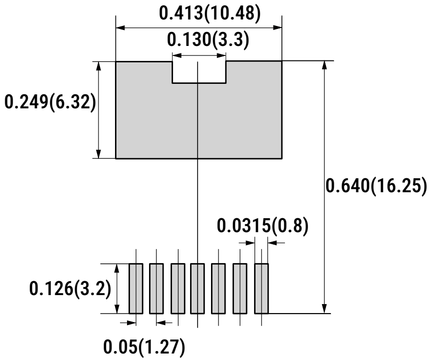


Package Dimensions

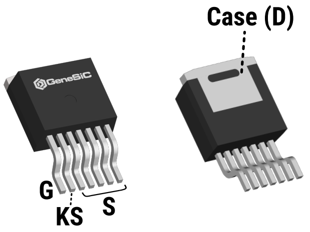
TO-263-7 Package Outline



Recommended Solder Pad Layout



Package View



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

Disclaimer

GeneSiC Semiconductor, Inc. reserves right to make changes to the product specifications and data in this document without notice. GeneSiC disclaims all and any warranty and liability arising out of use or application of any product. No license, express or implied to any intellectual property rights is granted by this document.

Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

Related Links

• SPICE Models:	https://www.genesicsemi.com/sic-mosfet/G2R120MT33J/G2R120MT33J_SPICE.zip
• PLECS Models:	https://www.genesicsemi.com/sic-mosfet/G2R120MT33J/G2R120MT33J_PLECS.zip
• CAD Models:	https://www.genesicsemi.com/sic-mosfet/G2R120MT33J/G2R120MT33J_3D.zip
• Gate Driver Reference:	https://www.genesicsemi.com/technical-support
• Evaluation Boards:	https://www.genesicsemi.com/technical-support
• Reliability:	https://www.genesicsemi.com/reliability
• Compliance:	https://www.genesicsemi.com/compliance
• Quality Manual:	https://www.genesicsemi.com/quality

Revision History

- Rev 21/Jan: Updated with most recent test data
- Supersedes: Rev 20/Nov

www.genesicsemi.com/sic-mosfet/

Published by GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155, Dulles, VA 20166; USA