HF920B

900V, Fixed-Frequency, EMI-Optimized Flyback Regulator with Ultra-Low Standby

DESCRIPTION

The HF920B is a flyback regulator with a monolithic, 900V MOSFET. The HF920B is an enhanced version of the HF920 with EMI optimization. It provides excellent power regulation with very few external components for AC/DC applications that require high reliability, such as smart meters, large appliances, industrial controls, and products powered by AC grids.

The HF920B uses peak current control mode to provide excellent transient response and easy loop compensation. When the output power falls below a given level, the regulator enters burst mode. The IC is also optimized to achieve very low power consumption during standby conditions.

MPS's proprietary, 900V, monolithic process enables over-temperature protection (OTP) on the same silicon as the 900V power MOSFET, offering the most precise thermal protection. The HF920B also offers a full suite of protection features, such as VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and short-circuit protection (SCP).

The HF920B is designed to minimize EMI for power line communications (PLC) in home and building automation applications. The operating frequency is programmed externally with a single resistor, so the power supply's radiated energy can block interference to the PLC. In addition to the programmable frequency, the HF920B employs frequency jittering that greatly reduces the noise level and EMI filter costs.

Frequency doubling mode can be enabled through a simple external set-up. With this special operation mode, the switching frequency is doubled when the converter runs into an over-power condition. In this way, the converter is able to handle up to a 50% decrease of the transformer inductance caused by external magnetizing interference.

The HF920B is available in SOIC8-7A and SOIC14-11 packages, and the maximum output power is listed in Table 1 respectively.

FEATURES

- Monolithic 900V/15Ω MOSFET and High-Voltage Current Source
- Programmable Switching Frequency, Up to 150kHz
- Current Mode Control Scheme
- Frequency Jittering
- Low Standby Power Consumption via Active Burst Mode
- <30mW No-Load Consumption
- Frequency Doubling Mode
- Internal Leading-Edge Blanking (LEB)
- Built-In Soft Start (SS)
- Internal Slope Compensation
- External Input PRO Pin Protection with Hysteresis and Auto-Restart Recovery
- Over-Temperature Protection (OTP)
- VCC Under-Voltage Lockout (UVLO) with Hysteresis
- Over-Voltage Protection (OVP) on VCC
- Time-Based Overload Protection (OLP)
- Short-Circuit Protection (SCP)
- Available in SOIC8-7A and SOIC14-11 Packages

APPLICATIONS

- E-Meters
- Industrial Controls
- Large Appliances

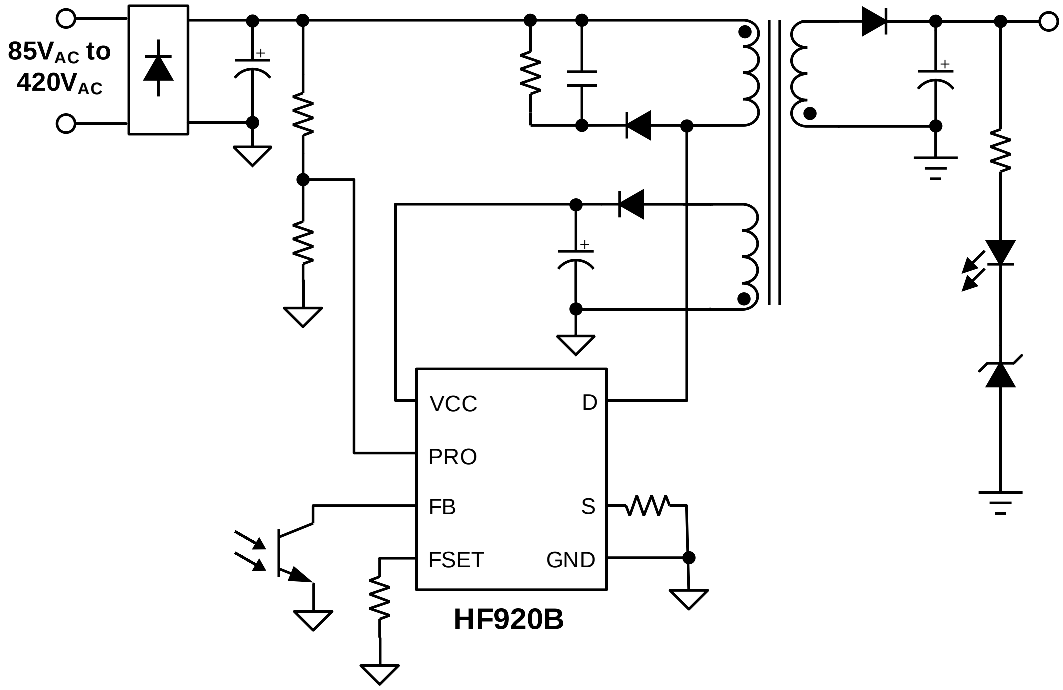
Table 1: Maximum Output Power

Package	P_{MAX} (W)	
	$85V_{AC}$ to $420V_{AC}$	$230V_{AC}$ ±15%
SOIC8-7A	6.5	9.5
SOIC14-11	7	10

Table 1 Notes:

- The maximum output power is limited by junction temperature.
- The test is done at T_A = 50°C. The test board is placed into a box about 20cmx15cmx10cm.
- To reduce V_{DS}, set the turns ratio to 5.
- Single output, V_{OUT} = 12.5V.
- GND of the SOIC8-7A package is connected to a 3cm^2 copper area with exposed copper strips. GND of the SOIC14-11 package is connected to a 2.5cm^2 copper area.
- The working mode when under the minimum input voltage is set to BCM.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
HF920BGSE*	SOIC8-7A	*See Below*	2
HF920BGS**	SOIC14-11	*See Below*	

* For Tape & Reel, add suffix –Z (e.g. HF920BGSE–Z).

** For Tape & Reel, add suffix –Z (e.g. HF920BGS–Z).

TOP MARKING (HF920BGSE)

HF920B
LLLLLLLL
MPSYWW

HF920B: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

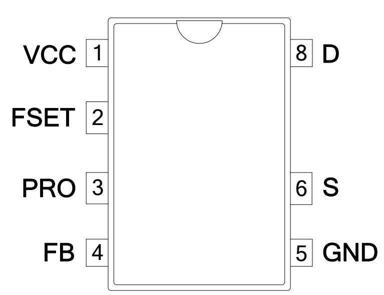
TOP MARKING (HF920BGS)

MPSYYWW
HF920B
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HF920B: Part number
LLLLLLLLL: Lot number

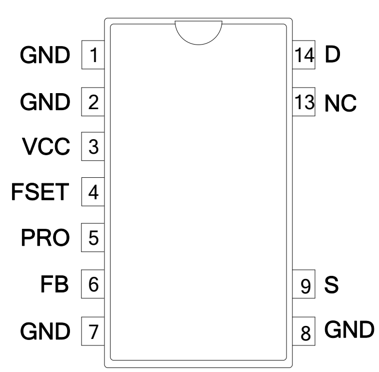
PACKAGE REFERENCE

TOP VIEW



SOIC8-7A

TOP VIEW



SOIC14-11

PIN FUNCTIONS

Pin #		Name	Description
SOIC8-7A	SOIC14-11		
1	3	VCC	**IC power supply.** Connect an electrolytic capacitor and a small ceramic decoupling capacitor to VCC.
2	4	FSET	**Switching frequency setting.** Connect a resistor from FSET to GND to set the switching frequency, which can be up to 150kHz. FSET is also used for enabling frequency doubling mode by placing a typical 1nF capacitor in parallel with the frequency-setting resistor.
3	5	PRO	**External protection.** When pulled up, PRO shuts down the IC with a hysteresis.
4	6	FB	**Feedback.** The output voltage is regulated according to the feedback signal on FB. OLP detection and burst mode control are also performed on FB.
5	1, 2, 7, 8	GND	**IC ground.**
6	9	S	**Source of the internal MOSFET.** S is the input for the primary current-sense signal.
-	13	NC	**No connection.**
8	14	D	**Drain of the internal MOSFET.** D is the input for the start-up high-voltage current source.

ABSOLUTE MAXIMUM RATINGS (1)

D .... -0.3V to +900V
V_{CC} .... -0.3V to +30V
All other pins .... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC8-7A 1.3W
SOIC14-11 .... 1.78W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -60°C to +150°C

ESD Rating

Human body model (HBM) .... ±2kV
Charged device model (CDM).................... ±2kV

Recommended Operation Conditions (3)

VCC to GND .... 10V to 24V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8-7A	96	45	°C/W
SOIC14-11	70	35	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to 125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-Up Current Source and Internal MOSFET (D Pin)						
Supply current from drain	I_{CHARGE}	VCC = V_{CCH} - 0.1V, V_D = 400V	1	2	3	mA
Leakage current from drain	I_{LEAK}	V_D = 400V, V_{GS} = 0V, T_J = 25°C			1	μA
		V_D = 400V, V_{GS} = 0V			10	μA
Breakdown voltage	$V_{(BR)DSS}$		900			V
On-state resistance	$R_{DS(ON)}$	V_{CC} = 10V, I_D = 100mA, T_J = 25°C		15	18	Ω
		V_{CC} = 10V, I_D = 100mA, T_J = 125°C		25	29	Ω
Supply Voltage Management (VCC Pin)						
VCC upper level at which the IC switch turns on	V_{CCH}		12	13	14	V
VCC lower level at which the IC switch turns off	V_{CCL}		8.4	9	9.6	V
VCC hysteresis	V_{CC_HYS}		3	4	5	V
VCC OVP level	V_{OVP}		24.4	25.5	26.5	V
VCC OVP delay time	t_{OVP}			70		μs
VCC recharge level after protections	V_{CCR}		4.8	5.5	6.2	V
Quiescent current during protections	I_{PRO}	VCC = V_{CCL}			300	μA
Quiescent current	I_Q	VCC = V_{CCH} - 0.1V		200	300	μA
Operating current	I_{CC}	VCC =13V, f_{SW} = 100kHz		510	610	μA
		VCC = 13V, FB = 0V		300	400	μA
Feedback Management (FB Pin)						
Internal pull-up resistor	R_{FB}	Normal operating		39		kΩ
Internal pull-up voltage	V_{UP}		4.1	4.4	4.7	V
FB to current-set-point division ratio	K_{DIV}			3.4	3.7	
Internal soft-start time	t_{SS}			6.7		ms
FB decreasing level at which the regulator enters burst mode	V_{BURL}		0.4	0.5	0.6	V
FB increasing level at which the regulator exits burst mode	V_{BURH}		0.6	0.7	0.8	V
Overload set point	V_{OLP}		3.3	3.65	4	V
Overload counter				8192		
Threshold for frequency to recover	V_{FR}	C_{FSET} = 1nF	2.85	3	3.15	V
Frequency-doubling entry/ recovery counter		C_{FSET} = 1nF		31		
Frequency Setting (FSET Pin)						
FSET reference voltage	V_{FSET}		1.18	1.25	1.32	V
Frequency spectrum jittering range, in percentage of f_{SW}	$R_{JITTERING}$			±3.5		%
Typical operating frequency	f_{SW}	R_{FSET} = 200kΩ	43	49	55	kHz
		R_{FSET} = 200kΩ, C_{FSET} = 1nF, V_{FB} = 3.5V	87	99	111	kHz
Maximum switching duty	D_{MAX}		79	83	87	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to 125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

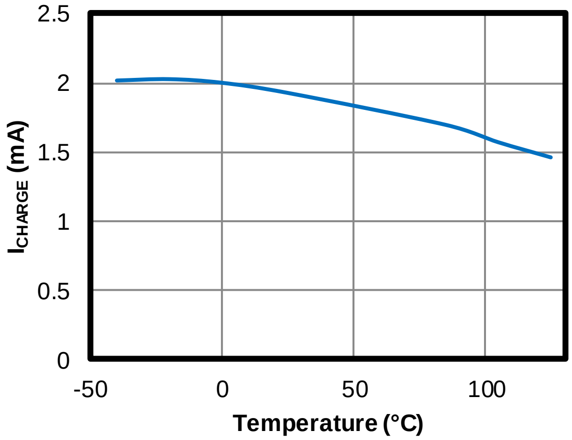
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current-Sense Management (S Pin)						
Leading-edge blanking for current sensor	t_{LEB1}			385		ns
Leading-edge blanking for SCP	t_{LEB2}			350		ns
Maximum current set point	V_{CSL}		0.91	0.97	1.02	V
Short-circuit protection set point	V_{SCP}		1.43	1.5	1.57	V
Slope compensation ramp	S_{RAMP}	R_{FSET} = 200kΩ		21		mV/µs
Protection Management (PRO Pin)						
Protection voltage	V_{PRO}		2.92	3.1	3.32	V
Protection hysteresis	$V_{PRO-HYS}$			0.2		V
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown recovery hysteresis (5)				30		°C

Note:

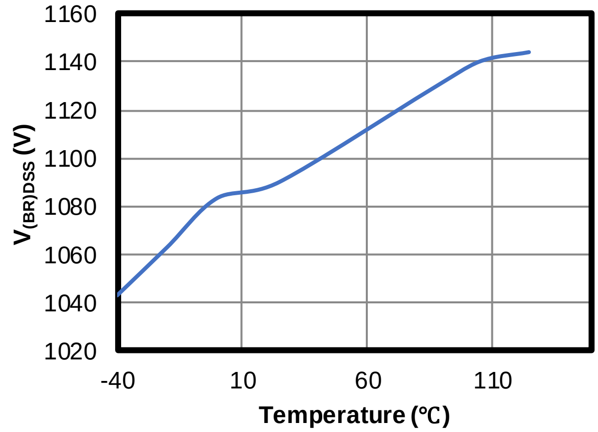
5) Guaranteed by design.

TYPICAL CHARACTERISTICS

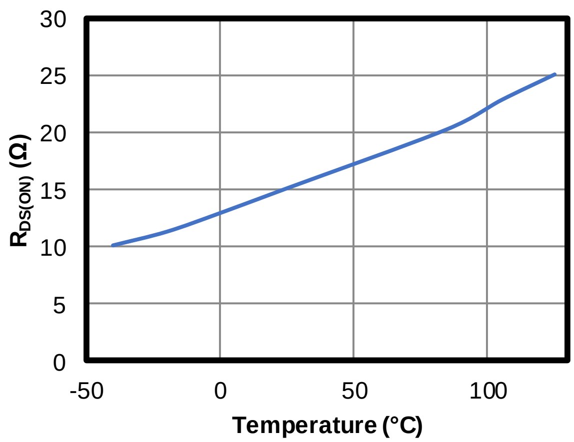
I_{CHARGE} @ V_D = 400V vs. Temperature



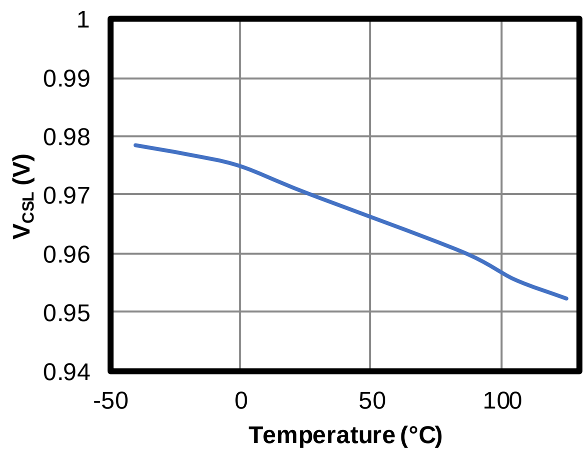
$V_{(BR)DSS}$ @ I_{LEAK} = 100µA vs. Temperature



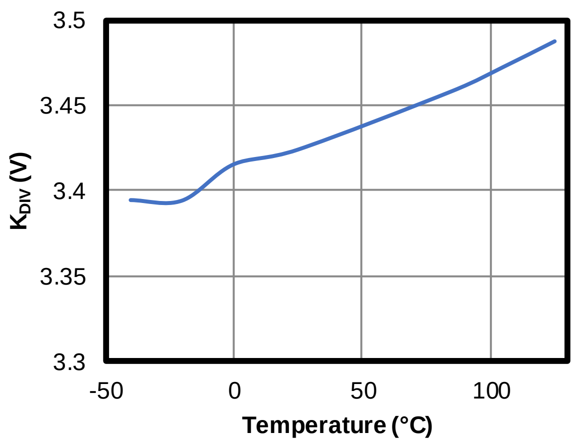
$R_{DS(ON)}$ vs. Temperature



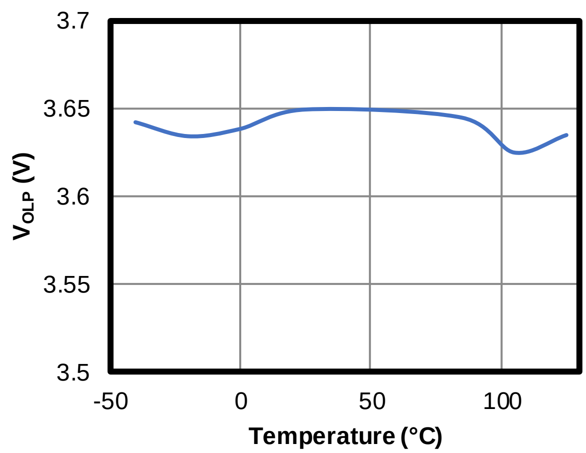
V_{CSL} vs. Temperature



K_{DIV} vs. Temperature

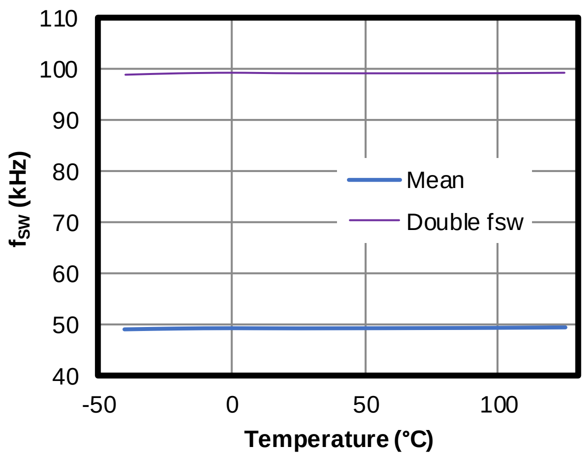


V_{OLP} vs. Temperature

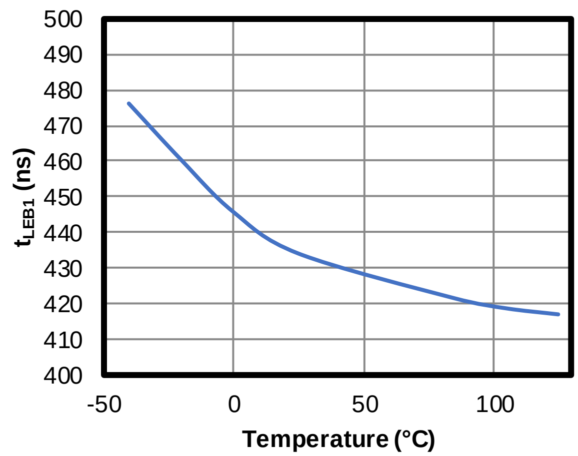


TYPICAL CHARACTERISTICS *(continued)*

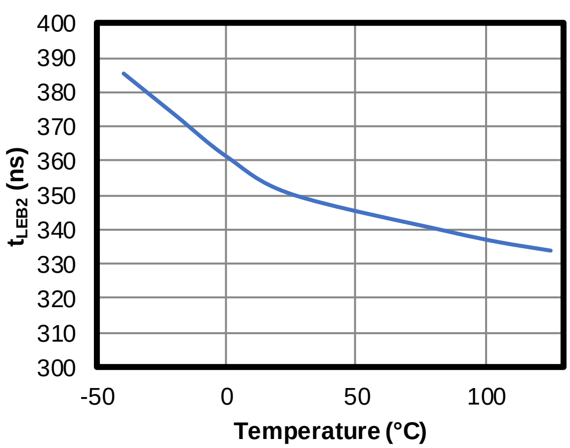
f_{SW} vs. Temperature



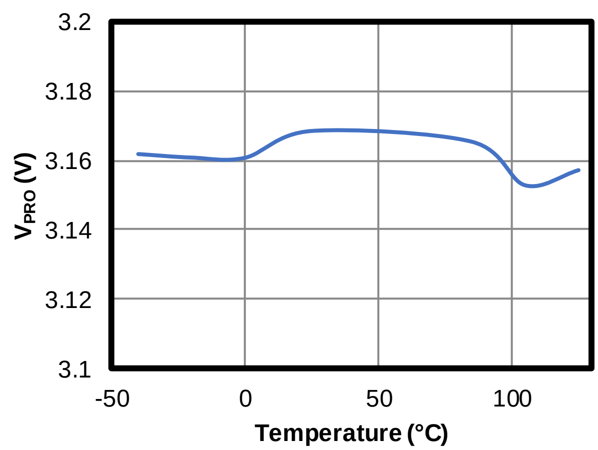
t_{LEB1} vs. Temperature



t_{LEB2} vs. Temperature



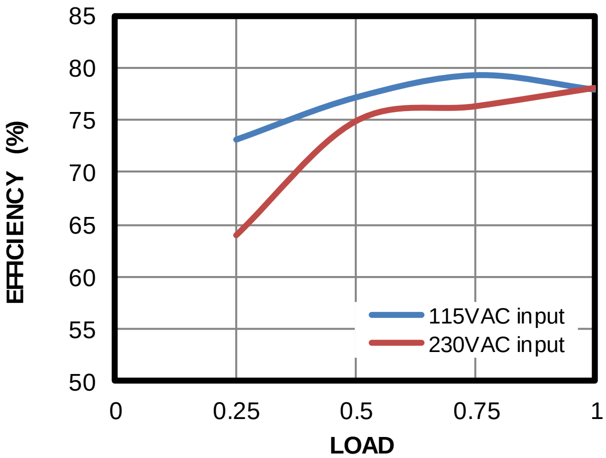
V_{PRO} vs. Temperature



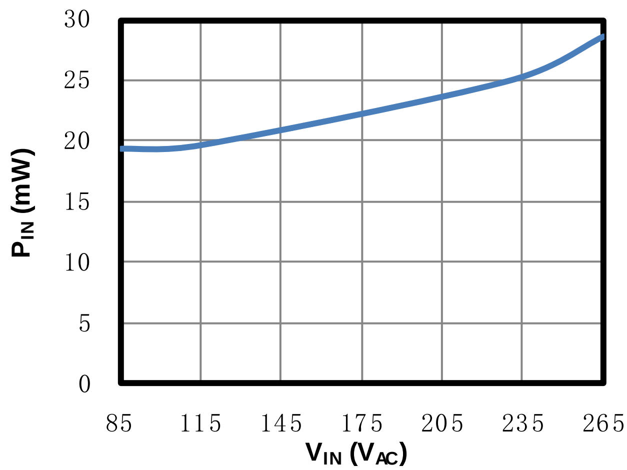
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested with the evaluation board in the Design Example section on page 18. V_{IN} = 230V, V_{OUT1} = 13.5V, I_{OUT1} = 300mA, V_{OUT2} = 8V, I_{OUT2} = 50mA, V_{OUT3} = 8V, I_{OUT3} = 50mA, T_A = 25°C, unless otherwise noted.

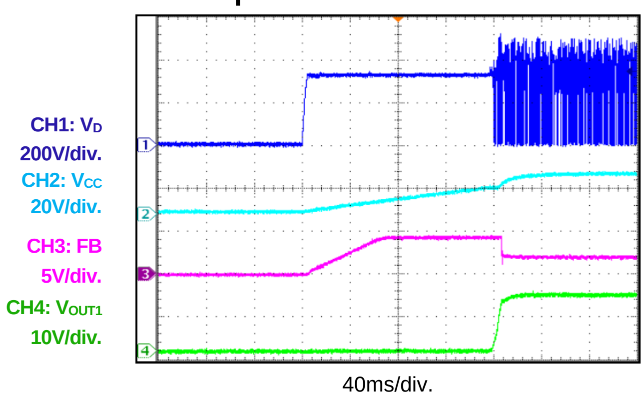
Efficiency



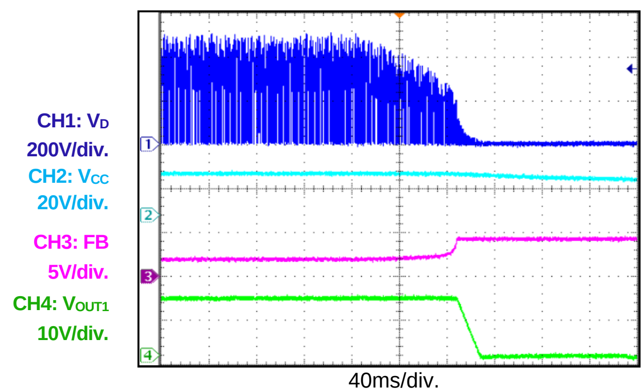
No-Load Consumption (6)



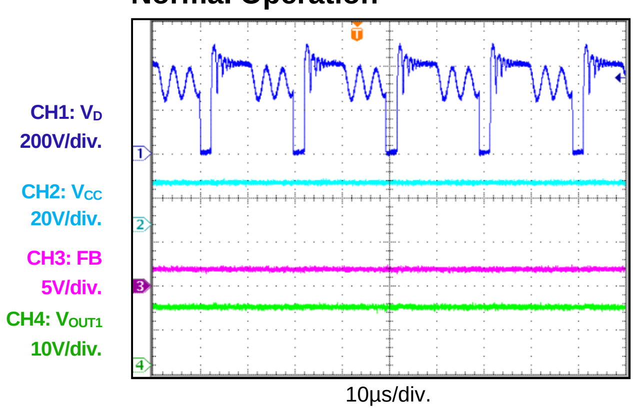
Start-Up



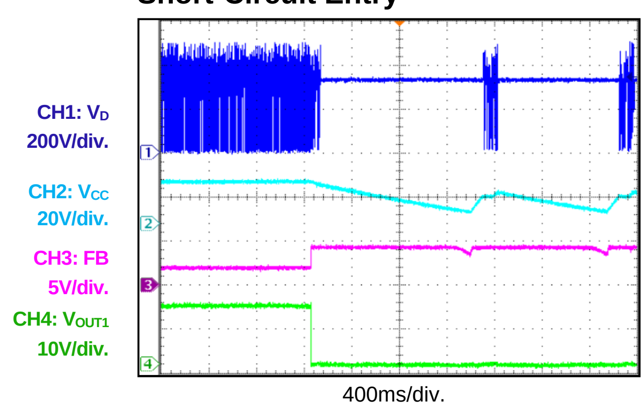
Shutdown



Normal Operation



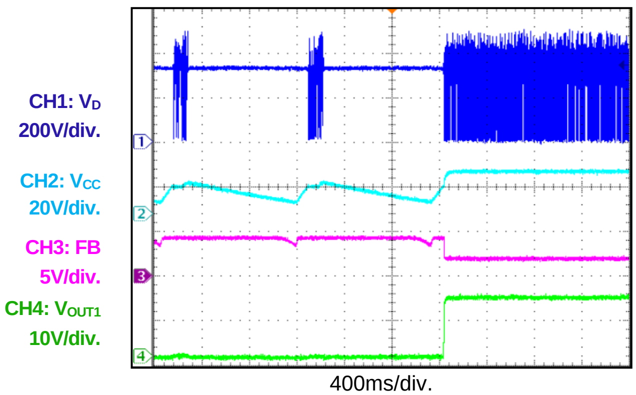
Short-Circuit Entry



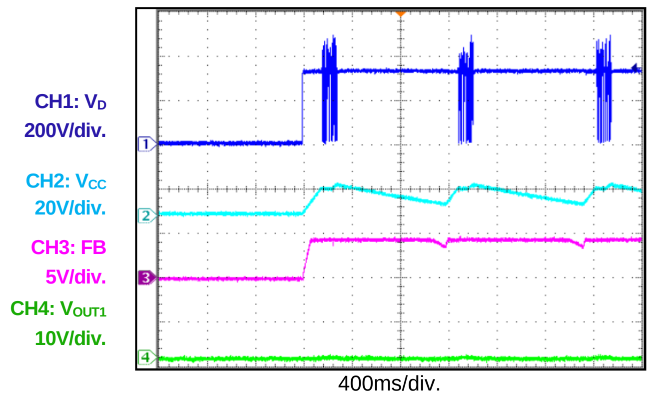
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested with the evaluation board in the Design Example section on page 18. V_{IN} = 230V, V_{OUT1} = 13.5V, I_{OUT1} = 300mA, V_{OUT2} = 8V, I_{OUT2} = 50mA, V_{OUT3} = 8V, I_{OUT3} = 50mA, T_A = 25°C, unless otherwise noted.

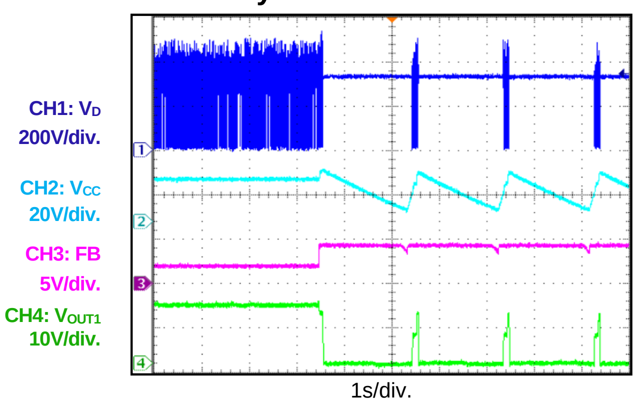
Short-Circuit Recovery



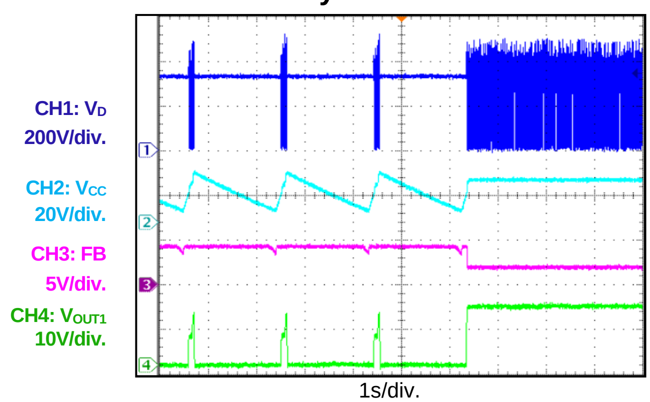
Short-Circuit Start-Up



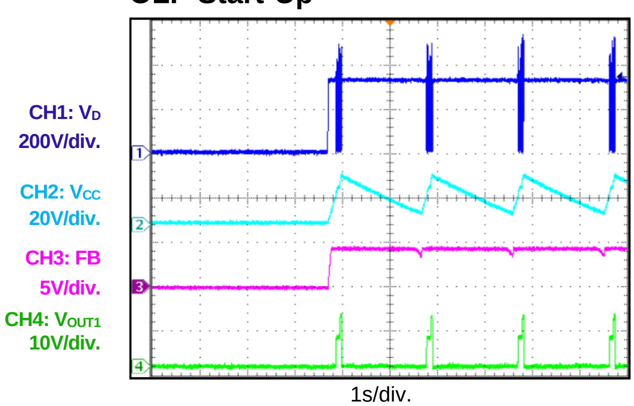
OLP Entry



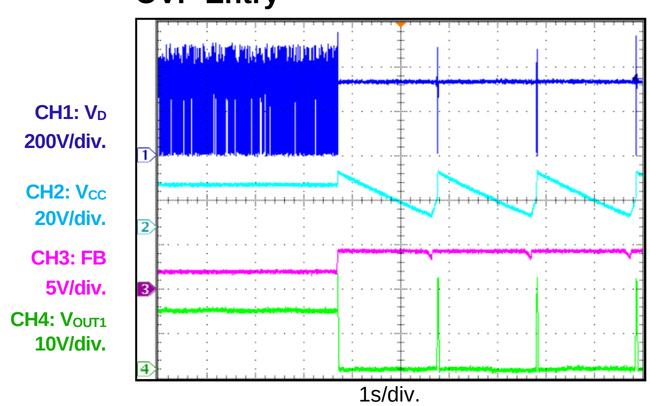
OLP Recovery



OLP Start-Up



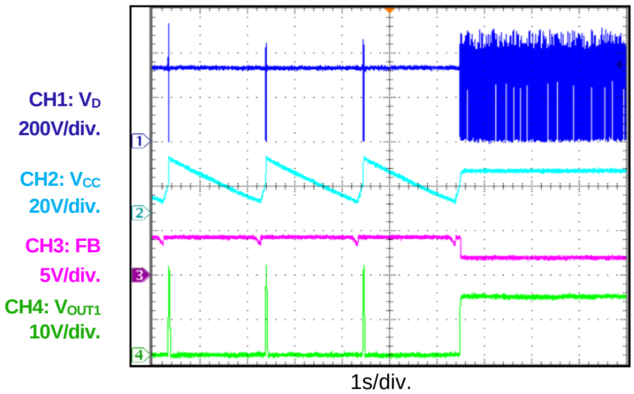
OVP Entry



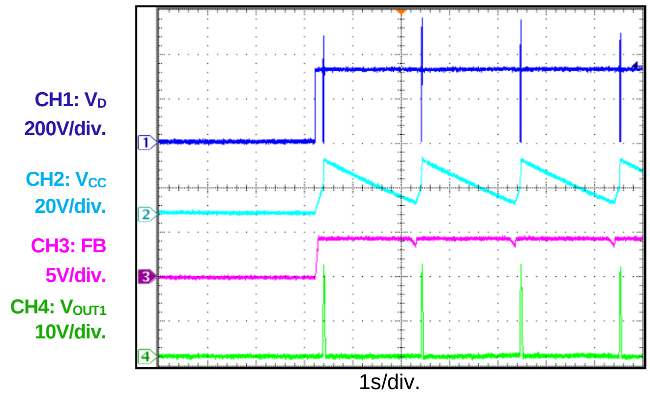
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested with the evaluation board in the Design Example section on page 18. V_{IN} = 230V, V_{OUT1} = 13.5V, I_{OUT1} = 300mA, V_{OUT2} = 8V, I_{OUT2} = 50mA, V_{OUT3} = 8V, I_{OUT3} = 50mA, T_A = 25°C, unless otherwise noted.

OVP Recovery



OVP Start-Up



Note:

6) No-load consumption is tested with OUT2 and OUT3 open.

FUNCTIONAL BLOCK DIAGRAM

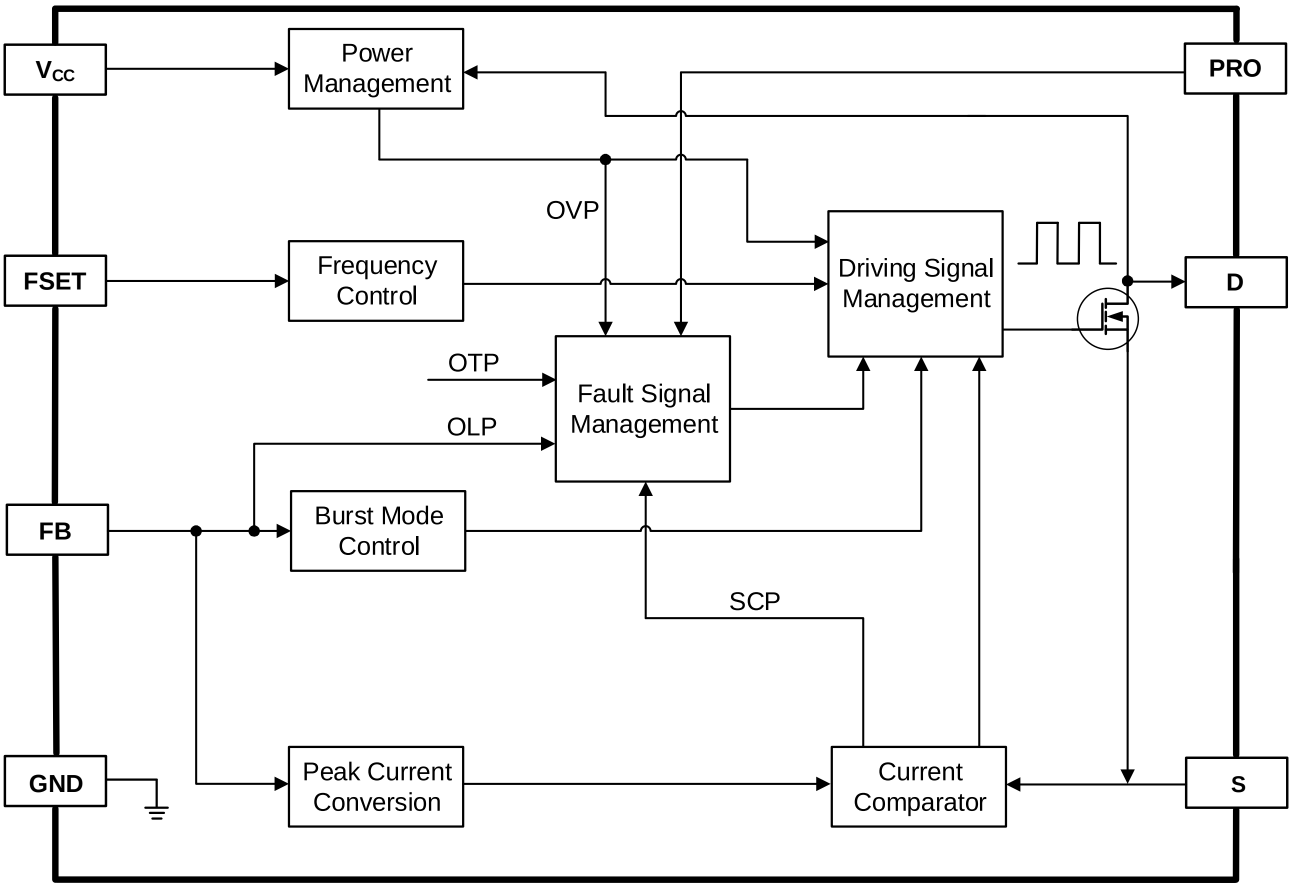


Figure 1: Internal Functional Block Diagram

OPERATION

The HF920B incorporates all of the necessary features required by a reliable switch-mode power supply. The proprietary, 900V, monolithic integration enables a highly integrated power supply solution. The HF920B uses burst mode to minimize standby power consumption at light-load. To improve EMI performance, the HF920B uses frequency jittering and implements an optimized method of electromagnetic compatibility (EMC).

Protection features such as auto-recovery for overload protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), and thermal shutdown for over-temperature protection (OTP) contribute to a safer converter design with minimal external components.

Pulse-Width Modulation (PWM) Operation

The HF920B employs peak current control mode. On the secondary side, the output voltage is regulated by the compensation network, and the compensation output is fed back to the primary side as an input signal to FB through an optocoupler. The FB voltage (V_{FB}) controls the peak current on the primary-side winding of the flyback transformer based on the current-sensing on S. The integrated 900V MOSFET turns on at the beginning of each cycle based on the internal oscillator, and turns off based on the peak current control.

Start-Up and VCC UVLO

Initially, the IC is driven by the internal current source drawn from the high-voltage D pin. The IC begins switching, and the internal high-voltage current source turns off once the VCC voltage (V_{CC}) reaches its upper threshold (V_{CCH}). Then the IC supply is taken over by the auxiliary winding of the transformer. Whenever V_{CC} falls below its lower threshold (V_{CCL}), the regulator stops switching, and the internal high-voltage current source turns on again (see Figure 2).

The lower VCC under-voltage lockout (UVLO) threshold decreases from V_{CCL} to V_{CCR} when a fault condition (such as SCP, OLP, OVP, or OTP) occurs.

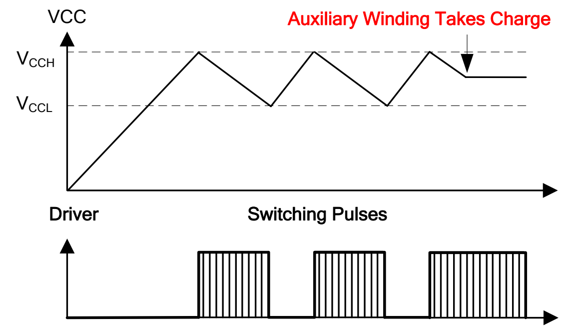


Figure 2: VCC Start-Up

Soft Start (SS)

The HF920B implements an internal soft-start circuit to reduce stress on the primary-side MOSFET and secondary diode, and to smoothly establish the output voltage during start-up. The internal soft-start circuit increases the threshold of the peak current comparator gradually from the minimal level until the feedback control loop takes over. The maximum soft-start time is t_{SS}. Within the soft-start duration, the switching frequency also increases progressively from 20% to 100% of the programmed switching frequency.

Switching Frequency (f_{SW})

The switching frequency (f_{SW}) can be set by a resistor between FSET and GND. The oscillator frequency can be calculated with Equation (1):

$$f_{SW} = \frac{1}{523 \times 10^{-9} + 123.4 \times 10^{-12} \times \frac{R_{FSET}}{V_{FST}}} \text{ Hz} \qquad (1)$$

Where V_{FSET} is the internal reference voltage on FSET.

Frequency Jittering

The HF920B provides a frequency jittering function, which simplifies the input EMI filter design and decreases system cost. The HF920B has optimized frequency jittering with a ±3.5% frequency deviation range and a $256T_S$ carrier cycle that improves EMI by spreading the energy dissipation over the frequency range.

Frequency Doubling

Connect a 1nF capacitor to FSET to enable frequency doubling. The switching frequency is doubled when the converter enters an over-power condition (V_{FB} rises to V_{OLP}). This way, the converter is able to handle up to a 50% decrease in the transformer inductance caused by external magnetizing interference.

Peak Current Limit

The primary peak current is sensed by a sensing resistor between S and GND. When the sum of the sense resistor voltage and the slope compensation voltage reaches the peak current limit (V_{CS}), the MOSFET turns off.

The peak current limit is set by V_{FB}, as $V_{CS} = V_{FB} / K_{DIV}$, for all normal operations. The maximum value of the peak current limit is limited to V_{CSL} internally. This way, the output power is always limited to prevent excessive stress on the power supply.

Burst Operation

The HF920B implements burst mode during no-load and light-load conditions. Burst mode enables and disables the switching pulse of the MOSFET alternately to reduce switching loss. This helps minimize standby power consumption so the device can achieve high light-load efficiency.

As the load decreases, V_{FB} decreases. The IC stops switching when V_{FB} drops below V_{BURL}. As the converter stops and the output voltage drops, V_{FB} rises again due to the negative feedback control loop. Once V_{FB} goes over V_{BURH}, the switching pulse resumes. If the load condition remains the same, V_{FB} decreases and the entire process is repeated.

Figure 3 shows the HF920B's operation in burst mode .

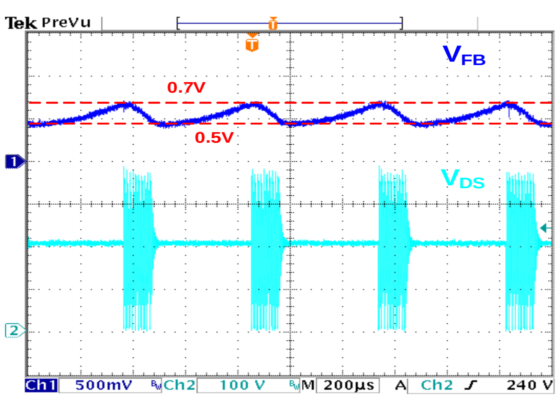


Figure 3: Burst Mode

Over-Voltage Protection (OVP)

The HF920B shuts down using over-voltage protection (OVP) when V_{CC} exceeds V_{OVP} for t_{OVP}. In a flyback application, the auxiliary winding output voltage is proportional to the output voltage, so OVP protects the circuit from overstress during an output over-voltage condition. The HF920B restarts automatically after V_{CC} drops to V_{CCR}. Once the fault disappears, the regulator resumes normal operation.

Overload Protection (OLP)

The HF920B shuts down when OLP is triggered. The OLP fault occurs when V_{FB} is pulled up to V_{OLP} for 8192 switching cycles. The HF920B restarts automatically when V_{CC} drops to V_{CCR}. When the fault disappears, the power supply resumes operation.

If frequency doubling is enabled, the HF920B doubles the switching frequency when V_{FB} rises to the OLP point.

Short-Circuit Protection (SCP)

The HF920B shuts down when the S voltage exceeds V_{SCP}, which indicates a short circuit. The HF920B enters short-circuit protection (SCP) to prevent any thermal or stress damage. The HF920B restarts automatically when V_{CC} drops to V_{CCR}. Once the fault disappears, the power supply resumes normal operation.

Thermal Shutdown (OTP)

When the junction temperature of the IC exceeds 150°C, over-temperature protection (OTP) is activated, and the main power MOSFET stops switching to protect the HF920B from thermal damage. During the protection period, the regulator is latched off.

VCC is discharged to V_{CCR} and recharged to V_{CCH} by the internal high-voltage current source. Once the junction temperature drop exceeds the thermal shutdown recovery hysteresis, the HF920B resumes normal operation.

PRO

PRO provides external protection. The HF920B shuts down when the PRO voltage exceeds V_{PRO}, and resumes normal operation once the fault disappears. PRO protection can be used for input OVP or any other protections (e.g. input UVP, OTP for key components, etc.).

Leading-Edge Blanking (LEB)

The HF920B implements a leading-edge blanking (LEB) unit to prevent the MOSFET from turning off prematurely due to its high turn-on current spike. During the blanking time, the current-sensing signal on S is blocked.

The LEB unit contains two LEB times. The current sensor LEB inhibits the current limitation comparator for t_{LEB1}, and the SCP LEB inhibits the SCP current comparator for t_{LEB2}. Figure 4 shows the primary current-sense waveform and the LEB.

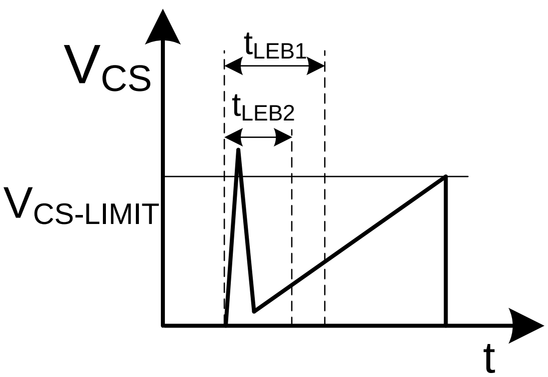


Figure 4: Leading-Edge Blanking

APPLICATION INFORMATION

Selecting the Input Capacitor

The input bulk capacitor filters the rectified AC input voltage and holds the bus voltage for the converter. Figure 5 shows the typical DC bus voltage waveform for a full-bridge rectifier.

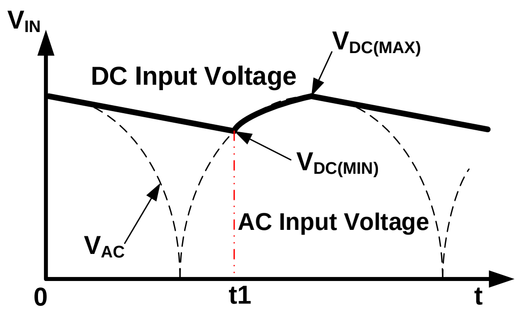


Figure 5: Input Voltage Waveform

When a full-bridge rectifier is used, the input capacitor is typically set at 2μF/W for the universal input condition (85V_{AC} to 265V_{AC}). For high-voltage input applications (>185V_{AC}), cut the capacitor values in half. Very low DC input voltages can cause thermal problems under heavy-load conditions. It is recommended for the minimum DC voltage to be above 70V. Estimate the minimum DC voltage with the following procedure:

First, estimate the input power (P_{IN}) with Equation (2):

$$P_{IN} = \frac{V_O \times I_O}{\eta} \tag{2}$$

Where V_O is the output voltage, I_O is the rated output current, and η is the estimated efficiency. Generally, η is between 0.75 and 0.85 depending on the input range and output application.

Then, the linear part of the DC input voltage (V_{DC}) can be calculated with Equation (3):

$$V_{DC}(t) = \sqrt{{V_{AC(PEAK)}}^2 - \frac{2 \times P_{IN}}{C_{IN}} \times t} \tag{3}$$

At t1, the DC bus voltage reaches its minimum value, and the AC input starts charging the input capacitor. t1 can be calculated with Equation (4):

$$V_{DC}(t1) = V_{AC}(t1) \tag{4}$$

$V_{DC(MIN)}$ can then be calculated with t1 and Equation (4). A larger input capacitor should be used if the estimated $V_{DC(MIN)}$ is too low.

As a 900V offline regulator, the HF920B is ideal for very high-voltage input applications, which means a very high bus voltage is beyond the rated voltage of normal high-voltage electrolytic capacitors. To meet the high bus voltage requirement, stack the capacitors (see Figure 6).

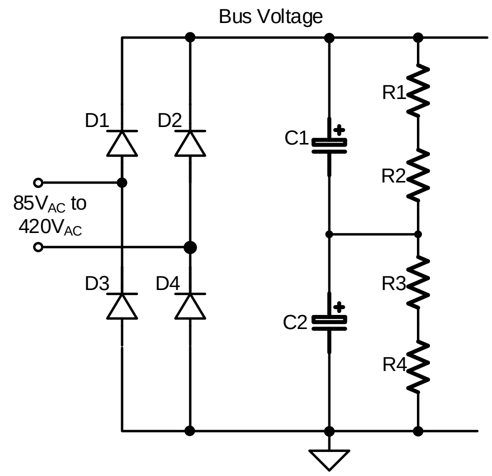


Figure 6: Stacked Input Capacitor Circuit

The same type of capacitors should be chosen for C1 and C2 to balance their voltages. Each capacitor endures half of the bus voltage, but due to the capacitance distribution (typically ±20% for electrolytic capacitors), their voltage varies in mass production. In this case, R1 through R4 should be used as the voltage-balancing resistors.

To balance the voltage on C1 and C2, R1 through R4 should have the same value. R1–R4 should each have a 1206 package size to meet the voltage rating requirement. The R1–R4 values should also be large enough for energy savings. For example, the total value of R1–R4 is 20MΩ, which consumes about 18mW at a 600V_{DC} bus voltage.

Voltage Stress on the Primary MOSFET

Typically, the maximum voltage stress on the primary MOSFET is designed to be less than 90% of its breakdown voltage for reliable operation.

The maximum voltage stress occurs when the primary MOSFET turns off, and can be calculated with Equation (5):

$$V_{DS(MAX)} = V_{BUS(MAX)} + N(V_O + V_F) + V_{SPIKE} \quad (5)$$

Where V_F is the rectifier diode's forward voltage, V_O is the output voltage, N is the primary-to-secondary turns ratio, and V_{SPIKE} is the voltage spike caused by the transformer's primary leakage inductance.

According to Equation (5), voltage stress can be reduced either by choosing a small N or V_{SPIKE}. However, a small N leads to larger secondary stress, which means a tradeoff must be made. A small V_{SPIKE} requires a strong snubber to suppress the voltage spike.

The input circuit should be designed to guarantee a proper $V_{BUS(MAX)}$ (i.e. using suppression components to protect it from surge).

Primary-Side Inductor Design (L_M)

Typically, the converter is designed to operate in continuous conduction mode (CCM) under a low input voltage for universal input applications. With a built-in slope compensation function, the HF920B supports stable CCM control when the duty cycle exceeds 50%.

Set the ratio (K_P) of the primary inductor ripple current amplitude vs. the peak current value to $0 < K_P \le 1$, where a smaller K_P means a deeper CCM, and $K_P = 1$ stands for boundary conduction mode (BCM) and discontinuous conduction mode (DCM). Figure 7 shows the relevant waveforms. A larger primary inductance leads to a smaller K_P, which reduces the RMS current but increases the transformer size. For most HF920B applications, an optimal K_P value is between 0.8 and 1, considering the wide input range.

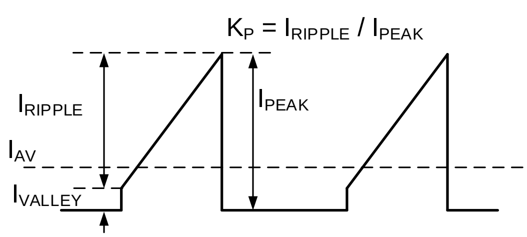


Figure 7: Typical Primary Current Waveform

For CCM at a minimum input, the converter duty cycle can be calculated with Equation (6):

$$D = \frac{(V_O + V_F) \times N}{(V_O + V_F) \times N + V_{DC(MIN)}} \quad (6)$$

Where V_F is the secondary diode's forward voltage, and N is the transformer turns ratio.

The MOSFET turn-on time can be calculated with Equation (7):

$$t_{ON} = \frac{D}{f_{SW}} \quad (7)$$

Where f_{SW} is the operating frequency.

The input average current, ripple current, peak current, and valley current of the primary side are calculated using Equation (8), Equation (9), Equation (10), and Equation (11), respectively:

$$I_{AV} = \frac{P_{IN}}{V_{DC(MIN)}} \quad (8)$$

$$I_{RIPPLE} = K_P \times I_{PEAK} \quad (9)$$

$$I_{PEAK} = \frac{I_{AV}}{(1 - \frac{K_P}{2}) \times D} \quad (10)$$

$$I_{VALLEY} = (1 - K_P) \times I_{PEAK} \quad (11)$$

Estimate L_M using Equation (12):

$$L_M = \frac{V_{DC(MIN)} \times t_{ON}}{I_{RIPPLE}} \quad (12)$$

Current-Sense Resistor

Figure 8 shows the peak current control waveform with slope compensation.

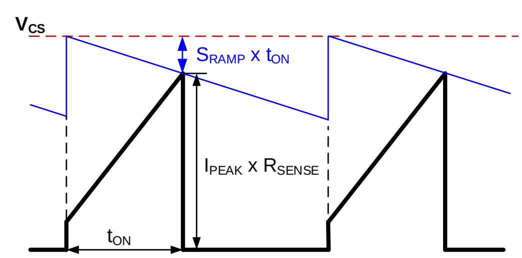


Figure 8: Peak Current Control Waveform with Slope Compensation

When the sum of the sense resistor voltage and the slope compensation voltage reaches the peak current limit (V_{CS}), the HF920B turns off the internal MOSFET. V_{CS} equals the maximum current-set point (V_{CSL}) under full-load conditions. Considering the margin, use 0.95 x V_{CSL} for designs. The voltage on the sense resistor can be calculated using Equation (13):

$$V_{SENSE} = 0.95 \times V_{CSL} - S_{RAMP} \times t_{ON} \quad (13)$$

Where S_{RAMP} is the slope compensation ramp in proportion to f_{SW}. Typically, S_{RAMP} = 21mV/μs when R_{FSET} = 200kΩ.

The value of the sense resistor is calculated using Equation (14):

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK}} \quad (14)$$

The current-sense resistor should be chosen with an appropriate power rating. Its power loss can be calculated with Equation (15):

$$P_{SENSE} = \left[\left(\frac{I_{PEAK} + I_{VALLEY}}{2}\right)^2 + \frac{1}{12} \times (I_{PEAK} - I_{VALLEY})^2\right] \times D \times R_{SENSE} \quad (15)$$

Input Over-Voltage Protection on PRO

Figure 9 shows a typical input OVP circuitry of the HF920B. The input OVP point can be calculated with Equation (16):

$$V_{INOVP} = V_{PRO} \times \frac{R5 + R6 + R7 + R8}{R8} \quad (16)$$

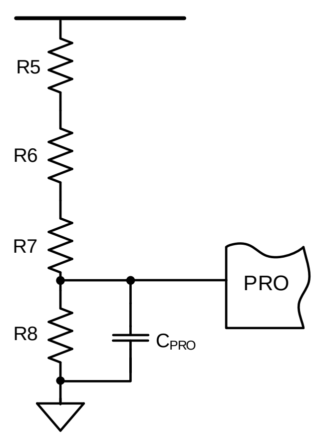


Figure 9: Input Over-Voltage Protection Set-Up

For resistors R5 through R7, 1206 packages should be used to meet the voltage rating requirements. The total value should be greater than 10MΩ for energy saving purposes.

Switching noise may couple to these large resistors and interfere with PRO protection. It is recommended to connect a bypass ceramic capacitor to PRO. Place this capacitor as close to the IC as possible.

Thermal Performance Optimization

The HF920B is dedicated to high input voltage applications. However, the high input voltage can cause a greater switching loss on the MOSFET, which can lead to poor thermal performance. Measures should be taken to reduce the switching loss when designing these applications.

Use a lower switching frequency if possible, and use a small transformer turns ratio to minimize the reflected voltage on the primary winding. These steps reduce V_{DS}.

Finally, reduce the turn-on loss, since the turn-on loss composes a large part of the switching loss. Turn-on loss is the product of the turn-on current spike and V_{DS}. Reducing the turn-on loss can be achieved by reducing V_{DS} or the turn-on current spike.

Besides reducing V_{DS} by using a small turns ratio as discussed above, another way of reducing V_{DS} when the MOSFET turns on is to set the HF920B to work in deep DCM. In deep DCM, the V_{DS} oscillation is fully damped, so there is no chance of turning on at the high peak value.

The turn-on current spike is caused by parasitic capacitance and output diode reverse recovery.

DCM operation helps prevent the output diode's reverse recovery. The transformer structure should be designed to achieve minimum parasitic capacitance of each winding and between the primary and secondary windings.

Design Example

Table 2 shows a design example using the application guidelines for the given specifications.

Table 2: Design Example

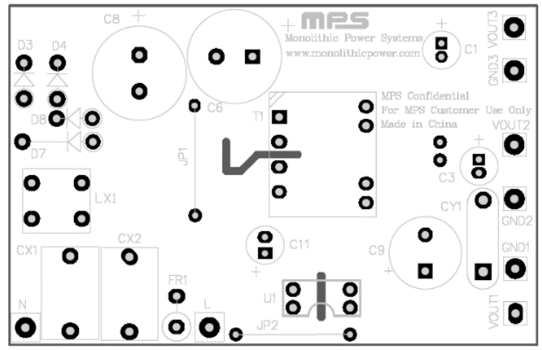
V_{IN}	85 to 420VAC
V_{OUT1}	13.5V
I_{OUT1}	0.3A
V_{OUT2}	8V
I_{OUT2}	0.05A
V_{OUT3}	8V
I_{OUT3}	0.05A
f_{SW}	50kHz

For the detailed application schematic, see Figure 11 on page 20. For typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 9. For more device applications, refer to the related evaluation board datasheets.

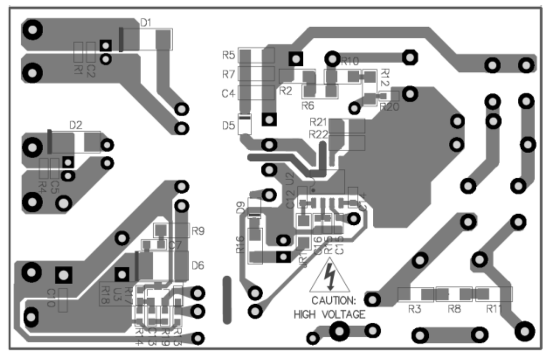
PCB Layout Guidelines

Efficient PCB layout is critical for achieving reliable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 10 and follow the guidelines below:

1. Minimize the power stage switching stage loop area. This includes the input loop (C8–C6–T1–U2–R21/R22–C8), the auxiliary winding loop (T1–D9–R16–C11–T1), the output loop (T1–D6–C9–T1, T1–D1–C1–T1, and T1–D2–C3–T1), and the RCD loop (T1–D5–R5/R7/C4–T1).
2. Ensure that the power loop ground does not pass through the control circuit ground.
3. If a heatsink is used, connect it to the primary GND plane to improve EMI performance and thermal dissipation.
4. Place the control circuit capacitors (for FB, PRO, and VCC) close to the IC to decouple the switching noise.
5. Enlarge the GND pad near the IC for good thermal dissipation.
6. Keep the EMI filter far away from the switching point.
7. Ensure that there is enough clearance distance to meet the insulation requirements.



Top Side



Bottom Side

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

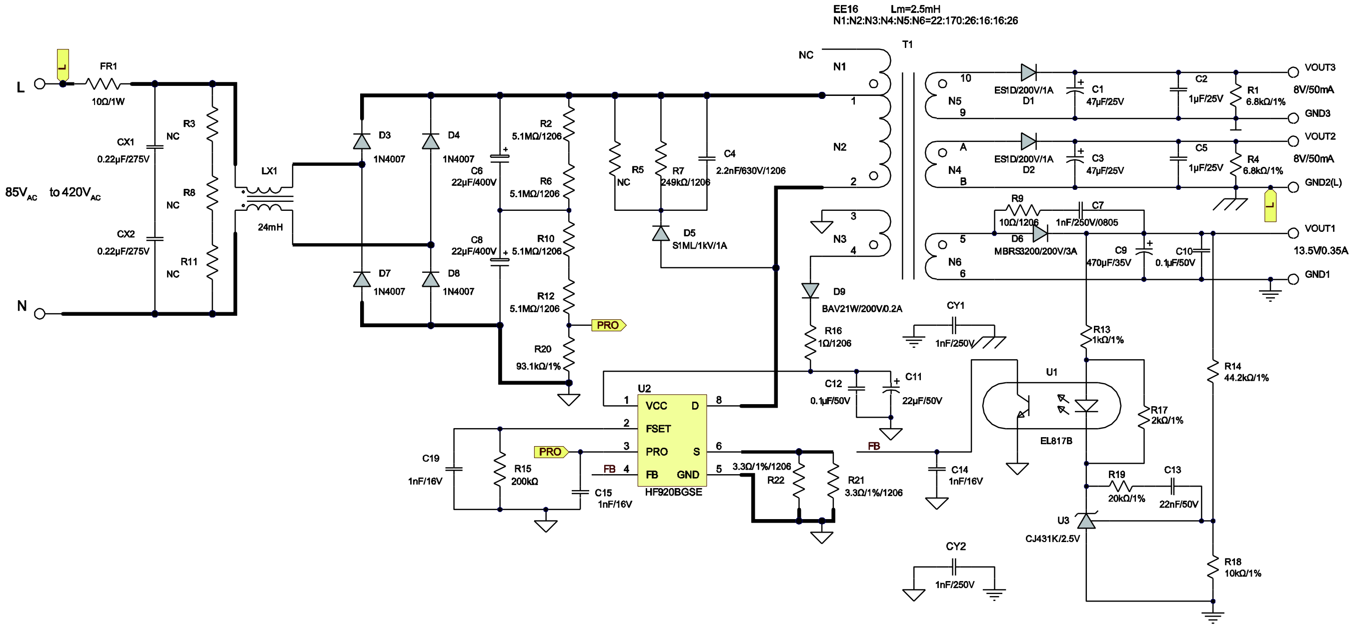
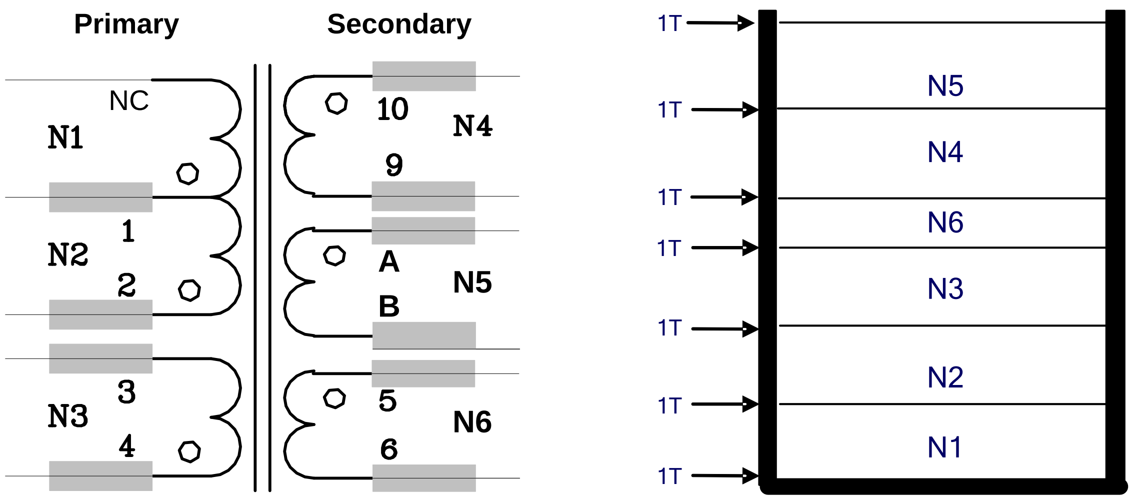


Figure 11: Typical Application Circuit



a) Connection Diagram

b) Winding Diagram

Figure 12: Transformer Structure

Table 3: Winding Order

Tape (T)	Winding	Terminal Start → End	Wire Size (Φ)	Turns (T)
1	N1	1 → NC	0.15mm x 2	22
1	N2	2 → 1	0.15mm x 1	170
1	N3	4 → 3	0.1mm x 1	26
1	N6	5 → 6	0.3mm TIW x 1	26
1	N4	10 → 9	0.16mm TIW x 1	16
1	N5	A → B	0.16mm TIW x 1	16

FLOWCHART

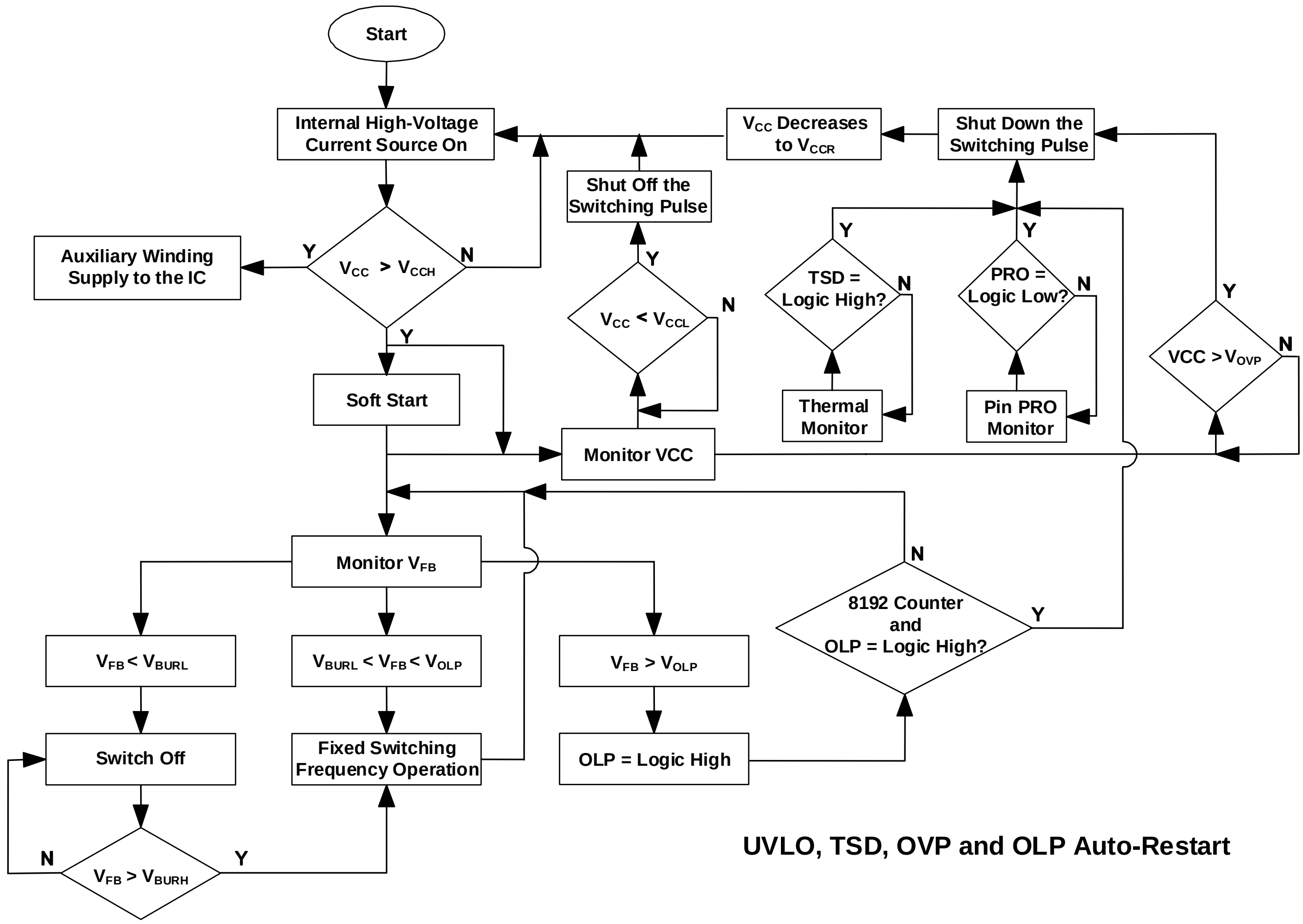


Figure 13: Control Flowchart

EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

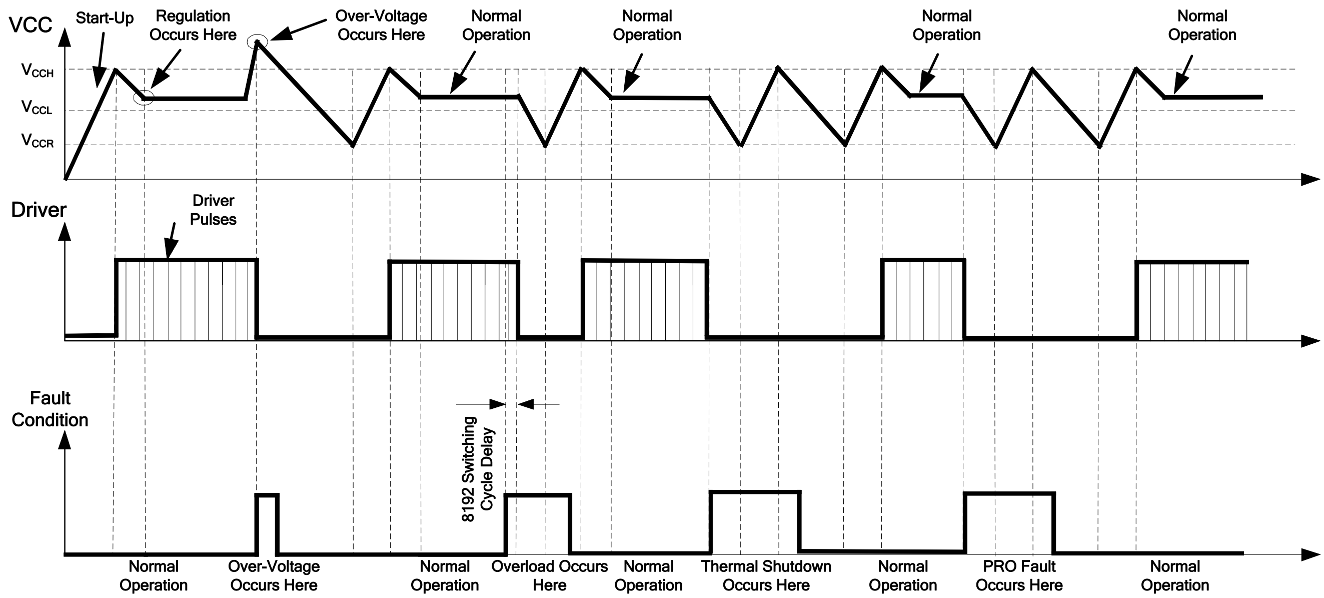
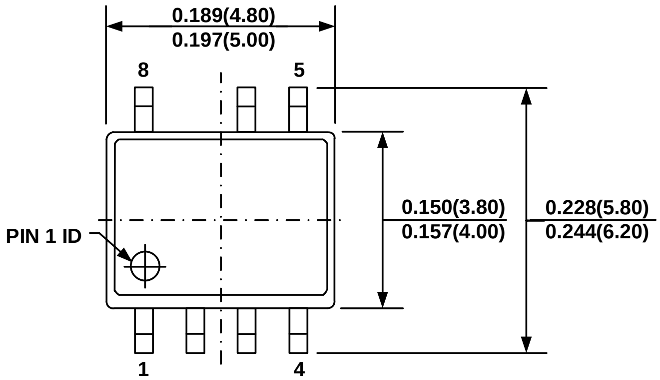


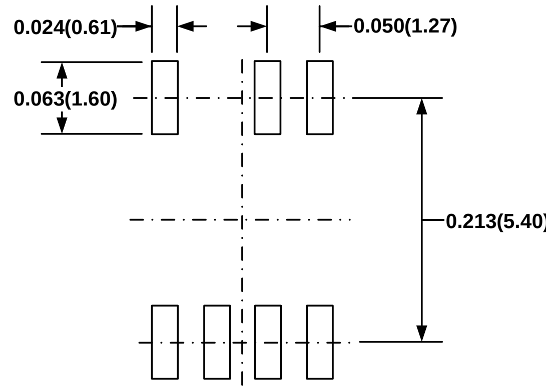
Figure 14: Evolution of the Signals in Presence of Faults

PACKAGE INFORMATION

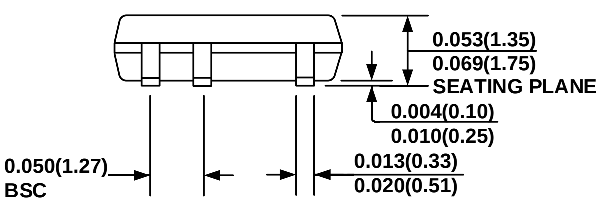
SOIC8-7A



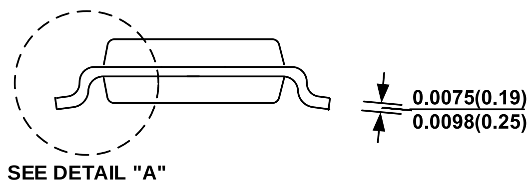
TOP VIEW



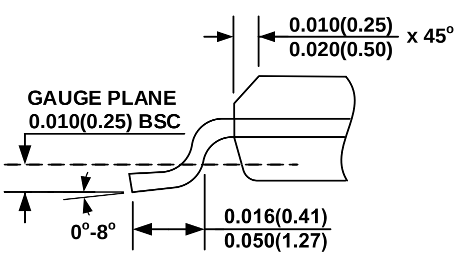
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



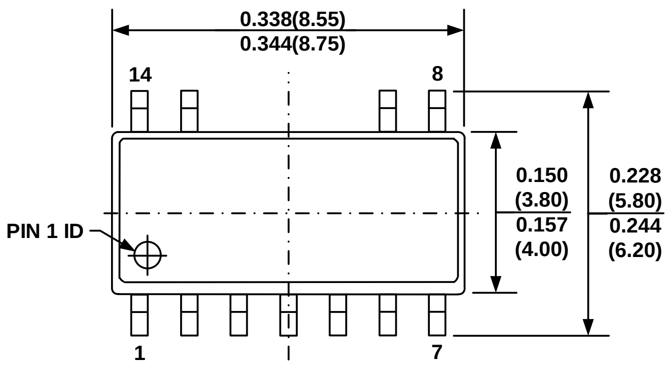
DETAIL "A"

NOTE:

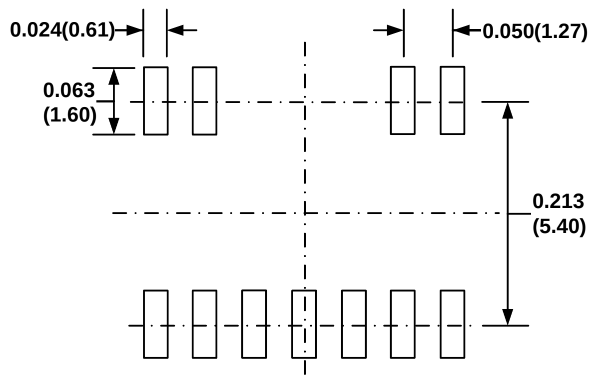
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

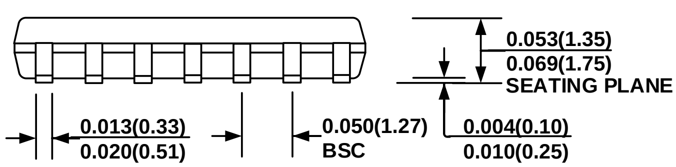
SOIC14-11



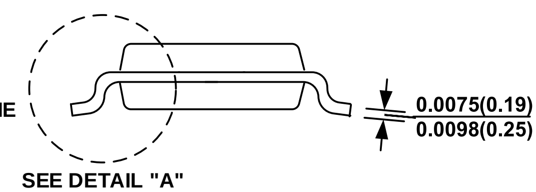
TOP VIEW



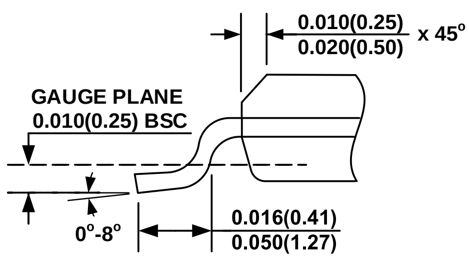
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



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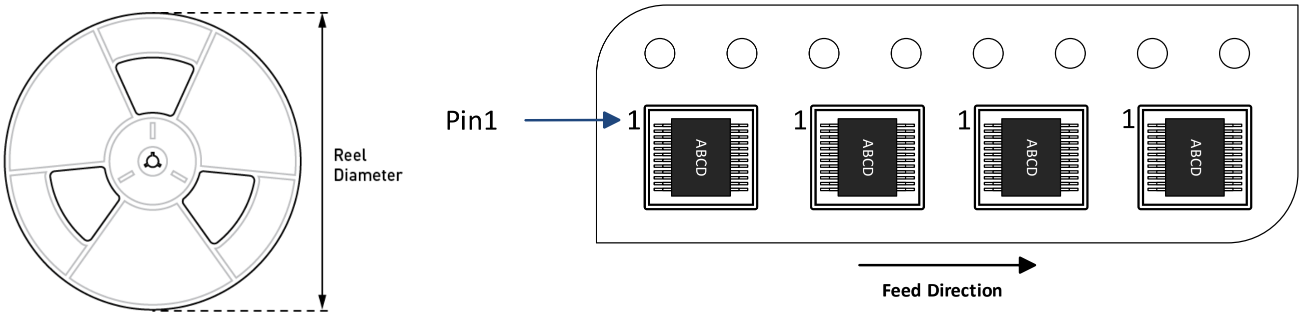
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HF920BGSE–Z	SOIC8-7A	2500	100	N/A	13in	12mm	8mm
HF920BGS–Z	SOIC14-11	2500	57	N/A	13in	16mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/16/2020	Initial Release	-