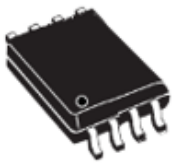
STISO621

Datasheet

Dual channel digital isolator



SO-8W

Features

- Dual channel, digital isolator with 1 – 1 channel directionality
- High data rate up to 100 Mbps
- Wide Ta range operation: - 40ºC to 125ºC
- High common-mode transient: >50k V/µs
- From 3 V to 5.5 V supply levels
- 3.3 V and 5 V level translation
- Low power consumption
- Pulse width distortions < 3 ns
- 6k V Galvanic isolation

Application

- Optocoupler replacement in industrial application
- Industrial field bus isolation
- Battery monitor and motor drive
- Size-critical multichannel isolation

Description

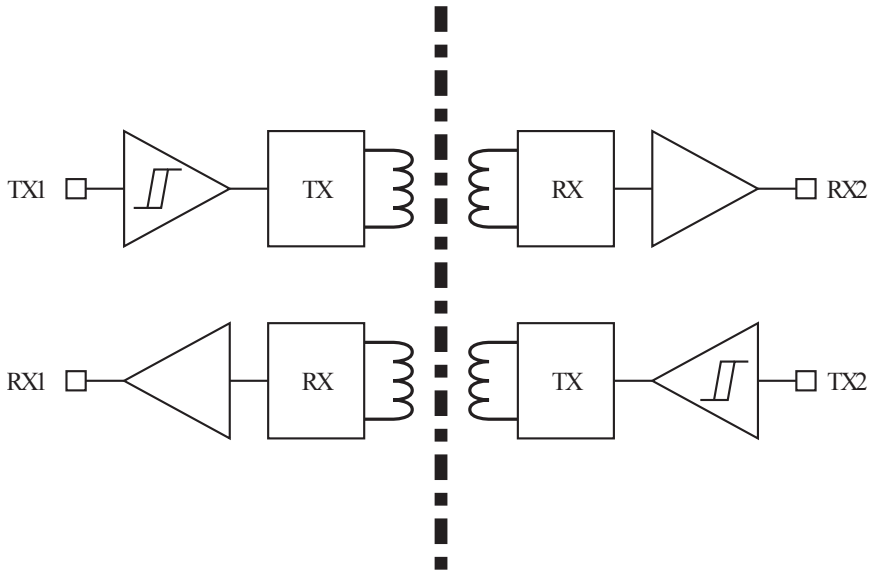
The STISO621 are dual-channel digital isolators based on the ST thick oxide galvanic isolation technology. The devices provide two independent channels in opposite direction with Schmitt trigger input, providing robustness to noise and high speed input/output switching time.

Product status link
STISO621

Product label
SUSTAINABLE TECHNOLOGY

1 Block diagram

Figure 1. **Block diagram**



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test Condition	Value	Unit
V_{DDX}	Supply voltage (each side)		-0.3 to 7	V
V_{IN}	Logic input voltage		-0.3 to 7	V
I_O	Output current		5	mA
T_j	Junction temperature		-40 to 150	°C

2.2 Electrical sensitivity

Table 2. ESD protection ratings

Symbol	Parameter	Test Condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	+/- 2	kV
CDM	Charge Device Model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2B	+/- 750	V
MM	Machine Model	Conforming to EIA/JESD22-A115-C	NC	+/- 200	V

2.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DDX}	Supply voltage (each side)		3		5.5	V
V_{IN}	Logic input voltage		0		5	V
T_{amb}	Ambient temperature		-40		125	°C

2.4 Electrical caracteristic

Table 4. Electrical characteristics at VDD1 = VDD2 = 5V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DDXon}	V_{DDX} on threshold	V_{DDX} rising from 0 V			2.8	V
$V_{DDXhyst}$	V_{DDX} off hysteresis	V_{DDX} falling from 5 V			0.1	V
IDDX	Supply current	DC		1.65	2	mA
		10 Mbps, C_L = 20 pF		3.65	5	mA
		100 Mbps, C_L = 20 pF		18	20	mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IHL}	Low level Schmitt trigger threshold	Logic input falling Full supply range	0.8			V
V_{ILH}	High level Schmitt trigger threshold	Logic input rising Full supply range			2	V
VI_{Hyst}	Schmitt trigger input hysteresis				0.5	V
V_{OL}	Low level output voltage	I_{OH} = 4 mA			0.4	V
V_{OH}	High level output voltage	I_{OL} = 4 mA	V_{DDX} – 0.3			V
Z_O	Output impedance		-40%	50	+40%	Ω
f_{MAX}	Maximum data rate	V_{IH} = 5 V	100			Mbps
t_r	Output rise time	C_L = 15 pF		2	4	ns
t_f	Output fall time	C_L = 15 pF		2	4	ns
t_{DHL}	Propagation delay H to L	See Figure 3		25	42	ns
t_{DLH}	Propagation delay L to H	See Figure 3		25	42	ns
t_{POWUP}	Power-up time				30	µs
$t_{REFRESH}$	Refresh time			1	2	µs
t_{WD}	Watchdog timeout		2		6	µs
PWD	Pulse width distortion $\lvert t_{DHL} - t_{DLH} \rvert$	Full temperature range (1)			3	ns
CMTI	Common mode transient immunity	(2)	50	65		kV/µs

1. *Not tested in production. Limit is guaranteed by characterization on a limited number of samples representing the worst case of production flow.*
2. *Not tested in production. Limit is guaranteed by characterization on a limited number of samples and simulations.*

Note: ***Testing conditions: Typical values are defined at T_{amb} = 25°C and VDD1 = VDD2 = 5 V, minimum and maximum limits applies to the full temperature range (Tested in production at T_{amb} = 25°C and the limits in the full temperature range are guaranteed by characterization on a limited quantity of samples), unless otherwise specified.***

Table 5. Electrical characteristics at VDD1 = VDD2 = 3V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DDXon}	V_{DDX} on threshold	V_{DDX} rising from 0 V			2.8	V
$V_{DDXhyst}$	V_{DDX} off hysteresis	V_{DDX} falling from 5 V			0.1	V
I_{DDX}	Supply current	DC		1.5	2	mA
		10 Mbps, C_L = 20 pF		3	5	mA
		100 Mbps, C_L = 20 pF		11	20	mA
V_{IHL}	Low level Schmitt trigger threshold	Logic input falling Full supply range	0.8			V
V_{ILH}	High level Schmitt trigger threshold	Logic input rising			2	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
		Full supply range				
V_{IHyst}	Schmitt trigger input hysteresis				0.5	V
V_{OL}	Low level output voltage	I_{OH} = 4 mA			0.4	V
V_{OH}	High level output voltage	I_{OL} = 4 mA	VDDX – 0.3			V
Z_O	Output impedance		-40%	50	+40%	Ω
f_{MAX}	Maximum data rate	V_{IH} = 3.3 V	100			Mbps
t^r	Output rise time	C_L = 15 pF		1.5	4	ns
t_f	Output fall time	C_L = 15 pF		1.5	4	ns
tDHL	Propagation delay H to L	See Figure 3		25	42	ns
t_{DLH}	Propagation delay L to H	See Figure 3		25	42	ns
t_{POWUP}	Power-up time				30	µs
$t_{REFRESH}$	Refresh time			1	2	µs
t_{WD}	Watchdog timeout		2		6	µs
PWD	Pulse width distortion $\lvert t_{DHL} - t_{DLH} \rvert$	Full temperature range (1)			3	ns
CMTI	Common mode transient immunity	(2)	50	65		kV/µs

1. *Not tested in production. Limit is guaranteed by characterization on a limited number of samples representing the worst case of production flow.*
2. *Not tested in production. Limit is guaranteed by characterization on a limited number of samples and simulations.*

Note: ***Testing conditions: Typical values are defined at Tamb = 25°C and VDD1 = VDD2 = 3 V, minimum and maximum limits applies to the full temperature range (Tested in production at T_{amb} = 25°C and the limits in the full temperature range are guaranteed by characterization on a limited quantity of samples), unless otherwise specified.***

3 Isolation characteristics

Table 6. Isolation and safety-related specifications

Parameter	Symbol	Conditions	Value	Unit
Clearance (Minimum external air gap)	CLR	Measured from input terminals to output terminals, shortest distance through air	8	mm
Creepage (Minimum external tracking)	CPG	Measured from input terminals to output terminals, shortest distance path along body	8	mm
Comparative Tracking Index (Tracking resistance)	CTI	DIN IEC 112/VDE 0303 Part 1	≥ 400	V
Isolation Group		Material Group (DIN VDE 0110, 1/89, Table 1)	II	

Table 7. Isolation characteristics

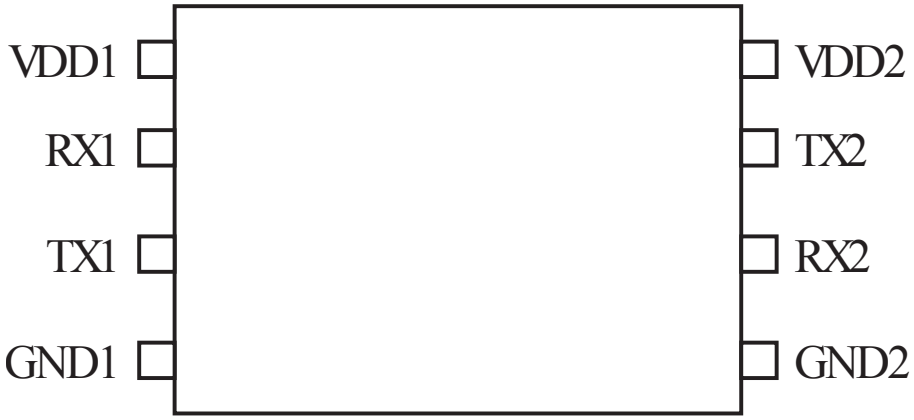
Parameter	Symbol	Test Conditions	Characteristic	Unit
Maximum working isolation voltage	V_{IORM}		1200	V_{PEAK}
Input to output test voltage	V_{PR}	Method a, type test (1) $V_{PR} = V_{IORM} \times 1.6$, tm= 10 s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b, 100 % production test (1) $V_{PR} = V_{IORM} \times 1.875$, tm = 1 s Partial discharge < 5 pC	2250	VPEAK
Isolation withstand voltage	V_{ISO}	1min (type test) (2)	5000	V_{PEAK}
Isolation test voltage	$V_{ISOtest}$	1sec (100% production) (2)	6000	V_{PEAK}
Transient overvoltage (Highest allowable overvoltage)	V_{IOTM}	tini= 60 s Type test (1)	6000	V_{PEAK}
Maximum surge isolation Voltage	V_{IOSM}	Type test (1)	6000	V_{PEAK}
Isolation resistance	R_{IO}	V_{IO} = 500 V at T_S	$>10^9$	Ω

1. *Test performed in accordance with IEC 60747-5-2.*
2. *Test performed in accordance with UL 1577.*

Note: ***For three-phase systems the values in the table refer to the line-to-neutral voltage.***

4 Pin connection

Figure 2. **Pin connection (top view)**



5 Pin list

Table 8. **Pin description**

N.	Name	Type	Function
1	VDD1	Supply	Supply voltage side 1
2	RX1	Logic output	Receive data side 1
3	TX1	Logic input	Transmit data side 1
4	GND1	Ground	Ground side 1
5	GND2	Ground	Ground side 2
6	RX2	Logic output	Receive data side 2
7	TX2	Logic input	Transmit data side 2
8	VDD2	Supply	Supply voltage side 2

6 Description

The STISO621 is a dual high-speed isolated communication channel. It integrates one channel for each communication direction and provides low levels of pulse width distortion in the full operation range.

6.1 Device operation

The device operation is described in the following table:

Table 9. Device operation table

VDD1	VDD2	TX1	RX2	TX2	RX1
Above UVLO	Above UVLO	H	H	H	H
		L	L	H	H
		H	H	L	L
		L	L	L	L
Below UVLO	Above UVLO	X	L(1)	X	Unknown
Above UVLO	Below UVLO	X	Unknown	X	L(1)
Below UVLO	Below UVLO	X	Unknown	X	Unknown

1. *Safe state imposed by default after the watchdog timeout.*

Figure 3. Timing diagram

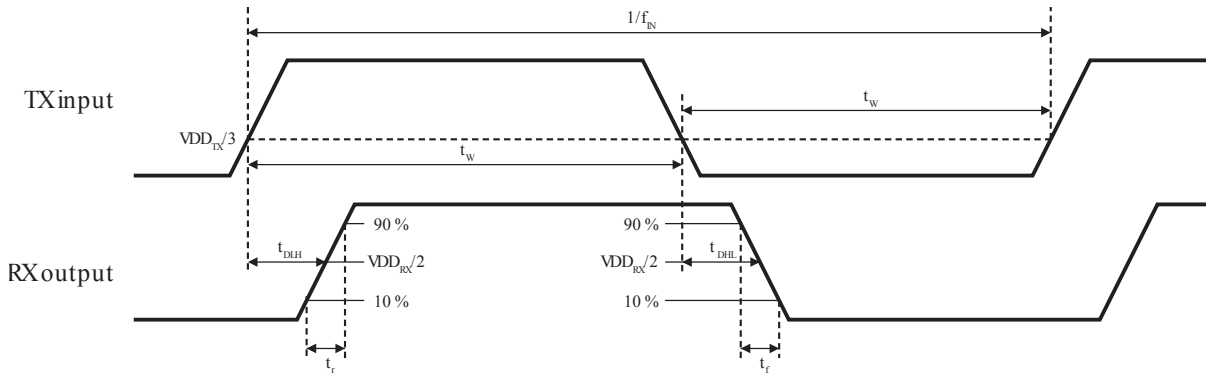
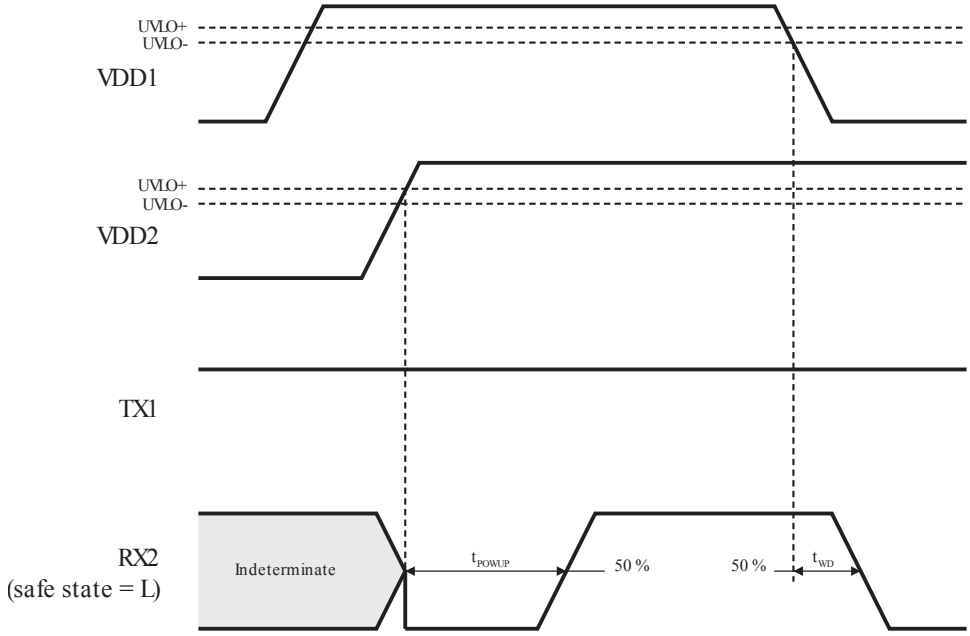


Figure 4. **Timing diagram – power up and power down**



7 Package mechanical data

Table 10. **SO8 wide package dimensions**

Symbol	Min.	Nom.	Max.	Note
A	2.34		2.64	
A1	0.10		0.30	
b	0.30		0.51	
c	0.20		0.33	
D	5.64		6.02	
e		1.27 BSC		
E1	7.39		7.59	
E	10.11		10.52	
L	0.61		0.91	
h	0.25		0.76	
θ	0°		8°	
aaa		0.25		
bbb		0.25		
ccc		0.10		

Figure 5. **SO8 wide package drawings**

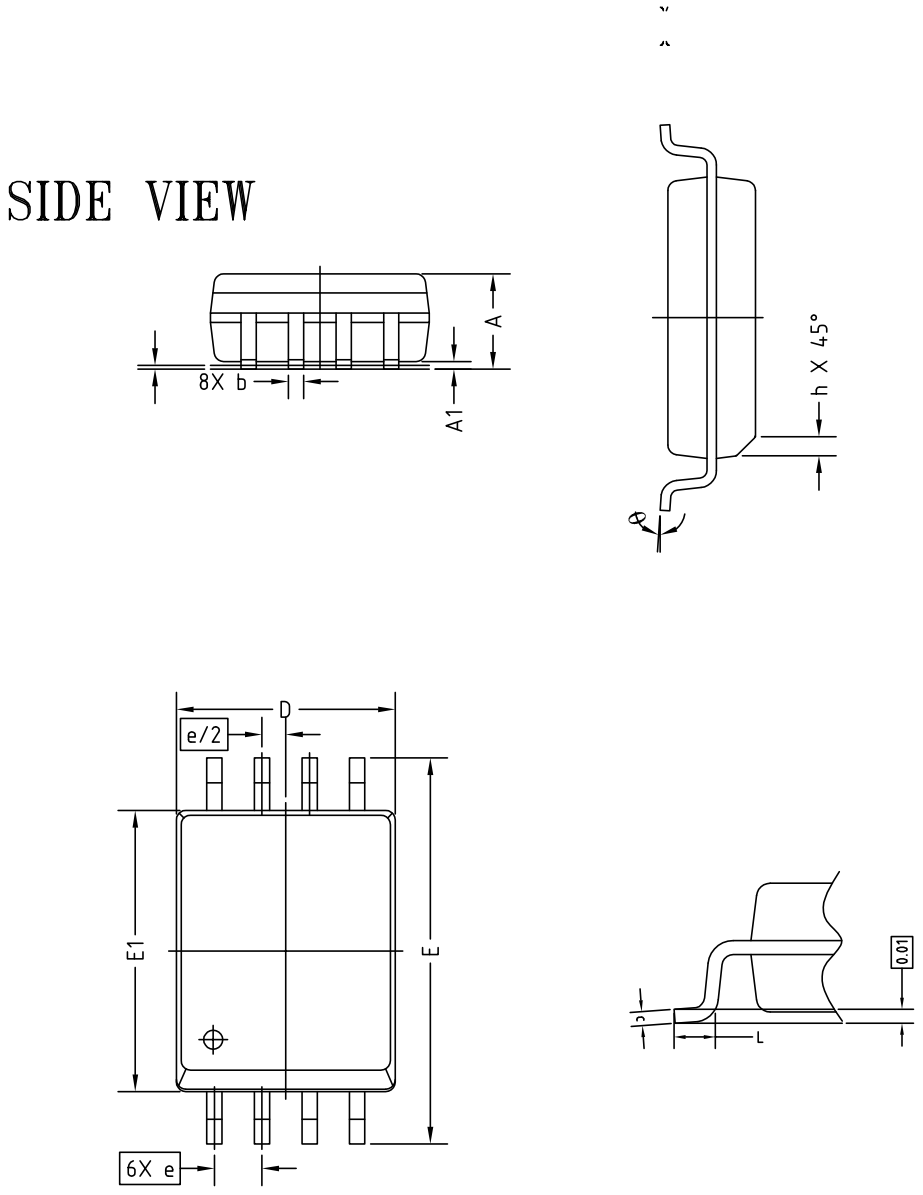
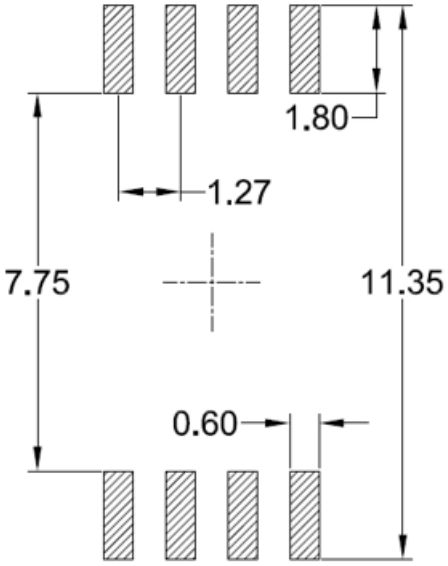


Figure 6. **SO8 wide package recommended footprint**



8 Order Information

Table 11. **Order Information**

Order Code	Package	Packing
STISO621W	S08 wide body	Tube
STISO621WTR	S08 wide body	Tape & Reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
03-Aug-2020	1	Initial release.

Contents

List of tables

List of figures