Product Change Notification / SYST-09EZDY012

Date:

11-Feb-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC16(L)F18857/18877 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-09EZDY012_Affected_CPN_02112021.pdf
SYST-09EZDY012_Affected_CPN_02112021.csv

Notification Text:

SYST-09EZDY012

Microchip has released a new Product Documents for the PIC16(L)F18857/18877 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F18857/ 18877 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added Module 1.4 (ADC Offset Error)

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 11 Feb 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC16(L)F18857/ 18877 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F18857-E/ML
PIC16F18857-E/MLVAO
PIC16F18857-E/SO
PIC16F18857-E/SP
PIC16F18857-E/SS
PIC16F18857-E/SSVAO
PIC16F18857-I/ML
PIC16F18857-I/SO
PIC16F18857-I/SP
PIC16F18857-I/SS
PIC16F18857-I/SSVAO
PIC16F18857T-E/MLVAO
PIC16F18857T-E/SSV01
PIC16F18857T-E/SSV04
PIC16F18857T-E/SSVAO
PIC16F18857T-I/ML
PIC16F18857T-I/SO
PIC16F18857T-I/SS
PIC16F18857T-I/SSC02
PIC16F18857T-I/SSVAO
PIC16F18877-E/ML
PIC16F18877-E/MV
PIC16F18877-E/MVVAO
PIC16F18877-E/P
PIC16F18877-E/PT
PIC16F18877-I/ML
PIC16F18877-I/MV
PIC16F18877-I/P
PIC16F18877-I/PREL
PIC16F18877-I/PT
PIC16F18877T-E/MV
PIC16F18877T-E/MVV02
PIC16F18877T-E/MVVAO
PIC16F18877T-E/NHXV03
PIC16F18877T-I/ML
PIC16F18877T-I/MV
PIC16F18877T-I/PT
PIC16LF18857-E/ML
PIC16LF18857-E/SO
PIC16LF18857-E/SP
PIC16LF18857-E/SS
PIC16LF18857-I/ML
PIC16LF18857-I/SO
PIC16LF18857-I/SP
PIC16LF18857-I/SS
PIC16LF18857T-I/ML

PIC16LF18857T-I/SO
PIC16LF18857T-I/SS
PIC16LF18877-E/ML
PIC16LF18877-E/MV
PIC16LF18877-E/P
PIC16LF18877-E/PT
PIC16LF18877-I/ML
PIC16LF18877-I/MV
PIC16LF18877-I/MVC04
PIC16LF18877-I/P
PIC16LF18877-I/PT
PIC16LF18877T-I/MV
PIC16LF18877T-I/MVC04
PIC16LF18877T-I/PT
PIC16LF18877T-I/PTC01
PIC16LF18877T-I/PTRA3

PIC16(L)F18857/18877 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F18857/18877 family devices that you have received conform functionally to the current Device Data Sheet (DS40001825**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18857/18877 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision **(A4)**.

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18857/18877 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID (Silicon Revision)(2)		
		A2	A3	A4
PIC16F18857	3074h	2002h	2003h	2004h
PIC16LF18857	3076h	2002h	2003h	2004h
PIC16F18877	3075h	2002h	2003h	2004h
PIC16LF18877	3077h	2002h	2003h	2004h

Note 1: The Revision ID and Device ID are located in the Configuration memory at addresses 8005h and 8006h, respectively.

2: Refer to the *"PIC16(L)F188XX Memory Programming Specification"* (DS40001753) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revision(1)		
				A2	A3	A4
Analog-to-Digital Converter with Computation (ADC2)	Computation Overflow Bit	1.1	The Computation Overflow bit will be erroneously set by the ADFLTR.	X		
Analog-to-Digital Converter with Computation (ADC2)	ADC Conversion	1.2	When using ADCRC as the ADC^2 clock source, there is a delay of one instruction cycle to set the ADGO bit.	X		
Analog-to-Digital Converter with Computation (ADC2)	Positive Voltage Reference	1.3	Using the FVR as the ADC positive voltage reference can cause missing codes.	X	X	X
Analog-to-Digital Converter with Computation (ADC2)	ADC Offset Error	1.4	ADC Offset Error specification changed.	X	X	X
Nonvolatile Memory Control	NVMREG Access	2.1	Self-writes on LF devices below 2.2V at -40˚C may not work.	X		
EEPROM	Indirect Read	3.1	Indirect read of EEPROM with FSR returns unexpected value.	X		
ECCP	Compare Mode	4.1	Toggle mode may output multiple pulses when the source clock has a prescaler other than 1:1.	X		
MSSP	I^{2}C Communication	5.1	Acknowledge failure on LF devices only.	X		
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	6.1	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X		
Secondary Oscillator (Sosc)	Low-Power Mode	7.1	SOSC may not properly operate in Low-Power mode at low temperatures.	X		
Comparators	Offset Voltage	8.1	Comparator input offset value is higher than specified.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision **(A3)**.

1. Module: Analog-to-Digital Converter with Computation (ADC^2)

1.1 Computation Overflow Bit

If the sign bit of ADFLTR (bit 7 of ADFLTRH) is set, the Computation Overflow bit will also be set, even though this is not a legitimate case of an overflow occurring.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X							

1.2. ADC Conversion

When using ADCRC as the clock source for ADC^2, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it set. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test (BTFSC) instruction on the ADGO bit, immediately after setting the ADGO bit. See the code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
BTFSC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

BTFSC will pass the very first time in this situation.

Work around

Add a NOP instruction after setting the ADGO bit and before testing the bit for completion of conversion. See the code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
NOP
BTFSC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

Affected Silicon Revisions

A2	A3	A4					
X							

1.3 Positive Voltage Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Increase the bit conversion time (TAD) to 8 us or higher.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

1.4 ADC Offset Error

The table containing the Offset Error specification (AD04: EOFF) for the Digital-to-Analog Converter is modified. The updated value for Offset Error specification is +/-3.0 LSb.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: Nonvolatile Memory Control

2.1 NVMREG Access

When performing self-writes through NVMREG access on PIC16LF18857/18877 devices with V_{DD} below 2.2V at a temperature of -40°C, the writes may not work. This applies to both PFM and EEPROM writes.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X							

3. Module: EEPROM

3.1 Indirect Read

Performing FSR reads of Data EEPROM addresses other than the lowest address (FSR = 7000h) will return unexpected values.

Work around

Set NVMADRH:L to the desired address (F000h through F0FFh) and retrieve the EEPROM value from the NVMDATL register by setting the NVMREGS and RD bits in the NVMCON1 register.

Affected Silicon Revisions

A2	A3	A4					
X							

4. Module: ECCP

4.1 Compare Mode

The ECCP Compare Toggle modes (CCPxCON<3:0> bits = 0010 or 0001) output multiple pulses instead of a single toggle pulse when its source clock has other prescaler than 1:1.

Work around

Use CCP Compare mode with pulse output (CCPxCON<3:0> bits = 1011) to clock a CLC configured as a JK flip-flop in Toggle mode.

Affected Silicon Revisions

A2	A3	A4					
X							

5. Module: MSSP

5.1 I^2C Communication

When using the MSSP to perform I^2C communication on LF devices and the voltage for VDD is above 3V, the Acknowledge signal (ACK) does not always occur after the second address byte is received, as expected. This issue exhibits itself when the MSSP is configured either for 7-bit or 10-bit addressing and in either Host or Client mode.

The issue occurs more frequently when using 10-bit addressing in Client mode and the lower address bits (A7-A0) are transmitted by the host on the SDA line.

Work around

Do not exceed 3V on VDD when using an LF device in this manner.

Affected Silicon Revisions

A2	A3	A4					
X							

6. Module: Electrical Specifications

6.1 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01, (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A2	A3	A4					
X							

7. Module: Secondary Oscillator (SOSC)

7.1 Low-Power Mode

While operating the device at low temperatures and using the SOSC in Low-Power mode (OSCCON3<6> = 0), the SOSC might fail to operate as expected.

Work around

If SOSC functionality is required at low temperatures, configure the SOSC for high-power operation (OSCCON3<6> = 1).

Affected Silicon Revisions

A2	A3	A4					
X							

8. Module: Comparators

8.1 Offset Voltage

The maximum value of the input offset voltage for the comparators is increasing from ±30 mV to ±60 mV.

The parameter in the data sheet is CM01, also known as VIOFF.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001825**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev J Document (2/2021)

Added Module 1.4 (ADC Offset Error).

Rev H Document (10/2020)

Added silicon revision A4.

Rev G Document (4/2020)

Added Module 8 (Comparators). Removed reference to A4.

Rev F Document (1/2020)

Added silicon revision A4.

Rev E Document (4/2018)

Added silicon revision A3.

Rev D Document (2/2018)

Added Module 7 (Secondary Oscillator).

Rev C Document (7/2017)

Added Modules 1.3 (PVR), 5 (MSSP) and 6 (Electrical Specifications).

Data Sheet Clarifications:

Removed all modules, data sheet updated.

Rev B Document (9/2016)

Modifications brought to Table 2.

Silicon Errata Issues:
Added ADC Conversion feature to Analog-to-Digital Converter with Computation (ADC^2). Added EEPROM and ECCP modules.

Data Sheet Clarifications:
Added modules 9 to 15.

Rev A Document (6/2016)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

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