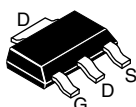


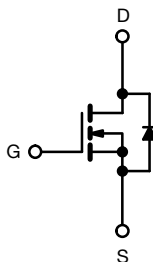
Power MOSFET

PRODUCT SUMMARY

V _{DS} (V)	60	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.20
Q _g max. (nC)	11	
Q _{gs} (nC)	3.1	
Q _{gd} (nC)	5.8	
Configuration	Single	

SOT-223


Marking code: FA



N-Channel MOSFET

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION

Package	SOT-223
Lead (Pb)-free and Halogen-free	SiHFL014TR-GE3 ^a
Lead (Pb)-free	IRFL014TRPbF ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	22	
Linear Derating Factor		0.025	W/°C
Linear Derating Factor (PCB mount) ^e		0.017	
Single Pulse Avalanche Energy ^b	E _{AS}	100	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	W
Maximum Power Dissipation (PCB mount) ^e		T _A = 25 °C	
Peak Diode Recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s	300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = 25 V, starting T_J = 25 °C, L = 16 mH, R_g = 25 Ω, I_{AS} = 2.7 A (see fig. 12).

c. I_{SD} ≤ 10 A, dI/dt ≤ 90 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mount) ^a	R_{thJA}	-	-	60	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$		-	0.068	-	$V/^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.6\text{ A}^b$	-	-	0.20	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 1.6\text{ A}$		1.9	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	300	-	pF
Output Capacitance	C_{oss}			-	160	-	
Reverse Transfer Capacitance	C_{rss}			-	29	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b	-	-	11	nC
Gate-Source Charge	Q_{gs}			-	-	3.1	
Gate-Drain Charge	Q_{gd}			-	-	5.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $I_D = 10\text{ A}$, $R_g = 24\text{ }\Omega$, $R_D = 2.7\text{ }\Omega$, see fig. 10 ^b		-	10	-	ns
Rise Time	t_r			-	50	-	
Turn-Off Delay Time	$t_{d(off)}$			-	13	-	
Fall Time	t_f			-	19	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.7	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	22	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 2.7\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 10\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	70	140	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.20	0.40	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

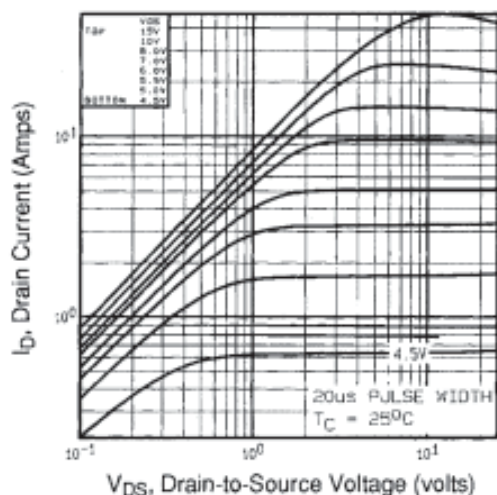


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

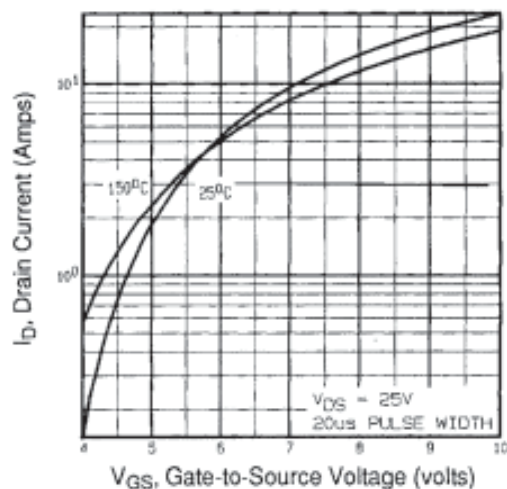


Fig. 3 - Typical Transfer Characteristics

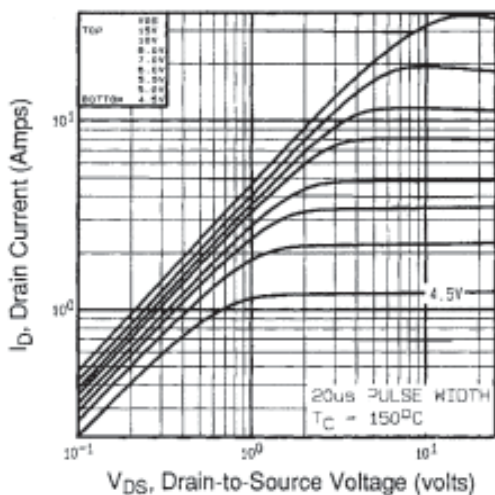


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

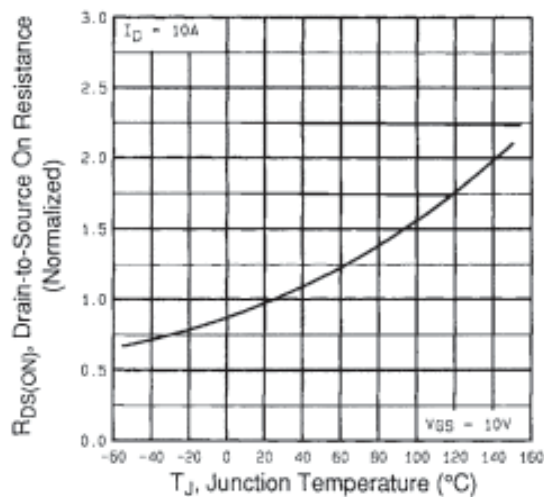
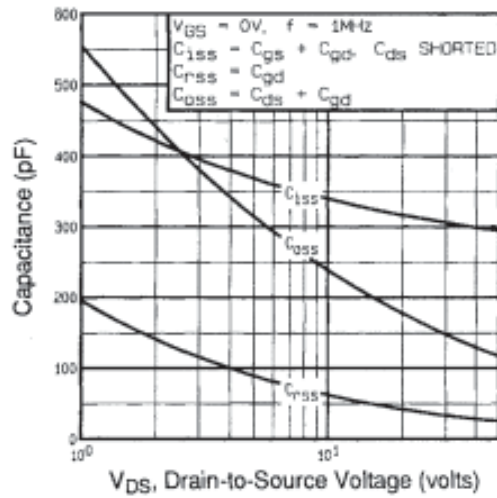
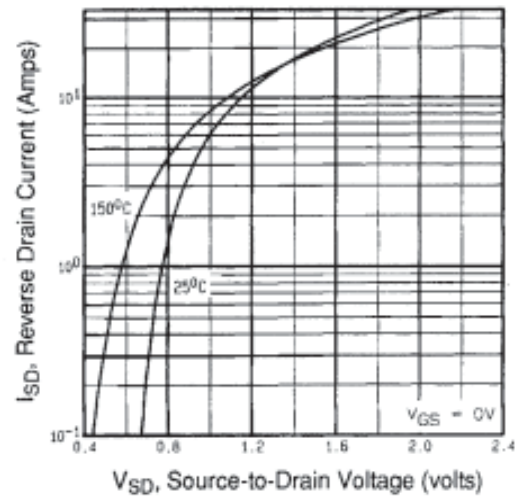
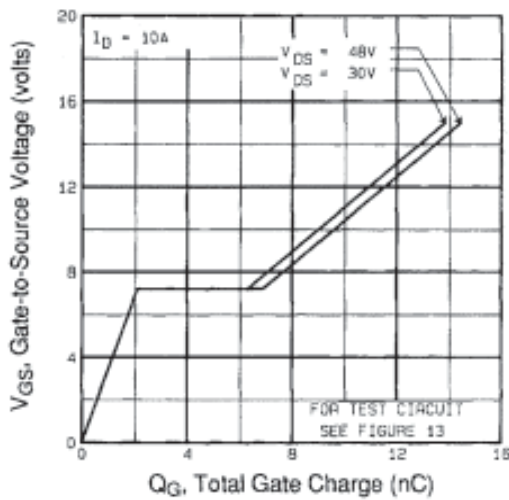
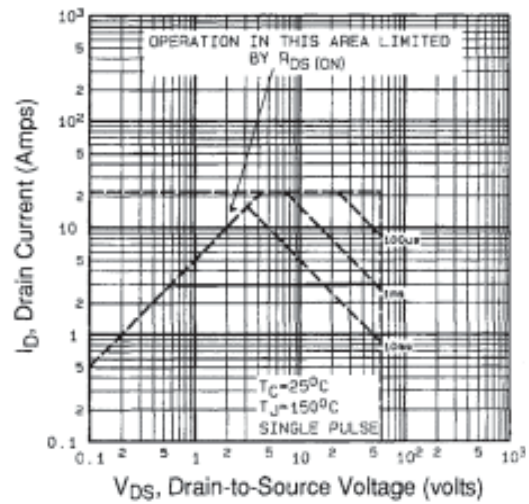
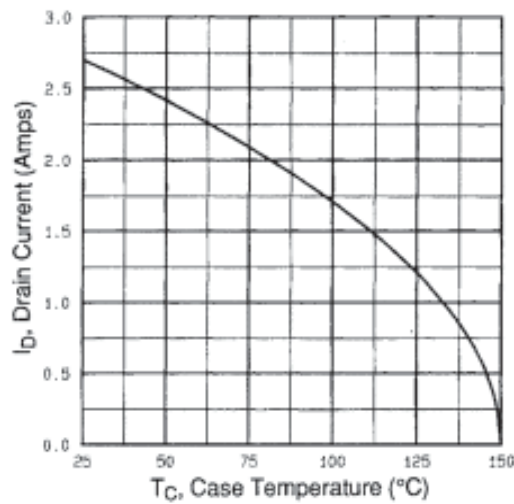
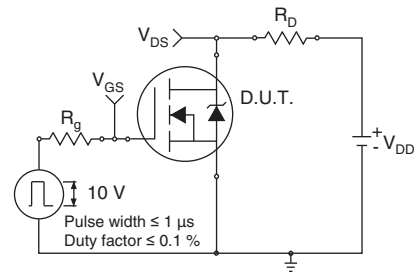
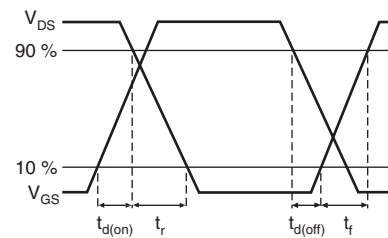
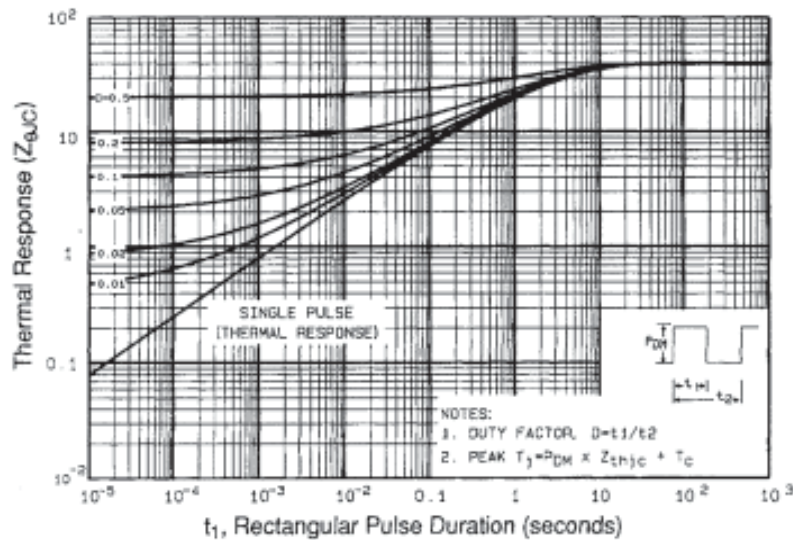


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a -Switching Time Test Circuit

Fig. 10b -Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

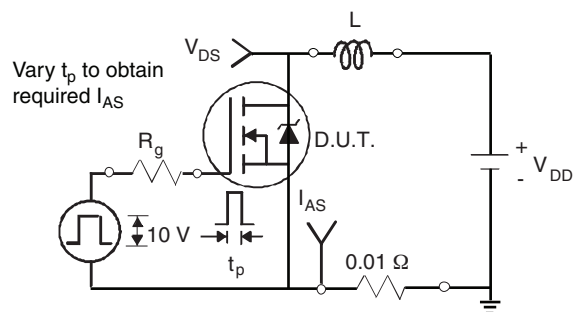
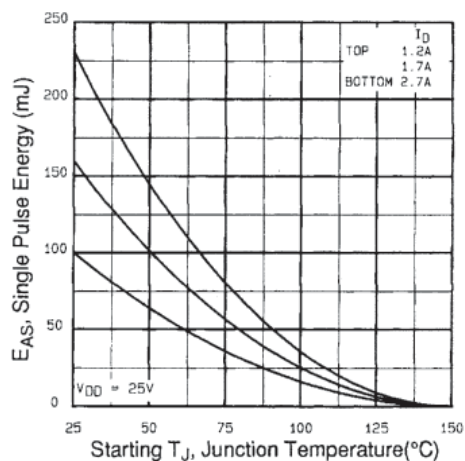
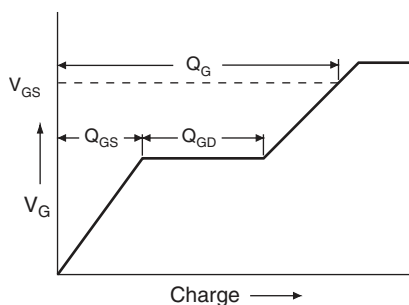
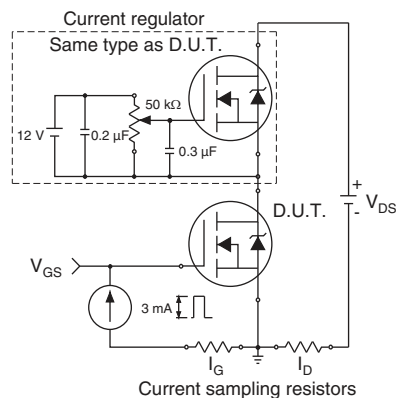
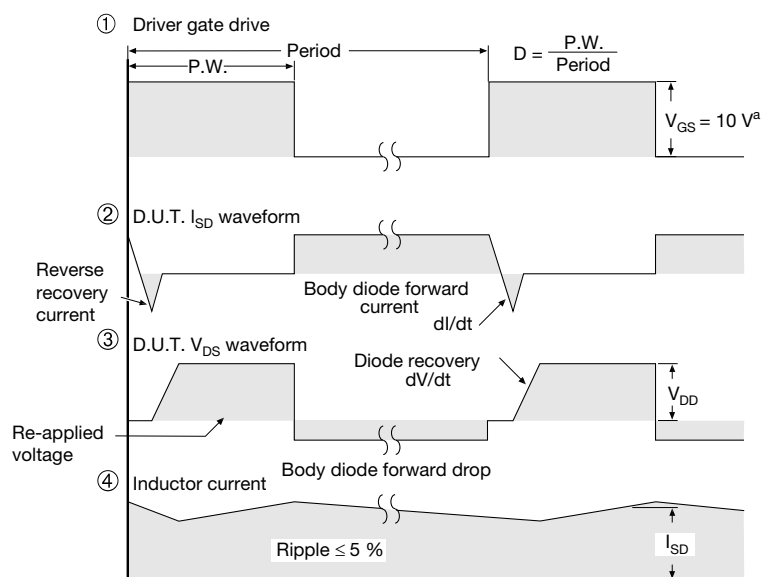
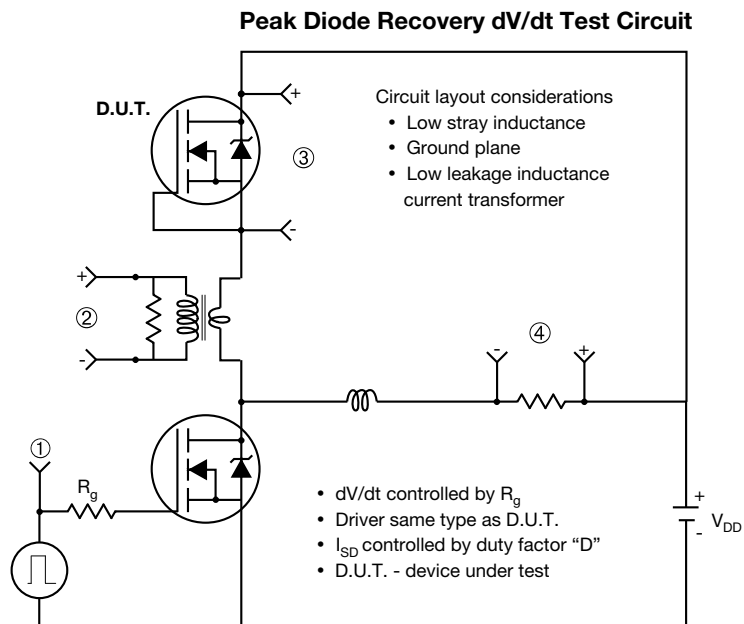

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit



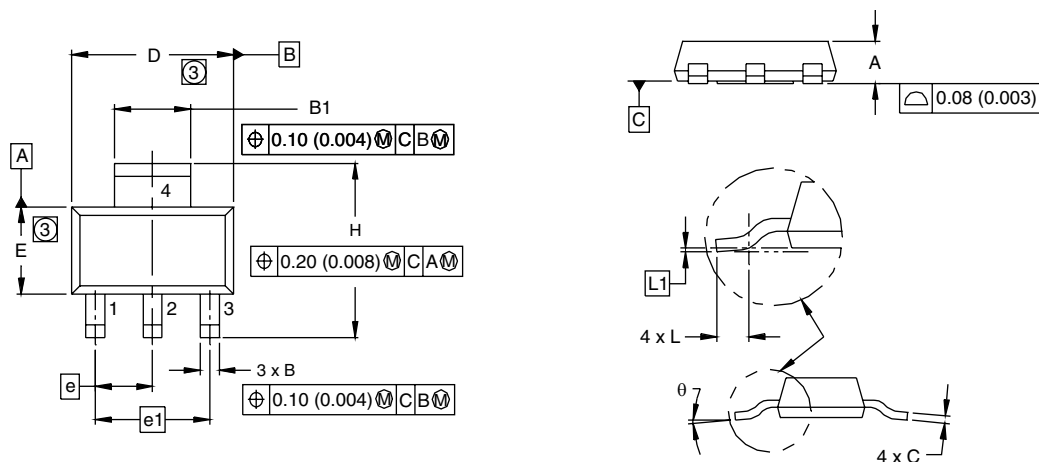
Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 12 - For N-Channel

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SOT-223 (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10°	-	10°

ECN: S-82109-Rev. A, 15-Sep-08
DWG: 5969

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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